The MDT Trigger Processor upgrade for ATLAS Muons at the HL-LHC

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on behalf of the ATLAS TDAQ collaboration

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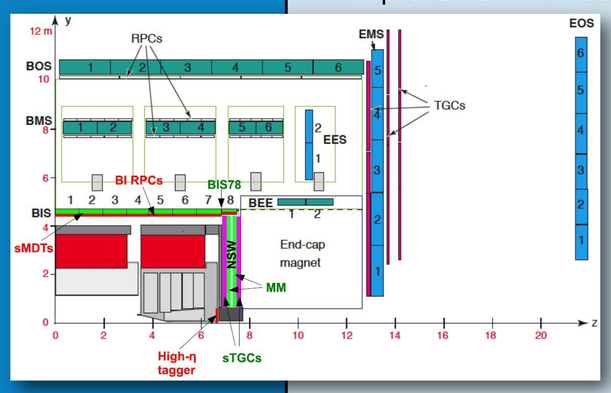
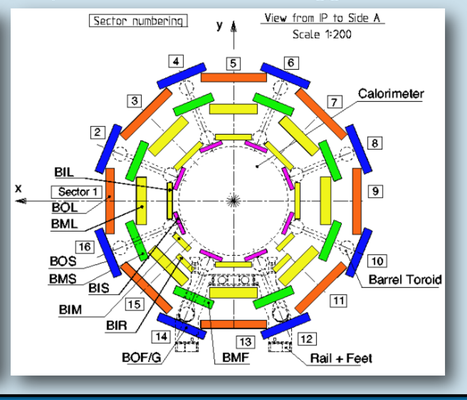
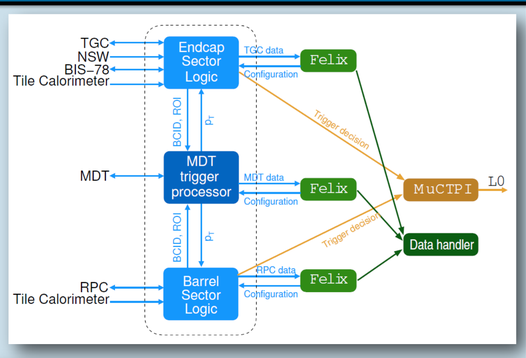
Motivation & Main Characteristics

The new **first-level muon trigger (L0Muon)** of the ATLAS experiment will be upgraded to operate in the substantially increased luminosity environment of the **HL-LHC**. The selectivity of the current system is limited by the moderate spatial resolution of **Resistive Plate Chambers (RPC)** and **Thin Gap Chambers (TGC)** trigger chambers.

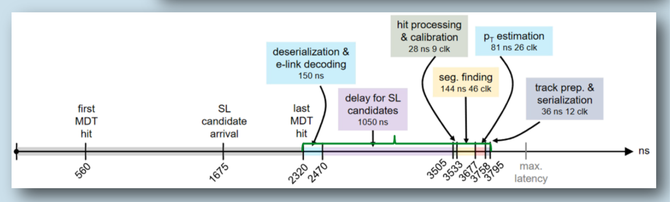
- The upgrade will make use of the high-resolution tracking capabilities of the **Monitored Drift Tubes (MDT)**.
- Improvement in the sharpness of the muon trigger efficiency turn-on curves with the new improved p_T resolution.







- **64 MDT Trigger Processor (MDT-TP) boards**, one per sector**: 16 sectors** in phi for, **2 regions** (barrel and endcap) and 2 sides.
- Each sector, side and region is divided in **3 stations**.
- The MDT-TP also provides the means to **read out the hits on the MDT chambers**. In addition to the trigger and readout, the MDT-TP is responsible for **configuring the MDT front-end electronics**.



- **Fixed latency of 1.764µs** in response to the incoming muon trigger candidate.

MDT-TP Hardware

Based on open-source **Apollo platform[1]**, comprised of two PCB modules:

Service Module (SM): common to all Apollo applications.

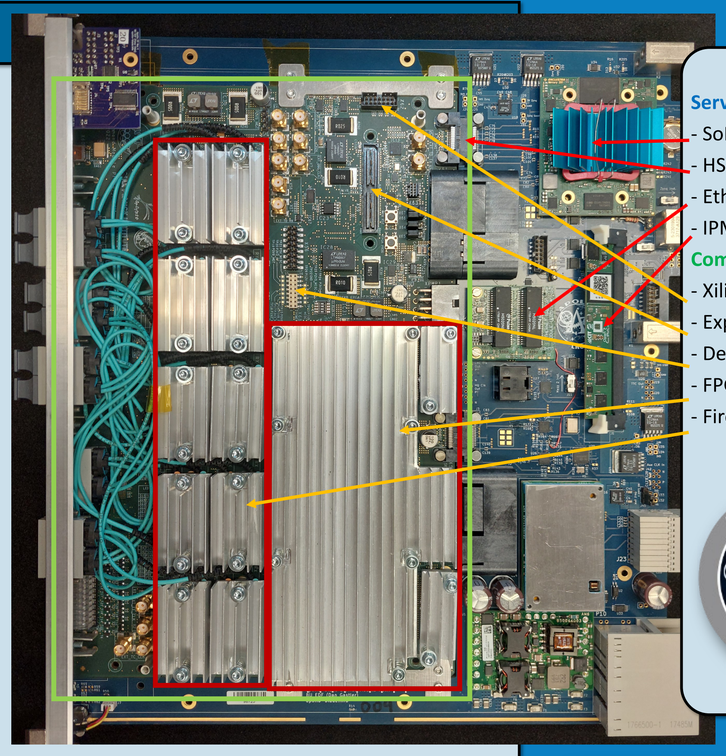
- provides **ATCA** Intelligent Platform Management Controller (**IPMC**).
- **power** entry and conditioning.
- powerful system-on-module (**SoM**) computer, Enclustra Mercury+.
- **flexible clock** and **communications** infrastructure.

Command Module (CM): application-specific module, provides the processing FPGA.

- Optical Transceivers for communication with other ATLAS systems.

CM production:

- 4 **Demonstrators** (KU15p & ZU11EG) for technology and capabilities validation.
- 2 **Prototypes** (VU13P) which are currently being integrated and tested to validate the design.



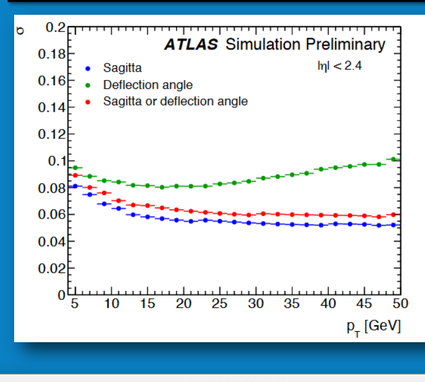
Service Module
- SoM (US+ MPSoC)
- HS Connector
- Ethernet Switch
- IPMC

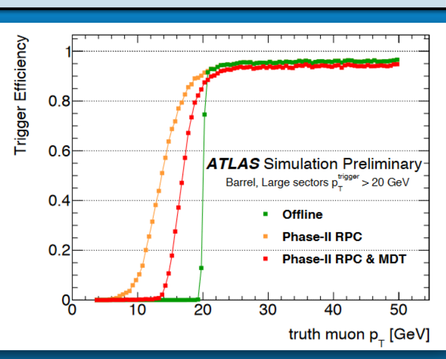
Command Module
- Xilinx JTAG
- Expansion Header
- Debug Header
- FPGA VU13P
- Firefly modules

Performance[2]

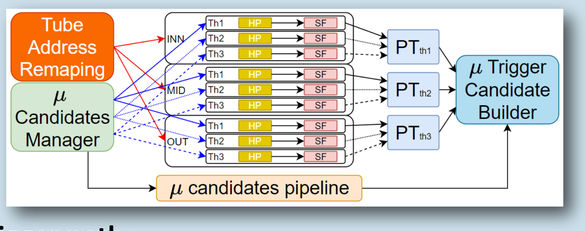
The MDT-TP trigger algorithm will:

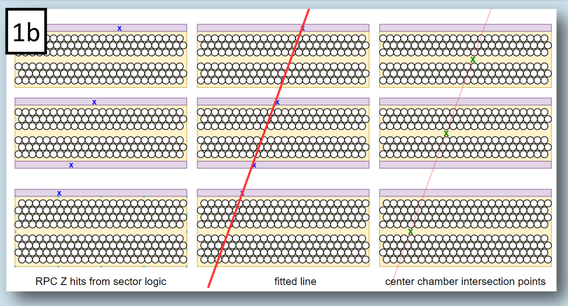
- help to **reject fake SL candidates**.
- increase the momentum resolution.
- **Reduce the output rate ~50-70%** while keeping high efficiency for muons with momenta above the 20 GeV threshold.





Algorithm (Trigger & DAQ)





Trigger path:

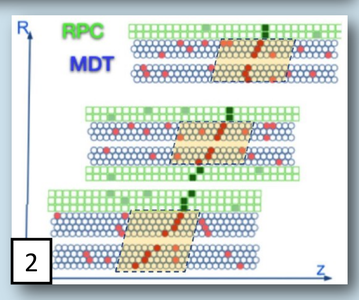
- capable of processing 3 simultaneous candidates.
- candidates received while system is busy are ignored.

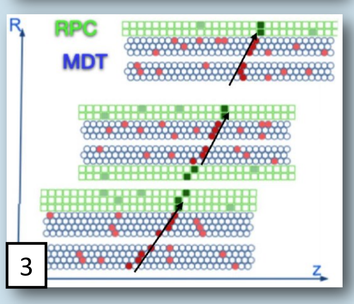
1a. Tube Address Remapping (TAR)

- MDT hits coordinates are calculated.
- pipelined waiting for the candidate to arrive.

1b. Muon Candidate Manager (UCM)

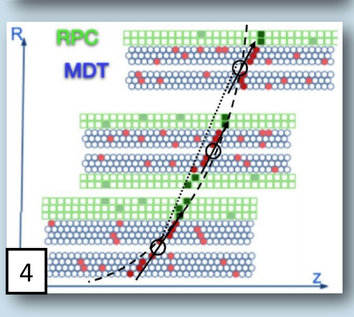
- **sorts the candidates** from the **Sector Logic (SL).**
- manages the multithreaded architecture.
- **processes** the candidates to obtain the track angle and crossing position at each MDT station from the **SL RPC/TGC** seeds.





2. Hit Processor (HP):

- Filters the MDT hits in space and time using the candidate information to define the boundaries of the filters.
- The valid hits are then processed to obtain their drift radius
- Calculates local position of the tube respect the ROI window origin.

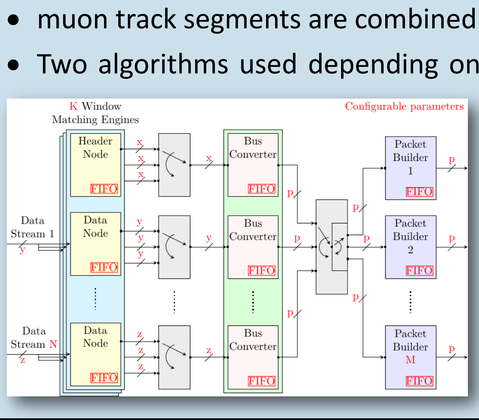


3. Segment Finder (SF):

- calculates the segment at each station.
- sends the position and angle to the momentum estimation block.
- Two different implementations are available with different algorithms: **Legendre Transform SF (CSF)** and **Compact SF (CSF)**.

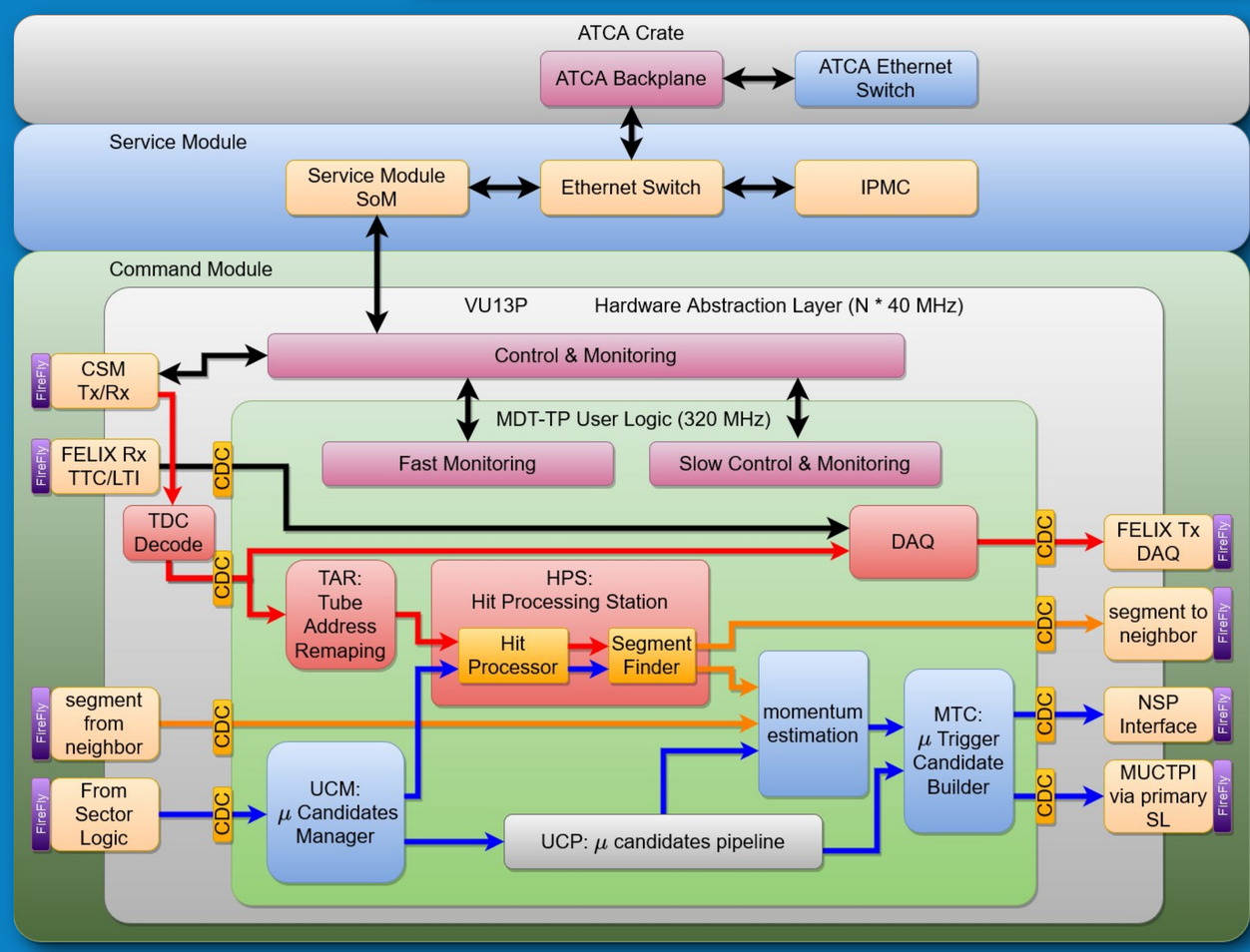
4. p_T estimator:

- muon track segments are combined to obtain the track momentum.
- Two algorithms used depending on number of available segments: when **3 segments Sagitta** algorithm and when **2 segments the deflection angle**.



DAQ Level-0/1 Accept module:

- parametrizable and flexible concurrent timestamp-based data selection and packet formatting.
- For each station of the MDT-TP project it is configured with 1 data stream, 4 output links, and 32 simultaneous searches.



Status of Developments

Firmware

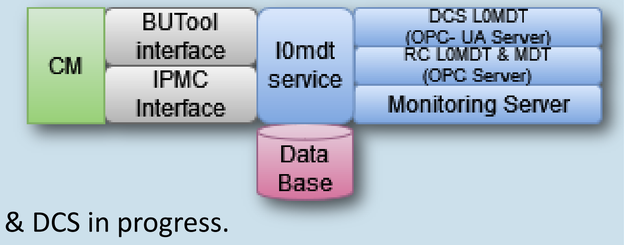
- All firmware blocks are developed and being debugged, tested and validated.
- Validation done with VHDL testbench & cocoTB framework.
- Continuous integration of Firmware is implemented using **Hog (HDL-on-Git)[3].**
- Algorithm resources are within parameters.
- Progress to complete integration of FW blocks and meet timing.
- Integrating control & monitoring blocks, including fast monitoring system, to spy the internal buses and perform playback tests.

Hardware

- Prototype being tested, including optical links, SM-CM C2C, etc.
- Integration with others systems in progress.

Software on Service Module SoM

- L0 MDT services as core of board operations, control and monitoring is being developed.
- Core elements in place to help testing.
- Integration of external systems as Run Control & DCS in progress.



First FELIX computers with Phase 2 FELIX [4] prototypes cards expected soon to start integration.

Test stands at institutes and CERN ready and working.

References:

[1] https://apollo-lhc.gitlab.io/

[2] https://twiki.cern.ch/twiki/bin/view/AtlasPublic/L0MuonTriggerPublicResults

[3] https://hog.readthedocs.io/

[4] https://atlas-project-felix.web.cern.ch