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"DOUBLE" SECURITY SYSTEM

FOR WEST AND NORTH EXPERIMENTAL AREA RECTIFIERS

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The existing and the additional protection circuits are described in a concise form in Table 1 and presented in a more schematic way in the attached block diagram.

The introduction of an additional parallel branch without comparison with the existing one would be an equivocal double security (a defective branch remains undiscovered). Therefore, additional circuits are complemented by a parity check. Both logic states of the two branches are monitored by exclusive OR gates and indicated on the supply crate. The computer obtains a common signal "parity fault" without switching off the supply. The operator should at least take notice which part of the double security system is defective.

Before each run the two logic states should be tested (assuming a non defective parity detection). The parity detection itself should be tested once a year. A special test programme will be prepared which simulates non-parity. This can only be done in conjunction with the supply simulator and the automatic test equipment.

Distribution :

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FAILURE	MAGNET INTERLOCK			RECTIF. TRANSF OVERCURRENT		
ACTION	BLOCK. + INV. ⇒ CURRENT DECAY → POL.REV.SW ⇒ 0 (Separation Magnet from Supply)		→ IF POL.REV.SW ⇒ 0 FAILS ⇒ MCB trip (delayed)	BLOCK. + INV. MCB trip (immed.) (Separation Power circuit from mains)	MCB OFF R-UNIT	MCB OFF D-UNIT
EXISTING CIRCUIT	Celduc rel. → Block. + Inv. ← Flip Flop ← Comm. pol.Rev.S ⇒ 0	Zero current detect. (logic level) ① ↓ Monitor check syst. ↓ Pol.Rev. direct. decision logic ↓ direct. dependent Celduc rel.	- Block + Inv AND persistent voltage ⇒ MCB off (del. 0,5s) - Comm. Pol.Rev.S. ⇒ 0 AND persist. current ⇒ MCB off (del. 40s) - Magn. or Supply fail. AND persist. N.I pos. ⇒ MCB off (del. 40s)	Comparator ↓ Flip Flop ↓ Celduc rel. ↓ Siemens rel.	Passive trip (undervoltage) Celduc rel. ↓ Siemens rel.	Passive trip (undervoltage) MCB-R-unit interrupts AC-Auxil. Volt.
ADDITIONAL CIRCUIT (parallel branch)	opto coupler → Block + Inv. ← Flip Flop ← Comm. pol.Rev.S ⇒ 0	Zero current detect. (logic level) ↓ Monitor check syst. ↓ direct. Celduc rel. / independ.	–	as above	- passive trip as above - Active trip (acts over spring loading motor)	- Passive trip MCB-R-unit interrupts rectif. Auxil. Volt. - Active trip as R-unit use of D-unit auxil. v.
PARITY CHECK	Flip Flops (individ.) Water Press. Water Temp. Coil Temp. Term. box Red button Rheost.	- Monitor check syst - pol.Rev.S. liberation - Celduc rel	–	see MCB parity check	- Passive channels - Active against pass. (only if active trips alone)	②
TEST ③ FACILITIES (parity detection assumed OK)	SK 101 (Magnet Interlock interrupt)	Automatically when Pos 0 ⇒ N.I ⇒ 0	–	Applic. +15V on Banana socket (overcurrent simul.)	- Automatic. for pass. branches (ON-OFF) - Passive and Active separately (push butt.)	- Passive and Active separately (push butt.)

TABLE 1

NOTES FROM TABLE 1

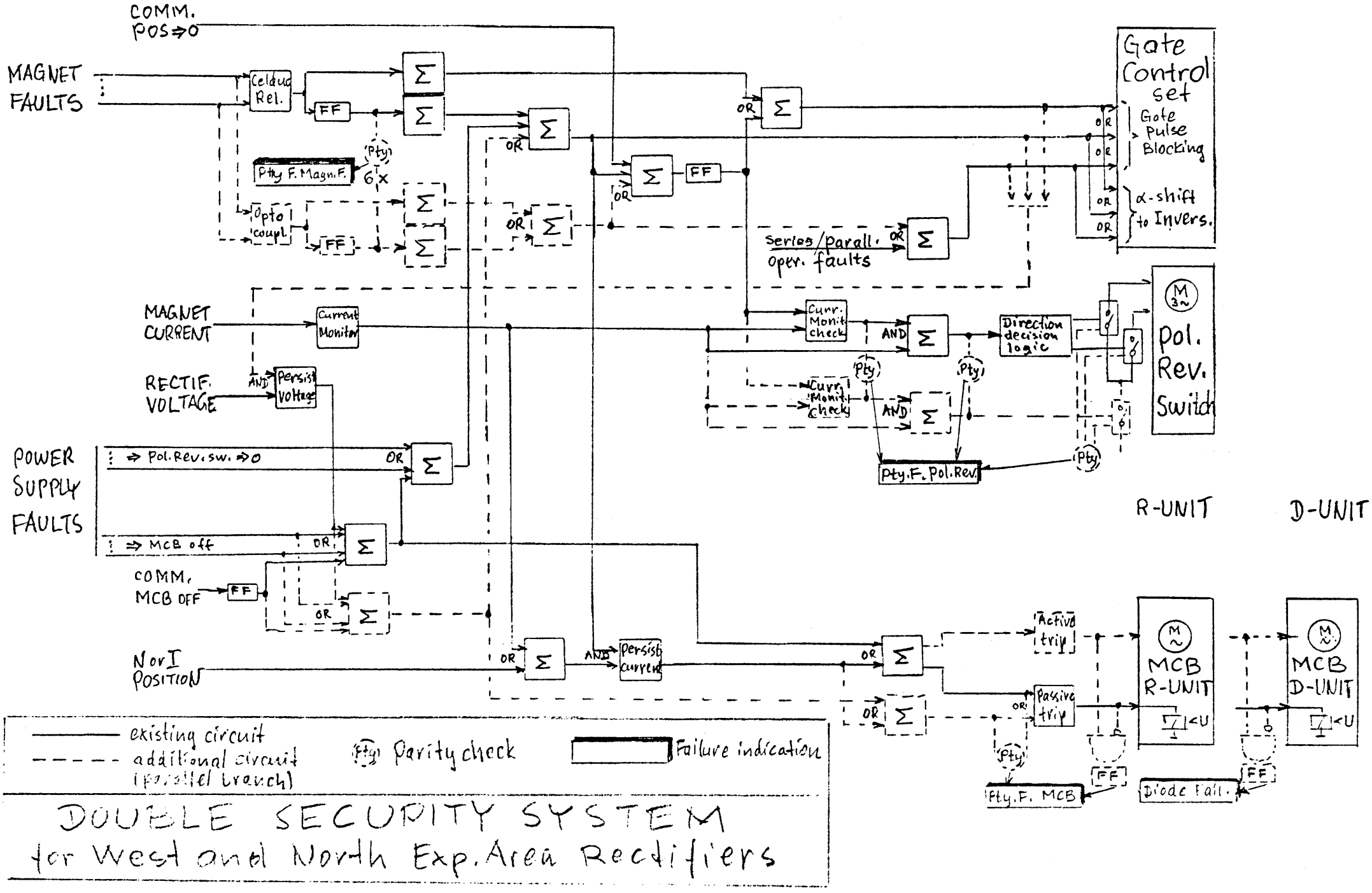
(1) Zero current detection uses the DCCT and could therefore not be doubled (cost and space), but the monitor check system tests the current detector : Current has to be recognized during operation before zero current signal is accepted after decay.

If the test is negative, polarity reversal switch remains in N or I position. In case of a magnet or supply failure the MCB will be tripped after 40 s.

(2) The D-unit has, like the R-unit, a passive and an active trip. Both are derivated directly from the R-unit MCB auxiliary contact and therefore do not permit a parity check.

Malfunctioning of the D-unit MCB will be detected by persistent voltage and persistent current protection.

(3) The correct functioning of double security should be tested as indicated before a run starts. A defective channel would be detected by parity failure, provided that the parity detection itself is not defective.



DOUBLE SECURITY SYSTEM
for West and North Exp. Area Rectifiers