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LOW-NOISE WIDEBAND RF AMPLIFIER FOR PS PICK-UPS

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The Closed Orbit Digital Display (CODD) is a system that measures the trajectories of the beam inside the Proton Synchrotron (PS) vacuum chamber. It is capable of measuring the position of bunches, containing more than 4E10 elementary charges, with a precision better than 0.5 mm. This precision deteriorates for bunches with a lower charge density, as is the case with the lead ion beams (2.5E8 charges per bunch).
The main subject of this paper is the design and realisation of a pick-up amplifier that will be capable of measuring the position of lead ion beams with a precision comparable to that attained for higher charge beams.

Geneva, Switzerland
21 November 2000

INTRODUCTION

The Closed Orbit Digital Display (CODD) is a system that measures the trajectories of the beam inside the Proton Synchrotron (PS) vacuum chamber. It is capable of measuring the position of bunches containing more than $4 \cdot 10^{10}$ elementary charges, with a precision better than 0.5 mm. This precision deteriorates for bunches with a lower charge density, as is the case with the lead ion beams ($2.5 \cdot 10^{8}$ charges per bunch).
The main subject of this paper is the design and realisation of a pick-up amplifier that will be capable of measuring the position of lead ion beams with a precision comparable to that attained for higher charge beams.

1. GENERAL DESCRIPTION OF THE AMPLIFIER

This chapter presents the basic ideas used in the design of the low-noise amplifier.

A simplified diagram of the pick-up (PU), represented as a capacitance C_e of 70 pF, connected to the measurement electronics can be seen in figure 1. The 5-m long transmission line has a characteristic impedance $Z_0 = 50\ \Omega$ and a capacitance of $C_{tl} = 100$ pF/m. For a detailed description of the position measurement chain please refer to **[1]**.

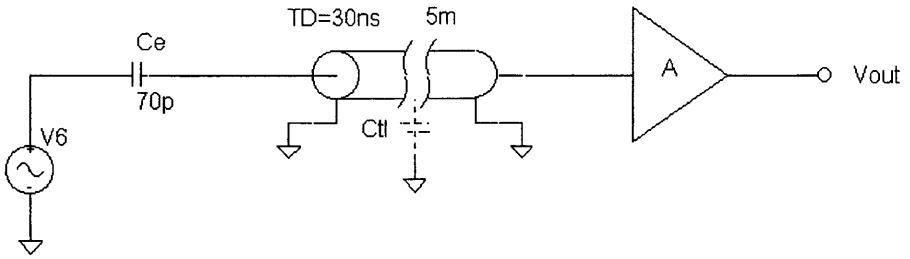


Figure 1: PU electrode connected to the amplifier

In the process of designing the PU Amplifier several of its general characteristics, such as input impedance and gain, can be specified from the beginning.

1.1 INPUT IMPEDANCE

The available signal at the input of the amplifier depends on its input impedance. Two possibilities have been considered: the first one is to make the input impedance equal to the characteristic impedance of the transmission line Z_0 (fig. 2), the second one is to make the input impedance a series RC with $R = Z_0$ (fig. 3).

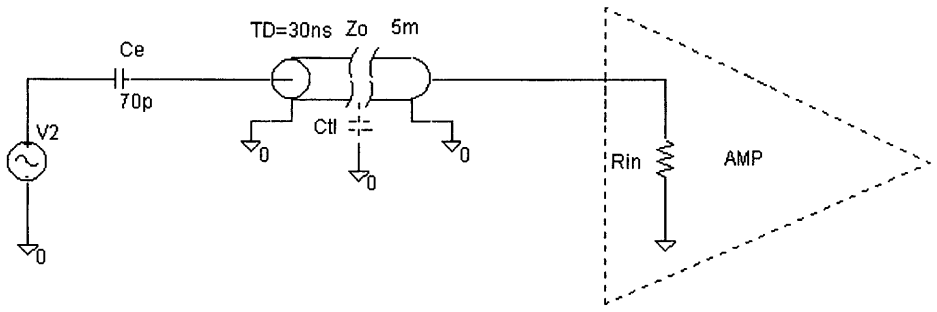


Figure 2: Amplifier real input impedance ($R_{in} = Z_0$)

A 50 Ω input impedance terminates the transmission line perfectly at all frequencies, but the main disadvantage is that most of the signal at lower frequencies is lost, because the impedance of the electrode is very large.

If the input impedance is a series RC, then $Z_{in} = Z_0 + \frac{1}{jC_{in}\omega}$. The transmission line will be properly terminated at high frequencies (HF, frequencies at which the length of the cable is comparable to λ/4) if the value of the corner frequency $\frac{1}{2\pi Z_0 C_{in}}$ is sufficiently low, that is, if C_{in} *is big enough.*

On the other hand, at low frequencies (LF) there is a capacitive divider between the capacitance of the PU and the capacitance of the parallel combination of the transmission line capacitance C_{tl} and C_{in}. Therefore *minimising* C_{in} increases the signal available at the input.

The choice of C_{in} is crucial to have a good compromise between a proper termination at HF and minimising the amount of signal loss at LF.

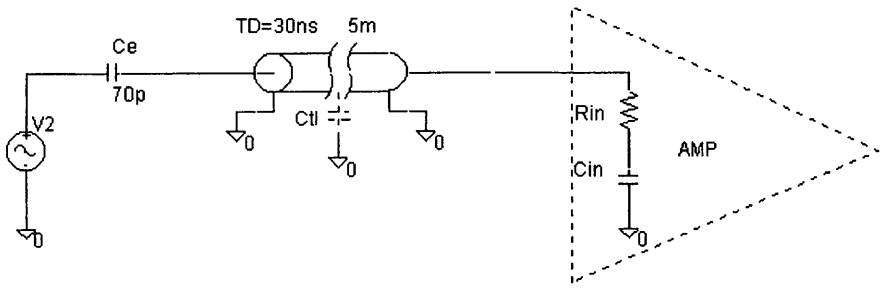


Figure 3: Amplifier complex input impedance ($R_{in} = Z_0$)

Note: The maximum signal available at the input is ultimately limited by the capacitance of the transmission line. Then, a transmission line with lower capacitance and therefore higher Z_0 would be best suited.

The signal available at the input of the amplifier for both a resistive input impedance and the RC input impedance is shown in figure 4 (C_{in} = 3 nF and R_{in} = 50 Ω).

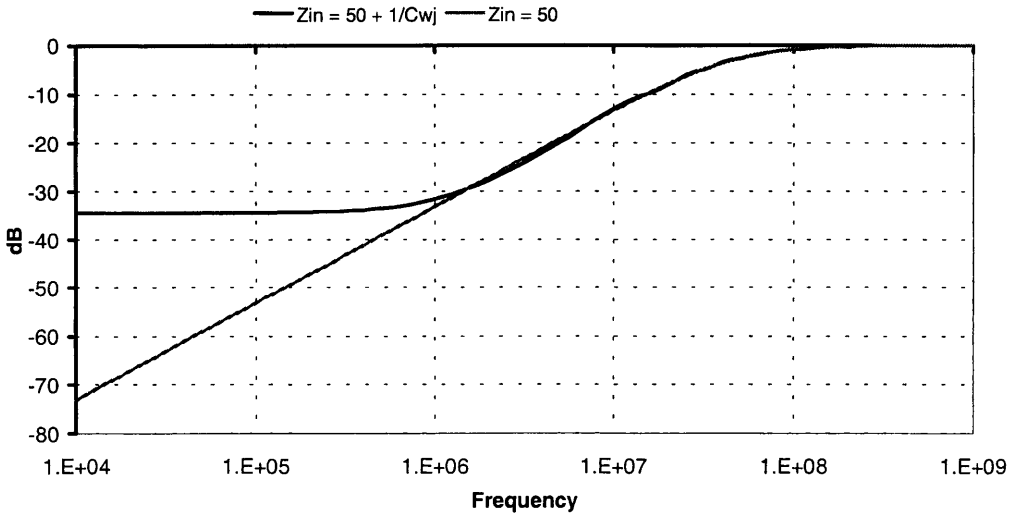


Figure 4: Signal at amplifier input, for R and RC terminations

The corner frequencies of the Z_{in} = 50 Ω +1/(jC_{in} ω) curve are given by:

$$f_{cl} = 1/(2\pi R_{in}C_{in}) = 1 \text{ MHz}$$
$$f_{ch} = 1/(2\pi R_{in}C_e) = 45 \text{ MHz}$$

Due to its obvious advantage at LF, the series RC configuration is the one retained.

1.1.1 Active impedance principle

An efficient way to reduce noise is to terminate the transmission line with an active impedance. Consider an amplifier with fixed gain $-A$ and infinite input impedance (fig. 5).

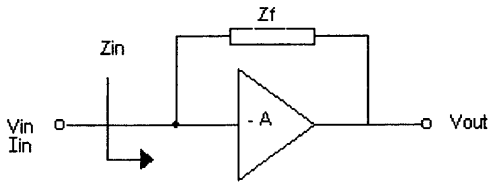


Figure 5: Active impedance architecture

The input impedance of this circuit can be calculated as follows:

$$V_{out} = -A \cdot V_{in}$$
$$V_{out} = V_{in} - Z_f \cdot I_{in}$$
$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{Z_f}{1+A}$$

Therefore the input impedance can be set to the desired value by choosing the appropriate Z_f.
Let us now calculate the noise created by both the active termination and the passive termination.

1.1.1.1 Active termination noise

The input equivalent noise for $Z_f = R_f$ (such that the input impedance Z_{in} is equal to R_S) is calculated by making V_S equal zero in the following circuit and only taking into account e_{Rf}.

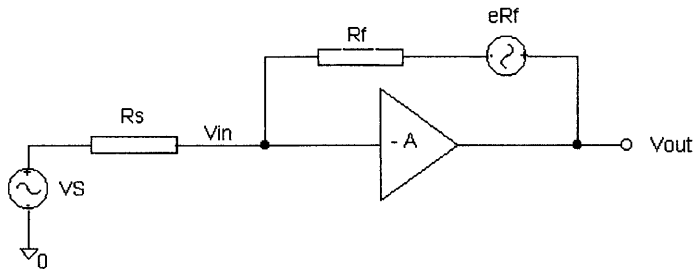


Figure 6: Noise source in an active impedance configuration

The equation obtained is the following:

$$\frac{V_{in}}{R_S} = \frac{V_{out} - e_{R_f} - V_{in}}{R_f}$$

Solving for V_{out}

$$V_{out} = \frac{A \cdot e_{R_f}}{2(1+A)}$$

The input equivalent noise is then

$$e_{i_{active}} = \frac{e_{R_f}}{2(1+A)} = \frac{\sqrt{4kTR_S(1+A)}}{2(1+A)} = \frac{e_{R_S}}{2\sqrt{1+A}}$$

1.1.1.2 Passive termination noise

In this case $R_{in} = R_S$.

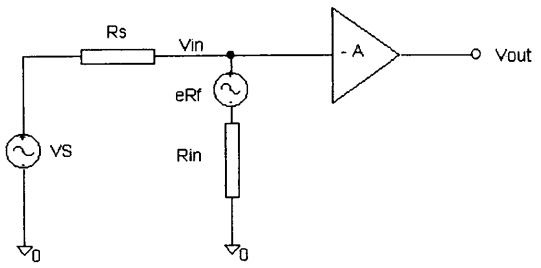


Figure 7: Noise source in a passive impedance configuration

$$V_{out} = -A\left(e_{R_f}/2\right)$$

The input equivalent noise is then

$$e_{i_{passive}} = \frac{e_{R_f}}{2} = \frac{e_{R_s}}{2}$$

This result shows that the active termination produces less noise:

$$e^2_{i_{active}} = \frac{e^2_{i_{passive}}}{1+A}$$

1.2 AMPLIFIER GAIN

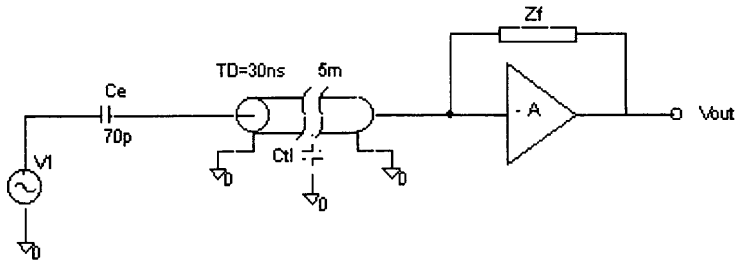


Figure 8: Electrode, transmission line and amplifier

To obtain a flat response, the input signal shape must be taken into account. From figure 4, in the input impedance section, it can be deduced that the response of the amplifier must have the following shape (where f_{cl} and f_{ch} have been calculated in the previous section).

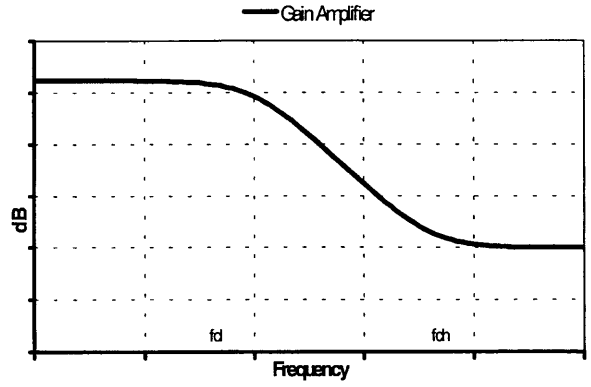


Figure 9: Required amplifier gain

As indicated in the "active impedance principle", the amplifier must be inverting, in order to be able to realise the active impedance.

2. REALIZATION PRINCIPLES

In this chapter, the design choices for the amplifier are made and justified, without going into implementation details such as values of elements, biasing, etc...

The amplifier will consist of two distinct blocks: a preamplifier and a gain-shaping block (fig. 10).

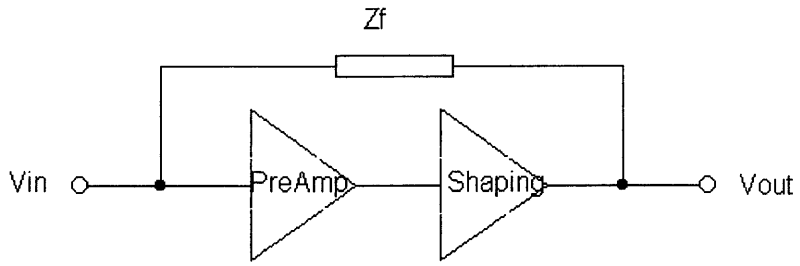


Figure 10: Amplifier structure

The preamplifier must raise the signal as much as possible from the noise level, and thus it will have to be low noise. Its gain will be constant (flat). The preamplifier is the most complicated part to design because its effect on the final noise figure is dominant and discrete components are used.
The gain-shaping block will give the gain the desired shape, as defined previously. It will be realised with an ultra-low noise integrated circuit.

2.1 PREAMPLIFIER

The preamplifier for the PS pick-ups uses a Paralleled JFET-Bipolar Cascode (fig. 11) for various reasons [2, 3]:
1. - It can have very low noise
2. - The cascode configuration reduces the input capacitance due to Miller effect

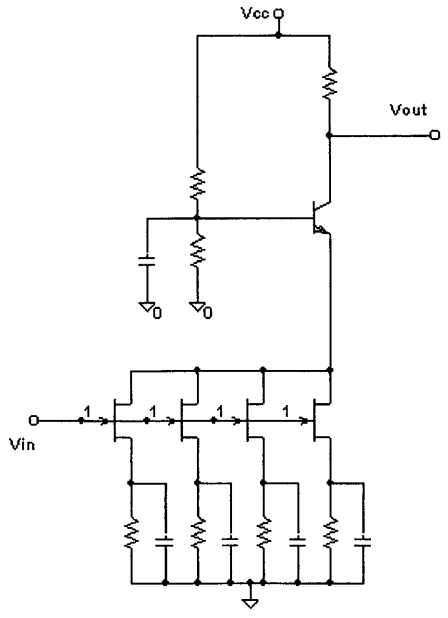


Figure 11: Paralleled JFET-Bipolar Cascode

2.1.1 Noise considerations

The source impedance is the capacitance of the pick-up, therefore its impedance is high at low frequencies; this is why it is worth using a transistor with low current noise, which offers the best noise performance with a high source impedance. JFETs are more adequate than BJTs, due to their very low current noise.

MOSFETs are not adequate as they tend to have much higher voltage noise than JFETs, with $1/f$ noise predominating, since the $1/f$ knee goes up to the MHz range.
On the other hand a BJT is better suited for the output stage of the cascode, due to the low impedance that it presents to the JFET.

Noise in a JFET is inversely proportional to its transconductance **[4, 5]**:

$$e_n^2 = \frac{\alpha}{g_m}$$

The transconductance is

$$g_m = \frac{i_d}{v_{gs}}$$

and it depends on the drain current I_D

$$g_m = \frac{2}{V_p}\sqrt{I_{DSS} \cdot I_D}$$

where I_{DSS} is the saturated drain current, at zero gate bias, and V_p is the pinch-off voltage of the channel.

The JFET voltage noise can be reduced either by operating it at high drain current, where the transconductance is the highest, or by placing N JFETs in parallel.

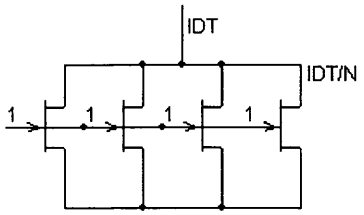


Figure 12: JFETs in parallel

$$i_{dT} = N \cdot i_d = N \cdot g_m \cdot v_{gs} = g_{mT} \cdot v_{gs}$$

$$g_{mT} = N \cdot g_m = N \cdot \frac{2}{V_p}\sqrt{I_{DSS} \cdot \frac{I_{DT}}{N}} = \sqrt{N} \cdot \frac{2}{V_p}\sqrt{I_{DSS} \cdot I_{DT}}$$

Thus the total transconductance of the circuit is $\sqrt{N}$ times the transconductance of a single JFET biased at I_{DT} (total of the drain currents). Therefore

$$e^2_{nNjfets} = \frac{e^2_{nsinglejfet}}{\sqrt{N}}$$

2.1.2 Input capacitance

Because the input capacitance increases with N, the number of JFETs that can be placed in parallel is limited by the bandwidth requirements of the circuit. Also noticeable is the effect of the feedback capacitance in the input; that is the input Miller capacitance, which increases with gain: $C_{mi} = (1 + Gain) \cdot C_{dg}$.

The gain of a single JFET, with a load resistance on its drain (fig. 13), is: $\frac{v_{out}}{v_{in}} = -g_m \cdot R_L$

Since the gain of the circuit depends directly on R_L, if it is large, the gain of the circuit is large and thus the input Miller capacitance is large too.

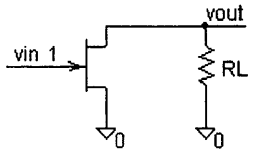


Figure 13: JFET gain

A cascode configuration (fig. 14) reduces the gain of the first stage of the circuit, by virtue of the low input impedance of a BJT in common base, whilst providing the same total signal gain.

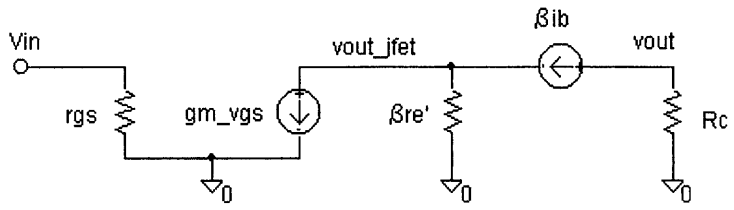


Figure 14: Small signal equivalent of cascode circuit

The input impedance of the common base BJT is

$$Z_{in} = \frac{v_{out\_jfet}}{i} = \frac{-i_b \beta r_e'}{-i_b(\beta+1)} \cong r_e'$$

And $r_e' = \frac{25\,\text{mV}}{I_E}$ is generally low (ohms to tens of ohms).

Therefore, the gain of the JFET stage ($-g_m r_e'$) is very small, thus reducing the value of the input Miller capacitance.

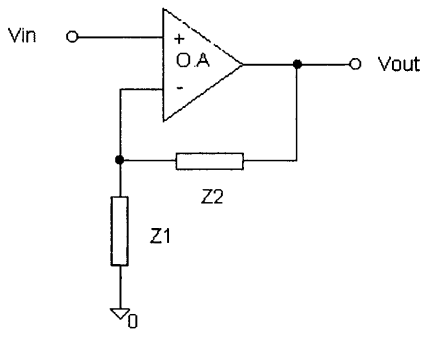
The total gain of the circuit however is the same as that of the single JFET circuit:

$$\frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_{out\_jfet}} \cdot \frac{V_{out\_jfet}}{V_{in}} = \frac{R_L}{r_e'} \cdot (-g_m) \cdot r_e' = -g_m \cdot R_L$$

2.2 SHAPING AMPLIFIER

To obtain the desired gain shape, a non-inverting operational amplifier configuration (fig. 15) has been chosen for the following reasons:

1. - The preamplifier already produces the necessary inversion
2. - The non-inverting amplifier presents a large input impedance



$$A = 1 + \frac{Z_2}{Z_1}$$

Figure 15: Shaping amplifier

The target gain shape (fig. 16) can be divided into 3 areas: a low frequency area with high gain, an intermediate frequency area with a constantly decreasing gain and a high frequency area with low gain.

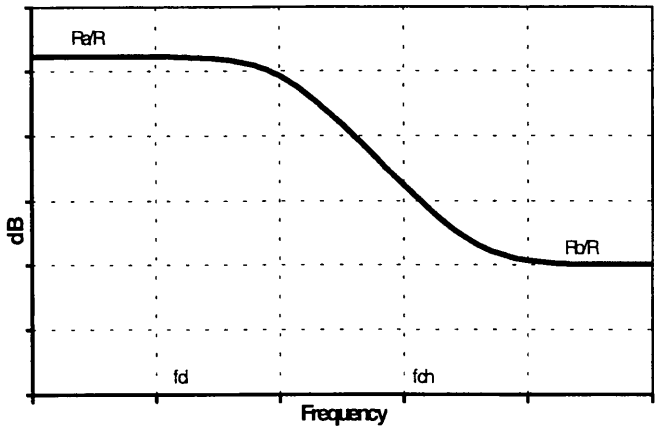


Figure 16: Shaping amplifier gain

Let us assume that Z_1 is a constant, i.e. a resistance R.

Notice that at low frequencies Z_2 must be bigger than Z_1. In the medium frequency area, the value of Z_2 decreases constantly, eventually reaching a minimum value in the high frequency area.

This can be implemented with the circuit of figure 17, if $R_a >> R_b >> R$.

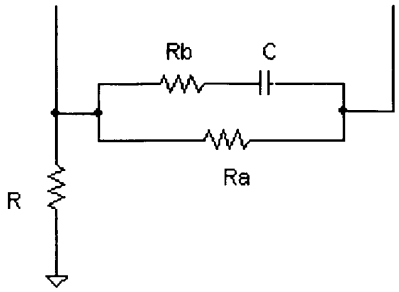


Figure 17: Resistor Network

The gain of the shaping amplifier is such that the signal gain (from the pick-up to the output of the amplifier circuit (pre-amplifier + shaping amplifier)) is flat.
It is the final value of Z_2 (R_b) that sets the total signal gain.

$$\frac{V_{out}}{V_{in}} = \frac{R_b}{R}$$

2.3 FEEDBACK IMPEDANCE

Once the gain and the input impedance are defined, it is straightforward to calculate the required feedback impedance. The formula relating these three values is:

$$Z_{in} = \frac{Z_f}{1+A} \cong \frac{Z_f}{A} \quad \text{(If gain } A \text{ is } >>1)$$

Which written in dB gives

$$Z_f \text{ dB}\Omega^{1} = Z_{in} \text{ dB}\Omega + A \text{ dB},$$

[1] $20\log\left(\frac{Impedance}{1\Omega}\right) \rightarrow \text{dB}\Omega$

Z_f can then be calculated graphically as follows:

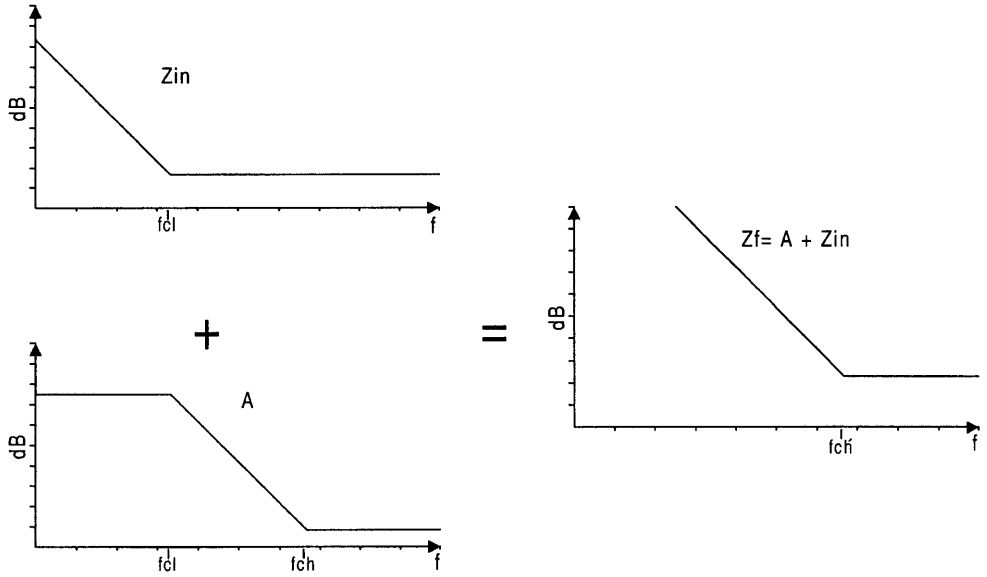


Figure 18: Graphical calculation of Z_f

The feedback impedance Z_f is a series RC with:

$$R = 10^{\left(\frac{Minimum(Z_{in}\ \mathrm{dB}\Omega) + Minimum(A\ \mathrm{dB})}{20}\right)}$$

C is given by $\frac{1}{RC} = 2\pi \cdot f_{ch}$

The resulting circuit using ideal amplifiers (infinite bandwidth) is shown in figure 19.

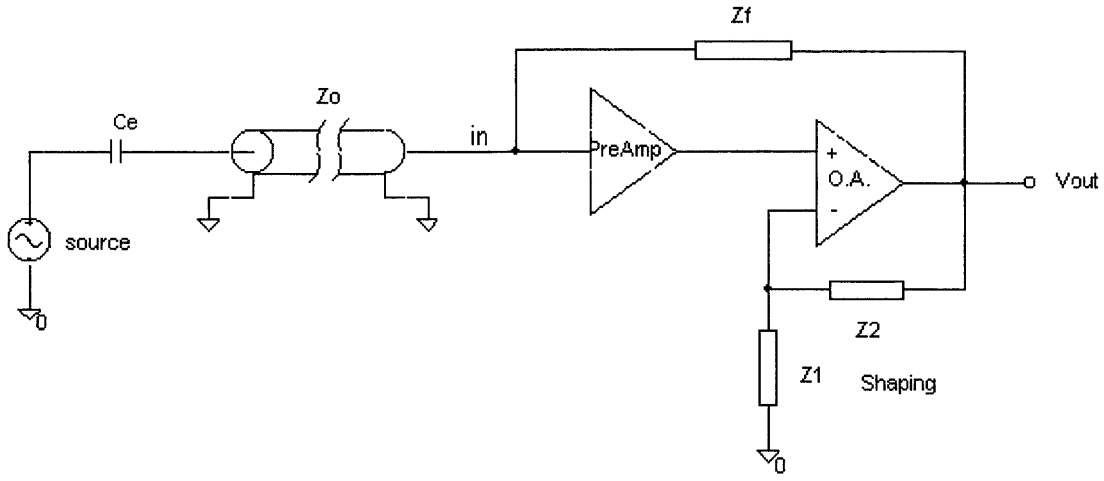


Figure 19: Principle, using ideal amplifiers

Defining: Amplifier Gain as $\frac{V_{out}}{V_{in}}$, Signal Gain as $\frac{V_{out}}{V_{source}}$ and Input Signal as $\frac{V_{in}}{V_{source}}$

The following graph is obtained:

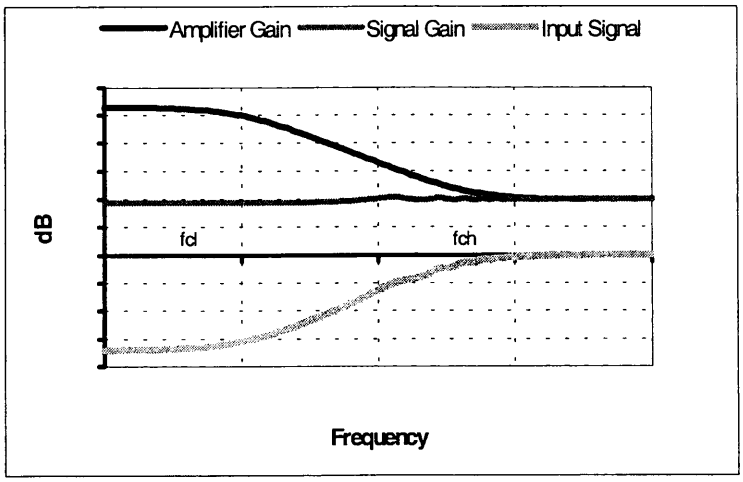


Figure 20: Gains in the ideal amplifier circuit

The ripple that appears before f_{ch} is caused by the fact that the input impedance at that frequency is not yet Z_0 (characteristic impedance), so the transmission line is not well terminated, and therefore reflections occur at the input of the amplifier. However, as frequency increases, the input impedance approaches Z_0 and the ripple decreases until it eventually disappears.

2.4 OUTPUT FILTER

To eliminate the noise outside the 100 kHz to 40 MHz band, a 6th order gaussian band-pass is placed at the output of the circuit [1]. It is designed as a low-pass and a high-pass combination, instead of directly a band-pass, to reduce the total number of inductances used.

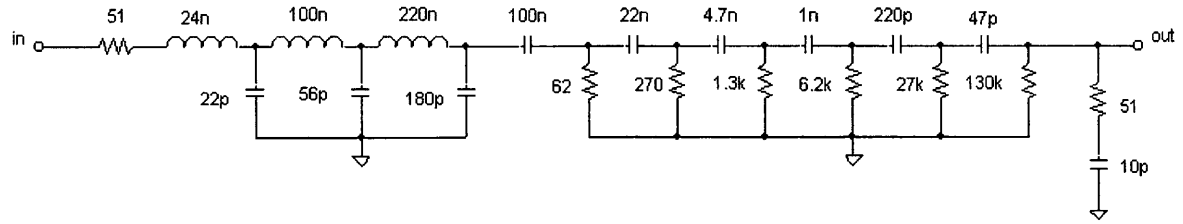


Figure 21: 10 kHz - 40 MHz band-pass filter

2.5 OUTPUT AMPLIFIER

A non-inverting amplifier has been placed at the output of the filter to avoid overloading it. The capacitance in series with the 30 Ω resistance provides DC unity gain, which reduces the output offset due to bias current.

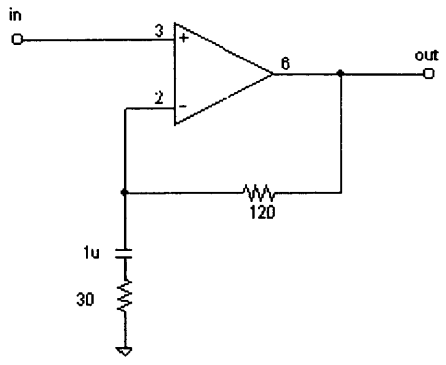


Figure 22: Output amplifier

3. PRACTICAL IMPLEMENTATION

In this chapter, all of the construction details are discussed: biasing, element values, etc...

3.1 FEEDBACK NETWORK

As was indicated in chapter 1, the input impedance of the amplifier must be a series RC, such as:

$$Z_{in} = 50\,\Omega + \frac{1}{jC_{in}\omega}$$

Figures 23 and 24 show respectively the signal available at the input of the amplifier and the input impedance for different values of C_{in}. Units are in dB with respect to 1Ω.

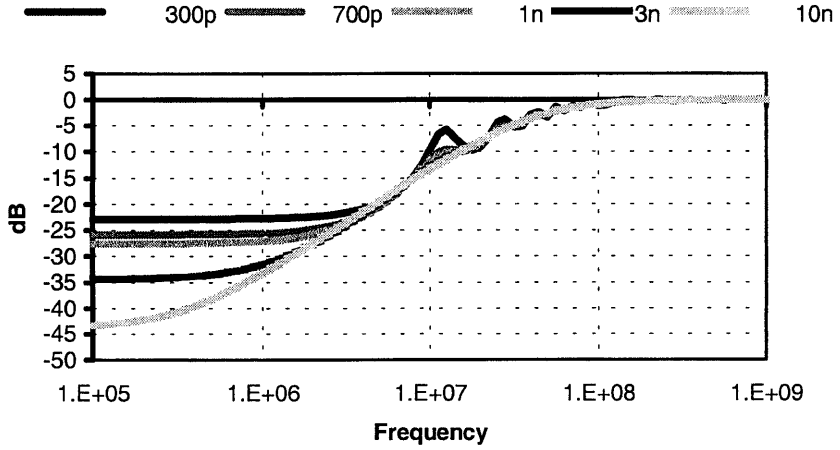


Figure 23: Signal at the input of the preamplifier

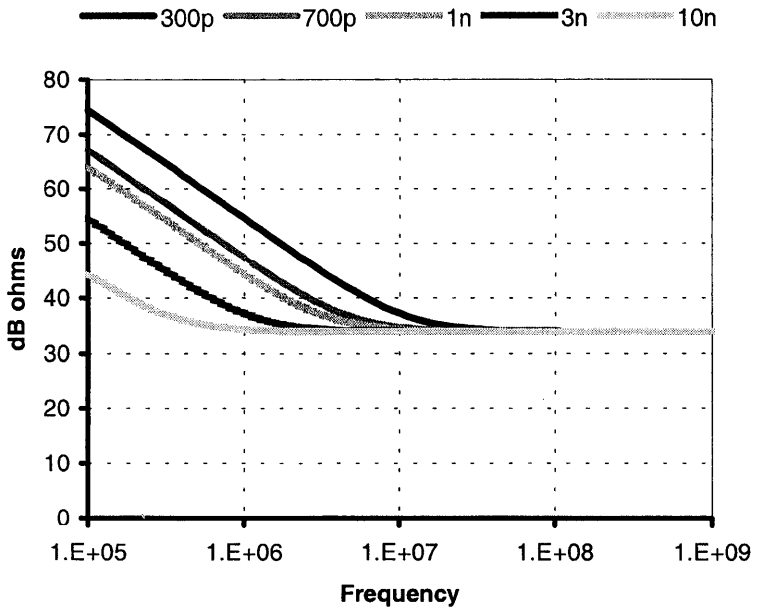


Figure 24: Input impedance of the preamplifier

The error at the input and the error in impedance at 12 MHz (where the maximum error occurs) are calculated for the following values of C_{in}.

Table 1: Impedance and input error

C_{in}	Maximum input error	Z_{in}	Z_{in} error
10 nF	1%	50.005	0.01 %
3 nF	4.2%	50.187	0.4 %
1 nF	16%	51.65	3.3 %
700 pF	28%	53.3	6.6 %

A value of C_{in} = 3 nF gives us the right compromise between a proper termination at HF and minimising the amount of signal loss at LF.

3.2 PREAMPLIFIER

The transistors used are the BF861C, a low noise JFET with a large high-frequency figure of merit g_m/C_{rss}, and the BFG540W, a low noise BJT with high transition frequency.

3.2.1 Number of JFETs per BJT cascode

From the BFG540W data sheet, the optimum collector current for low noise is 40 mA. And as it will be shown that the optimum I_D for the JFET is 10 mA, this gives 4 JFETs per cascode.

3.2.2 Number of cascodes

The number of cascodes is limited by bandwidth (BW) considerations. Stacking JFETs in parallel increases the input capacitance, and with 2 cascodes the required BW of 40 MHz is achieved.

3.2.3 DC biasing

Let us now study the DC biasing circuits used for the preamplifier:

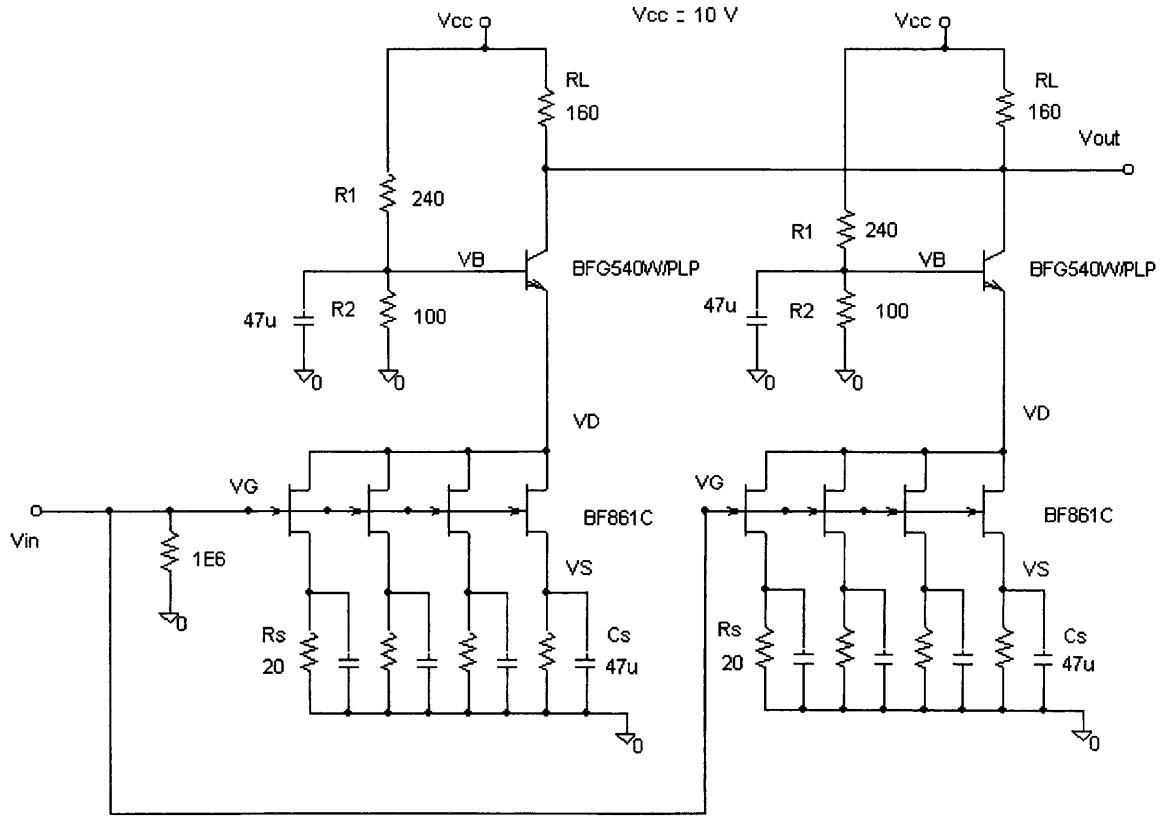


Figure 25: JFET preamplifier

3.2.3.1 JFET biasing

The value of R_S determines the current I_D flowing through the JFET and its transconductance.
The goal is to maximise transconductance to reduce noise, but taking into account the following considerations:

Can the BJT handle $4 \times I_D$ flowing through it?
The power dissipated in the JFET ($V_S \times I_D$) must be lower than 250 mW.
The dynamic range of the input increases (must not saturate output transistor).

From the BF681C "typical input characteristics" (I_D, V_{GS}), it can be seen that the transconductance gain reaches its maximum for small V_{GS}. For $V_{GS} = -0.2$ V, $I_D = 10$ mA and therefore $R_S = 20\ \Omega$.
The transconductance at this point is approximately 18.5 mS.

3.2.3.2 BJT biasing

The BJT base bias voltage divider ($R1$ and $R2$) determines the value of V_D. For the JFET to work as a current source (saturation area), V_D must be set so that $V_{DS} > V_P$ (pinch off voltage). From the data sheet, $V_{Pmax} = 2$ V, so $V_{DS} = 2$ V will guarantee that the JFET is in the saturation area.

$$V_D = V_B - 0.7 \geq 2.2 \text{ V}$$

With $V_{CC} = 10$ V, choosing 240 Ω and 100 Ω for the biasing resistors will satisfy these requirements.

The load resistance R_L is chosen to maximise circuit gain, but taking into account that:

The dissipation in BJT must be kept below 250 mW.
It is desirable to maximise the dynamic range.

Since $V_S = 0.2$ V, the input will always have to be under 0.2 V ($V_{GS} < 0$ for a JFET).

Regardless of dynamic range considerations, the maximum value of R_L is given by

$$R_L = \frac{V_{CC} - V_D}{I_D} = 195\ \Omega$$

For a given maximum input of 0.1 V, the gain of the preamplifier circuit is:

$$\frac{v_{out}}{v_{in}} = g_{mT} \cdot R_L = 4 \cdot g_m \cdot R_L = 4 \cdot 18.5 \text{ mS} \cdot R_L = 74 \text{ mS} \cdot R_L$$

$$0.1 \cdot Gain < \text{BJT dynamic range}$$

$$0.1 \cdot g_m R_L \leq V_{CC} - I_D R_L - V_S$$

Solving for R_L

$$R_L < 164\ \Omega$$

So R_L can still be increased if we sacrifice some dynamic range.

Minimum R_L is determined by the maximum power dissipation allowed on the BJT. The data sheet of the BFG540W specifies 500 mW, but the power dissipation limit will be established at 250 mW to prevent the BJT from heating up excessively. At 250 mW, with $I_C = 40$ mA (4 JFETs), $V_{CEmax} = 6.25$ V.

$$V_{CC} - I_D R_L - V_S < V_{CE\max}$$

Solving for R_L,

$$R_L > 40\ \Omega$$

Finally $R_L = 160\ \Omega$ is chosen because it gives the highest gain and it is the closest standard value to 164 Ω.

3.3 SHAPING AMPLIFIER

The current feedback amplifier chosen is the CLC 449, due to its low noise characteristics, large BW (1.2 GHz at gain of +2) and its stability at unity gain. As a compromise between maximum BW (smaller gains) and maximum stability (higher gains give a larger phase margin), the minimum gain is $A_v = 5$.

3.3.1 Resistor network

The resistor values are chosen as low as possible to reduce their noise effects.

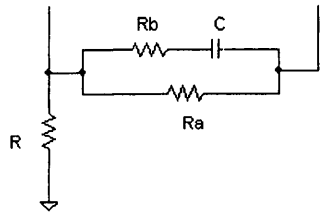


Figure 26: Resistor network for the shaping amplifier

For the CLC449, the feedback resistors have a minimum recommended value of 100 Ω for gains $A_v \geq 4$. This is the value chosen for R_b. The gain of the shaping amplifier, as described in the previous chapter, is:

$$Gain_{ShapingAmplifier} = \left(1+\frac{R_a}{R}\right) - \frac{1+j\omega C\left(\frac{R_aR_b+R_aR+R_bR}{R+R_a}\right)}{1+j\omega C(R_a+R_b)}$$

Since $R_a >> R_b$ the low cut-off frequency can be approximated by:

$$f_{CL} = \frac{1}{2\pi R_a C}$$

And, since

$$\frac{R_aR_b+R_aR+R_bR}{R+R_a} \approx \frac{R_a(R+R_b)}{R_a} \approx R+R_b$$

The high cut-off frequency can be approximated by

$$f_{CH} = \frac{1}{2\pi(R+R_b)C}$$

To obtain the minimum gain of 5, R = 25 Ω and R_b = 100 Ω.

The following values satisfy the preceding equations, giving f_{CL} = 1 MHz and f_{CH} = 45 MHz.

$$C = 30 \text{ pF}$$
$$R_a = 5.3 \text{ k}\Omega$$

3.3.2 Biasing

The bias resistance, placed at the non-inverting input of the operational amplifier (fig. 27), must be as large as possible to minimise its effect on the gain of the JFET circuit (R_L and R_{bias} are in parallel).

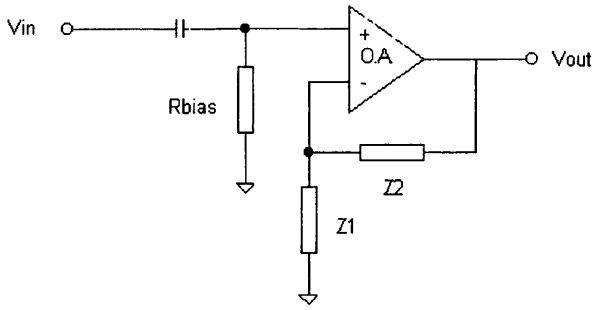


Figure 27: Shaping amplifier with bias resistor

Due to the fact that the gain of the amplifier is very large at low frequencies, a reasonably large R_{bias} produces a large offset output voltage. This effect is eliminated using DC unity gain, by adding a 5.3 kΩ resistor and a capacitor to Z_l. The resulting network is shown in fig. 28.

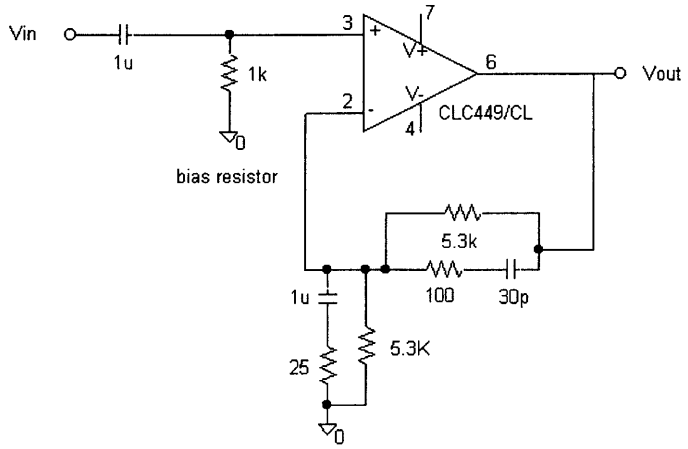


Figure 28: Shaping amplifier and biasing resistors

3.4 INPUT IMPEDANCE IMPROVEMENTS

The active impedance is an elegant solution to the noise problem, but its usefulness is limited at high frequency, due to the amplifier BW. The input impedance of the JFETs is capacitive, so its value decreases with frequency and therefore the reflections start to be very noticeable at higher frequencies.

To solve this problem, the input impedance of the circuit is raised only at HF with a paralleled LR, placed in series with the input of the pre-amplifier (fig.29).

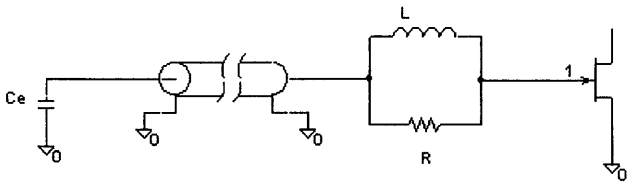


Figure 29: Circuit input with paralleled LR

R is equal to the characteristic impedance Z_0 (50 Ω) and L is chosen so that $2\pi fL$ = 50 Ω when f = 45 MHz (point where the impedance starts to decrease). This gives us L = 180 nH.

The results are shown in figures 30 and 31. Signal gain $\left(\frac{V_{out}}{V_{source}}\right)$

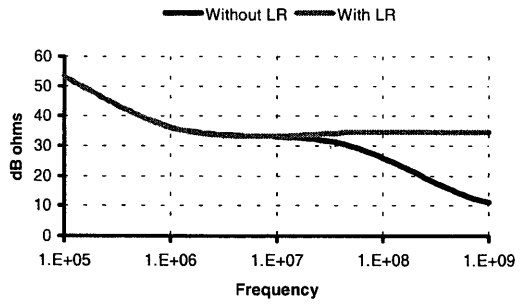


Figure 30: Input impedance, with and without LR

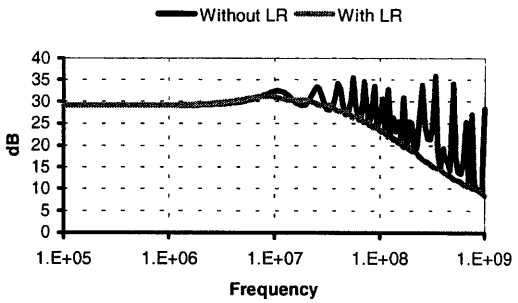


Figure 31: Signal gain, with and without LR

The improvement obtained by including a parallel LR in series is very noticeable.
The schematic of the final implementation is shown in figure 32.

3.5 IMPLEMENTED CIRCUIT

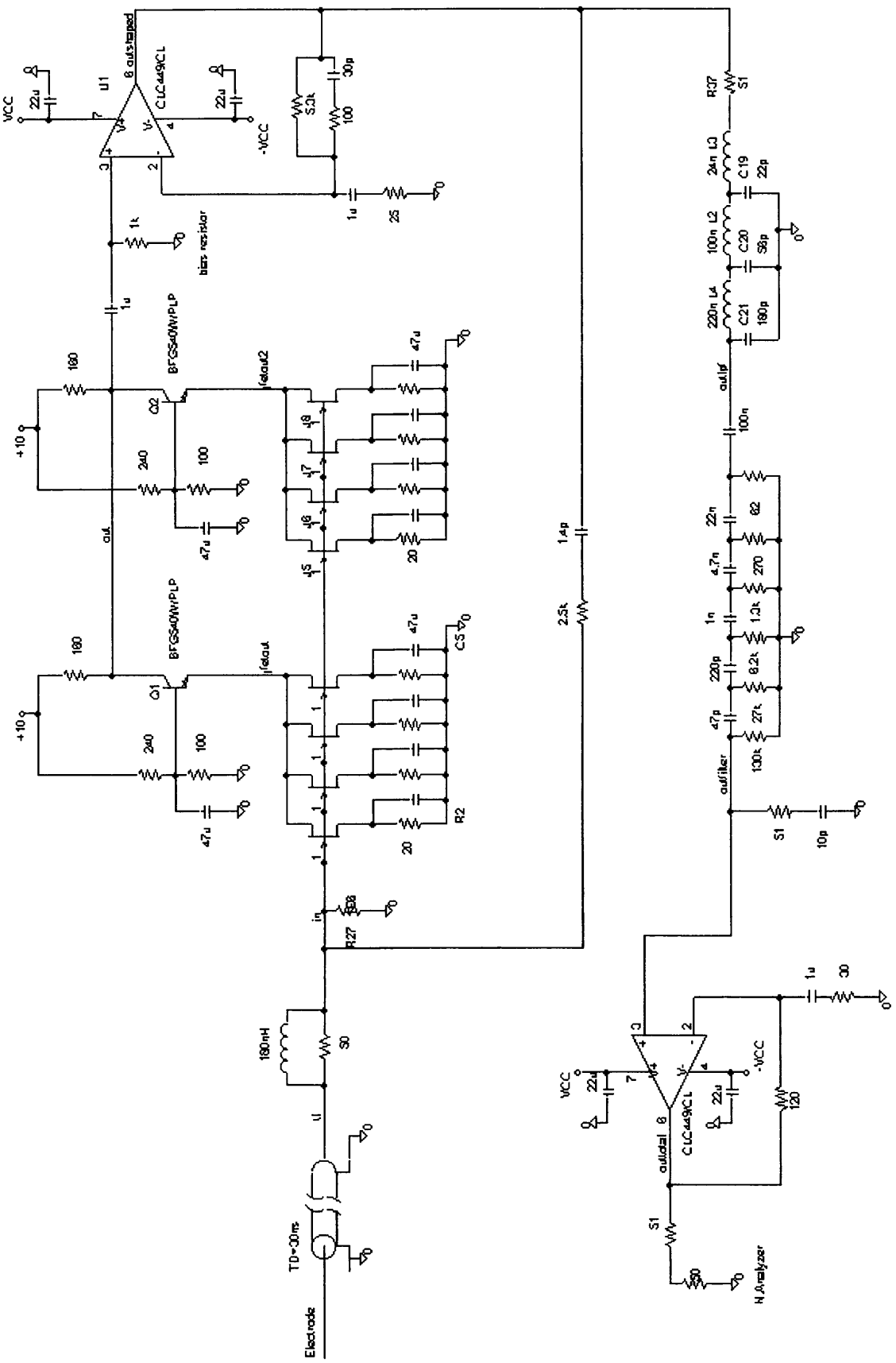


Figure 32: PU amplifier circuit

4. MEASUREMENTS

4.1 FREQUENCY RESPONSE

The frequency response has been measured using a test bench (fig 33) that emulates one of the PS pick-ups.

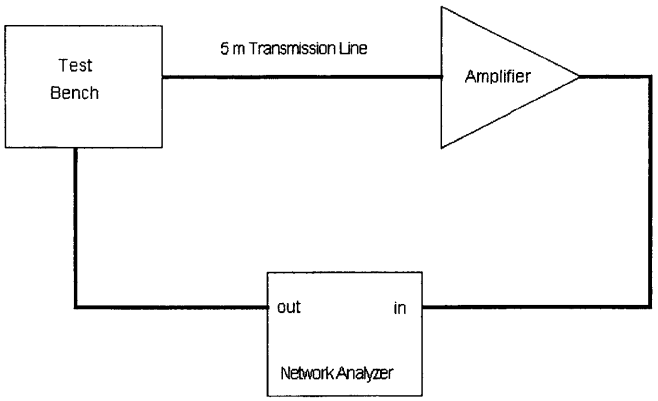


Figure 33: Frequency response measurement setup

The frequency response is

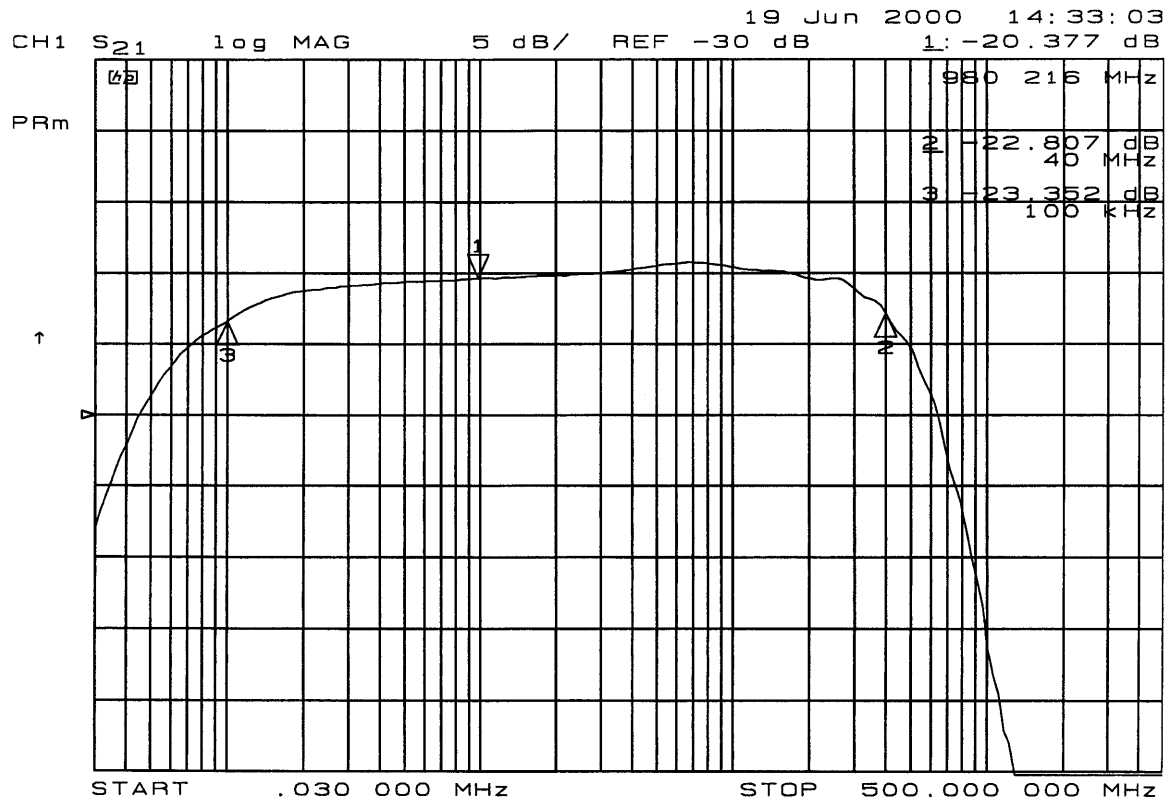


Figure 34: Frequency response

4.2 INPUT IMPEDANCE

The measurement setup for the input impedance is shown in figure 35.

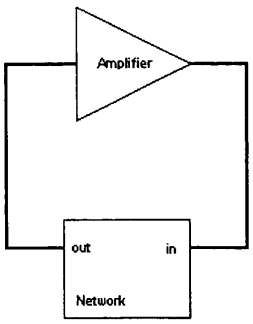


Figure 35: Input impedance measurement setup

The input impedance is within specifications. The corner frequency is very close to 1 MHz and, once the impedance reaches the resistive area (slope zero), the variations of resistance are under 1 dB up to 40 MHz and even beyond. The input impedance stays practically constant up to 500 MHz.

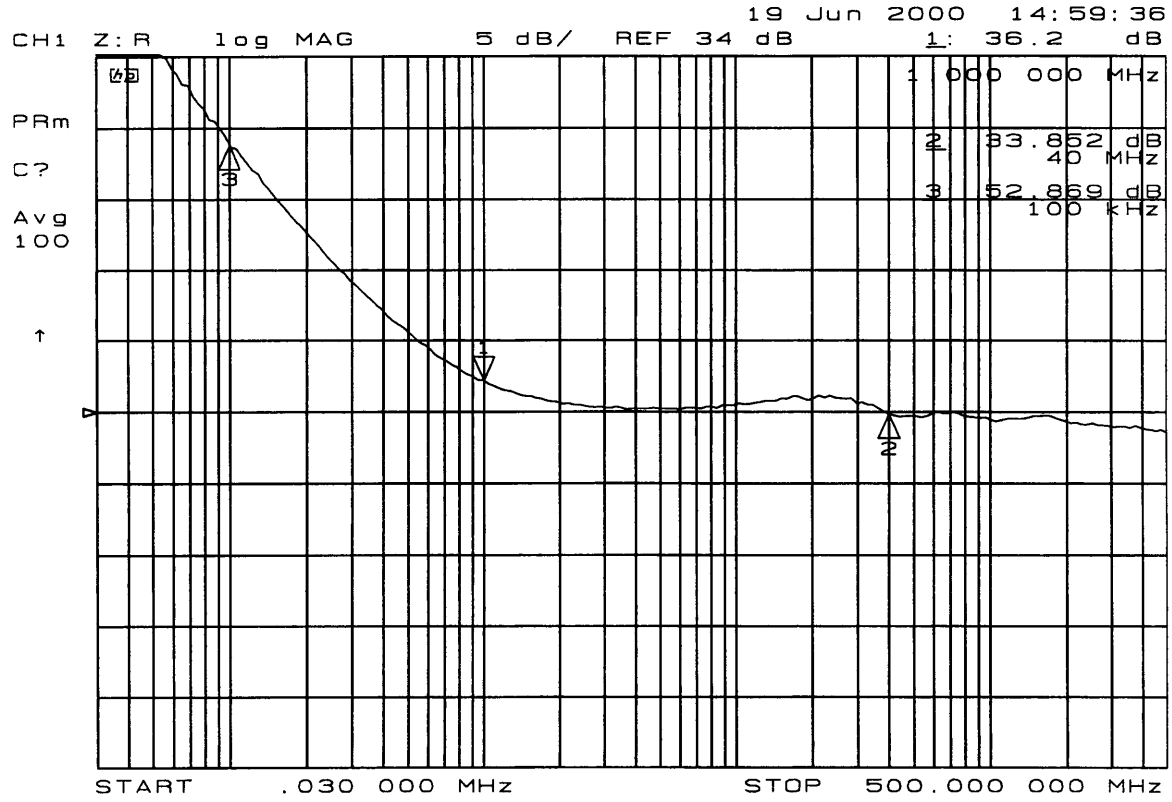


Figure 36: Input impedance (5 dBΩ scale)

The resistive value of the impedance is not quite 34 dB (50 Ω), but it has been retained because it has been determined experimentally to reduce the ringing of the pulse response.

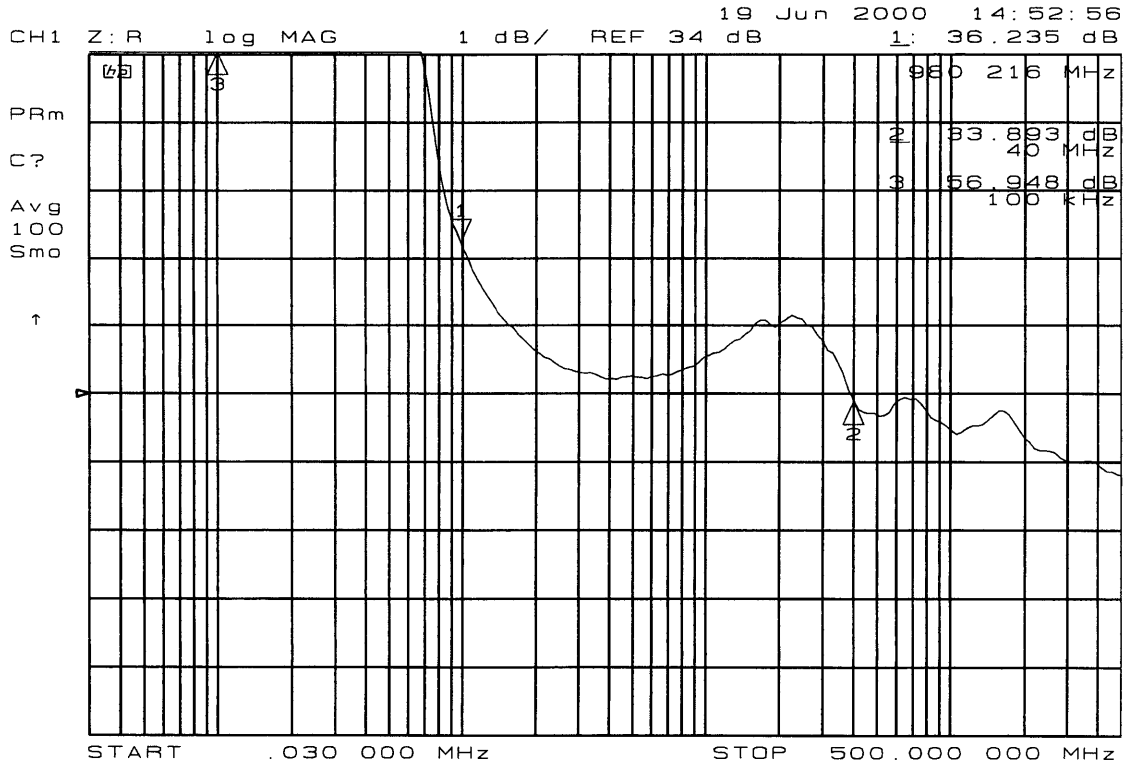


Figure 37: Input impedance (1 dBΩ scale)

The effect of the LR network in the input impedance is especially obvious in figure 38. The input impedance drops sharply after 40 MHz, due to the capacitive characteristic of the input impedance of the JFET preamplifier.

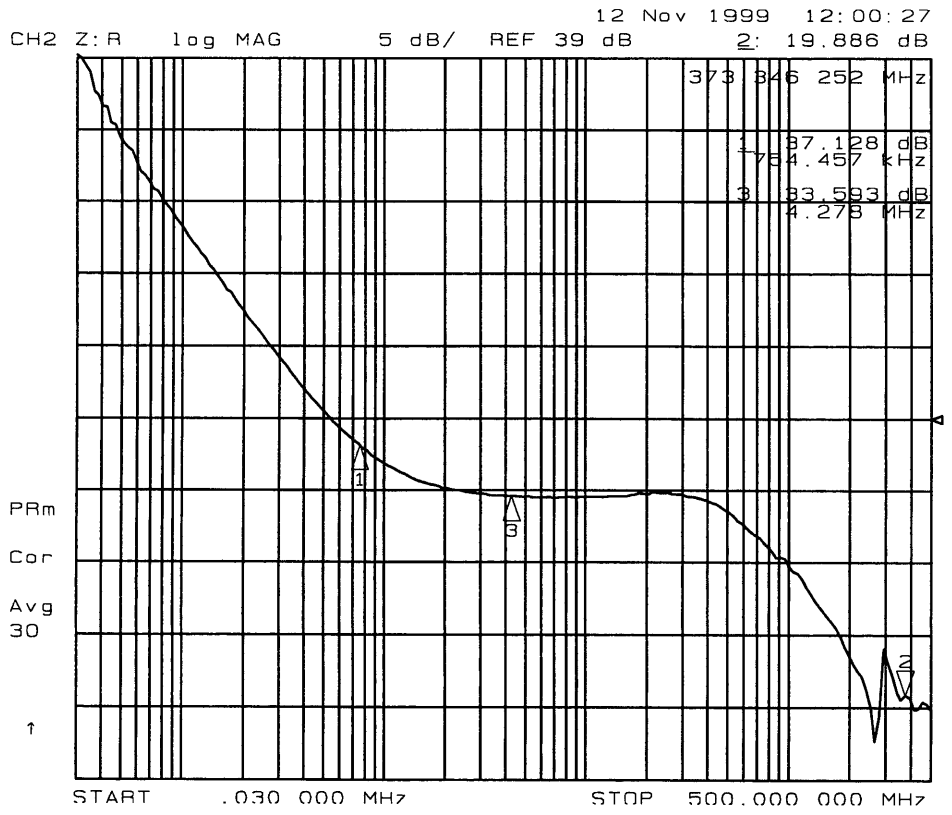


Figure 38: Input impedance, without LR

4.3 PULSE RESPONSE

The response of the amplifier to a 50 ns gaussian pulse (fig. 39 and 40) shows practically no undershoot, due to the good termination at high frequencies.

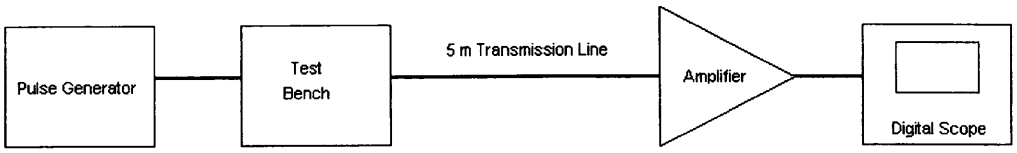


Figure 39: Pulse response measurement setup

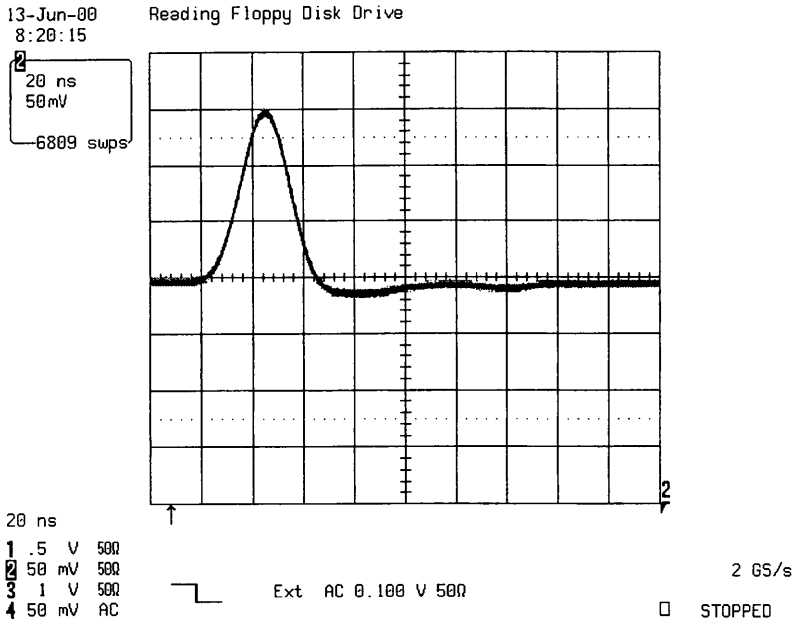


Figure 40: Gaussian pulse response

4.4 SENSITIVITY

Our laboratory is a very noisy room, and not the ideal place to measure sensitivity and noise, due to the large amount of signals coming from the accelerator that the circuit picks up directly via its input.

In order to check the sensitivity of the circuit the input signal to the PU test bench is attenuated until the output pulse is barely visible (fig. 42).

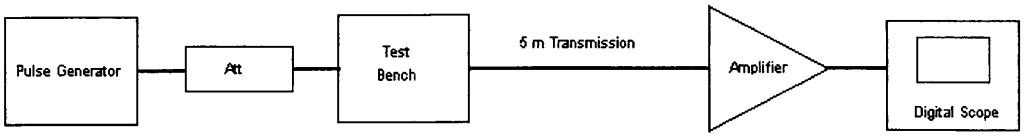


Figure 41: Sensitivity measurement setup

With no attenuation (fig. 40), the output pulse is 150 mV_p. Therefore, since the gain of the amplifier is 38 dB, the input pulse is 2 mV_p.

With 43 dB attenuation the output signal is still visible (fig. 42), which corresponds to an input signal of 14 μV_p.

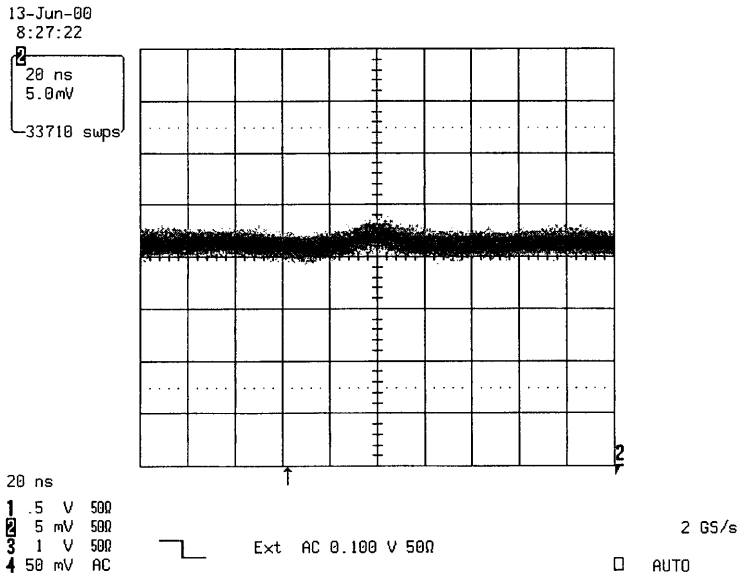


Figure 42: Output with 43 dB attenuation

When the attenuation is increased to 46 dB, the signal is not visible any more (fig. 43).

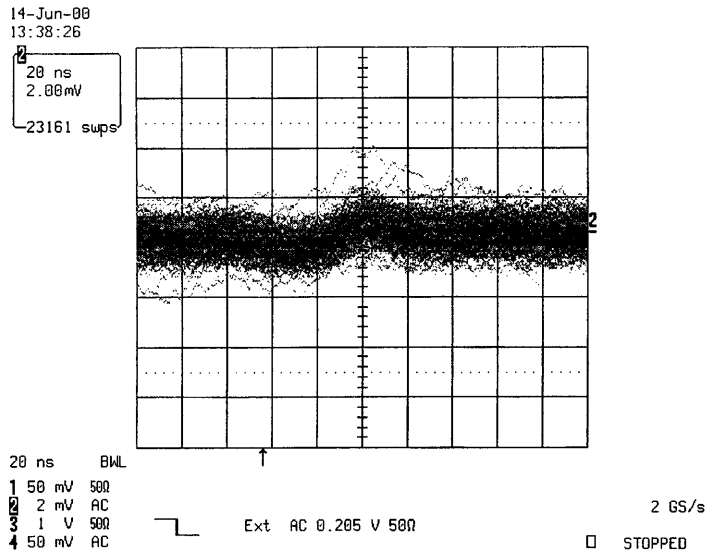


Figure 43: Output with 46 dB attenuation

4.5 NOISE

It is difficult to have a meaningful measurement of noise. For example, the measurement of Noise Figure, as used in many RF amplifiers, doesn't have much sense in this context, as the source is capacitive. For this reason it is also difficult to measure input equivalent noise. The only way to easily compare the performance of the amplifier with its predecessors is by measuring directly the output noise. This measurement must be interpreted with extreme caution, due to the fact that the lab environment is very noisy and has a noticeable influence in this output noise.

Using the tangential scope method [7], the measured output noise is 1.5 mV_{rms}.

Here is a measurement of the output noise; no signal was applied on the test bench.

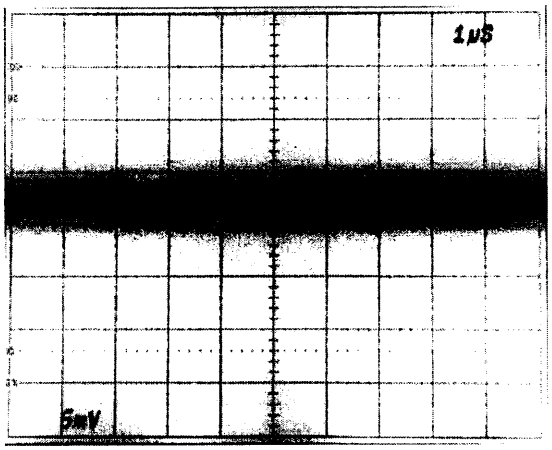


Figure 44: Output noise, as seen on the analogue scope

5. CONCLUSIONS

The behaviour of the implemented circuit is indeed satisfactory. Its measured characteristics accurately reflect the calculated ones, that is, its frequency response and input impedance follow very closely the specifications laid down in chapter 1.

The circuit has the same gain as the original CODD amplifier, but it is 12 dB more sensitive, however it does not match the sensitivity of the amplifier designed by Thomas Baglin [1]. In order to better compare the performance of the cascode topology with the complementary darlington, a board containing both amplifiers is going to be implemented. The choice of one of the two topologies will be done according to the conclusions extracted from this comparison.

The easiest and most immediate improvement consists in replacing the CLC449 shaping amplifier with a CLC425. Indeed, even further improvement can be expected if, instead of an operational amplifier, discrete components are used.

It is also interesting to note that the maximum amount of signal available at the input of the amplifier is ultimately limited by the capacitance of the transmission line, therefore a transmission line with lowest capacitance would be best suited.

6. ACKNOWLEDGEMENTS

We would like to thank Lars Soby and Carlota Gonzalez for introducing us to the cascode amplifier configuration.
Thanks also go to Jean-Marc Digonzelli for all his help in the lab.

7. REFERENCES

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[5] Horowitz, Hill, "The Art of Electronics", Cambridge University Press, Second Edition.

[6] Michael Steffes, "Noise Analysis for Comlinear's Op Amps", Application Note OA-12, Comlinear Corporation, Solutions with speed, 1993-1994.

[7] Jos De Neef, "Le bruit électronique et sa mesure", Electronique Applications N8, pages 37-50.

ANNEX 1: DETAILED NOISE ANALYSIS

The goal of this section is to analyse the contribution of each stage of the pick-up amplifier to the total noise of the circuit. To achieve this, all noise sources in each stage are taken into account and an expression for the input equivalent voltage and current noise sources will be found for each stage.
It is convenient for the noise analysis to consider the pre-amplifier and the shaping amplifier stages, as shown in figure 45.

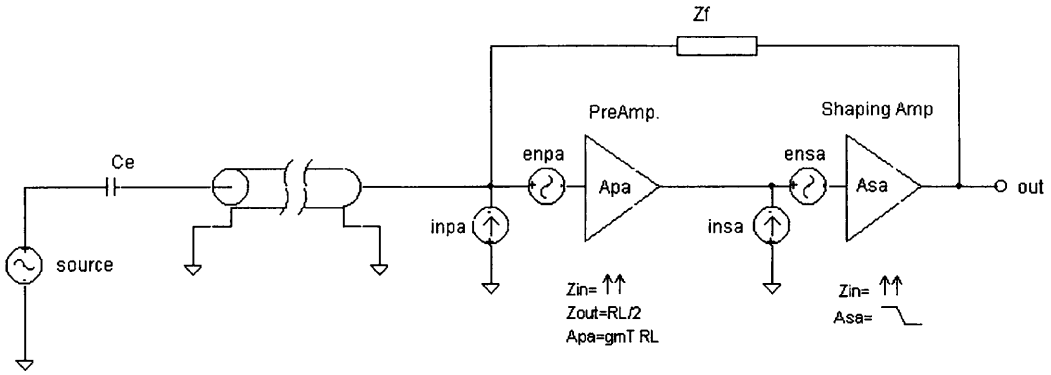


Figure 45: Amplifier with equivalent noise sources for each stage

A1.1 Preamplifier stage (cascode pair)

The AC equivalent circuit of the preamplifier stage is shown in figure 46. The first step is to calculate the individual noise of both active elements: the JFET and the BJT. Then, it will be shown why it is more advantageous to use a cascode pair than a single cascode. Finally, the contribution of the two BJTs to the output noise of the cascode pair will be calculated.

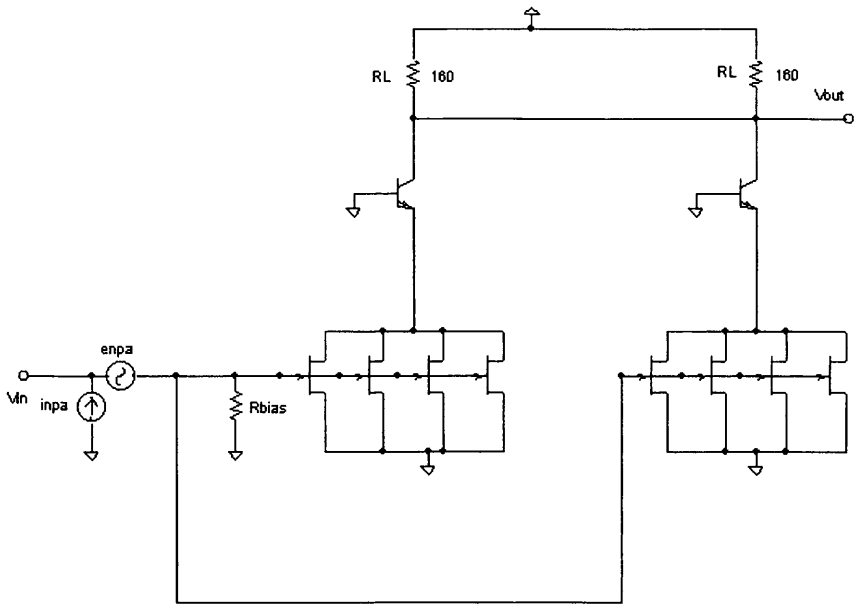


Figure 46: AC equivalent circuit of the preamplifier stage

A1.1.1 Contribution of the JFETs to output noise:

A1.1.1.1 Noise in a single JFET

The values of voltage and current noise sources for the *BF861C* are not available directly from the data sheet and thus must be calculated.

The voltage noise is given by

$$e_n = \sqrt{4kT\left(\frac{2}{3g_m}\right)}$$

From the data sheet, when the JFET is biased at I_D = 10 mA, the transconductance g_m is 18.5 mS. At 20°C, this gives:

$$e_n = 0.76\ \text{nV}/\sqrt{\text{Hz}}$$

The current noise is given by

$$i_n = \sqrt{\frac{4kT}{R_n}}$$

With

$$R_n = \frac{1}{\omega^2 g_m C_{rss} C_L R_L^{\ 2}}$$
$$C_L = C_{ds} + C_D$$
$$R_L = r_{ds} // R_D$$

The data sheet gives g_{os} and b_{os}

$$Y_{os} = g_{os} + b_{os} \cdot j = 0.2 \cdot 10^{-3} + 10^{-3}\, j$$
$$Z_{os} = \frac{1}{Y_{os}} = r_{ds} + \frac{1}{jC_{ds}\omega}$$
$$C_{ds} = 3.31\ \text{pF}$$
$$r_{ds} = 190\ \Omega$$

and, for V_{GS} = –2 V, the data sheet gives

$$C_{rss} = 2.25\ \text{pF}$$

R_D is the input resistance of the common base BJT, that is r_e'

$$r_e' = \frac{25\ \text{mV}}{I_E} = \frac{25\ \text{mV}}{40\ \text{mA}} = 0.625\ \Omega$$

C_D is the input capacitance of the common base BJT, which is negligible. Therefore,

$$R_L = r_e' // r_{ds} \approx r_e'$$
$$C_L = C_{ds} + C_D \approx C_{ds}$$

Finally, at 20°C,

$$R_n = 188\ \text{M}\Omega$$

and

$$i_n = 9.3\ \text{fA}/\sqrt{\text{Hz}}$$

A1.1.1.2 N JFETs in parallel

It can be shown that 4 JFETs in parallel behave like one single JFET of larger geometry. Then, the double cascode circuit can be represented with only two FETs (fig. 47). In this case, (with g_m, C_{rss} and C_{ds} being the values of a single *BF861C* JFET) the equivalent JFET has the following properties:

$$g_{mT} = 4 \cdot g_m$$
$$C_{rssT} = 4 \cdot C_{rss}$$
$$C_{dsT} = 4 \cdot C_{ds}$$

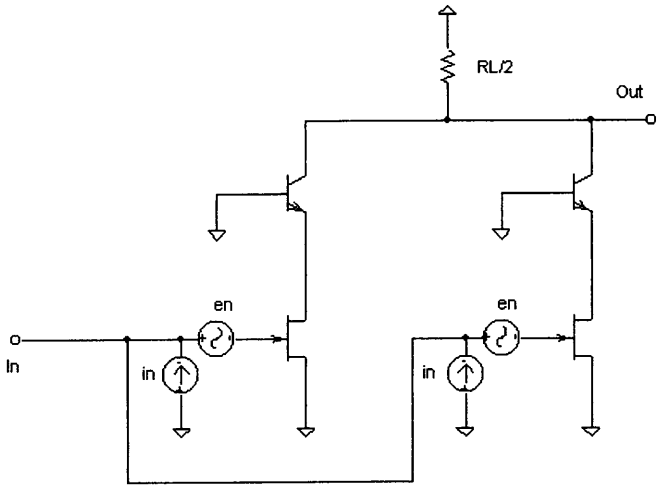


Figure 47: AC equivalent circuit with noise sources

Therefore the voltage and current noise are now:

$$e_{n4\,jfets} = \left.\frac{e_{n\,singlejfet}}{\sqrt{N}}\right|_{N=4} = \frac{e_{n\,singlejfet}}{2} = 0.38\,\text{nV}/\sqrt{\text{Hz}}$$

$$i_{n4\,jfets} = \sqrt{N} \times i_{n\,singlejfet}\Big|_{N=4} = 18.56\,\text{fA}/\sqrt{\text{Hz}}$$

A1.1.1.3 Advantages of using a cascode pair

Let us demonstrate that connecting two cascodes reduces the contribution of the JFETs to the total output noise. To do this, all the elements, except the JFETs, are idealised as noise free, and the input equivalent noise of the circuit is calculated. Then this is compared to the idealised single cascode, in which all the output noise would be caused by the JFET and therefore the input equivalent noise of the cascode can be represented by the current and voltage noise sources of the JFET.

The total gain of the cascode pair is $A_v = g_m R_L$.

- Contribution of e_n

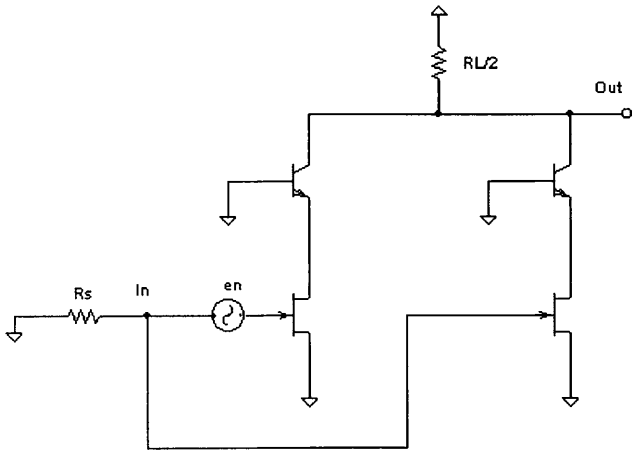


Figure 48: JFET voltage noise source

As the input impedance of the JFET is much larger than R_S, the voltage drop in this resistance is negligible and the second JFET is therefore off, giving

$$v_{out} = -g_m e_n \frac{R_L}{2}$$

As the circuit is symmetric, the output due to the other JFET voltage noise source is the same, and therefore:

$$v_{out}^2 = 2g_m^2 e_n^2 \left(\frac{R_L}{2}\right)^2$$

- Contribution of i_n

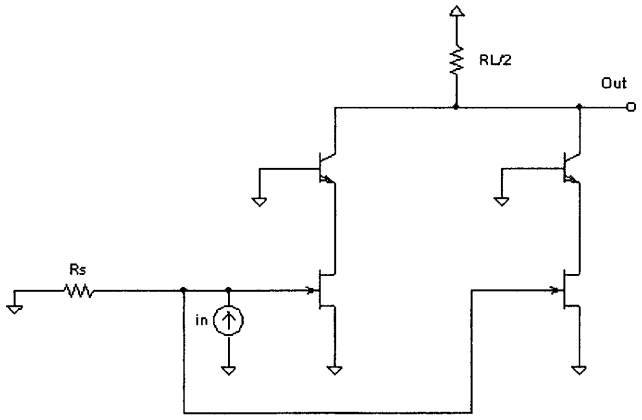


Figure 49: JFET current noise source

Since the input impedance of the JFETs is much larger than R_S, all the current flows through this resistance and

$$v_{out} = -g_m R_L i_n R_S$$

And, due to symmetry, the effect of the other JFET current noise source is the same, therefore:

$$v_{out}^2 = 2g_m^2 R_L^2 i_n^2 R_S^2$$

The equivalent input noise is found by dividing the total output noise by the circuit gain A_v

$$e_{ni}^2 = \frac{2g_m^2 e_n^2 \left(\frac{R_L}{2}\right)^2 + 2g_m^2 R_L^2 i_n^2 R_S^2}{g_m^2 R_L^2} = \frac{e_n^2}{2} + 2i_n^2 R_S^2$$

To compare the input noise of the cascode pair with that of a single cascode, it is best to calculate the equivalent input voltage and current noise, which are the parameters required to completely represent amplifier noise and use those as a comparison. The total equivalent input noise e_{ni}^2 has been calculated previously. The voltage and current noise can be derived from the general amplifier noise equation that relates them all:

$$e_{ni}^2 = e_{R_s}^2 + e_n^2 + i_n^2 R_S^2$$

From this formula

$$e_n^2 = e_{ni}^2\Big|_{R_S=0}$$

$$i_n^2 = \lim_{R_S \to \infty} \frac{e_{R_s}^2 - e_n^2 - i_n^2 R_S^2}{R_S^2} = \lim_{R_S \to \infty} \frac{e_{ni}^2}{R_S^2}$$

In our particular analysis all the elements, except the JFET transistors, have been supposed noise free; so the noise from the resistance R_S is zero and therefore

$$e_{n_{cascodepair}}^2 = \frac{e_n^2}{2}$$

$$i_{n_{cascodepair}}^2 = \lim_{R_S \to \infty} \frac{\left(e_n^2/2\right) + 2i_n^2 R_S^2}{R_S^2} = 2i_n^2$$

So it is evident that a cascode pair reduces the voltage noise, while increasing the current noise.

A1.1.2 Contribution of the BJTs to output noise:

In the BJT literature, the formulas to obtain the input voltage and current noise values are valid for the common emitter case. Unfortunately, in the cascode case, the BJT is in common base configuration, therefore the input is no longer the base but the emitter and the value of output noise will have to be calculated taking into account the individual noise sources inside the transistor.

A1.1.2.1 Output noise for a single cascode

A simplified π model of a BJT transistor including the noise sources is depicted in figure 50.

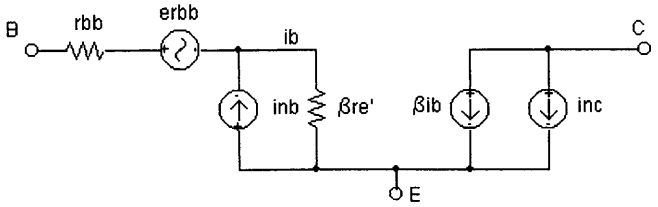


Figure 50: BJT π model with noise sources

With i_{nb} Shot noise given by $\sqrt{2qI_B}$

i_{nc} Shot noise given by $\sqrt{2qI_C}$

e_{rbb} Thermal noise given by $\sqrt{4kTr_{bb}}$

e_{RL} Thermal noise given by $\sqrt{4kTR_L}$

In the cascode, the BJT is in common base configuration and, as the output impedance of a JFET is very large, the circuit can be represented as in figure 51.

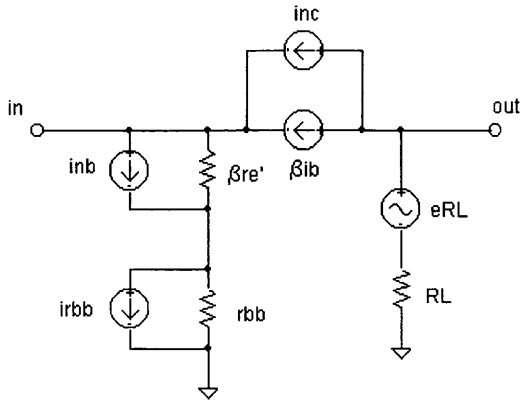


Figure 51 BJT π model in common base

Let us analyse, by superposition, the contribution of the different BJT noise sources on the output of a single cascode

- Contribution of i_{nb}: $\sqrt{2qI_B}$

From figure 51 and only taking into account i_{nb}

$$output \equiv e_{no_{IB}} = -\beta \cdot i_b \cdot R_L$$
$$i_b - i_{nb} = -\beta i_b$$
$$i_b = \frac{i_{nb}}{\beta + 1}$$
$$e_{no_{IB}} \approx -R_L i_{nb}$$
$$e^2_{no_{IB}} \approx R_L^2 i^2_{nb}$$

For R_L = 160 Ω and I_B = 344 μA (β ≈ 120), $e^2_{no_{IB}}$ = 2.86 10^{-18} V^2/Hz

- Contribution of e_{rbb}: $\sqrt{4kTr_{bb}}$

$$output \equiv e_{no_{rbb}} = \beta \cdot i_b \cdot R_L$$
$$i_b = \beta \cdot i_b$$
$$Therefore\ i_b can\ only\ be = 0$$

Then, e_{rbb} has no influence in the output noise.

- Contribution of i_{nc}: $\sqrt{2qI_C}$

$$output \equiv e_{no_{IC}} = -(\beta\, i_b + i_{nc})R_L$$
$$i_b + \beta\, i_b = -i_{nc}$$
$$e_{no_{IC}} = -(\beta \frac{-i_{nc}}{\beta + 1} + i_{nc})R_L$$
$$e^2_{no_{IC}} = i^2_{nc}(1 + \frac{\beta}{\beta + 1})^2$$

For β =120 and R_L = 160 Ω, $e^2_{no_{IC}}$ = 22.5 10^{-21} V^2/Hz

- Contribution of e_{nRL}: $\sqrt{4kTR_L}$

$$i_b = \beta \cdot i_b \rightarrow i_b = 0$$
$$output \equiv e_{no_{RL}} = e_{RL}$$
$$e^2_{no_{RL}} = 4kTR_L$$

For R_L = 160 Ω, $e^2_{no_{RL}}$ = 2.59 10^{-18} V^2/Hz

The total output noise is therefore

$$e^2_{no} = e^2_{no_{IB}} + e^2_{no_{IC}} + e^2_{no_{RL}} \approx e^2_{no_{IB}} + e^2_{no_{RL}}$$

A1.1.2.2 Output noise for a cascode pair

In the pick-up amplifier there is a cascode pair. Thus, both BJTs contribute e_{noIB} shot noise and, since the load resistance is R_L/2, the noise at the output of the cascodes is

$$e^2_{no} \approx 2e^2_{no_{IB}} + e^2_{no_{RL/2}}$$

with

$$e^2_{no_{IB}} = \left(\frac{R_L}{2}\right)^2 i^2_{nb}$$
$$e^2_{no_{RL/2}} = 4kT\frac{R_L}{2}$$

A1.1.2.3 Preamplifier equivalent input noise

Now that the design choices for the preamplifier have been justified, its equivalent input noise can be calculated.

$$e_{no}^2 = 2g_{mT}^2 e_{n4\,jfets}^2 \left(\frac{R_L}{2}\right)^2 + 2g_{mT}^2 R_L^2 i_{n4\,jfets}^2 R_S^2 + \left(\frac{R_L}{2}\right)^2 i_{nb}^2 + 4kT\frac{R_L}{2} + e_{R_S} g_{mT}^2 R_L^2$$

Dividing by the cascode pair gain $g_{mT} R_L$

$$e_{ni}^2 = \frac{e_{n4\,jfets}^2}{2} + 2i_{n4\,jfets}^2 R_S^2 + \frac{i_{nb}^2}{4g_{mT}^2} + \frac{2kT}{g_{mT}^2 R_L} + e_{R_S}$$

To obtain the preamplifiers (pa) equivalent input noise voltage and current sources:

$$e_{n_{pa}}^2 = e_{ni}^2\big|_{R_S=0} = \frac{e_{n4\,jfets}^2}{2} + \frac{i_{nb}^2}{4g_{mT}^2} + \frac{2kT}{g_{mT}^2 R_L}$$

$$i_{n_{pa}}^2 = \lim_{R_S \to \infty} \frac{e_{ni}^2}{R_S^2} = 2i_{n4\,jfets}^2$$

A1.2 Shaping amplifier stage

The main contributors to noise in this stage are the operational amplifier and the bias resistor (fig. 52). The feedback resistors have been chosen small to minimise their noise contribution, so their effect is neglected.

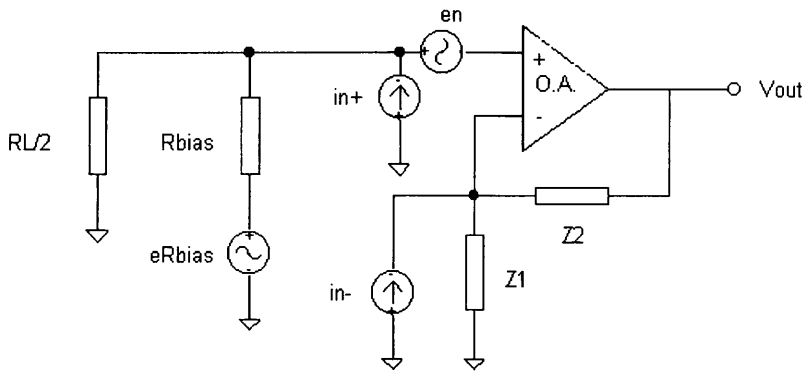


Figure 52: Shaping amplifier and associated noise sources

From the CLC449 data sheet

$$i_{n+} = 3\,\text{pA}/\sqrt{\text{Hz}}$$
$$i_{n-} = 15\,\text{pA}/\sqrt{\text{Hz}}$$
$$e_n = 2\,\text{nV}/\sqrt{\text{Hz}}$$

The output impedance of the cascode amplifier is $R_L/2$.

By superposition **[6]**, the contributions of the different noise sources are:

Contribution of i_{n+} $\quad V_{out} = i_{n+} \cdot \left(R_{bias} // \frac{R_L}{2}\right) \cdot A_{sa}$

Contribution of e_n $\quad V_{out} = e_n \cdot A_{sa}$

Contribution of i_{n-} $\quad V_{out} = i_{n-} \cdot R_a \quad with\, R_a = Z_1 // Z_2$

Contribution of e_{Rb}

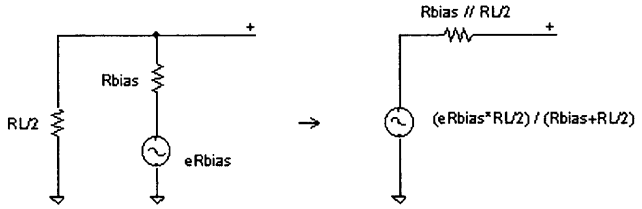


Figure 53: R_{bias} noise source and Thevenin equivalent

From the Thevenin equivalent (fig. 53) and since $R_{bias} >> R_L/2$, it can be easily deduced that the effect of R_{bias} is negligible. Note that the effect of $R_L/2$ has been taken into account in the preamplifier stage. Therefore, the total output noise is:

$$e_{no}^2 = \left(i_{n+} \cdot \left(R_{bias} // \frac{R_L}{2} \right) \cdot A_{sa} \right)^2 + (e_n \cdot A_{sa})^2 + (i_{n-} \cdot R_a)^2 \approx \left(i_{n+} \cdot \frac{R_L}{2} \cdot A_{sa} \right)^2 + (e_n \cdot A_{sa})^2 + (i_{n-} \cdot R_a)^2$$

Both i_{n-} and i_{n+} contribute in a much smaller proportion than e_n to the total output noise, and since i_{n+} is the smallest of the contributors the expression can be further simplified to

$$e_{no}^2 = (e_n \cdot A_{sa})^2 + (i_{n-} \cdot R_a)^2$$

So, the total input equivalent noise is

$$e_{ni}^2 = e_n^2 + \left(\frac{i_{n-} R_a}{A_{sa}} \right)^2$$

And therefore the noise from the amplifier can be totally characterised by a single voltage noise source at its input, with no current noise source. This voltage noise will be represented by:

$$e_{nsa}^2 = e_{ni}^2$$

A1.3 Circuit equivalent input noise

Now that the equivalent input noise sources for the preamplifier and the shaping amplifier stages have been calculated, it is time to calculate the pick-up amplifier total equivalent input noise at the signal source. This is done by referring all noise sources to the signal source location.

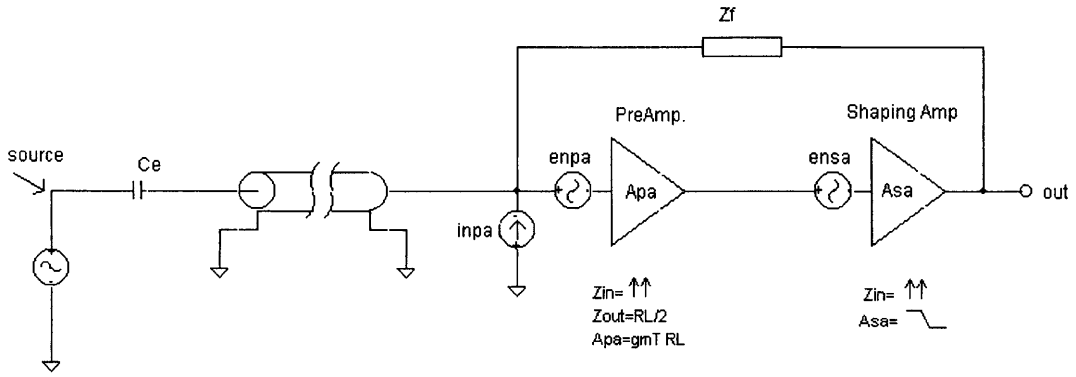


Figure 54: Amplifier stages and their respective noise sources

The circuit gain, seen from the source and calling $A = A_{pa} \cdot A_{sa}$, is

$$\frac{V_{out}}{V_{source}} = \frac{\frac{Z_f}{1+A}}{Z_S + \frac{Z_f}{1+A}} \cdot A = K$$

The total signal gain is designed to be a constant!

The output noise due to each noise source can be calculated by superposition.

A1.3.1 Contribution of the preamplifier stage voltage noise source

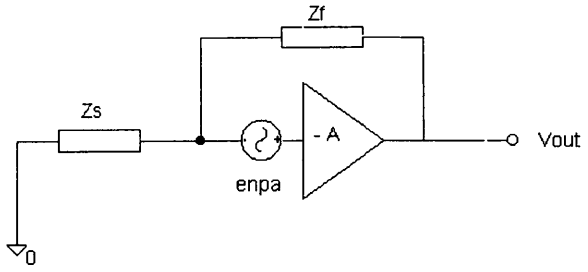


Figure 55: Effect of the preamplifier voltage noise source

$$v_{out} = \frac{-(Z_S + Z_f)A}{Z_S(A+1) + Z_f} e_{n_{pa}}$$

If Z_S is sufficiently large, so that the product $Z_S(A+1)$ is much larger than Z_f, the equation reduces to

$$v_{out} = \left(1 + \frac{Z_f}{Z_S}\right) e_{n_{pa}}$$

At lower frequencies, Z_S can be approximated by a capacitance C_s and $Z_f = R_f + 1/(jC_f\omega)$, therefore

$$v_{out} = \left(1 + \frac{R_f + \frac{1}{jC_f\omega}}{\frac{1}{jC_S\omega}}\right) e_{n_{pa}} = \ldots = \left(1 + \frac{C_S}{C_f}\right)\left(1 + j\omega R_f \frac{C_S C_f}{C_S + C_f}\right) e_{n_{pa}}$$

since C_f is much smaller than C_S, it can be further reduced to

$$v_{out} = \left(1 + \frac{C_S}{C_f}\right)\left(1 + j\omega R_f C_f\right) e_{n_{pa}}$$

A1.3.2 Contribution of the preamplifier stage current noise source

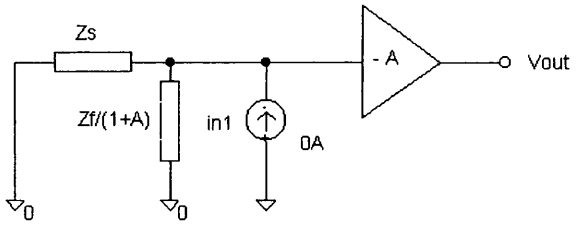


Figure 56: Effect of the preamplifier current noise source

$$v_{out} = -i_{n_{pa}}\left(Z_S // \frac{Z_f}{1+A}\right)\cdot A = \left(-A\frac{Z_S Z_f}{Z_f + Z_S(1+A)}\right) i_{n_{pa}}$$

If Z_S is sufficiently big, so that the product $Z_S(1+A)$ is much larger than Z_f, the equation reduces to

$$v_{out} \approx -i_{n_{pa}} Z_f = \left(R_f + \frac{1}{jC_f\omega}\right) i_{n_{pa}} = \left(\frac{1+j\omega R_f C_f}{jC_f\omega}\right) i_{n_{pa}}$$

Finally the output noise due to the preamplifier stage is

$$e_{no}^2 = e_{n_{pa}}^2\left(1+\frac{Z_f}{Z_S}\right)^2 + i_{n_{pa}}^2 Z_f^2$$

A1.3.3 Contribution of the shaping amplifier stage voltage noise source

The input impedance of the shaping amplifier stage is much larger than the output impedance of the preamplifier stage, which is $R_L/2$, therefore the output noise of the shaping amplifier is

$$e_{no}^2 = e_{n_{sa}}^2 A_{sa}^2$$

A1.3.4 Total output noise

The total output noise is calculated by summing each contribution in mean square values

$$e_{no}^2 = e_{n_{pa}}^2\left(1+\frac{Z_f}{Z_S}\right)^2 + i_{n_{pa}}^2 Z_f^2 + e_{n_{sa}}^2 A_{sa}^2$$

To obtain the output noise, a PSpice simulation has been used, which gives the results of figure 57. Observe that the effect of current noise is dominant up to 500 kHz and the effect of e_n is noticeable at higher frequencies. It is the transmission line that causes the ripple observed at higher frequencies.

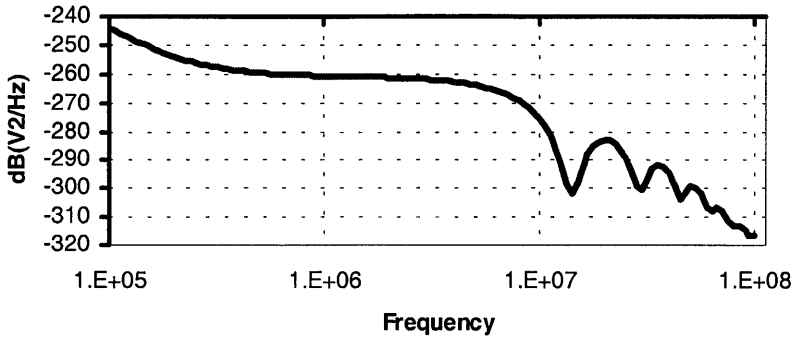


Figure 57: Pick-up amplifier total output noise power

A1.3.5 Input equivalent voltage noise

To obtain the input equivalent voltage noise, the output noise is divided by the signal gain. Using the fact that

$$\frac{V_{out}}{V_{source}} = K$$

$$e_{ni}^2 = \frac{1}{K^2}\left(e_{n_{pa}}^2\left(1+\frac{Z_f}{Z_S}\right)^2 + i_{n_{pa}}^2 Z_f^2 + e_{n_{sa}}^2 A_{sa}^2\right)$$

The theoretical input equivalent noise, calculated using PSpice, is plotted on figure 58.

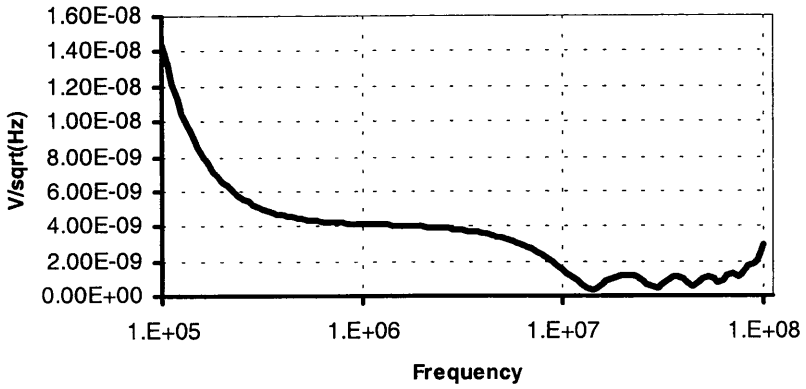


Figure 58: Input equivalent noise

A1.3.6 Conclusions

1. - The noise e_{nsa}, from the shaping amplifier, has a noticeable effect because $e^2_{n_{sa}}$ is of the same order of magnitude as $e^2_{n_{pa}}\left(1+\frac{Z_f}{Z_S}\right)^2$.

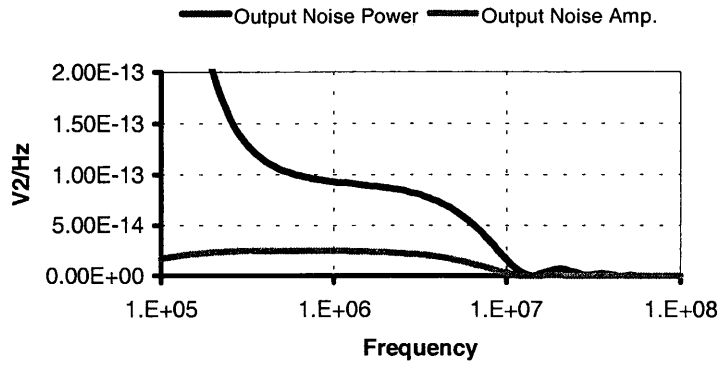


Figure 59: Operational amplifier noise and total noise

The voltage noise of the operational amplifier is the main constituent of e_{nsa}, therefore it would be advantageous to use an operational amplifier with lower e_n, such as the CLC425, or even to design the shaping stage with discrete components.

2. - Observing the individual noise contributors of the preamplifier

$$e^2_{n_{pa}} = \frac{e^2_{n4jfets}}{2} + \frac{i^2_{nb}}{4g^2_{mT}} + \frac{2kT}{g^2_{mT}R_L}$$

$$i^2_{n_{pa}} = 2i^2_{n4jfets}$$

It is obvious that increasing g_{mT} and R_L will reduce noise. However, these values have already been maximised during the design process and $e_{n4jfets}$ has also been minimised.

A1.4 Effect of input LR

There is a final element to be taken into consideration. As it has been explained in section 3.4, "input impedance improvements", the input impedance of the circuit is raised at HF by means of a paralleled LR, placed at the input. Obviously the resistance will have an increasing effect in the output noise as frequency raises. However, it is only noticeable above 10 MHz, where the total noise is at least 20 dB under the noise level of the 100 kHz to 10 MHz region, so its effect is hardly noticeable (fig. 60).

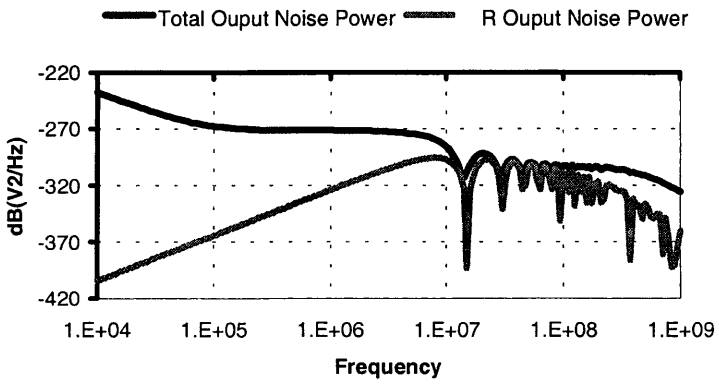


Figure 60: Effect on the input impedance of LR

ANNEX 2: INPUT IMPEDANCE ADJUSTMENT PROCEDURE

Once the amplifier is built, slight differences in the gain of the amplifier with respect to the theoretical gain will make it necessary to manually adjust the feedback RC to obtain the desired input impedance.

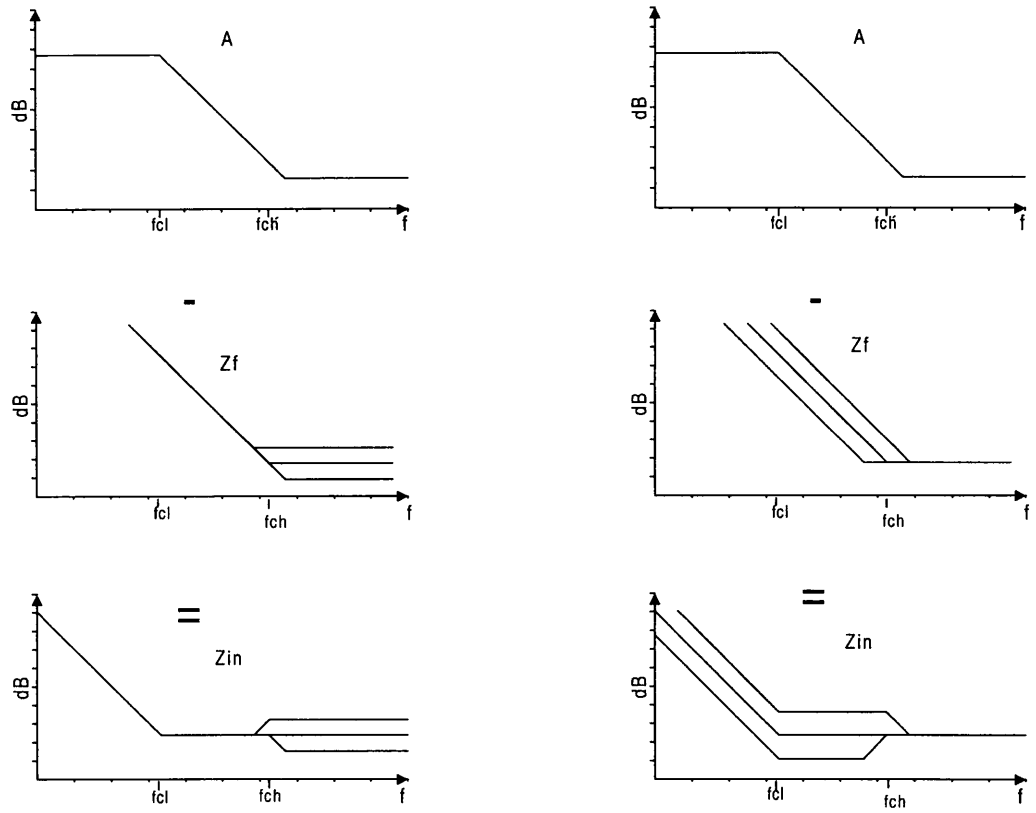
The purpose of this annex is to show the effect on the input impedance of the variation of either R or C in the hope of speeding up the tweaking process.

A2.1 Variation of resistance R

If the value of R is varied, only the final value of Z_f is modified (fig. 61-a), that is an area around f_{ch}, but the rest remains unchanged. Therefore the value of Z_{in} around f_{cl} will not be modified, it will stay at 50 Ω and only the value around f_{ch} will vary.

A2.2 Variation of capacitance C

It is the value of C that modifies the value of Z_{in} around f_{cl}, without affecting Z_{in} after f_{ch} (fig. 61-b).



a. Varying R in Z_{in} b. Varying C in Z_{in}

Figure 61: Effects of R and C in Z_{in}

If both R and C are adjustable it is easy to obtain the desired value of Z_{in} by modifying them independently.

ANNEX 3: INPUT TRANSFORMER

A transformer is a very useful device when trying to reduce the circuit equivalent input noise, because not only can it raise the signal level but it is also used for noise matching, by transforming the source resistance into the optimum resistance for low noise.

The reason why it is not used in the project is because the transformer together with the electrode capacitance and the transmission line capacitance create resonances within the BW of interest and it does not seem possible to eliminate or displace them.

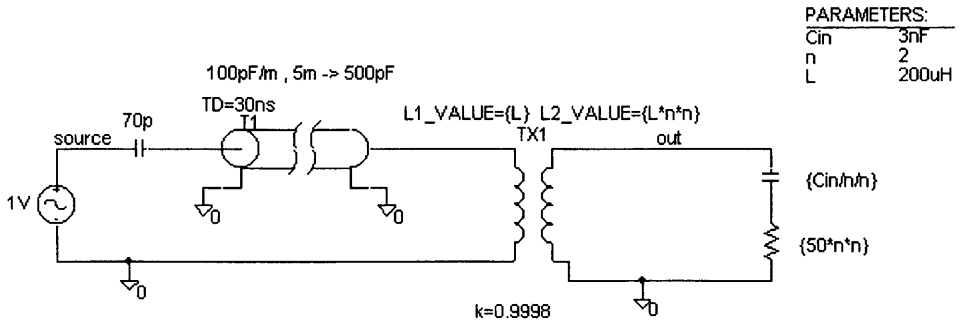


Figure 62: Equivalent circuit with transformer

The output signal, with the transformer and the ideal output signal are:

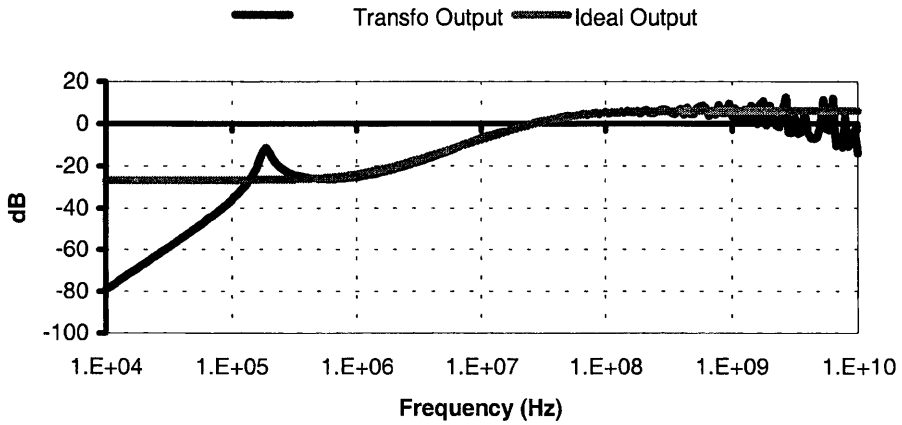


Figure 63: Output signal

A resonance can be observed at low frequencies around 190 kHz, and another resonance of much lower Q at around 70 MHz. The cause of these resonances can be determined by analysing the circuit in two separate areas, a low frequency area and a high frequency area.

The LF equivalent circuit seen from the secondary is:

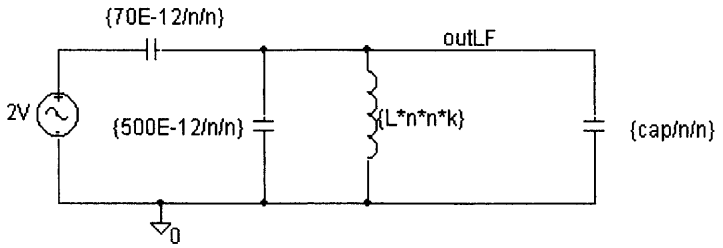


Figure 64: Low frequency equivalent circuit

If $C_1 = C_e/n^2$ and $C_2 = C_{LT}/n^2 + C_{in}/n^2$, the output of the circuit can be expressed as:

$$\frac{V_{out}}{V_{source}} = \frac{\dfrac{\dfrac{Ln^2k}{C_2}}{j\omega\, Ln^2k + \dfrac{1}{j\omega C_2}}}{\dfrac{1}{j\omega\, C_1} + \dfrac{\dfrac{Ln^2k}{C_2}}{j\omega\, Ln^2k + \dfrac{1}{j\omega\, C_2}}} = \frac{Ln^2kC_1(j\omega)^2}{Ln^2k(C_1+C_2)(j\omega)^2+1}$$

For C_{LT} = 500 pF and C_{in} = 3 nF, the resonance peak falls within the desired BW (100 kHz - 40 MHz):

$$f_{rLF} = \frac{1}{2\pi\cdot\sqrt{Ln^2k(C_1+C_2)}} \approx \frac{1}{2\pi\cdot\sqrt{Lk(C_{in}+C_{LT})}} = 190\text{ kHz}$$

The HF equivalent circuit, seen from the secondary, is:

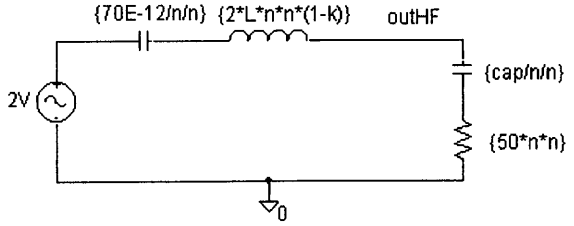


Figure 65: High frequency equivalent circuit

$$C_T = \frac{C_e\cdot C_{in}}{n^2(C_e+C_{in})} \approx \frac{C_e}{n^2}$$

Resonance peak is at

$$f_{rHF} = \frac{1}{2\pi\cdot\sqrt{2Ln^2(1-k)C_T}} \approx \frac{1}{2\pi\cdot\sqrt{2L(1-k)C_e}} = 68\text{ MHz}$$

How can these resonances be eliminated or moved out of harms way?
Let's first review their influences of the different elements on these resonances:

Elements	Effect
Lkn^2 $C_{LT}/n^2 + C_{in}/n^2 = C_2$	LF resonance peak
$2Ln^2(1\text{-}k)$ C_e	HF resonance peak

What possible ways are there to displace the resonances?

Solution	Effect
Make L bigger	Reduces both the LF and the HF resonances
Make C_{in} bigger	Reduces just LF resonance More signal is lost at LF
Make k closer to 1	Increases BW of transformer L can be increased to reduce the LF resonance

Increasing k has no drawbacks, except for it being technologically challenging. Using transmission line transformers, a value of k closer to 1 than 0.9999 can be obtained (and has been obtained). The problem is realising a transformer with a sufficiently large L to lower the LF resonance. The value of L required is around 700 μH, but it has been determined experimentally that the largest reasonable value of L is around 200 μH.