EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH
ORGANISATION EUROPEENNE POUR LA RECHERCHE NUCLEAIRE

CERN - PS DIVISION

PS/ BD/ Note 99-10

NEW HARDWARE OF THE TUNE MEASUREMENT SYSTEM FOR THE PROTON SYNCHROTRON BOOSTER ACCELERATOR

M. Gasior, J.L. Gonzalez

Abstract

This paper describes the tune measurement system, based on FFT analysis, for the 1.4 GeV CERN Proton Synchrotron Booster. We present the final version of the 14-bit ADC module, with its tracking filter, and the memory unit, which have been developed to improve the system capabilities and fulfil most recent machine requirements. The description and specification of both modules are presented. We also estimate system accuracy as well as dynamic range and show that it can provide good results, even with input signal amplitudes much lower than the voltage corresponding to one LSB of the ADC. This system is very flexible and, just changing a few components, it can also replace the obsolete tune measurement system of the 26 GeV Proton Synchrotron.

Geneva, Switzerland
15 September 1999

1. Introduction

The CERN 1.4 GeV Proton Synchrotron Booster (PSB) accelerates particles from a linear accelerator (LINAC) and either injects them into the 26 GeV Proton Synchrotron (PS) or sends them to the ISOLDE facility. It consists of four superposed 50-m-diameter rings.

This paper describes the tune measurement system, based on Fast Fourier Transform (FFT) analysis, for the PSB accelerator. We present the final version of the 14-bit ADC module, with its tracking filter, and memory unit, which have been developed to improve the system capabilities and fulfil most recent machine requirements **[1]**. The software part is to be described in a separate note **[2]**.

The description and specification of both modules are presented. We also estimate the system accuracy as well as the dynamic range and show that it can provide good results, even with input signal amplitudes much lower than the voltage corresponding to one LSB of the ADC.

This system is very flexible and, just changing a few components, it can also replace the obsolete tune measurement system of the PS **[3] [4]**.

2. Overview of the new PSB tune measurement system

The tune value, or so-called Q value, is one of the most important parameters that characterise an accelerator ring. It is the number of transverse betatron oscillations that particles perform about the closed orbit during one revolution around the machine. To measure the tune, it is usually necessary to excite the beam, using a kicker, in order to produce coherent oscillations that can be observed on electrostatic pick-ups, which are installed in the ring for both the horizontal and vertical planes. The frequency of the betatron oscillation f_β is related to the revolution frequency f_{rev} and the oscillation mode m by:

$$f_\beta = (m \pm Q) f_{rev} \tag{1}$$

For stability reasons, Q must not be an integer, but since its integer part remains constant (respectively 4 and 5 for the PSB horizontal and vertical planes, and 6 for both planes in the PS), it is sufficient to measure its fractional part q or $(1 - q)$. Considering the betatron oscillation frequency ranging from $0.1 \times f_{rev}$ to $0.5 \times f_{rev}$ and mode m (4, 5 or 6) leads to:

$$\frac{f_\beta}{f_{rev}} = q \quad \text{or} \quad (1-q) \tag{2}$$

which one, needs to be determined by other means. For the PSB and the PS, it is q in both planes.

Generally, the beam is not centred in the pick-up and the resulting signal spectrum contains f_β and f_{rev}, which both vary during acceleration. Then, a convenient way to calculate q is to digitise the signal at a rate proportional to f_{rev} and perform FFT analysis on N samples. Taking into account the sampling rate $k \times f_{rev}$ and the spectral line n_β that corresponds to the betatron frequency, equation (2) can be rewritten as:

$$q = k \frac{n_\beta}{N} \tag{3}$$

where n_β is the bin number corresponding to f_β, in the N point FFT spectrum,
k is the oversampling ratio, i.e. digitising clock = $k \times f_{rev}$.

Horizontal (H) and vertical (V) tune measurements can be performed separately, according to commands issued by an application program that runs on a workstation, which can display the results of a machine cycle in graphical format. This application communicates, via a network link, with the Device Stub Controller (DSC, based on a RIO8062 VME computer with PowerPC CPU) on which some real time tasks run continuously, under LynxOS. These tasks control all of the hardware in the DSC and download the program for the digital signal processor (Motorola's floating point DSP 96002), on the DBV96 VME board **[5]**. The block diagram of the system is shown in **figure 1**.

The TG8 timing generator delivers trigger signals for H and V channels at requested times, during the machine cycle. Each trigger is then synchronised, by the Burst and RF Trigger Generator modules **[6]**, to both the revolution frequency f_{rev} and the RF frequency f_{rf}, which is the frequency the beam is accelerated with. These triggers cause the kickers to produce power pulses that excite the beam during one revolution period.

The resulting beam oscillations are sensed by dedicated pick-ups. Each pick-up has two pairs of electrodes, one pair for each plane, and the beam position is measured by subtracting the signals of opposite electrodes. These signals can have quite different amplitudes because they are proportional to both the beam distance to the electrode and the beam intensity; the stable orbit can be offset significantly from the middle of the beam pipe. Most of this variation can be cancelled by means of a Beam Offset Signal Suppressor (BOSS) **[7]**, which adjusts the gain of each electrode channel prior to realising the difference, in order to get the beam position output signal containing the betatron frequency signal f_β.

Each of the four rings of the PSB, which are individually equipped with a pick-up and a BOSS, can be connected to the tune measurement system by means of an analogue multiplexer, controlled by the DSC via a standard I/O card. Since the beam intensity varies over a wide range, in order to make the most of the ADC input dynamics it is necessary to adjust the signal level before digitising it. This is done by means of a Gain Controlled Amplifier (GCA), which buffers the signal to the 14-bit NIM ADC.

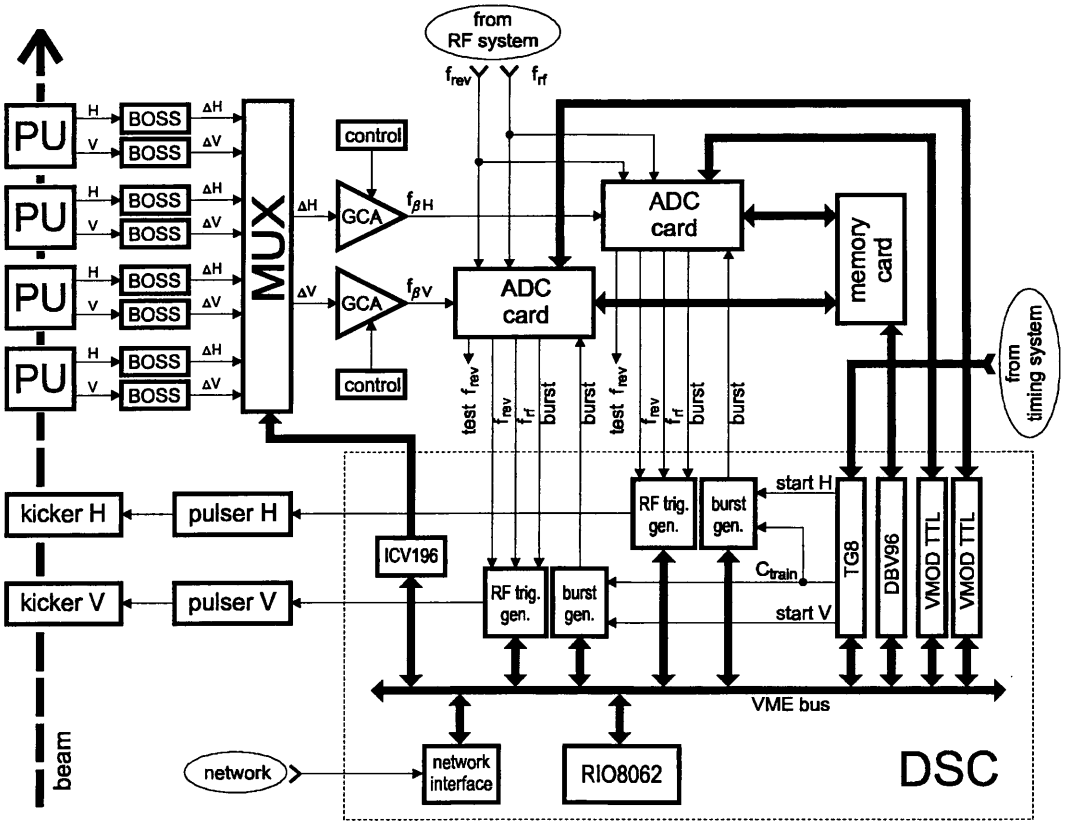

Fig. 1. Block diagram of the PSB tune measurement system. Abbreviations: BOSS – Beam Offset Signal Suppressor; DBV96 – DSP VME board with DSP96002/40MHz; DSC – Device Stub Controller; GCA – Gain Controlled Amplifier; ICV196 – general purpose I/O ports; RIO8062 – VME embedded computer with PowerPC 603e/166MHz processor; PU – pick-up, TG8 – timing generator; VMOD TTL – general purpose I/O ports.

The timings that initiate beam excitation also trigger data accumulation in two independent channels of the memory card, one for each plane. Then, the DSP board takes this data, performs FFT analysis and searches for the spectrum peak corresponding to f_β. After further interpolation of its position, which improves system resolutions by about one order of magnitude, q values from 0.1 to 0.5 are calculated according to equation (3) with $k = 4$, $N = 2048$ and n_β a real number ranging from 50 to 256.

When all required data are collected, they are sent to the DSC, which stores them for the main application program.

The DSP is capable of servicing one channel in less than 5 ms, thus q values for H and V planes can be obtained every 10 ms during a machine cycle. Furthermore, double buffering of data allows up to 5 ms delay between H and V acquisitions, so that one can test the coupling between both planes.

The ADC card can be switched to simulation mode using either its front panel switch or by means of the VMOD TTL standard I/O module **[8] [9]**. This allows easy testing of the system, because each ADC card can internally generate f_β, f_{rev} and f_{rf} signals.

3. 14-bit ADC module

3.1. Structure and operation

The ADC input dynamics must handle the level of the betatron signal, which is proportional to both the beam position oscillations caused by the kicker and the beam intensity that extends over a wide range. To improve system performance, previous 12-bit ADC has been replaced with a new 14-bit ADC. Since the LSB is about 300 μV, with 5 V full scale input range, the analogue part of this board must be perfectly isolated form the

digital part, which is to work with clock signals up to 8 MHz. Thus, analogue and digital grounds are separated and digital signals are transmitted via optocouplers while analogue signals use transformers. To achieve low noise operation, this ADC was realised in a NIM module. For clock frequencies ranging from 0.1 MHz to 10 MHz, the RMS noise, calculated on 2048 digital data, is about 0.5 LSB according to this equation:

$$V_{nRMS} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(d_i - \frac{1}{N}\sum_{k=1}^{N} d_k\right)^2} \qquad (4)$$

where d_i, d_k are acquired data values,
N is the number of samples in one acquisition, $N = 2048$.

So, the ADC has an effective resolution of 13.5 bits, which corresponds to a dynamic range of about 81 dB. Indeed, measurements with input signals much lower than the LSB voltage have shown that the dynamic range of this system exceeds 90 dB. Actually, when performing a 2048 point FFT, one can still find a peak corresponding to f_β, because these input signals modulate the ADC noise.

The block diagram of the ADC module is shown in **figure 2** and the structures of both the operation mode as well as the simulation mode, which depend on the settings of the *Simulator & Control* block, are presented in **figure 3** and **figure 4** respectively.

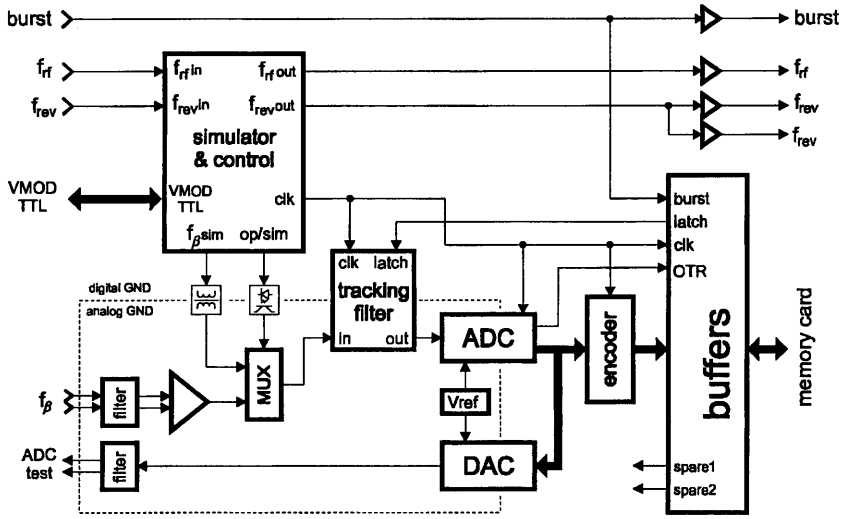

Fig. 2. Block diagram of the 14-bit ADC module. The *simulator & control* and *tracking filter* blocks are detailed later.

In the operation mode, the betatron signal goes first through the filter that separates the card from other noisy grounds. This filter includes a differential choke, which suppresses common mode signals up to relatively high frequencies. Sufficient common mode rejection ratio (CMRR) for low frequencies is achieved using a differential amplifier. Measurement results of CMRR are shown in **figure 5**. For the 10 Hz-200 MHz frequency range, CMRR is better than 57 dB.

The input signal contains the betatron frequency f_β and the revolution frequency f_{rev}, whose level is much larger than the level of f_β. Since only f_β is needed for further processing, f_{rev} must be attenuated before digitising, which is achieved using the tracking filter.

The 14-bit ADC continuously digitises the filtered betatron signal at a rate of $4 \times f_{rev}$. One can also choose f_{rf} as the ADC sampling clock in order to analyse some other modes of beam oscillations. This can be done remotely using the VMOD TTL interface (see **figure 3**).

Then, a dedicated encoder converts the ADC 14-bit natural binary data into 16-bit two's complement data for the DSP. Moreover, using the two most significant bits *D15* and *D14*, it adds overload information to every sample, according to the following convention. The input signal exceeds the positive limit when $D15 = 0$ and $D14 = 1$; it exceeds the negative limit when $D15 = 1$ and $D14 = 0$. During normal operation $D15 = D14$. When overflow occurs, the DSP sends an error message to the DSC, which can be used for automatic setting of the Gain Controlled Amplifier.

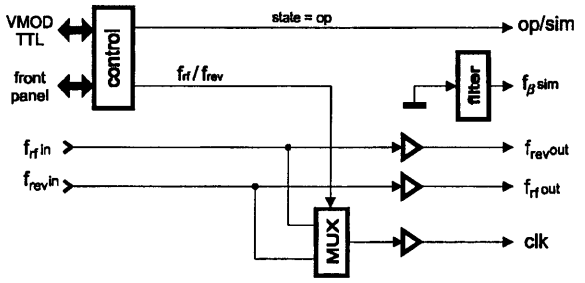

Fig. 3. The *simulator & control* block in operation mode.

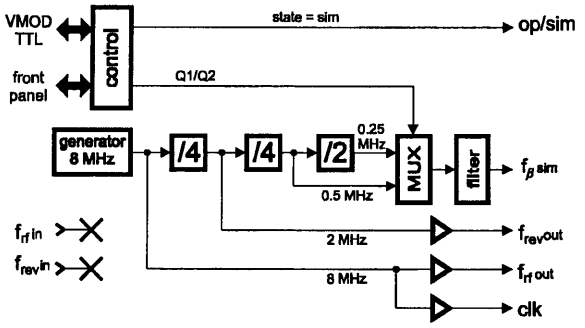

Fig. 4. The *simulator & control* block in simulation mode.

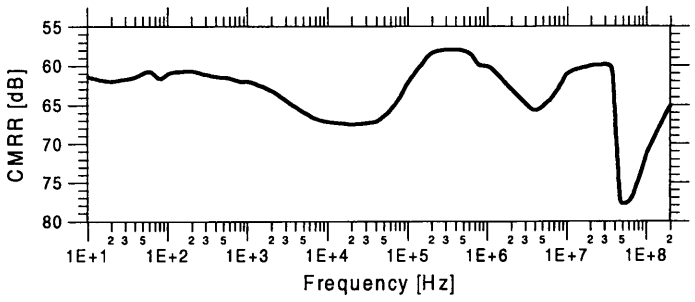

Fig. 5. CMRR of the ADC card.

Overload is also indicated internally, by means of two on-board LEDs, and the ADC *out of range* (OTR) signal is available on the *MEMORY INTERF* front panel socket.

The ADC card also includes a 12-bit DAC, connected to the 12 most significant bits of the ADC, so that digital data is converted back to analogue signal for easy testing.

The signal *burst* triggers the memory card, which initiates the acquisition of 2048 samples, at the ADC clock rate, and, when the acquisition is completed, data is transferred to the DSP memory for further processing.

To achieve fast transfer rates, signals between the ADC module and the memory card are exchanged in differential format, via twisted pair flat cables.

In simulation mode all of the signals f_β, f_{rev} and f_{rf} are generated internally. Some details are presented in **figure 4**. In this mode, $f_{rev} = 2$ MHz, $f_{rf} = 8$ MHz and ADC clock = 8 MHz (i.e. $4 \times f_{rev}$) and the input multiplexer connects the on-board signal $f_{\beta sim}$ to the ADC. Since $f_{\beta sim}$ can be selected as 250 kHz or 500 kHz, either with a front panel switch or remotely, the simulated q values are $q_1 = 0.125$ and $q_2 = 0.25$.

3.2. The tracking filter

During the PSB machine cycle, the revolution frequency f_{rev} varies from 0.6 MHz to 1.8 MHz and the fractional tune value is expected to be within 0.1 and 0.5. Thus, the betatron frequency range can be 60-300 kHz at the beginning of the machine cycle and 180-900 kHz at the end. The ADC clock, which is four times f_{rev}, ranges from 2.4 MHz to 7.2 MHz.

Due to this wide variation of f_β and f_{rev}, a fixed cut-off frequency filter could not be envisaged and a tracking filter whose cut-off frequency follows the ADC clock has been developed. In order to keep it simple, only 16 cut-off frequency values have been chosen, allowing it to cover the whole ADC frequency range and to work also as an efficient anti-aliasing filter.

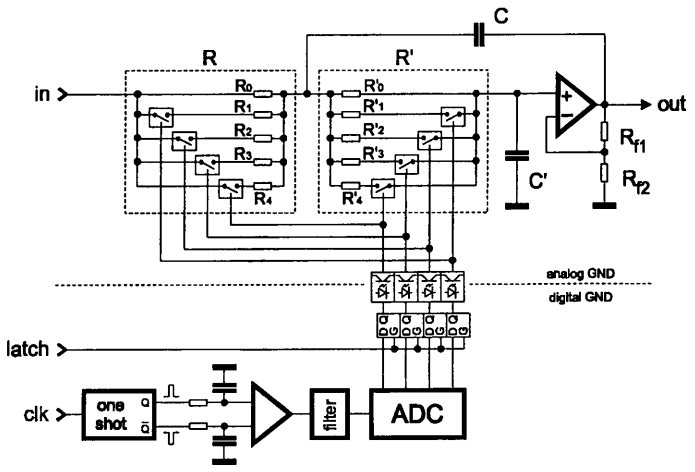

Fig. 6. Block diagram of the tracking filter.

The block diagram of the tracking filter is shown in **figure 6**.

Frequency to voltage conversion of the ADC clock is achieved using a stable ECL one shot generator and discrete low-pass filters. Both positive and negative pulses are integrated, in order to increase the output voltage span as well as to improve linearity and stability of the converter. An auxiliary ADC digitises the converter output voltage, so that its four most significant bits can be used to control the filter cut-off frequency.

The analogue part of the tracking filter is a second order low-pass Sallen-Key filter. CMOS switches, driven by the auxiliary ADC, control two resistive elements of that filter by connecting or disconnecting parallel resistors. In that way the filter cut-off frequency varies according to the main ADC clock frequency.

The signal *burst*, which determines the beginning of the acquisition, latches the output bits of the auxiliary ADC to avoid glitches in the analogue path. Then, when the state of the filter is stored, after a delay of 64 main ADC clocks, the memory board starts collecting ADC samples. Finally, when the acquisition is completed the latches become transparent and the filter cut-off frequency again follows the main ADC clock.

During the acceleration part of a PSB machine cycle, which lasts about 0.5 s, only 16 cut-off frequency values are used, so the auxiliary ADC can be slow. However, switching glitches must be as short as possible to reduce the delay before acquisition. Thus, switching must be fast.

Depending on the actual ADC clock, a 2048 sample acquisition lasts from 0.28 ms to 0.85 ms. So, the accelerator parameters remain almost constant and the filter state can be frozen during acquisition.

The filter architecture that has been adopted allows easily changing the kind of the filter response, by just varying the amplifier gain. Some main responses are presented in **table 1 [10]**, together with the corresponding gains and the B coefficients, which are used to calculate their cut-off frequency. In this application, we have chosen the Butterworth response.

Filter response	Gain	B coefficient
critical attenuation	1.000	0.644
Bessel	1.268	0.786
Butterworth	1.586	1.000
Chebyshev (3 dB ripple)	2.234	1.389
oscillations	3.000	-

Table 1. Some main responses of the tracking filter, as a function of gain = $1+R_{f1}/R_{f2}$.

When $R = R'$ and $C = C'$ the 3-dB cut-off frequency of the filter f_c is:

$$f_c = \frac{B}{2\pi RC} \tag{5}$$

where B is the coefficient from **table 1**.

To attenuate f_{rev} without affecting f_β, the filter cut-off frequency f_c is selected as 75% of the f_{rev} range, i.e. 0.45-1.35 MHz. It means that, at the switching points, f_β is always 50% smaller than f_c and f_{rev} is always 25% larger than f_c. Finally, for the PSB accelerator, the 16 points of a staircase characteristic $f_c = f(f_{CLK})$ were chosen according to the equation below:

$$f_c[\text{MHz}] = 0.45 + 0.09 \cdot \text{int}\left(15 \cdot \frac{f_{CLK}[\text{MHz}] - 2.4}{7.2 - 2.4}\right) \tag{6}$$

where function int(x) = integer part of x,
f_{CLK} is the ADC clock frequency ranging from 2.4 MHz to 7.2MHz and $f_{CLK} = 4 \times f_{rev}$.

In order to satisfy this equation with sufficient accuracy, it was necessary to take into consideration the parasitic output capacities of the switches as well as their series resistances.

The frequency characteristics of the ADC analogue channel is shown in **figure 7**.

At the beginning of the tuning range, f_{rev} is 0.6 MHz and the maximum f_β can be 0.3 MHz. For these frequencies, f_{rev} is attenuated 4.5 dB more (5.5 dB) than f_β (1 dB). At the end of the tuning range, the channel has similar gains and the highest f_{rev} and f_β are respectively 1.8 MHz and 0.9 MHz. The difference between the attenuation of f_{rev} and f_β is also about 4.5 dB (respectively 6 dB and 1.5 dB).

Since the amplitude of the input signal is almost equal to the f_{rev} component, the ADC input characteristic is shifted by about 4.5 dB towards lower amplitudes without ADC overloading, which means that the ADC input dynamics increased by some 4.5 dB.

ADC converts input signals with frequency f and $f_{CLK} \pm n \times f$, where n is an integer number, to same digital data. The betatron signal spectrum extends from $0.1 \times f_{rev}$ to $0.5 \times f_{rev}$ and, since $f_{CLK} = 4 \times f_{rev}$, that means $0.025 \times f_{CLK}$ to $0.125 \times f_{CLK}$. So, due to aliasing, the first frequency outside the working range that can be shifted into the working range and which can disturb the system is:

$$f_{CLK} - 0.125 \times f_{CLK} = 0.875 \times f_{CLK}$$

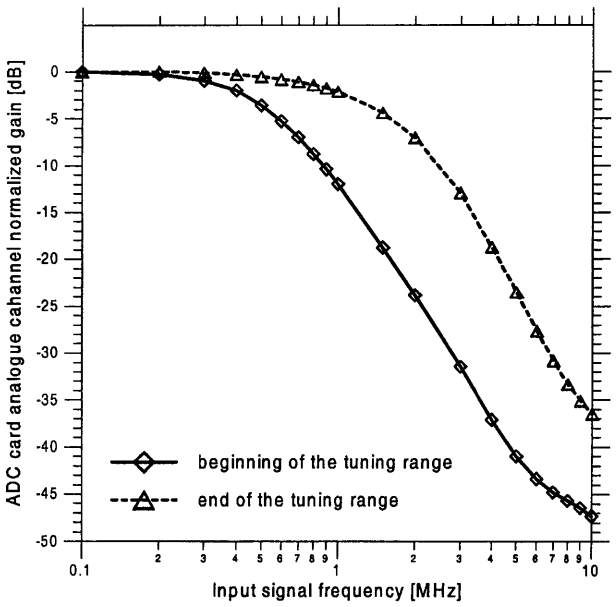

Fig. 7. Normalised gain vs frequency of the ADC card analogue channel.

At the beginning and at the end of the tuning range $0.875 \times f_{CLK}$ amounts to 2.1 MHz and 6.3 MHz. Normalised gains for these frequencies are −25 dB and −29 dB respectively, which means that aliasing is also cancelled.

3.3. Input and output signals

Signals going to or coming from the ADC card are listed in **table 2** with their main parameters. The betatron signal input FB and the ADC TEST output use insulated Lemo sockets that avoid direct connection of the internal analogue ground to external noisy grounds.

The ADC card can be remotely controlled by means of the VMOD TTL general purpose I/O module,

via a 26 pin flat cable on the ADC side and a 25 pin Canon male connector on the VMOD TTL side. The interface signals are described in **table 3** together with bit assignments as seen by the software. Remote control of the ADC module is allowed only if the OP/SIM switch on the front panel is left in OP position, otherwise the VMOD TTL cannot override front panel settings.

Signals from ADC module and memory card are exchanged in differential format through a twisted pair flat cable with 50-pin female connectors. These signals and their assignments are described in **table 4.**

Signals *spare1* and *spare2*, directly available on the ADC board, can be controlled by the DSP using dedicated registers on the memory module. This is convenient for further development or test purposes, e.g. measuring execution times of DSP software parts using an oscilloscope.

Signal name	in / out	Connector	Z [Ω]	source / destination	Description
FB	in	insulated lemo	1k	Gain Controlled Amplifier	differential input of the betatron signal; **ADC-module full scale input range ≥ 1.8 V_{pp}, adjustable on the board**
FREV	in	lemo	50	RF system	revolution frequency input, TTL level
FRF	in	lemo	50	RF system	RF frequency input, TTL level
RF BURST	in	lemo	50	Burst Gen.	trigger starting accumulation of 2048 samples by memory card, TTL level
FREV	out	lemo	50	RF Trig. Gen.	revolution frequency output, TTL level
FREV	out	lemo	50	test purposes	revolution frequency output, TTL level
FRF	out	lemo	50	RF Trig. Gen.	RF frequency output, TTL level
RF BURST	out	lemo	50	RF Trig. Gen.	RF Trigger Generator burst drive, TTL level
ADC TEST	out	insulated lemo	200	test purposes	DAC output, monitoring of ADC operation, amplitude 2.5V_{pp} for ADC full scale
VMOD TTL	in out	26 pin flat cable	-	VMOD TTL I/O module	remote control of ADC card, TTL levels, detailed description later
MEMORY INTERF.	in out	50 pin flat cable	100 diff.	memory card	twisted pair differential interface to memory card, detailed description later

Table 2. ADC module input and output signals. Power supplies, on NIM connector: +6V, –6V, +24V and –24V.

Signal name	in / out	pin #	Corresponding VMOD TTL 25 pin Cannon	Corresponding VMOD TTL register bit	Description
OP/SIM	in	1	1	A0 (LSB)	1: sets the card in operation mode; 0: sets the card in simulation mode
Q1/Q2	in	24	25	A1	valid only in simulation mode - 1: sets $q = q_1 = 0.125$; 0: sets $q = q_2 = 0.25$
Frev/Frf	in	3	2	A2	ADC clock: 1 sets f_{rev}; 0 sets f_{rf}
VMTled	in	18	22	A7 (MSB)	front panel VMOD TTL LED: 1 - off, 0 - on
OP/SIM	out	11	6	B0 (LSB)	1: operation mode, 0: simulation mode
Q1/Q2	out	14	20	B1	Simulated q value: 1 for 0.125; 0 for 0.25
Frf	out	13	7	B2	RF frequency: 1 f_{rf} present; 0: f_{rf} missing
Frev	out	12	19	B3	Revolution frequency: 1: f_{rev} present; 0: f_{rev} missing
GNDtest	out	8	17	B7 (MSB)	1: connection cable to VMOD module missing; 0: connection present

Table 3. ADC card connections to VMOD TTL module. Pin numbers # correspond to the 26-pin male flat cable connector of the card. States are in positive logic. Port A of the VMOD TTL module should be configured as output and port B as input.

Signal name	in / out	pin # (-,+)	Description
D15	out	1, 2	ADC data signal #15, MSB; normally D15=D14, D15≠D14 means that input signal exceeds full scale
D14	out	3, 4	data signal #14; D15=0 & D14=1: positive overflow, D15=0 & D14=1: negative overflow
D13 - D2	outputs	5 – 28	even pin always positive differential signal (+), odd pin always negative differential signal (-)
D1	out	29, 30	ADC data signal #1
D0	out	31, 32	ADC data signal #0 (LSB)
GND	-	33, 34	Digital ground
BURST	out	35, 36	trigger *burst* starting accumulation of 2048 samples by the memory card
OTR	out	37, 38	out of range signal from the ADC, additional error coding are done on bits D15 and D14
GND	-	39, 40	Digital ground
CLK	out	41, 42	ADC clock signal that is necessary for memory writings on the memory card
GND	-	43, 44	Digital ground
LATCH	in	45, 46	delayed and modified signal *burst* produced on the memory card that locks tracking filter control
SPARE1	in	47, 48	spare signal #1 software controlled from memory card, for testing purposes and further development
SPARE2	in	49, 50	spare signal #2 software controlled from memory card, for testing purposes and further development

Table 4. Memory card connections. Pin numbers correspond to the 50-pin male flat cable connector of the ADC card.

3.4. ADC card adaptation for the PS tune measurement system

The tracking filter is the only part of the ADC module that needs to be modified to adapt the module to the PS tune measurement system. **Table 5** includes comparison between main parameters of the PSB and future PS tune measurement systems.

Since the PS frequency values are much smaller than those of the PSB, the parasitic elements will play a smaller role when adapting the filter for the PS operation. In order to adjust it, one needs to:

- shift the beginning of the filter cut-off frequency range by changing values of R_0 and R'_0 (see tracking filter schematic on **figure 6**),
- change the span of the filter cut-off frequency by changing values of C and C',
- modify the range of the frequency to voltage converter by changing the capacitance value that defines the time constant of the one shot generator.

To summarise, requirements of the PS machine tune measurement are much easier to satisfy, and to adapt the ADC module to the PS parameters, it is enough to change only five element values.

Parameter	PSB	PS
minimum Q value	0.1	0.1
maximum Q value	0.5	0.5
minimum revolution frequency	0.6 MHz	100 kHz
maximum revolution frequency	1.8 MHz	500 kHz
oversampling rate	4	4
minimum ADC clock frequency	2.4 MHz	400 kHz
maximum ADC clock frequency	7.2 MHz	2 MHz
minimum betatron frequency	60 kHz	10 kHz
maximum betatron frequency	900 kHz	250 kHz

Table 5. Some main parameters of the PSB tune measurement system and required parameters of similar system for the PS accelerator.

4. The memory module

The memory module interfaces the ADC card to the DBV96 DSP board. It collects data from the ADC at fast clock rates and, when acquisition is completed, the DSP reads these data, through a fast dBeX extension bus **[5]**, for further processing. Then, once the DSP has prepared the module for next acquisition, new filling up of memory can start.

The memory module has two channels for servicing H and V planes. Each channel can accommodate 512 K of 16-bit words. Data is acquired using two ADC cards and processed on one DSP board.

Prior to each acquisition, the DSP sets the memory card parameters and "arms" it for data acquisition. After arming, the memory waits for a hardware trigger that initiates the acquisition sequence. First, a *latch* logic signal is sent to the ADC module that locks the tracking filter control input. After 64 ADC clocks (about 3% of the duration of one acquisition, some 8.9 to 26.7 us depending on ADC clock), acquired data start to be stored in the memory module. When the proper amount of data has been stored, acquisition stops and the *latch* signal releases the tracking filter. Then, either a DSP interrupt can be generated or the DSP can check whether the data is ready by testing a dedicated bit in the control register.

Mechanically the memory module is a VME card, equipped only with a connector P2, and it does not use any of the VME signals. A special bus adapter connects "user pins" on three P2 slots in the VME crate (one spare connection is foreseen), in order to establish the dBeX extension from the DBV96 board to the memory module. On the DSP board, another adapter connects the dBeX extension bus to user pins of the board P2 connector. In order to improve the ground connection, instead of using 24 data lines, while only 16 are necessary, the dBeX bus has been modified to add ground lines. Nevertheless, even with such an improvement, during fast data transfers the bus does not stand the full DSP speed and some software slowing down may be necessary. It is recommended to put the DSP board and the memory card in two adjacent slots to keep bus connections as short as possible.

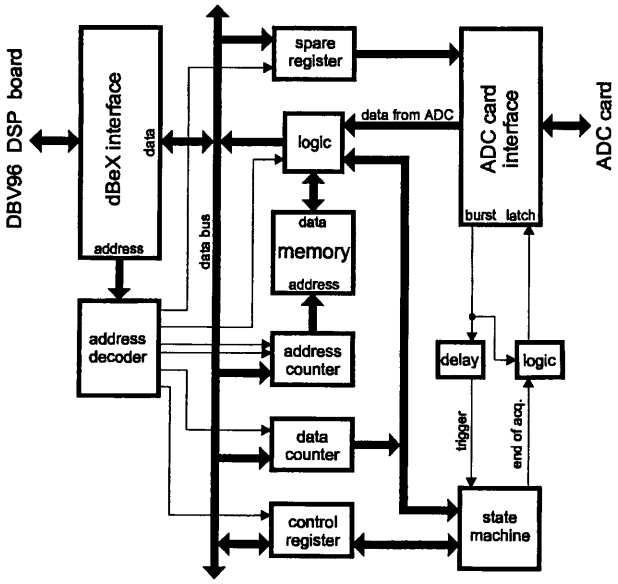

Fig. 8. Partial block diagram of the memory module.

The block diagram of one channel is shown in **figure 8**. The second channel is almost the same and only the *dBeX interface* block is common to both channels. Each channel has its own dBeX addressing.

The address counter drives the 19 memory address lines. Prior to each acquisition, the DSP loads it with the starting address from which the

data will be stored. Because the connection to the DSP board data bus is 16-bit wide, the start address loading must be done in two steps, at different dBeX addresses: first, higher bits A18-A16 are loaded as data D2-D0 and then, lower bits A15-A0 as data D15-D0. The address counter is incremented either by the ADC clock, during acquisition, or at every dBeX read cycle, during DSP access.

The 16-bit data counter, which is pre-set with the number of acquisitions to be made, is decremented at each ADC clock until it reaches 0, which means the end of acquisition. The state machine block with the associated 4-bit control register determines all of the memory module operations. One can check or change the current state of the state machine by reading from or writing to this control register. The control register bit assignment is shown in **table 6**.

Bit #	Name	Description
0 (LSB)	AcqArmed	0: possible access to all counters and registers 1: access restricted to control register and spare register; next active *burst* will trigger the acquisition
1	AcqRunning	1: acquisition is running, setting it causes a software trigger and acquisition starts without hardware trigger 0: acquisition not running
2	AcqFinished	1: acquisition is finished; testing this bit allows to detect the end of acquisition 0: acquisition not finished
3	IntEnable	1: interrupt enabled, when acquisition is finished a dBeX interrupt is generated 0: interrupt disabled

Table 6. Control register bit assignment.

The state machine block is described by the following states: *NotArmed*, *Armed*, *Running* and *Finished*. Its block diagram is shown on **figure 9**.

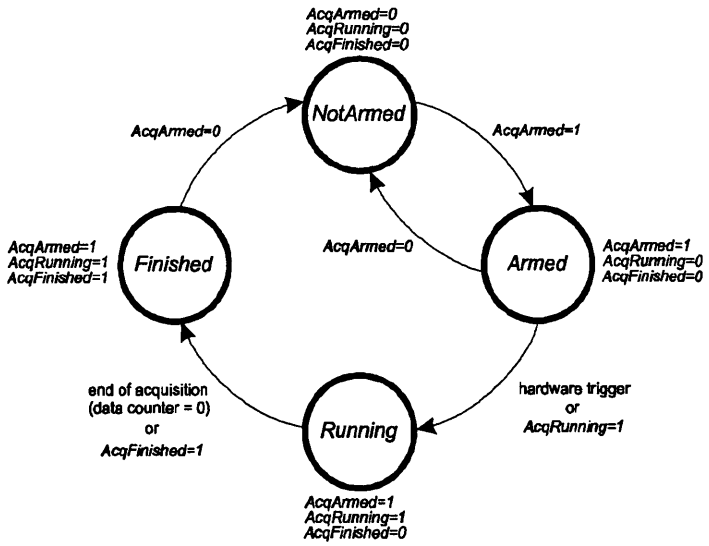

Fig. 9. Memory module state diagram.

In the *NotArmed* state, every counter and register can be loaded from the dBeX bus and the hardware trigger *burst* has no influence on the card operation. When the acquisition parameters are already prepared, one can set the *AcqArmed* bit, which means that the next active signal *burst*, coming from the ADC module, will start the acquisition. The *AcqRunning* bit is automatically set when the trigger occurs. For test purposes, it is possible to generate a software trigger by setting the *AcqRunning* bit, from the dBeX bus.

When the data counter reaches 0 (i.e. the desired data is already stored) the *AcqFinished* bit is set and the dBeX interrupt can be generated if the *IntEnable* bit is previously set. *AcqFinished* = 1 means that the acquired data can be copied to DSP memory so that next acquisition can be initiated.

Both channels of the memory board are equipped with three LEDs, which reflect their current state: *ARMED*, *WRITE* and *READ*.

The *ARMED* LED monitors the state of the control register *AcqArmed* bit, but the LED flashing duration is not smaller than 10 ms, even if the bit is set for shorter time. When the channel is armed, the LED stays on until a trigger occurs.

The *WRITE* LED is set (for at least 10 ms) when the ADC samples are stored in the memory and the *READ* LED is set (for at least 10 ms) when the data are transferred to memory on the DSP board.

ST6	ST5	base address
short	short	Y:$FFFFFF80
short	open	Y:$FFFFFF90
open	short	Y:$FFFFFFA0
open	open	Y:$FFFFFFB0

Table 7. Memory card: base address configuration.

Seen from the DSP, the dBeX bus is located in external Y memory, from address Y: $FFFFFF80 to Y: $FFFFFFBF and the memory card is also inserted into this space. The base address of the card is set using memory board jumpers ST5 and ST6, according to **table 7**.

Memory counter and register addresses are listed in **table 8**. The 2-bit wide spare register can be loaded from the dBeX bus at any time. These two bits are available on the ADC board for test purposes.

Channel	Address	Write access meaning	Read access meaning
0	base + 0	Address Counter bits 18-16	memory data @ address pointed by Address Counter
0	base + 1	Address Counter bits 15-0	Control Register
0	base + 2	Data Counter	Control Register
0	base + 3	Control Register	Control Register
0	base + 4	Spare Register	Control Register
1	base + 8	Address Counter bits 18-16	memory data @ address pointed by Address Counter
1	base + 9	Address Counter bits 15-0	Control Register
1	base + 10	Data Counter	Control Register
1	base + 11	Control Register	Control Register
1	base + 12	Spare Register	Control Register

Table 8. Memory module addressing.

5. Results

Because the ADC takes into account internal and external input noise as well as offset voltages, its digital output does not remain constant, even without any signal at the board analogue input. Furthermore, the ADC noise distribution varies when applying an input signal, whose amplitude may be much smaller than the equivalent LSB voltage. In this case, the probability of having certain digital values at the ADC output is modified and values farther from mean value are more likely. When the input signal varies it modulates the noise distribution and some digital values appear more often or more rarely, depending on the amplitude of the signal. This means that, in the spectrum of the output signal, a peak corresponding to the modulating frequency appears. If the spectrum is calculated for longer signal duration, more energy of the modulating signal is accumulated and frequencies of smaller input amplitudes can be found in the spectrum. Thus, the number of samples, which are acquired to calculate the spectrum, is extremely important.

In the tune measurement system, this ADC noise modulation phenomenon, by signals smaller than one LSB, is also observed.

Figure 10 shows 2048 samples of a 500 kHz sine wave signal. Its peak-peak amplitude is 100 dB smaller than the ADC full scale (FS = 5 V) and 23.7 dB smaller than the voltage corresponding to one LSB. This signal was digitised with f_{CLK} = 8 MHz so the equivalent q value is 0.25.

Even with such small amplitude, the period of the input signal, amounting to 256 sampling clocks (i.e. 32 μs), is still visible as a noise pattern.

Figure 11 represents the spectrum of previous signal, from bin numbers 50 to 256 that correspond to tune values ranging from 0.1 to 0.5. Notice that the peak related to input frequency is nicely visible. In this case, the DSP calculated the tune value of 0.25 with 0.1% error. But for such small amplitudes, sometimes the system does not give good results because calculations are based on stochastic data.

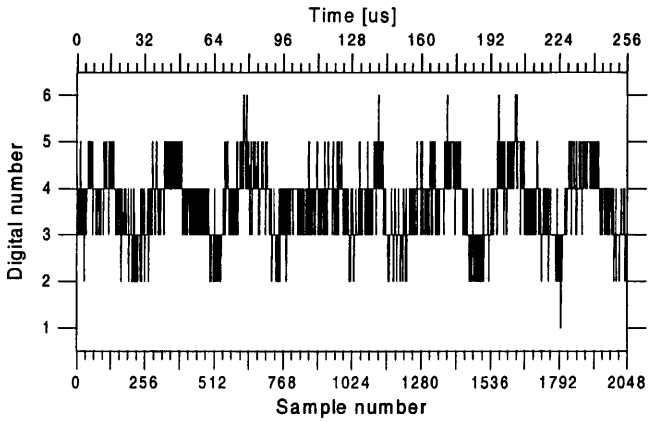

Fig. 10. Digitised input signal with amplitude FS–100dB.

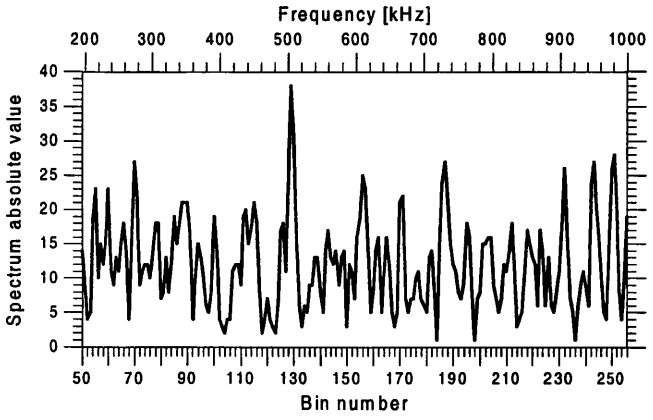

Fig. 11. Spectrum of the signal shown above in ranges seen by peak search routine.

Several sets of acquisitions, of one thousand measurements each, have been used to estimate the yields of measurements that satisfy predefined accuracy levels, as a function of input signal amplitude, when frequency position lies between two spectrum bins. For the interpolation process, it appears that the worst position is ¼ bin spacing distance from a bin line on both directions. In these points, the interpolation error is the biggest.

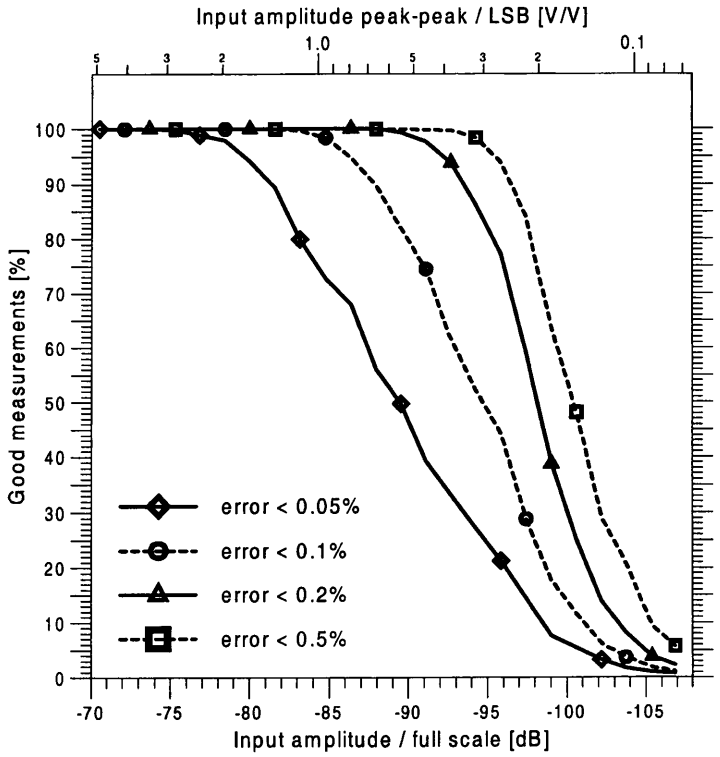

Fig. 12. Good measurement yield for 1000 measurements, as a function of the input signal amplitude, for worst case spectrum peak fitting around $q = 0.25$ (bin number 128+¼).

Worst case results are presented on **figure 12**, for a frequency value lying about the middle of the system working range. Spectrum position is 128+¼, which corresponds to $q = 0.25049$ and to frequency 500.98 kHz.

We assume the system works if at least 90 % of measurements are good. With such a threshold, using input peak-peak amplitudes 81.5 dB, 88 dB, 94 dB and 96.5 dB smaller than the ADC full scale (voltage ratios equivalent to one LSB: 1.4, 0.65, 0.33 and 0.25) we obtained results with relative errors lower than 0.05%, 0.1%, 0.2% and 0.5% respectively.

Because the error absolute value is almost constant and depends only on the size of the FFT and the interpolation process, for extreme tune values 0.1 and 0.5, errors can be respectively 2.5 times bigger and 2 times smaller than presented **[2]**.

Note that these results have been measured with a pure sine wave. So, in the case of a beam signal, which includes at least two components (f_β and f_{rev}), the input dynamic range could be slightly smaller than presented.

6. Conclusions

We have shown that, to improve noise immunity and dynamic range, it was necessary to replace the previous 12-bit VME-ADC with a new 14-bit ADC, realised in a NIM module. The ADC card also includes a tracking filter that attenuates the revolution frequency component and serves as an efficient anti-aliasing filter.

The dedicated memory module, which is accessible from the DSP, allows for fast ADC acquisitions. The sampling frequency has been increased from $2 \times f_{rev}$ to $4 \times f_{rev}$ without sacrificing tune measurement resolution, because the FFT analysis is done now using 2048 points instead of 1024, respecting same timing constraints. Indeed, the system can provide good results even with input signal amplitudes much smaller than one LSB of the ADC.

Test and diagnostic facilities have also been introduced on the ADC card and they can be accessed via the DSP and the memory board. Switching the ADC into simulation mode permits testing the whole acquisition and processing system, including the application program, and overload signalling can be used to automatically control the gain of the analogue system channels.

Furthermore, the new hardware, which has been especially developed for the PSB tune measurement, has significantly improved the system, allowing for measurements of relatively low intensity beams using the modest kicker voltage that is available now (500 V). In order to measure lower intensity beams, a new pulser must be developed.

Finally, just changing a few components, on the ADC board, allows this system to be used also for the tune measurement of the 26 GeV PS accelerator.

7. Acknowledgements

We are indebted to all those who were involved in the system hardware development, especially to A. Chapman-Hatchett, J.M. Digonzelli, J.T. Pons and L. Soby. Many thanks also to D.J. Williams for his constant support and invaluable comments.

8. References

[1] A. Chapman-Hatchett, V. Chohan, E.T. d'Amico, *Tune measurement for the CERN Proton Synchrotron Booster rings using DSP in VME.* CERN/PS 99-031 (BD). Particle Accelerator Conference, New York, USA, March 29-April 2, 1999.

[2] M. Gasior, J.L. Gonzalez, *DSP Software of the Tune Measurement System for the Proton Synchrotron Booster Accelerator.* CERN/PS/BD Note 99-11, September 1999.

[3] J.L. Gonzalez, J.T. Pons, *Q-Measurement System Hardware for the PS and PSB Accelerators.* CERN/PS/BD Note 98-10 (Tech), July 1998.

[4] J. Gonzalez, S. Johnston, E. Schulte, *Fast Q-measurement for the PS by FFT analysis.* CERN/PS 94-1 (BD). European Particle Accelerator Conference, London, UK, June 23-July 1, 1994.

[5] Loughborough Sound Images plc, *VME Floating-Point DSP Board.* Technical Reference Manual. Version 3.00, June 1994.

[6] J.L. Gonzalez, J.T. Pons, *Burst and RF Trigger Generator Modules (VMOD_BURST and VMOD_RFTRIG).* CERN/PS/BD Note 98-09 (Tech), July 1998.

[7] L. Soby, O. Marqversen, *private communication.*

[8] JANZ Computer AG, *VMOD-IO VME MODULbus carrier board Ver. 2.2.* January 1993.

[9] A. Gagnaire, W. Heinze, *Replacement of the ICV196 by the VMOD-TTL Module.* CERN/PS/CO Note 94-13 (Tech), March 1994.

[10] U. Tietze, C. Schenk, *Halbleiter-Schaltungstechnik*, Springer-Verlag, Berlin-Heidelberg, 1985.