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Q-MEASUREMENT SYSTEM HARDWARE FOR THE PS AND PSB ACCELERATORS

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ABSTRACT

This note describes new hardware, for the Q-Measurement system of the PS and PSB accelerators. The main objective of this project is to have a standard system for both accelerators, in order to facilitate their maintenance. Currently, the PSB Q-Measurement is based on Fast Fourier Transform (FFT) analysis, performed by the 96002 Digital Signal Processor (DSP), from Motorola. For the acquisition, new electronics have been developed: an ADC NIM-module, a VME Memory Controller, between the ADC and the DSP, and a pair of piggyback modules, the VME Burst Generator and the VME RF Trigger Generator.

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1. Introduction

This note describes new hardware for the Q-Measurement system of the PS and PSB accelerators. The main objective of this project is to have a standard system for both accelerators, in order to facilitate their maintenance.

The Q-measurement calculates the tune-value, defined as the number of betatron oscillations performed by the particles during one revolution period. Previously, the PSB calculated the tune value using the accelerator optics parameters, but for LHC-beams the resolution of this method was not sufficient. Thus, a second objective of this project is to provide the required resolution.

The present PS Q-measurement is based on Fast Fourier Transform (FFT) analysis, performed by the VASP-16 Digital Signal Processor (DSP) [1]. In order to obtain coherent betatron oscillations of sufficient amplitude, it is necessary to excite the beam. Currently, this is done with an air-core magnetic kicker, which receives a capacitor discharge pulse of one revolution period duration. The system is fast enough to allow measurements of rapid Q-changes, e.g. during chromaticity measurements using beam position modulation.

The PSB system is also based on FFT analysis achieved by the 96002 DSP, from Motorola. For the acquisition, new hardware has been developed: an ADC NIM-module, a VME Memory Controller, between the ADC and the DSP, and a set of piggyback modules, the VME Burst Generator and the VME RF Trigger Generator [2]. The kicker electronics should also be upgraded.

2. The present PS Q-measurement system

The PS Q-measurement is a VME-based system, which may be used to perform acquisitions, FFTs or q-value interpolation on beam-position data from a pick-up. Its two main components are a Motorola MVME147 controller and a VASP16 DSP. The system also uses a general purpose I/O module (ICV196), for various controls, the Burst and RF Trigger Generators (VMOD-BURST and VMOD-RFTRIG) and a TG8. The VASP-16 has its own interface to a NIM chassis, which contains a 12-bit Analogue to Digital Converter (10 MHz ADC). The Program Line Sequencer (PLS), which consists of bit streams containing PS accelerator timing information, provides the necessary user and cycle synchronisation.

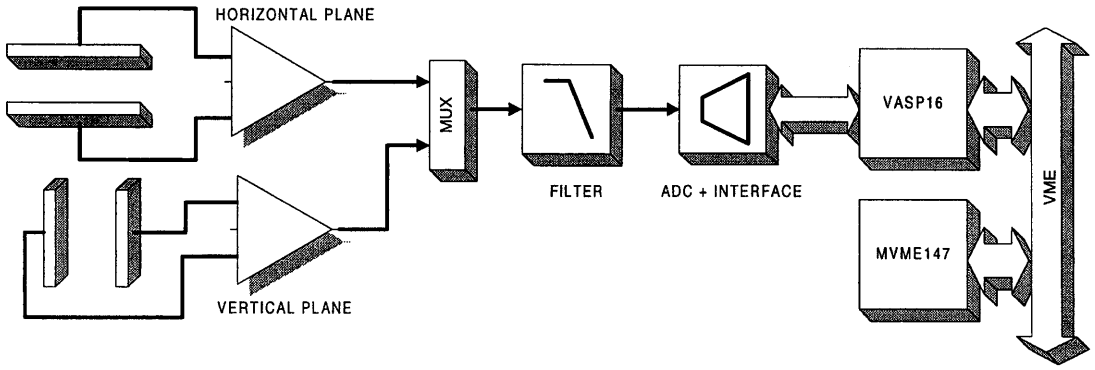

Figure 1: Present hardware of the PS Q-measurement system

Figure 1 shows a block diagram of this system. It uses an analogue multiplexer to select the horizontal or vertical beam position information, from an electrostatic pick-up. Since the spectrum of this signal extends beyond the sampling frequency, a band-pass anti-aliasing filter precedes the NIM-ADC. Digital data are then transferred into one of the two memory banks of the VASP-16, via a custom 16-bit bus. The DSP board is

controlled by the Texas TMS320C25 processor, and signal processing is performed by four Zoran ZR34161 vector processors. An arbitration unit governs access to the two data banks, allowing concurrent data acquisition and processing.

The ADC clock is chosen according to the type of signal analysis to be performed: while spectral analysis may use the accelerating frequency f_{RF} to observe higher modes of oscillation, now the Q-measurement uses f_{rev}. Depending upon the choice, either a tracking or fixed-frequency anti-aliasing filter is selected. In the case of Q-calculation, the filter does not need to be very steep, since the processing system uses amplitude interpolation and can accept some lightly attenuated image frequencies.

3. The PSB Q-measurement system

The PSB system is based on the Motorola 96002 DSP [3], which performs the FFT analysis. The DSP is a fully compatible IEEE 754 floating-point processor, with an advanced arithmetic unit. When clocked at 40 MHz, it achieves up to 60 MFLOPS peak processing power. The DSP is installed on the VME DBV96 commercial board [4], from Loughborough Sound Images. The DBV96 is a modular motherboard that can be fitted with one or two 96002 DSP, with shared and local memory for each processor. Either of the two processors can become VME master, including full VMEbus arbiter and slot 1 functions. Each processor can generate VME interrupts and respond to VME or external interrupts. The board may also operate as a slave interface, with external VMEbus masters, which are able to access the main DSP memory. The board includes a real time I/O expansion bus (dBeX), which is used for data transfers, independent of the VMEbus.

Block diagram, on Figure 2, shows the future system, which is very similar to the present PS Q-measurement. Two electrostatic pick-ups, one for the horizontal plane and another for the vertical plane, sense the beam. The signal is then amplified, filtered, digitised and transferred into the Memory Controller.

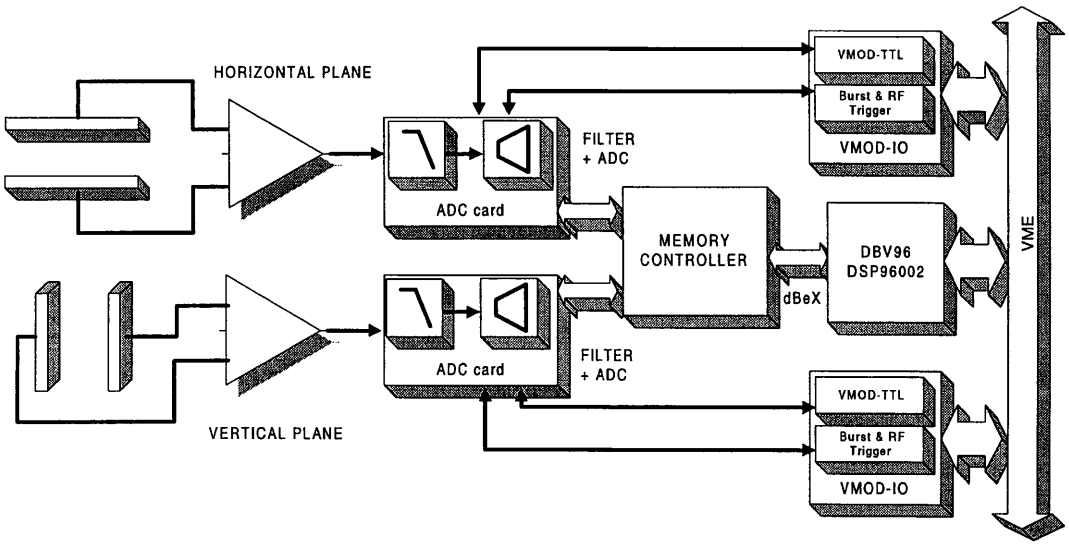

Figure 2: Block diagram of future PS and PSB Q-measurement system

The ADC and the Memory Controller modules are described in detail in this paper.

The system uses two VME VMOD-IO boards, from JANZ Computer AG. These motherboards can hold up to four plug-in piggyback modules. Three piggybacks are installed on each board: a VMOD-TTL and the Burst and the RF Trigger Generators. The VMOD-TTL is a commercial 20-bit TTL I/O piggyback module [5], which controls the ADC card. It is used for the generation of strobe pulses and consists of one 4-bit and two 8-bit I/O registers. The Burst and the RF Trigger Generators are full custom piggybacks, which can be used in numerous applications that require synchronised

signals. They accept the accelerator timing signals and generate the *Start* pulse, which indicates the beginning of an acquisition.

4. The ADC module

Since the VME environment is quite noisy, the ADC has been realised in a NIM module. The ADC samples the betatron signal and converts it into digital data. It acts as an interface to the whole system and includes a signal simulator, for test purposes, and a programmable low-pass anti-aliasing filter. Other features are programmable resolution (12 or 14 bits) and data format (normal or 2's complement).

The programmable resolution is achieved using two low-power fast ADCs, from Analog Devices: a 12-bit-25 MSPS and a 14-bit-10 MSPS. The ADC outputs are buffered, which allows mounting both of them or only one. Two jumpers are used to select respectively the resolution and normal or 2's complement data. Both parameters can be modified dynamically by the DSP if no jumpers are mounted. This module has an output to the Memory Controller, a control input/output from the VMOD-TTL module, and dedicated inputs as shown in Table 1.

I/O	Type	Function
Input	Lemo	Accelerating frequency f_{RF}
Input	Lemo	Revolution frequency f_{rev}
Input	Lemo	Betatron signal f_β from pick up
Input	Lemo	Burst_IN signal from the Burst Generator module
I/O	25-pin, flat cable connector	Interface with VMOD-TTL module
Output	Lemo	f_{RF} signal, to Burst Generator
Output	Lemo	f_{rev} signal, to Burst Generator
Output	BNC	f_{rev} signal, to Kicker
Output	BNC	Burst_OUT signal, to kicker
Output	Lemo	f_β test output
I/O	Xx-pin flat cable connector	To Memory Controller card

Table 1: ADC card Input/Output assignments

A VMOD-TTL piggyback module controls the ADC. It consists of two 8-bit I/O registers, A and B, and one 4-bit register, C. The ADC only uses register A (as output) and register B (as input). Figure 3 shows the interface pin assignments.

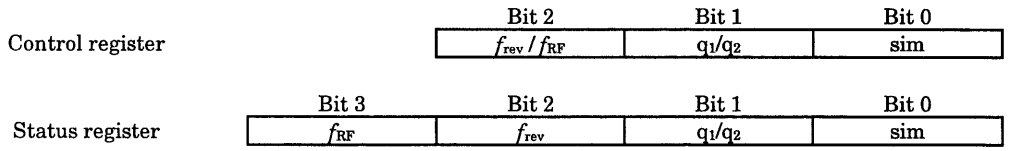

Figure 3: Pin assignment of the VMOD-TTL interface

Bit 2 of the control register selects the ADC sampling frequency, which can be either f_{rev} or f_{RF}. Q-measurement always uses f_{rev}, while spectral analysis may also be performed using the accelerating frequency f_{RF} to observe higher modes of oscillation. A frequency to voltage converter automatically adjusts the cut-off frequency of the low-pass filter, as shown in Figure 4.

Bits 0 and 1 are used to control the Q-simulator, included in the ADC card to test the whole system. When bit *sim* is set to "0" the f_{RF} signal is generated by an 8 MHz internal clock, and the f_{rev} signal is a 400 KHz clock produced by a frequency divider. Then, bit 1 selects $f_{rev}/4$ or $f_{rev}/8$ as the analogue signal to be digitised, instead of the betatron signal f_β. Thus, simulated Q-values are respectively 0.25 and 0.125. This can be used to test the system without beam or external timing. The card also allows manual control of the simulation, via two front panel switches, one to choose operational/simulation and the other to select $f_{rev}/4$ or $f_{rev}/8$.

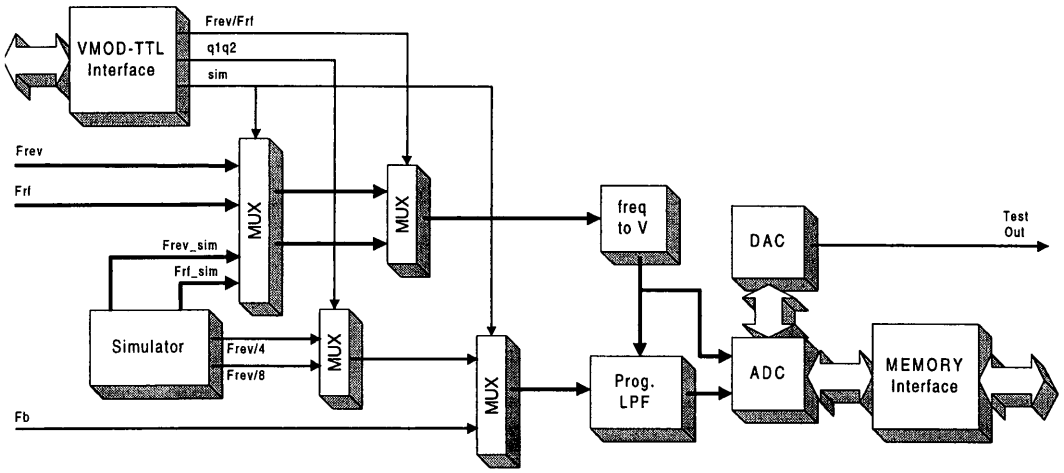

Figure 4: Block diagram of the ADC card

The status register is a read-only register. Bits 2 and 3 are set to '1' when f_{rev} and f_{RF} are applied to the module. Bit 0 is set when simulation is active, and bit 1 shows which simulated betatron frequency is in use: $f_{rev}/4$ or $f_{rev}/8$.

Front-panel connectors feed data and control signals to the Memory Controller. These control signals are the clock (f_{rev} or f_{RF}), the ADC overflow flag and the *Start* signal provided by the *Burst Generator Module*. It also receives three signals for control purposes: one to select resolution (12 or 14 bits), another for normal or 2's complement data and the last one is a spare signal.

5. The Memory Controller card

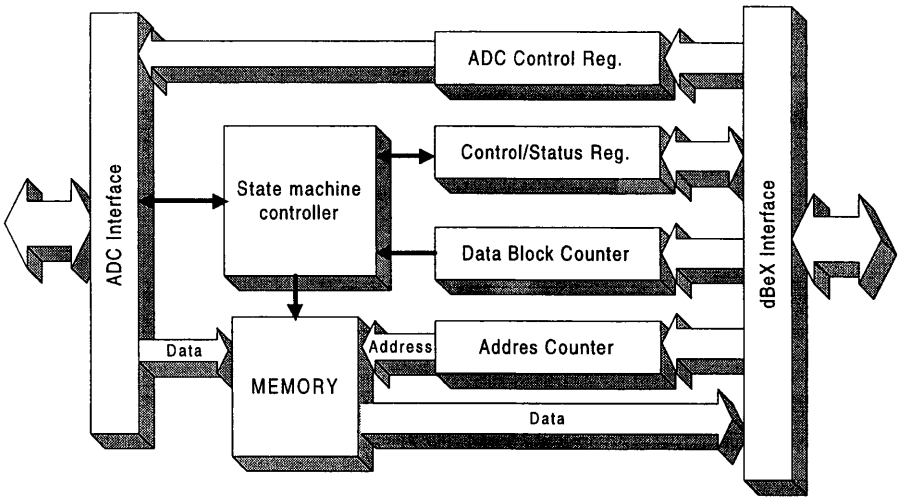

Figure 5: Block diagram of the Memory Controller (one channel)

The Memory Controller card is a memory interface between the ADC card and the 96002 DSP. It allows the DSP to control the writing sequence of ADC data into the 512K by 16-bit on-board memories. The DSP is installed on the DBV96 VME commercial board and communicates with the ADC Memory Controller through the dBeX, a real time I/O expansion bus. Two ADCs can be connected to the Memory Controller using flat cable connectors. This module is also of VME mechanical format (6U) without the P1 connector (i.e. it does not have interface to the VME bus). The user pins on the P2 connector are used to implement a modified dBeX bus: reduced 16 bit I/O data and increased number of ground/supply pins.

Figure 5 shows a block diagram of the card. It consists basically of two counters, two registers, and a controller that performs the arbitration to the memory. All the logic, including the state machine and the registers, has been implemented in an ALTERA EMP7128 PLD. The card has two channels and, therefore two PLDs, both with the same program. The differences have been set on the PCB.

The memory map of this module is shown in the following table:

Channel	Address	Write	Read
0	Base Address + 0	Memory Address Counter, High Bits	Data
0	Base Address + 1	Memory Address Counter, Low Bits	Status Register
0	Base Address + 2	Data Block Counter	Status Register
0	Base Address + 3	Control/Status Register	Status Register
0	Base Address + 4	ADC Control Register	Status Register
1	Base Address + 8	Memory Address Counter, High Bits	Data
1	Base Address + 9	Memory Address Counter, Low Bits	Status Register
1	Base Address + 10	Data Block Counter	Status Register
1	Base Address + 11	Control/Status Register	Status Register
1	Base Address + 12	ADC Control Register	Status Register

Table 2: Memory map of the Memory Controller

The *Memory Address Counter* is a 19-bit binary up-counter. This counter is loaded from the dBeX data bus. Bits 0 to 2 of the dBeX bus correspond to high bits 16 to 18 of the counter. The next bits 0 to 15 of the dBeX data bus correspond to bits 0 to 15 of the counter. High-word must be set up before low-word. The counter automatically increments by one, after each enabled write operation from the ADC, or after each read data operation by the DSP through dBeX data bus. The outputs of the counter permanently drive the memory address lines.

The *Data Block Counter* is a 16-bit binary down-counter. This counter is loaded from the dBeX data bus with a 16-bit word that indicates the data block size to be acquired. The counter decrements by one after each enabled write or read operation.

The *ADC Control Register* is a 3-bit register. The output of the register permanently drives three signals to the ADC, for control purposes. Bit 0 is used to set the ADC resolution to 12 or 14 bits (the default value, *resol* = 0 selects the 12 bit ADC). Bit 1 sets the data format: *2com* = 0 (default value) selects 2's complement, and *2com* = 1 selects straight binary. Bit 2 is a spare signal for future development.

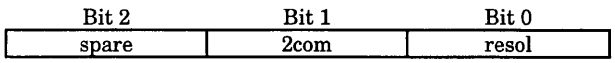

Figure 6: ADC Control register

The *Control/Status Register* can be written or read, whatever the state of the current acquisition. Loading '1' from the dBeX sets all bits and the VME bus signal /SYSRESET clears them all. Figure 7 shows assignments.

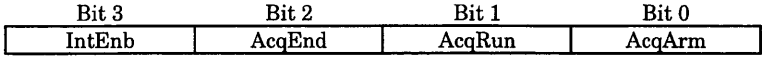

Figure 7: Control/Status register

The 4 bits in the control register have the following functions. When *AcqArm* (bit 0) is set, it enables the next trigger pulse to set the *AcqRun* (bit 1). The *AcqRun* can also be set from the dBeX bus (loading '1') or with a trigger pulse, when *AcqArm* is high and *AcqEnd* is low. When *AcqRun* is high and *AcqEnd* is low, the memory write operation and counter clocks are enabled. The *AcqEnd* is set from the dBeX bus or, when *AcqRun* is high, by a data block counter output pulse. An interrupt to the dBeX bus is generated when both *IntEnb* (bit 3) and *AcqEnd* are high.

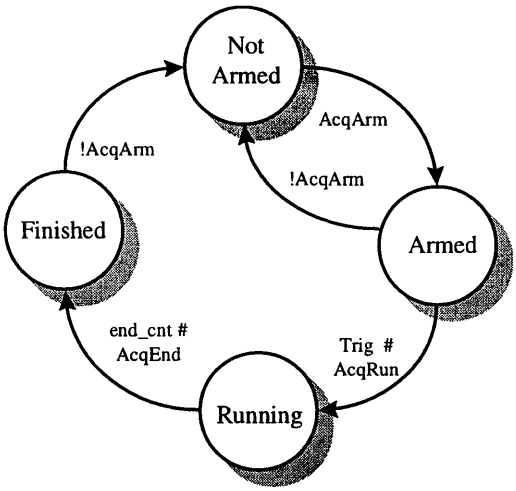

Figure 8: State machine diagram

A simple state machine controls that board (Figure 8). It has four states: *Not Armed*, *Armed*, *Running* and *Finished*. In the *Not Armed* state the DSP can read data from memories and program all registers. When bit 1 of control register is set, the machine changes to the *Armed* state. Then, the DSP cannot read data from memories or write to the register (except the control register that can be read or written whatever the state). When bit 1 of the control register is set or a *Start* signal is received the machine changes to the *Running* state, and the acquisition begins. Data is loaded with the clock signal from the ADC interface to the memories. The acquisition finishes when the Data Block counter reaches zero. The DSP can also stop the acquisition by setting the *AcqEnd* bit of the control register. Then the state machine changes to the *Finished* state, generating a dBeX interrupt if the *IntEnb* bit was set.

6. Conclusion

Compared to the present systems, the analogue-to-digital conversion of the pick-up signal has been improved: the new system uses low power ADCs and has more resolution (up to 14-bit). Moreover, simultaneous horizontal and vertical acquisitions are now possible with this system. The VME hardware compatibility has been increased, because all of the Loughborough DSP boards are equipped with the dBeX interface.

The PS Q-measurement system needed a VME Serial CAMAC interface to control preset-counters. The Burst and RF Trigger Generators have replaced them, improving the timing generation features and making the CAMAC crate unnecessary. On the new system, a VMOD-TTL module will also replace the ICV196 I/O register module.

For the PSB system to deal with high energy and high intensity beams, the kicker electronics must be upgraded to provide programmable pulse amplitude and width.

7. Acknowledgements

We are indebted to J. Belleman and A. Chapman-Hatchett for their kind advice and helpful comments.

References

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