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VME RF-MUX AND SYNCHRONISER

J.M. Belleman, J.L. Gonzalez, C. Gruber

Abstract

This note describes the design of the RF-MUX and Synchroniser, a VMEbus module to generate timing signals for the closed orbit display (CODD) of the CERN PS machine. Based on the machine revolution frequency, a pick-up signal and timing inputs, it produces a beam-synchronous reference frequency and a number of acquisition triggers, as needed by the remainder of the CODD system.

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1. Introduction

The RF-MUX and Synchroniser is a VME module implementing part of the CODD synchronisation system [1]. In combination with a separate DDS PLL, a few TG8 modules and 10 BLR & Gate Generators, it produces all timing and RF signals needed for orbit acquisitions and calibration. CODD is initially synchronised with the reference frequency of the injecting machine. After injection, it uses a pick-up signal to derive its timing, and during calibration, a local calibration source is used. The RF-MUX selects the appropriate frequency source, according to the measurement mode, and provides synchronisation and acquisition triggers, whenever necessary during the PS acceleration cycle.

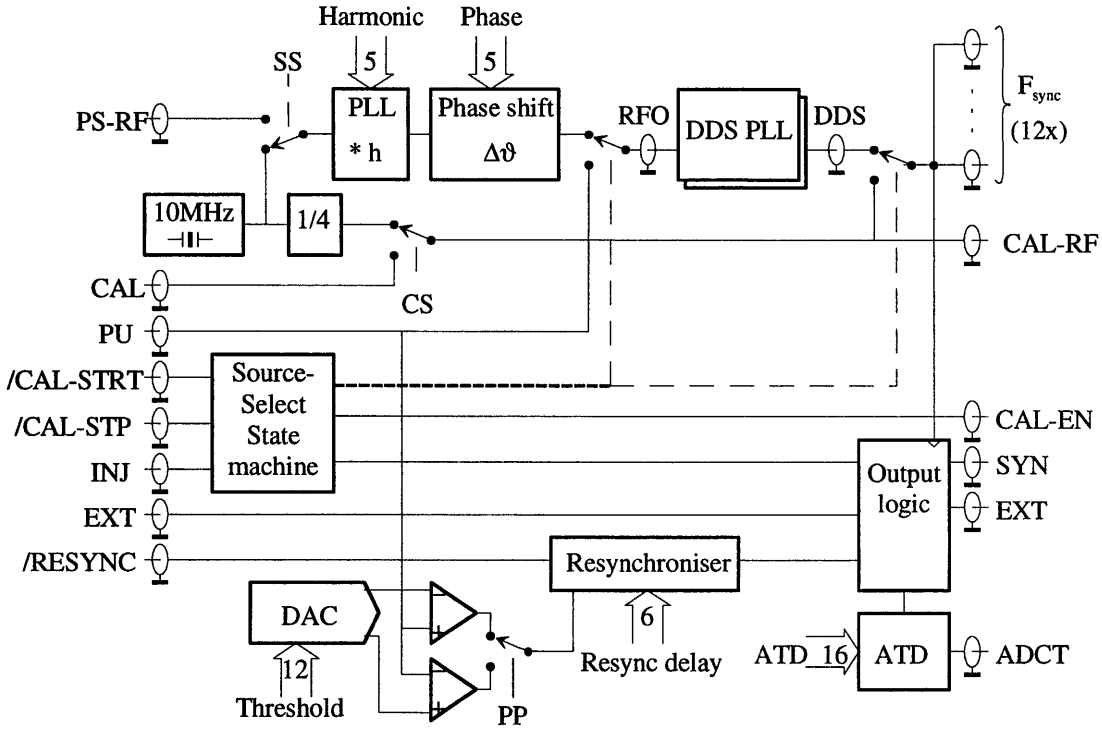

Fig. 1 Block-diagram of the VME RF-MUX and Synchroniser

The PS-RF input, normally the revolution frequency, is multiplied up by the machine harmonic number to recreate a signal at the RF bucket rate, which must lie between 2 and 10 MHz (Fig. 1). It is followed by a programmable phase shifter, to align the bucket clock with the PU signal and allow a smooth transition. The block labelled DDS PLL is not part of the RF-MUX and consists of a set of NIM modules in a nearby crate. Its function is to produce a clean version of the PS machine's RF frequency, based on a look-up table plus a correction derived from its input.

The output signal, F_{sync}, which can be either the DDS signal or a calibration clock, is distributed over 12 outputs to the BLR & Gate Generators [2], which in turn produce the appropriate gating signals for the analogue orbit acquisition hardware.

The RF-MUX and Synchroniser uses TG8-timing information to select the source signals: calibration-RF between Calibration Start and Calibration Stop, PS-RF thereafter, and the PU signal following Injection.

The re-synchroniser is used for harmonic number changes. During such operations, the system momentarily looses synchronism. When the situation has stabilised on the new harmonic, the RESYNC trigger initiates a sequence which aims to lock on the first non-empty RF bucket detected.

A pulse on RESYNC marks the end of RF-Gymnastics. The re-synchroniser must be loaded with ppm information related to the final harmonic number, prior to reception of the RESYNC trigger.

1.1. Operation

The RF-MUX and Synchroniser can be roughly divided into three functionally distinct sections. The first is a state-machine (Fig. 2), driven by three of the input triggers, which switches one of three RF sources to a common output. The second section, in the top half of the block diagram, is the RF switchyard. The third section synchronises the triggers with the appropriate RF and passes the result on to the appropriate outputs.

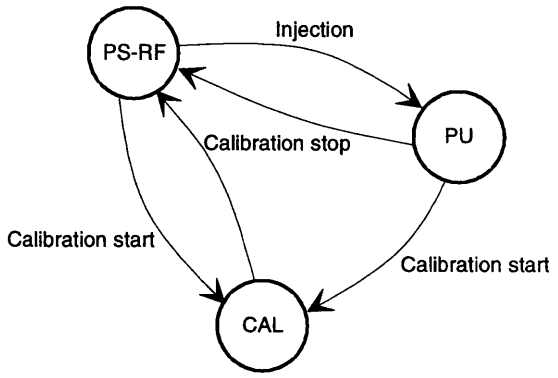

Fig. 2 The RF-MUX state machine

Referring to Fig. 2, the normal sequence of states is that which traverses the three states in the clockwise direction. Initially, the PS-RF input signal, multiplied by *h*, is passed to the output. When an injection trigger is received, and after a short delay, it switches over to an RF derived from the PU signal. Upon reception of a calibration Start trigger, it connects the calibration RF to the output. Finally, a calibration Stop trigger resets it to the original state.

The input triggers can also generate output triggers. In Table 1, the first column lists the input triggers. The remaining columns show which outputs are generated for each. Note that to produce an output trigger, an RF appropriate for the module's state must also be present. To ease testing, internal sources have been provided.

in↓ out→	SYN	EXT	CAL-TRIG	ADCT
INJ	X			X
EXT		X		X
RESYNC	X			
CAL GEN			X	X
CAL STRT				
CAL STOP				

Table 1 Input vs. output triggers

The SYN output trigger serves to mark the instant a bunch of particles first traverses the first PU after the injection point. In doing so, it marks, as it were, a bunch as being the first. Since the injection orbit is to be measured at all times, the ADCT, which triggers an orbit acquisition, is also generated. The EXT output is used for all other orbit measurements during the acceleration process. It merely requests a measurement to be made within the next millisecond or so, the fine timing being the responsibility of another module, the BLR & Gate generator [2]. During bunch merging or splitting operations, or during harmonic number changes, colloquially known as 'RF gymnastics', the tracking of the first bunch fails. The RESYNC input tells the RF-MUX to accept any bunch to pass through the PU it's looking at as being the first and to convey this information to the BLR & Gate generators by means of the SYN output. No acquisition is desired in this case, hence the absence of ADCT.

2. Address map

The address space covered by the module extends over 16 words, mapped into the VME short I/O space, but only 9 of them are actually used. Both supervisory and unprivileged access (AM = 0x2d or 0x29) are accepted [3]. All registers can be read or written using 16 bit word operations. The base address of the module is set using three coding switches: S1, S2 and S3. The LSB of switch S3 is ignored. The switches are connected to the VME address lines according to this table:

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
$S1_8$	$S1_4$	$S1_2$	$S1_1$	$S2_8$	$S2_4$	$S2_2$	$S2_1$	$S3_8$	$S3_4$	$S3_2$	--	--	--	--	--

The addresses of the internal registers, as byte offsets from the base address, are given below.

Offset	Register name
0	RF-Phase

2	Status/Control
4	Trigger
6	Resynchroniser
8	Threshold
0xa	Interrupt vector
0xc	Interrupt control
0xe	ADC trigger delay
0x10	Harmonic

Based on the above description, a possible C-language structure definition mapping out one module can be written as follows:

```
typedef struct {
    unsigned short phase,       /* RF phase */
       ctrl,                    /* Control and status */
       trig,                    /* Trigger register */
       resync,                  /* Resynchroniser delay in half-buckets */
       threshold,               /* Bunch trigger level DAC */
       vector,                  /* Interrupt vector */
       ictrl,                   /* Interrupt control */
       atd,                     /* ADC trigger delay */
       harmonic;                /* Harmonic number */
}mux;
```

3. Detailed register descriptions

3.1. The RF-Phase register (Offset 0)

The PS-reference frequency can be aligned with the injected beam by writing to this register. The phase can be adjusted in steps of $^1/_{32}$ of a bucket period. Only bits Ph00 to Ph04 are used. The remaining bits are ignored and read back as '0'.

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
phase	-	-	-	-	-	-	-	-	-	-	-	Ph04	Ph03	Ph02	Ph01	Ph00

3.2. The status/control register (Offset 2)

The status register informs about and controls the state of various sections of the module.

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ctrl	-	-	-	-	-	-	-	LOCK	RFdet	PS-RF	PU	CAL	INT	PP	CS	SS

The SS bit selects the source of the reference frequency. When set to '0', an internal 10 MHz signal is used. When set to '1', PS-RF is taken from the front panel input. Similarly, the CS bit selects the source of the calibration RF. When set to '0', an internal source is used. When set to '1' the signal from the CAL-RF front panel input is used instead.

The particle polarity is selected with the PP bit ('0' for positive particles and '1' for negative particles). This bit controls the polarity of the circuit used to detect the passage of the first bunch of particles after a resynchronisation trigger.

D03..D06 are the image of the corresponding front panel LEDs INT, CAL, PU and PS-RF. They indicate the origin of the RF signal available on the FSYNCH outputs. The INT bit is set when the signal from the internal 10 MHz source is active. The CAL bit is set during calibration (between Calibration Start and Stop). The PU bit is set when the signal from the PU input is active. This is normally the case after injection. The PS-RF bit is set when the signal from the PS-RF input is active. This is normally the case between Calibration Stop and injection, provided SS is set.

The RFdet bit is set when a reference frequency is present, either from the PS-RF input if SS is set, or internally generated if SS is cleared. The LOCK bit is set when the RF-Phase Shifter internal PLL circuit has locked onto the reference.

3.3. The trigger register (Offset 4)

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
trig	-	-	-	-	-	-	-	-	-	-	Cal	Stop	Start	Sync	Ext	Inj

To simulate external timings such as injection trigger, external trigger, resynchronisation trigger, calibration start, calibration stop and calibration trigger, software triggers can be produced by writing '1' to the associated register bits: Inj, Ext, Sync, Start, Stop and Cal. This is a write-only register. The effect of multiple simultaneous triggers is undefined.

3.4. The resynchroniser register (Offset 6)

Only bits R00 to R05 are used. The remaining bits are ignored and read back as '0'. This register tells how many RF buckets should pass after detection of the first bunch following RF gymnastics, before a SYN output must be produced.

The value in this register is interpreted as a number of half-buckets. This allows sufficient resolution to keep the synchronisation trigger at a safe distance from the active edge of the BLR and Gate Generator clock. The value to be written here would normally be two or three half-buckets short of h, so that the first bunch to trigger the bunch detector after a RESYN trigger is designated to be the new 'first' bunch one turn later.

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
resync	-	-	-	-	-	-	-	-	-	-	R05	R04	R03	R02	R01	R00

3.5. The threshold register (Offset 8)

The bunch detection threshold level, used to detect the first bunch after RF gymnastics, is set with a 12-bit word. The remaining bits are ignored and read back as '0'. Referred to the required absolute trigger level V_T at the PU input connector, the value to be written into this register should be $N=1000(2.5-V_T/2)$. Values of $N>2500$, corresponding to negative values of V_T, do not yield useful behaviour. The correct sign of the detection threshold is set with the PP bit of the status and control register (0 for positive particles). V_T=100mV, i.e., N=2450, has proved to be a good setting for CODD.

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
threshold	-	-	-	-	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

3.6. The interrupt vector register (Offset 0xa)

The interrupt vector is an 8-bit value that will be applied to the bus during VMEbus interrupt acknowledge cycles. This register will not be cleared by /SYSRESET. Its value upon power-up is undefined. Unused bits read back as '1'.

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
vector	-	-	-	-	-	-	-	-	v7	v6	v5	v4	v3	v2	v1	v0

3.7. The interrupt control register (Offset 0xc)

The interrupt level can be written to bits L[0..2]. Only levels from 1 to 5 will result in interrupts being generated on the VME bus. Levels 6 and 7 are accepted, but are not put on the bus. Setting these bits to zero effectively disables interrupts. The whole register is cleared upon power-up and /SYSRESET.

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ictrl	-	Ical	Istop	Istrt	Isync	Iext	Iinj	Ecal	Estop	Estrt	Esync	Eext	Einj	L2	L1	L0

When set, the Einj, Eext, Esync, Estrt, Estop and Ecal bits enable the generation of the corresponding interrupts upon detection of Injection, External trigger, Resynchronisation, Calibration Start, Calibration Stop and Calibration trigger. The Iinj, Iext, Isync, Istrt, Istop and Ical bits are read-only flags, set when the associated triggers are the cause of an interrupt. Interrupts can be cleared individually by momentarily clearing the appropriate Exxx bit.

3.8. The ADC trigger delay register (Offset 0xe)

This 16 bit wide register specifies the delay to be inserted between the generation of an output SYN or EXT trigger and the associated ADC trigger. This is necessary because the BLR & Gate generator can wait for a programmable number of turns after receiving a trigger before actually producing a gate. The delay is specified in RF buckets, i.e., *h* times the number of turns. This delay is in addition to the hardwired delay of 24 μs which allows the analogue hardware to settle before A-to-D conversion.

3.9. The harmonic register (Offset 0x10)

This 5 bit wide register specifies the harmonic number. Only bits D04..D00 are used. The remaining bits are ignored and always read back as '0'. The input reference frequency, PS-RF, normally at the revolution frequency, is multiplied by the harmonic number to reconstruct the bucket frequency, which must lie between 2 and 10 MHz. The value actually written to this register should be h-1.

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
harmonic	-	-	-	-	-	-	-	-	-	-	-	h04	h03	h02	h01	h00

The frequency multiplier is implemented as a phase locked loop. About 2 ms are needed to achieve lock.

4. Inputs, outputs and indicators

The RF-MUX has numerous I/O connectors, with many different electrical specifications and, sometimes, confusing names. Enumerating them as they appear on the front panel from top to bottom:

PU	in	Terminated into 50Ω. Protected from overloads with clipping diodes.
RFO	out	1Vpp into 50Ω. Back terminated.
ADCT	out	TTL compatible. May be terminated into 50Ω to GND.
DDS	in	800mVpp into 50Ω (100Ω to GND and 100Ω after a coupling capacitor.)
GEN	in	TTL, low true. With internal 4k7 pullup resistor to +5V.
RESYN	in	TTL, low true. With internal 4k7 pullup resistor to +5V.
TRIG-EXT	out	TTL compatible. May be terminated into 50Ω to GND.
TRIG-SYN	out	TTL compatible. May be terminated into 50Ω to GND.
CAL_RF	out	TTL compatible. May be terminated into 50Ω to GND.
CAL_EN	out	TTL compatible. May be terminated into 50Ω to GND.
INT	LED	Lit when the internal 10MHz clock source is active.
CAL	LED	Lit when the RF-MUX is in the calibration state.
PU	LED	Lit when the pick-up signal is selected.
PSRF	LED	Lit when the clock source is taken from the PS-RF input.
TRIG-INJ	in	TTL, high true. With internal 50Ω terminator to GND.
TRIG-EXT	in	TTL, low true. With internal 4k7 pullup resistor to +5V.
CAL-START	in	TTL, low true. With internal 4k7 pullup resistor to +5V.
CAL_STOP	in	TTL, low true. With internal 4k7 pullup resistor to +5V.
PS-CAL	in	800mVpp 50Ω ECL (100Ω to -2V and 100Ω after a coupling capacitor. No clipping diodes.)
PS-RF	in	800mVpp into 50Ω (100Ω to GND and 100Ω after a coupling capacitor. No clipping diodes)
F.SYNCH	out (12)	ECL into 50Ω to -2V.
LOCK	LED	Lit when the internal PLL has locked onto the reference source.
RF	LED	Lit when an RF signal is present, either from the PS-RF input or from the internal 10MHz source, according to the state of the ctrl-SS bit.
SYNCH	LED	Blinks when a pulse is applied to the TRIG-INJ input.
EXT	LED	Blinks when a pulse is applied to the TRIG-EXT input.
ADDRESS	LED	Blinks when the RF-MUX is addressed over the VME bus.

The TTL inputs are protected from overload by Schottky clipping diodes and will function correctly with the application of PS 'standard' impulses, (+30Vp, 1μs). The PS-CAL and PS-RF inputs will likely not survive such treatment.

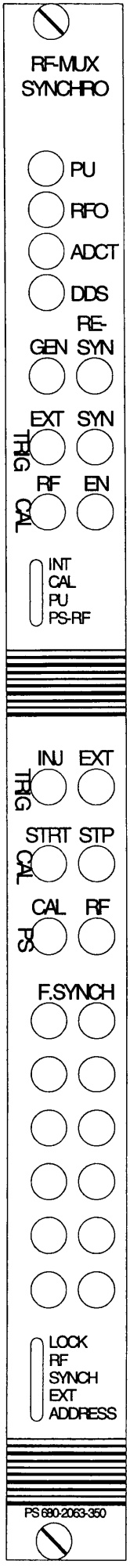

Fig. 3 Front panel

References:

[1] J.L. Gonzalez, "Specification for VME CODD Synchronisation", CERN/PS/BD/Note 98-05 (Tech.)

[2] J.M. Belleman, J.L. Gonzalez, C. Gruber, "The VME Gate and BLR generator", CERN/PS/BD/Note 98-07

[3] VMEbus International Trade Association, "The VMEbus specification", ANSI/IEEE STD1014-1987