EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH
ORGANISATION EUROPEENNE POUR LA RECHERCHE NUCLEAIRE

CERN - PS DIVISION

PS/BD/ Note 98-07 (Tech.)

VME GATE & BLR GENERATOR

J.M. Belleman, J.L. Gonzalez, C. Gruber

Abstract

This note describes the design of the Gate & BLR Generator, a VMEbus module to generate timing signals for the closed orbit display (CODD) of the CERN PS machine. Based on a reference frequency produced by another module, the RF-MUX and Synchroniser, this module produces gating signals for the analogue integrators used in the PS CODD system. The length and phase of the outputs with respect to the reference frequency are programmable over a wide range.

Geneva, Switzerland
28 July 1998

1. Introduction

The Gate and BLR generator is a VME module which, associated with another module, the RF-MUX and Synchroniser [1], generates accurate timing signals for the control of the integrators of the CERN Proton Synchrotron's closed orbit measurement system, CODD. The module accepts a reference frequency and start triggers, via front panel inputs, and produces appropriate timing pulses on its outputs, as directed by the settings of its internal registers. The generated timing is phase locked to the reference frequency input.

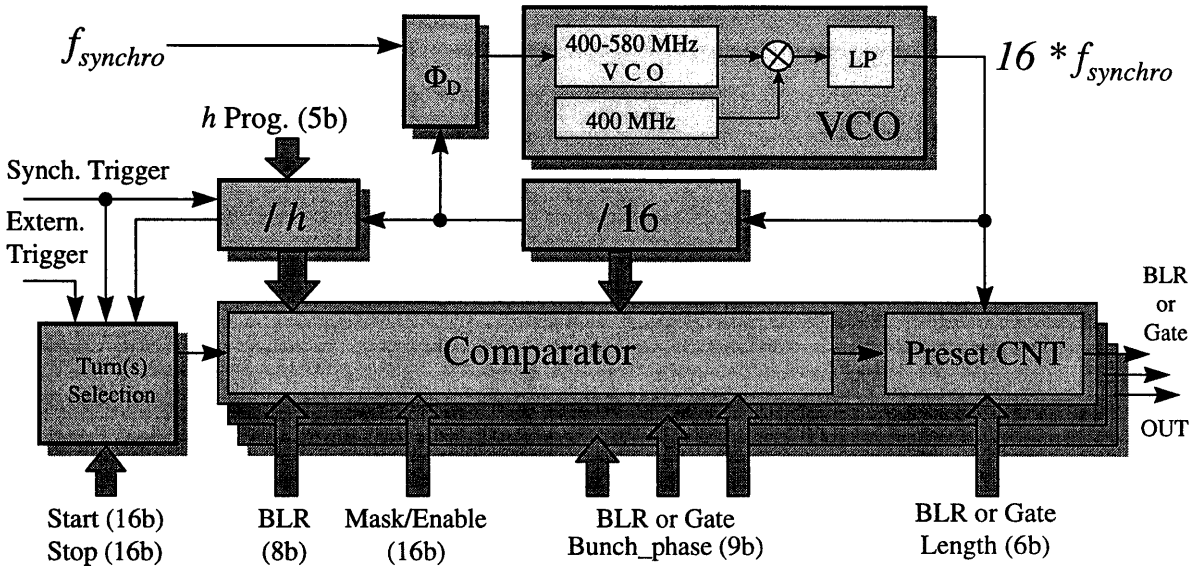

Fig. 1 Block-diagram of the Gate and BLR generator

Referring to Fig. 1, a phase locked loop circuit produces a frequency equal to sixteen times the bunch repetition frequency. A counter, dividing by sixteen and then by *h*, the harmonic number, traverses a full cycle at a rate equal to the revolution frequency of the particles in the accelerator. Eight comparators watch the counter and trigger an output signal when the counter reaches their respective comparison values. The comparators can be made to ignore one or more of the harmonic counter bits, allowing the generation of multiple pulses per turn. An individual length counter for each channel terminates the output after a pre-set number of counts, thus setting the length of the generated pulse.

Another counter keeps track of the number of turns since the last trigger. Its value is compared with the settings of a start and a stop register. The outputs are normally enabled only while the turn number falls between the start and stop values. All timings are scaled linearly with the period of the $f_{synchro}$ input.

2. Address map

The address space covered by the module extends over 16 words mapped into the VME short I/O space. Both supervisory and unprivileged access (AM = 0x2d or 0x29) are accepted. All registers can be read or written using 16 bit word operations. A front panel LED (address) blinks at each access from the VME bus.

The base address of the module is set using three coding switches, S1, S2 and S3. The LSB of switch S3 is ignored. The switches are connected to the VME address lines according to the table below:

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	
$S1_8$	$S1_4$	$S1_2$	$S1_1$	$S2_8$	$S2_4$	$S2_2$	$S2_1$	$S3_8$	$S3_4$	$S3_2$	--	--	--	--	--

The addresses of the internal registers are given below, as byte offsets from the base address.

Address	Register name
0	Harmonic
2	Status/Control
4	Turn start
6	Turn stop
8	Interrupt vector
0xa	BLR
0xc	Length
0xe	Enable/Mask

Address	Register name
0x10	Phase 0
0x12	Phase 1
0x14	Phase 2
0x16	Phase 3
0x18	Phase 4
0x1a	Phase 5
0x1c	Phase 6
0x1e	Phase 7

Based on the above definitions, a possible C-language structure definition mapping out one module can be written as follows:

```
typedef struct {
     unsigned short harmonic,
                    ctrl,
                    start, stop,
                    vector, blr, length,
                    mask,
                    phase[8];
} Ggen;
```

3. Detailed register descriptions

3.1 The harmonic number register (Offset 0)

The reference frequency $f_{synchro}$ is normally a harmonic of the revolution frequency of the accelerator. The harmonic number h can be set by writing to this register. The value actually written should be h-1. Only bits D00 to D04 are used. The remaining bits are ignored. Unused bits read back as '0'. The bucket field of the phase counter runs from 0 to h-1.

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
harmonic	-	-	-	-	-	-	-	-	-	-	-	h04	h03	h02	h01	h00

3.2 The status/control register (Offset 2)

The status register informs about and controls the state of various sections of the module. Although the register as a whole can be both written and read, the functionality of some of its bits implies unidirectional operation.

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
ctrl	Istp	Iext	Iinj	-	-	L2	L1	L0	IEstp	IEext	IEinj	SET	SIT	LOCK	RF	SS

The SS bit (R/W) is used to select the source of the reference frequency. When set to '0', an internal 10MHz signal is used. When set to '1', the reference is taken from the front panel input. The RF bit (RO) reads back as '1' when a reference frequency is present, either from the input if SS is set, or internally generated if SS is cleared. A front panel LED (RF) mirrors the state of the RF bit.

The LOCK bit (RO) is read as '1' when the internal phase locked loop circuit has successfully locked onto the reference. A front panel LED (LOCK) reflects this state. The accepted frequency range is 2..10 MHz.

Writing a '1' to the SIT bit simulates the arrival of an injection trigger pulse, including the generation of the associated interrupt, if enabled. An injection trigger clears all counters, thus marking the start of a new acceleration cycle.

Similarly, the SET bit allows simulation of an external trigger. An external trigger clears the turn counter, but leaves the phase and harmonic counters untouched to conserve the phase relationship defined by an earlier injection trigger. SIT and SET are always read back as '0'. Associated front panel LEDs blink at each occurrence of an injection or external trigger.

The interrupt level can be written to and read back from bits L[2..0]. Only levels from 1 to 5 will result in interrupts being generated on the VME bus. Levels 6 and 7 are accepted, but are not put on the bus. Setting these bits to zero effectively disables interrupts. These bits are cleared by /SYSRESET and upon power-up.

The IEinj bit, when set, enables the generation of an interrupt upon detection of an injection trigger. The Iinj bit is set if an injection trigger was the cause of an interrupt. The IEext bit enables generation of interrupts from the external trigger input. Its associated interrupt flag is Iext. IEstp enables generation of an interrupt upon the turn counter reaching the stop register value. The Istp bit flags that state. Interrupts can be cleared by momentarily clearing the appropriate IE bit.

3.3 The turn start and turn stop registers (Offset 4 and 6)

The number of revolutions after which output pulses will be generated can be written to the start register. When the turn count reaches the value in the stop register, no more pulses will be put out. Both registers are 16 bits wide. The turn count is cleared whenever an injection or external trigger is received. The effect of setting stop ≤ start is undefined. The start and stop registers can be both read and written. Note that the turn counter value cannot be accessed.

3.4 The interrupt vector register (Offset 8)

The interrupt vector is an 8 bit value which will be applied to the bus during interrupt acknowledge cycles. This register will not be cleared by /SYSRESET. Its value upon power-up is undefined. Unused bits read back as '1'.

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
vector	-	-	-	-	-	-	-	-	v7	v6	v5	v4	v3	v2	v1	v0

3.5 The BLR register (Offset 0xa)

This register is unused. See the BLR bit in the mask/enable register instead.

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
blr	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

3.6 The length register (Offset 0xc)

The value written into this register sets the length of the generated output pulse. It is common to all outputs. The pulse length can be set in increments of $^1/_{16}$ of the $f_{synchro}$ period. The length is determined as $(l+1)/(16\, f_{synchro})$. For example, with $f_{synchro}$ = 10 MHz, and length = 7, the output pulse length is $8/(16\, f_{synchro})$ = 50 ns. Only bits D00 to D05 are used. The range of accepted values is 0 to 63, but writing 0 yields a pulse length of $65/(16\, f_{synchro})$. Unused bits read back as '0'.

If the mask field of the enable/mask register is set to allow multiple output pulses, and the length is set such that successive pulses would overlap, only the first pulse of an overlapping set is generated correctly.

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
length	-	-	-	-	-	-	-	-	-	-	L05	L04	L03	L02	L01	L00

3.7 The mask/enable register (Offset 0xd)

The enable bit, when set, allows output pulses to be generated. It is common to all eight channels. The BLR bit, when set, instructs all channels to ignore the turn start and turn stop information, and to generate pulses every turn.

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
mask	-	-	-	-	-	-	-	-	-	BLR	E	m4	m3	m2	m1	m0

The m[4..0] bits act as a mask between the bucket comparator and the bucket field of the phase register (p[8..4]), allowing the generation of output pulses for multiple values of the bucket field. The mask is common to all channels.

An output pulse is generated when the bucket counter matches the value of the bucket field in the phase register. Setting a mask bit to zero prevents the corresponding bucket bit from participating in the comparison. As a result, several values of the bucket counter yield a match and an output pulse is generated for each. As an example, consider the case where the mask has been set to 0x18 and the phase register to 0. The bucket counter and bucket field now match for the buckets 0 to 7, and eight pulses result. This feature is used for the generation of Base Line Restoration pulses.

Note that the bucket counter runs from zero to the value h-1.

3.8 The phase registers (Offsets 0x10 to 0x1e)

This register sets the phase relationship between the $f_{synchro}$ input and the generated output signals. The value written into this register is taken to be in units of $^1/_{16}$ of an $f_{synchro}$ period. Only bits p0 to p9 are valid. Bits p0 to p3 span exactly one $f_{synchro}$ period. Bits p4 to p8 are mapped to the bucket counter (labelled */h* in the diagram), which runs through values 0 to h-1. Therefore, the value of this field should not exceed h-1, or no output will result. Bit p9 serves as a carry bit for the bucket field. When the value of the bucket field reaches h, this bit should be set, and the bucket field should start over at zero. In this way, the phase can reach over two consecutive turns.

	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
phase0	-	-	-	-	-	-	p9	p8	p7	p6	p5	p4	p3	p2	p1	p0
phase1	-	-	-	-	-	-	p9	p8	p7	p6	p5	p4	p3	p2	p1	p0
phase2	-	-	-	-	-	-	p9	p8	p7	p6	p5	p4	p3	p2	p1	p0
phase3	-	-	-	-	-	-	p9	p8	p7	p6	p5	p4	p3	p2	p1	p0
phase4	-	-	-	-	-	-	p9	p8	p7	p6	p5	p4	p3	p2	p1	p0
phase5	-	-	-	-	-	-	p9	p8	p7	p6	p5	p4	p3	p2	p1	p0
phase6	-	-	-	-	-	-	p9	p8	p7	p6	p5	p4	p3	p2	p1	p0
phase7	-	-	-	-	-	-	p9	p8	p7	p6	p5	p4	p3	p2	p1	p0

4. Front panel

The front panel gives access to the input and output connectors and some LED indicators.

0..7	out	Gate or BLR outputs. ECL. Must be terminated into 50Ω to -2V.
F beam	in	Reference frequency input. 2 to 10 MHz. ECL levels, internally terminated into 50Ω to -2V. The RF front panel LED lights if a signal is present on this input, provided it has been selected by setting the SS bit in the *ctrl* register. If the input frequency lies between 2 and 10 MHz, the LOCK front panel LED will also light.
INJ	in	Injection trigger input. TTL or 'standard' pulse (30V, 1µs). Unterminated, but with 10kΩ to +5V. Leading edge triggered. The 'INJ' front panel LED blinks in response to a pulse on this input.
EXT	in	External trigger input. TTL or 'standard' pulse (30V, 1µs). Unterminated, but with 10kΩ to +5V. Leading edge triggered. The 'EXT' front panel LED blinks in response to a pulse on this input.
LOCK	LED	The green 'LOCK' LED lights when the internal phase locked loop is locked onto the input frequency.
RF	LED	Lit when a signal is present on the F-BEAM input.
INJ	LED	Blinks in response to a pulse on the INJ input.
EXT	LED	Blinks in response to a pulse on the EXT input.
ADDRESS	LED	Blinks when the module recognises its VME address.

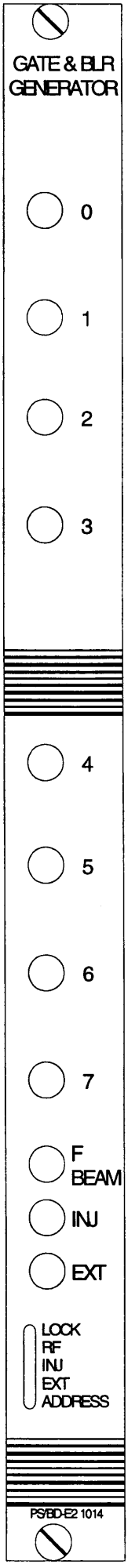

Fig. 2 Front panel

References

[1] VMEbus International Trade Association, "The VMEbus specification", ANSI/IEEE STD1014-1987

[2] J.L. Gonzalez, "Specification for VME CODD Synchronisation", CERN/PS/BD/Note 98-05 (Tech.)

[2] J.M. Belleman, J.L. Gonzalez, C. Gruber, "The VME RF-MUX and Synchroniser", CERN/PS/BD/Note 98-08