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SPECIFICATION FOR VME CODD SYNCHRONIZATION

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ABSTRACT

To cope with new operational aspects and new beam requirements, brought about by the needs of the LHC project, the PS Closed Orbit Acquisition (CODD) Synchronization has been upgraded. For this system to handle harmonic numbers 4, 7, 8, 10, 16... and such operations as bunch splitting or bunch merging, extra hardware has been designed.
Part of this system is implemented as VME modules, located in a dedicated VME crate, DCPSCODS. In the future, we aim at grouping all of the synchronization hardware in this crate.
On the software side, DCPSCODS must control this hardware and communicate with CODD application programs.

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1. Introduction

To cope with new operational aspects and new beam requirements, brought about by the needs of the LHC project, the PS Closed Orbit Acquisition (CODD) Synchronization has been upgraded. For this system to handle harmonic numbers 4, 7, 8, 10, 16... and such operations as bunch splitting or bunch merging, extra hardware has been designed. Since the signals distributed by the RF-group do not stay in-phase with the accelerated bunches, we must generate our own signals.

Part of this system is implemented as VME modules, located in a dedicated VME crate, DCPSCODS. In the future, we aim at grouping all of the synchronization hardware in this crate.

On the software side, DCPSCODS must control this hardware and communicate with CODD application programs. It needs then a 'standard equipment module' and specific programs.

2. VME Hardware

The VME crate DCPSCODS is equipped with:
- 1 SAC (remote reset module)
- 1 MVME 147SA-1 (CPU)
- 3 TG8 (8 channel timing generator)
- 1 VME PDFP-CTRL (serial link to NIM PDFP)
- 1 RF-Mux and Synchronizer (source signal selection and synchronization)
- 10 specific modules "GATE & BLR Generators" (acquisition timing signals for integrators)

3. NIM Hardware

The NIM crate associated to DCPSCODS contains:
- 1 PDFP (reference frequency tables)
- 2 DDS (frequency synthesisers)
- 1 Receiver and Phase Discriminator
- 1 ADC (phase-error signal to correct the DDS frequency)
- 2 RF-Distribution modules

4. Operation principles

CODD uses 40 pick-ups (PU) to measure the horizontal and vertical beam position during the PS acceleration cycle (excluding RF-gymnastics intervals). These pick-ups are installed in straight sections, according to the following distribution: 0, 3, 5, 7, 10, 13, 15, 17, 20, ... , 90, 93, 95, 97.

Position measurements are done with integrator modules that need timing signals, synchronous to the beam. These signals are generated in the 'Gate & BLR' modules. The Base Line Restoration (BLR) signals are usually produced on every bucket, however, for special operations, they can also be disabled. Depending on the injector machine, the acquisition gates must satisfy the following sequences (note that positive and negative particles turn in opposite directions):
- Booster injection: 43, 45, 47, ... , 37, 40
- EPA, e+ injection: 93, 95, 97, ... , 87, 90
- EPA, e- injection: 73, 70, 67, ... , 77, 75

Presently, CODD has two main operating modes: calibration and beam measurement over two consecutive turns [1]. Later on, CODD might acquire a single bunch, or the total number of bunches, over multiple revolutions, using fast integrators. The synchronization system must be prepared for that mode of operation too.

4.1 Calibration

The calibration process takes place during the "dead-time" of every machine cycle, between C0 and C100, and the calibration settings must be provided to the Gate & BLR Generators before C0. The PTIM-V start and stop signals are: PX.SCODDCAL and PX.ECODDCAL. The calibration frequency is selected in the RF-Mux and calibration pulses are produced at 5 ms intervals by a 'Burst Generator', allowing 16 acquisitions per cycle.

4.2 Beam measurements

For historical reasons, injection measurements are treated differently from C-timing measurements. Before the beam is injected, synchronization parameters such as harmonic number h, bunch number and turn number must already be set (this can be done after calibration, since injection usually occurs at C215).

4.2.1 Injection measurements

This is a ppm measurement that is automatically triggered on each cycle, according to operator settings. Bunch and turn numbers may be different for each PLS-Line. The most recent measurement parameters for a given PLS-Line override previous settings. The injection trigger `PIX.SCODD` (from a TG8 that counts PS RF-periods, after the injection kicker trigger) synchronises the Gate and BLR Generators.

Once, during initial set-up, the BLR and Gate settings must be hand adjusted. Then, the remaining settings can be calculated, since the Gate & BLR Generators are realised so as one revolution period can be expressed in units of their VCO period ($Trev = 16 \times h \times Tvco = 100$ straight sections).

4.2.2 C-Timing measurements

During a cycle, 10 ppm measurements can occur, with 10 ms between each acquisition (set by DCPSCODD). Since several consoles can ask for measurements, C-timings must be checked to avoid overlap. Bunch and turn information is necessary, essentially when either a Booster ring is not injected or any bunch is missing.

When RF-Gymnastics are applied during the cycle, two timing signals indicate the beginning and the end of the process: the first tells the software to set the hardware with new harmonic conditions and the last one permits re-synchronising to one of the remaining bunches.

4.2.3 C-Timing measurements for MRP

When the Mean Radial Position measurement system (MRP) asks for measurements, it takes possession of CODD for the required machine cycle and the calibration time of the next. CODD is then triggered every 5 ms by a burst generator and the whole information is acquired by DCPSMRP at the end of the cycle.

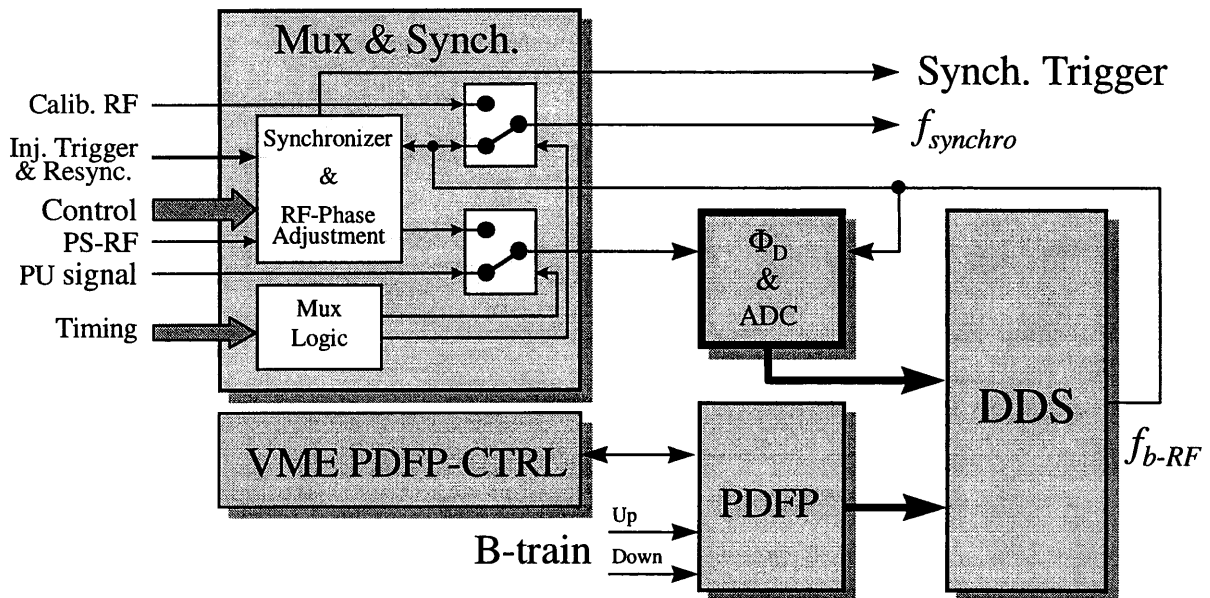## 5. New CODD $f_{b\text{-}RF}$ Generation

5.1 Principle

Figure 1: CODD $f_{b\text{-}RF}$ generation

Figure 1 shows a block-diagram of the frequency generator for the CODD synchronization, using PS-RF standards [2]. It is based on a digital Phase Locked Loop (PLL), which is a stripped version of the MRP hardware [3]. The PLL compares the phase of the output frequency $f_{b\text{-}RF}$ to either the PS-RF or the PU signal.

To avoid frequency or phase jumps when the beam is injected into the accelerator, the loop is first locked to the PS reference frequency, which must be aligned with the injected beam, and then switched to the beam signal from a pick-up.

The PLL is realised in NIM modules. It contains a Receiver and Phase Discriminator module, an ADC that converts the analogue phase error into digital words, two Direct Digital frequency Synthesisers (DDS), and a Programmable Digital Frequency Program (PDFP) [4].

The PDFP, controlled by programming the theoretical frequency tables for several PLS-Lines into dedicated memory banks of the VME PDFP-CTRL [5], allows ppm operation. Since RF-gymnastics require harmonic changes during the PS cycle, bank switching is achieved using external triggers, produced at the beginning of these processes.

5.2 PDFP control

Frequency programs $f(B, particle, harmonic)$ must be calculated in the DSC and downloaded into the PDFP, using one bank per particle-type and per harmonic (the present hardware has 8 banks). On the previous cycle, the injection bank is chosen at ELFT, so that B-count starts at C0 and the DDS-PLL locks to the PS-RF during the calibration process. Other external triggers and bank mappings must also be set before C0.

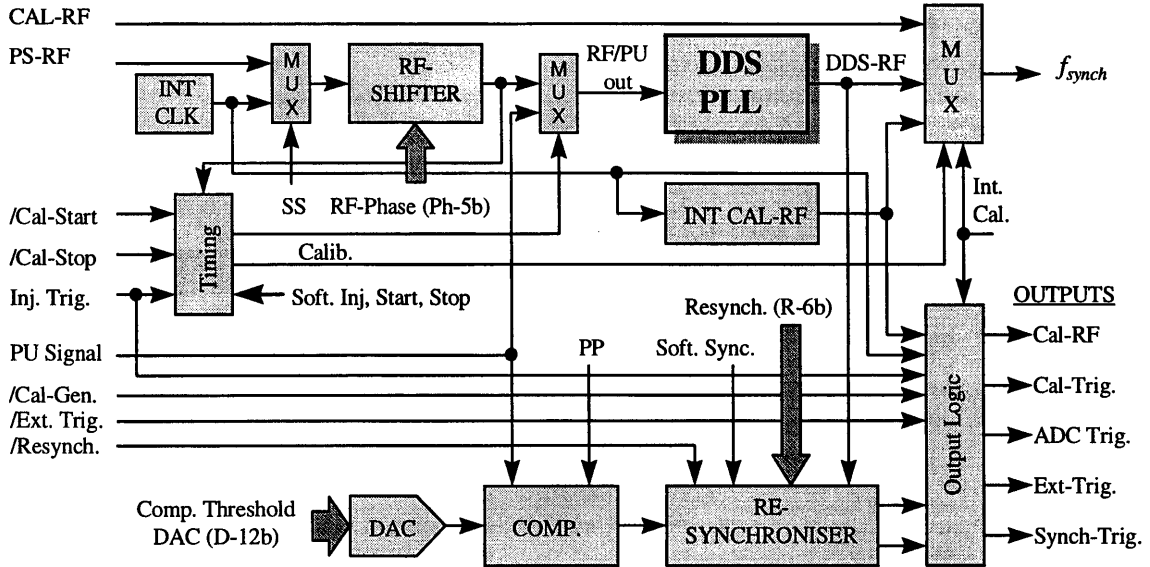## 6. RF-Mux and Synchronizer

Figure 2: RF-Mux and Synchronizer

Figure 2 shows a block-diagram of the RF-Mux and Synchronizer module [6]. Prompted by TG8-timings, it selects the appropriate source for the PLL: calibration-RF between C0 and C100, PS-RF after C100, and the PU signal after injection. Smooth transition from the PS-RF to the PU-signal is achieved using the ppm setting of the PS-RF Phase shifter (5 bits). To handle RF-Gymnastics and re-synchronise to a circulating bunch, the Synchronizer needs ppm information on the particle polarity (PP), the detection threshold (DAC, 12 bits) and new harmonic-dependent values (6 bits).
Extra control registers are used for the debugging of the module without external input signals.

7. VME CODD GATE and BLR Generators
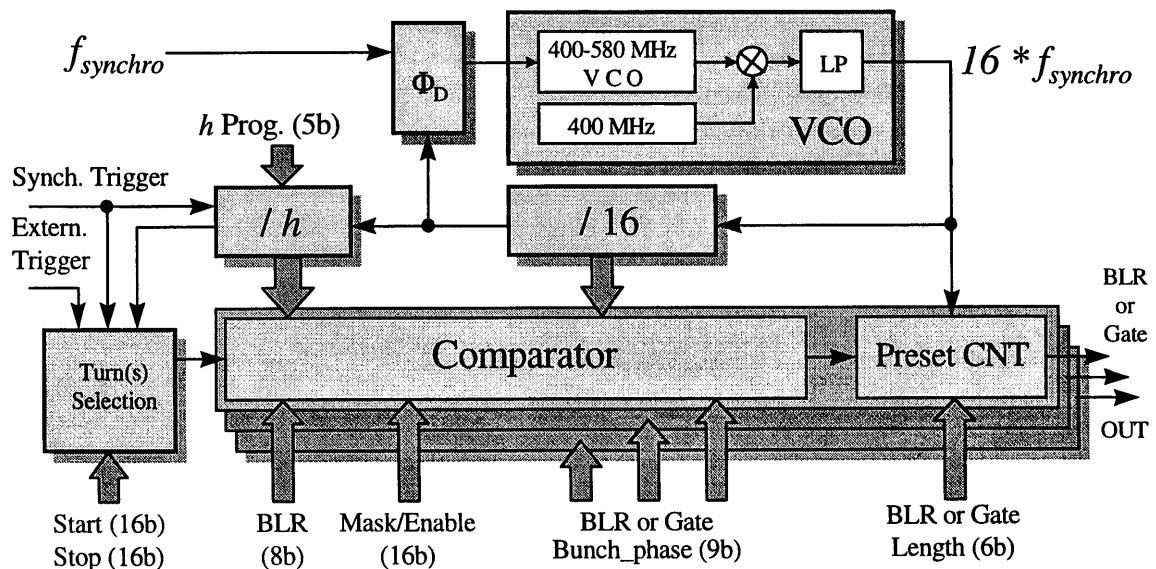
7.1 Principle

Figure 3: CODD GATE and BLR Generators

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Figure 3 shows the block diagram of the VME-module that generates the acquisition Gates or Base Line Restoration (BLR) pulse trains [7]. In order to ensure sufficient resolution (1/16 of $f_{synchro}$ period), a 9-bit comparator allows for the acquisition of any bunch on any pick-up.

Counting over a full revolution period is achieved with a bucket counter which uses the harmonic number information. The turn counter handles up to 64 K turns, after reception of either the Synchronisation Trigger or the External trigger. Considering this limit, contiguous acquisitions can start at a pre-selected turn.

Multiple BLR or Gate production over a single revolution period is achieved by programming the comparator mask (5 bits on the Enable/Mask Register). A 6-bit preset counter that counts $16 \times f_{synchro}$ periods sets the BLR or Gate length, which may cover more than a full bucket. The BLR and Gate output signals can be enabled or disabled, using one bit on the Enable/Mask Register.

7.2 Control

CODD Synchronisation uses 10 Gate & BLR Modules: 5 for BLR-functions and 5 for Gate-generation. Most of their operational settings are loaded after C100, when the calibration process is complete. Depending on the desired response, the Enable and Mask register is programmed accordingly. Harmonic Number h (5 bits) is set prior to injection, according to the PLS-Line. It is also modified at the beginning of RF-Gymnastics to allow the PLL to lock before re-synchronisation.

The Bunch-phase register (9-bit) contains 2 programmable areas: the bucket selection (5 bits) and the phase selection within a bucket (4 bits). Two parameters are used to control the output length (6 bits): the Gate length and the BLR length.

The Start and Stop registers (16 bits) set the turns that are to be acquired (only 2 now: Stop = Start + 2), starting after a predefined number of turns (Start).

8. CODD Application program

For each measurement, either at injection or using C-timings, CODD application program must send the bunch and turn information to both the DCPSCODD and DCPSCODS systems. Injection measurements use equipment numbers 6013-6019, depending on the injector. For a C-measurement, each equipment (6001-6010) sends also the C-measurement value.

References

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[3]   J. Belleman, V. Chohan, J.L. Gonzalez, S. Johnston, E. Schulte, E. Thivent, *Measurement of the Mean Radial Position of a Lead Ion Beam in the CERN PS*, EPAC-96, 10-14 June 1996, Sitges (Barcelona), Spain, CERN/PS 96-23 (BD), July 1997.

[4]   E. Thivent, *PDFP: Programmable Digital Frequency Program*, draft document.

[5]   E. Thivent, *PDFP-CTRL: Carte de Communication VME*, draft document.

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