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A fast bipolar gated integrator

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Abstract

This note describes the design of a bipolar gated integrator with base line restoration. Measurements are presented which show that non-linearity and noise are below 0.1% of full scale for 100 ns gates. Useful data can be obtained with gate lengths ranging from 30 ns to several microseconds. Three integrators and a peak detector, together with a 12-bit ADC, have been assembled on a single printed circuit board to create a data acquisition system for the beam position monitors in the TT2 and TT70 transfer lines of the CERN PS accelerator complex.

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1. Introduction

New gated integrators with base line restoration (BLR) have been developed for use with the electrostatic beam position monitors (BPMs) in the TT2 and TT70 transfer lines of the CERN PS accelerator complex. Three integrators, a fast peak detector, a four-channel 12-bit successive approximation ADC and the associated timing and control circuitry have been assembled onto a single printed circuit board (fig. 1). The board communicates with external logic via a simple interface bus consisting of two control and twelve data lines. The integrators are based upon commercially available high performance operational amplifiers and do not contain any exotic parts.

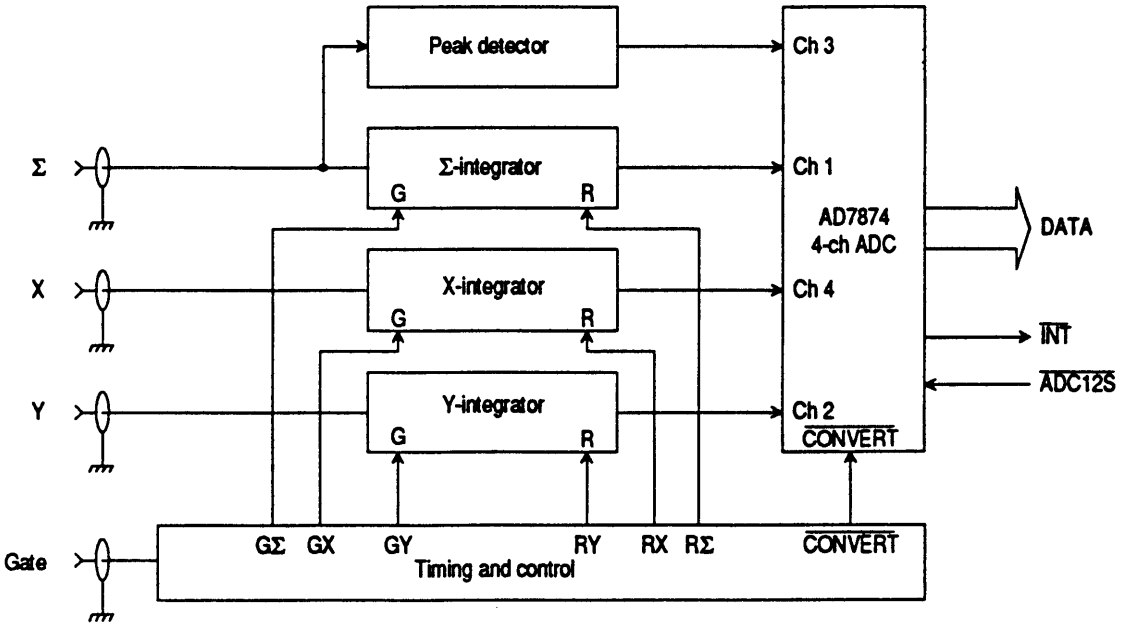

Fig. 1: Block diagram of integrator board

2. Principle of operation

2.1 Integrator

The circuit topology is basically a differential integrator built around an OPA627 OpAmp (fig. 2) [1, 2]. Base line shifts are removed by integrating only the deviations of the input signal with respect to a sample taken just prior to application of the gate. A Harris type HA5351 sample-and-hold is used for this function [3].

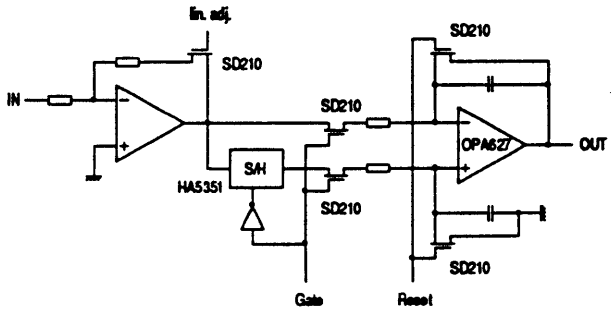

Fig. 2: Simplified integrator schematic diagram

The integrator is gated by a pair of SD210 DMOS FETs [4], and reset by another pair. The symmetry of the circuit all but cancels charge injection errors. The FETs are switched with large swings to ensure good linearity, at the expense of increased power dissipation in the drive circuitry. Part of the remaining non-linearity of the gate FETs is compensated by predistorting the signal in the first amplifier stage, which has the same type of FET in its feedback path. Thus, a linearity error of less than 1 part in 1000 is attained, the residue being mainly attributed to differences between individual FETs. No attempts were made to select matched sets, but a trim adjusts the gate voltage of

the predistortion FET to obtain best linearity. Possibly, the use of the SD5000 series quad monolithic FET chips would have yielded a better match.

Even though the SD210 series are claimed to be bilateral analogue switches, the orientation makes some difference, and was chosen experimentally for best linearity, at the cost of a slightly increased charge injection. Provisions have been made to compensate by injecting small charges derived from the gate and reset transitions, using capacitors which generally end up having sub-pF values.

The components setting the integrator time constant have been chosen so as to overwhelm parasitic effects, while still yielding a reasonable output voltage. With the typical shape of the input signal, the amplifier operates just below its 40 V/µs slew rate limit. A post-amplifier (not shown) matches the output voltage to the ±10 V range of the ADC. The ADC is an Analog Devices AD7874, a 4-channel, 12-bit, simultaneous sampling, successive approximation converter [5].

The input impedance of the integrator is 50 Ω. Full scale, at -2048/+2047 counts, is ±40 nVs, which sets the value of the conversion constant at -19.5 pVs/count. The integrator inverts. There is no gain trim.

2.2 Peak detector

The peak detector (fig. 3) [6], connected to the sum channel, is intended as a diagnostic tool and aid to correctly adjust the amplitude of the input signal. It provides a rough measurement of the peak input voltage. No special care has been taken to ensure accurate and linear performance. Note that this circuit actually adds the outputs of separate positive and negative peak detectors. This implies that signals with both positive and negative excursions may yield an output near zero. The peak detectors are not reset and decay naturally with a time constant of approximately 100 µs. The response function has a dead zone in the centre (fig. 4). Some gain has been added after the peak detector to match its output voltage range to the ADC, but this expands the size of the dead zone.

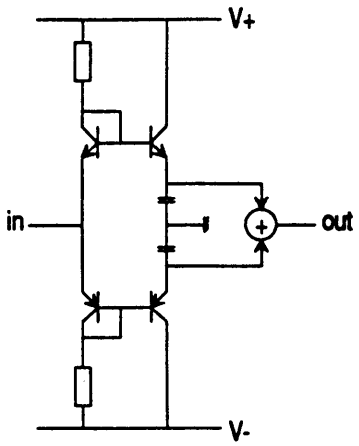

Fig. 3 Peak detector schematics

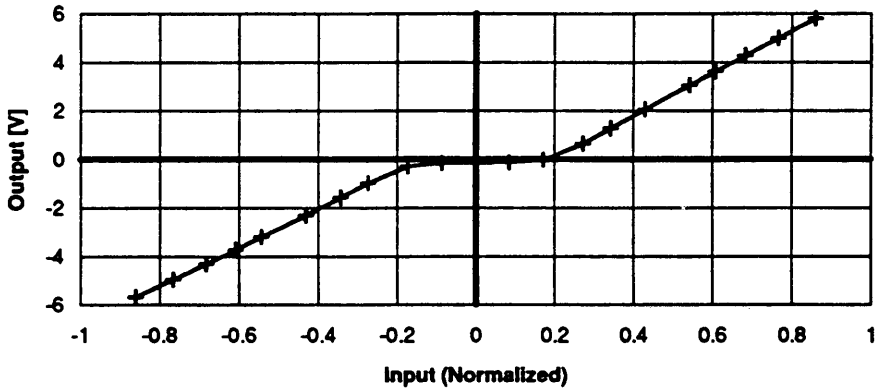

Fig. 4: Peak detector response

3. Timing

The integrator operates according to a fixed sequence, triggered by the application of an ECL high level at the gate input (fig. 5). The base line sampler is switched into the hold mode. The reset switches, which up to then held the integrator to zero, are released. Then the gate is opened. The input signal is integrated for the duration of the gate.

When the gate input is taken low, the gate is closed and the base line sampler is switched back to track mode. The exact timing relationship of these events is determined by the various driver circuit delays.

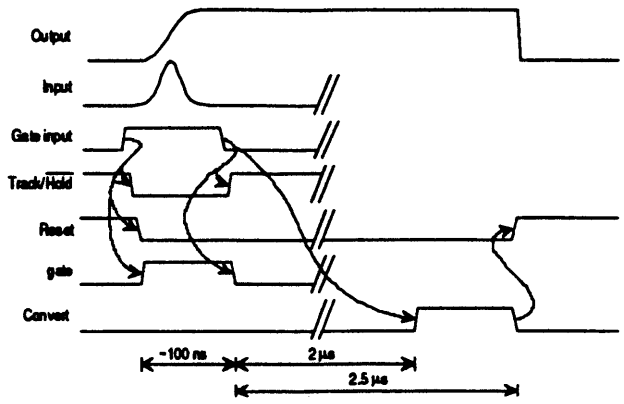

Fig. 5: Sequence of operation

After 2 µs, time required to allow the AD7874 ADC to sample its input, the A-to-D conversion is started, and 500 ns after that, reset is re-applied. Finally, about 60 µs after start of conversion, the ADC signals its readiness by taking the /INT line low (fig. 6). Four data words can then be read out by taking /ADC12S low four times consecutively. Note that /INT will go high during the first read. For exact timing information, refer to the AD7874 data sheet [5].

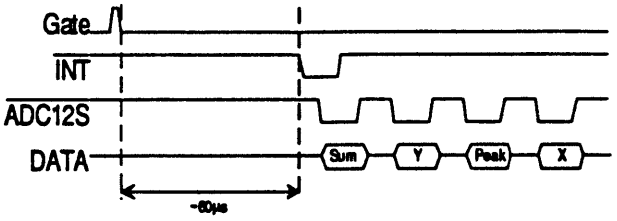

Fig. 6: Timing diagram of readout sequence

4. Interface

The integrator board is connected to the readout logic using a simple bus with 12 data lines and 2 control lines, connected through a 34-pin flat-cable connector type 3M-3431-6002 or equivalent (fig. 7). The data lines are buffered to relieve the ADC from having to drive the relatively heavy load of the data bus lines. The data format is 2's-complement binary.

GND	1	2	RD0
GND	3	4	RD1
GND	5	6	RD2
GND	7	8	RD3
GND	9	10	RD4
GND	11	12	RD5
GND	13	14	RD6
GND	15	16	RD7
GND	17	18	RD8
GND	19	20	RD9
GND	21	22	RD10
GND	23	24	RD11
GND	25	26	-
GND	27	28	-
GND	29	30	-
GND	31	32	/INT
GND	33	34	/ADC12S

Fig. 7: Interface connector layout (top view)

5. Measurement results

5.1 Responses

The integrator response is measured using a generator delivering approximately Gaussian pulses, akin in shape to a particle bunch as seen by the BPMs [7]. The pulse polarity can be selected positive or negative. The pulse area is estimated to be 34 nVs and $\sigma \approx 10$ ns. The generator is connected to the integrator via a precision Rohde & Schwartz attenuator [8].

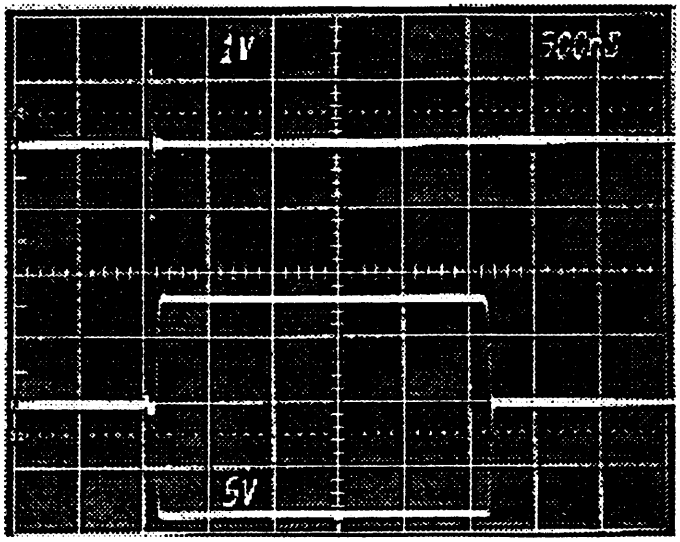

Fig. 8: Integrator doing positive/negative integrations

Fig. 8 shows a double exposure of the integrator input (top trace, 1 V/div) and analogue output (bottom trace, 5 V/div). The time base is set to 500 ns/div. The input pulses, hard to see on the picture, occur just after the second vertical division, and have about 1.2 V amplitude. A-to-D conversion is initiated 2μs later, at the 6th vertical division. The integrator is reset just after the 7th division. Clearly this timing is very relaxed, as far as the integrator is concerned.

The response function (fig. 9), measured between ±85% of full scale, appears a perfectly straight line.

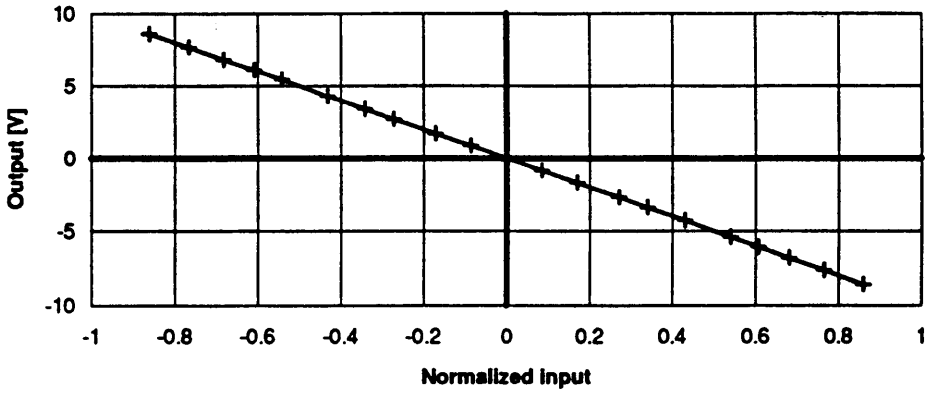

Fig. 9: Input to output response

The precision of the attenuator was found to be insufficient to accurately characterize linearity errors. Therefore, a correction table was made by applying a DC voltage to its input while measuring the output voltage with a precision, high resolution voltmeter, in accordance with a test procedure described by the manufacturer. The correction values are of the order of 10^{-3}. This procedure is justified by the observation that (relatively) wild excursions in the linearity error plot of the integrator, anti-symmetric with respect to zero, are strongly diminished. The validity of this result critically depends on the linearity of the high resolution voltmeter (a Solartron 7075) and on the assumption that the DC measurements are equally valid for pulse type signals.

The plot below (fig. 10), shows the deviation of the integrator response from a least-squares straight line fit. Both abscissa and ordinate are expressed as a fraction of full scale. The smoother curve has the forementioned correction for the attenuator errors applied. The irregular curve uses the nominal, uncorrected attenuation values.

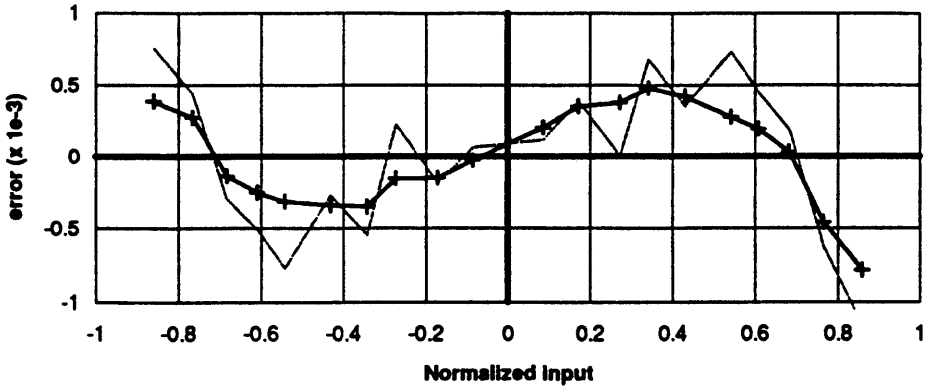

Fig. 10: Residual linearity error of integrator

The residual linearity error plot appears to be dominated by a curve of the 3rd degree. The magnitude of the error justifies the use of a 12 bit ADC. Each data point is the mean of 100 acquisitions, to increase resolution and filter the effects of random noise.

5.2 Noise

The noise of the integrator was determined by histogramming 1000 consecutive measurements with a 100 ns gate and zero input (fig. 11). The distribution matches a Gaussian with 0.83 counts standard deviation. This corresponds to 1/5000 of full scale. The noise appears to originate virtually entirely from the sample-and-hold used for base line restoration. This S/H has its output noise specified as 325 μV_{RMS} typical, which in this context is not continuous noise, but rather the standard deviation of its output value for a fixed input [3]. This looks to the integrator as a random constant DC input signal during the gate time and thus leads to an error which grows linearly with gate time (fig. 12). This error completely overwhelms the originally expected relation proportional to $\sqrt{T}$, associated with continuous white Gaussian input noise [9]. Noisy input signals compound the problem, because the instantaneous, rather than the mean value of the input voltage is held and integrated for the duration of the gate.

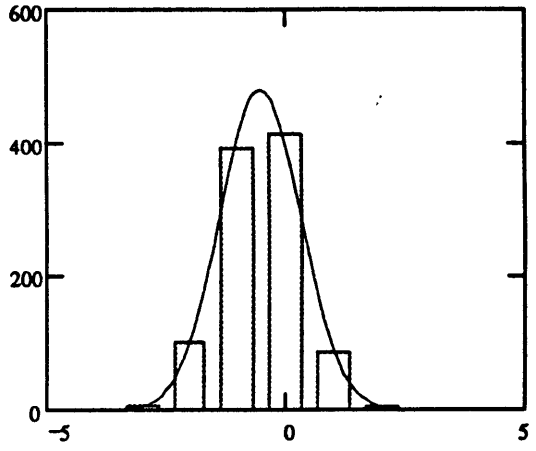

Fig. 11: Output noise histogram

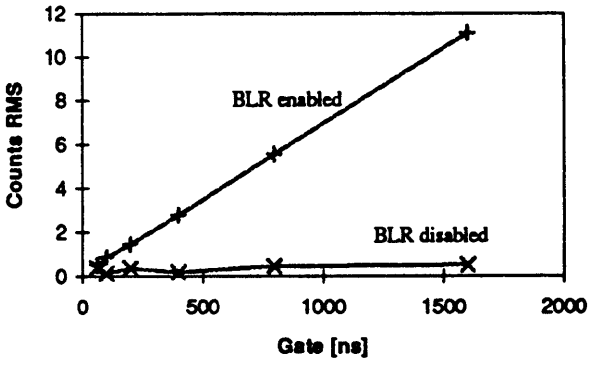

Fig. 12: Output noise vs. gate length

6. Summary of specifications

Integrator analogue inputs:

Input impedance	50 Ω
Input voltage range	± 1.7 V_p (Including base line shift.)
Full scale	± 40 nVs
Conversion gain	-19.5 pVs/count
Noise	20 pVs, 1 count (RMS)
Offset	± 10 counts
Non-linearity	± 1 count

Gate (ECL) :

gate input impedance	50 Ω (into -2 V)
gate high level voltage	-0.8 V
gate low level voltage	-1.9 V
gate delay	25 ns
Repetition rate	100 µs

Outputs:

/INT	TTL compatible, open drain output
/ADC12S	TTL input
D0..D11	TTL output, three state

Supplies:
+12 V, 180 mA
-12 V, 270 mA
5 V, 230 mA
-5 V, 320 mA

7. Conclusions

At the time of writing, ten boards (30 integrators) are installed in the TT2 and TT70 beam transfer lines of the CERN PS accelerator complex. The same development, with a different ADC and some minor modifications in the timing, will also be applied to the PS closed orbit acquisition system, allowing single bunch, multi-turn trajectory measurements to be carried out.

8. Acknowledgements

I am indebted to E. Schulte, who never ceased to urge me to get this project done, to J. Gonzalez, for his readiness to always discuss myriad circuit details, and to J-L. Chouvet for his painstaking work on the printed circuit board layout and for his patience incorporating the large number of detailed modifications I kept bringing in.

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