UNIVERSITY OF OXFORD

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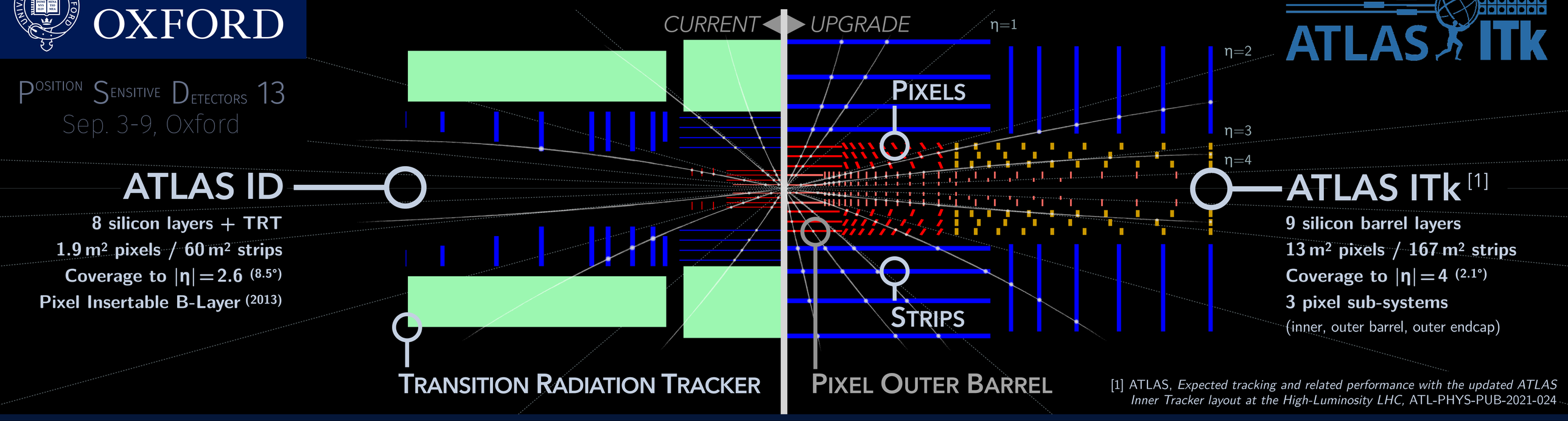
Position Sensitive Detectors 13
Sep. 3-9, Oxford

ATLAS ITk



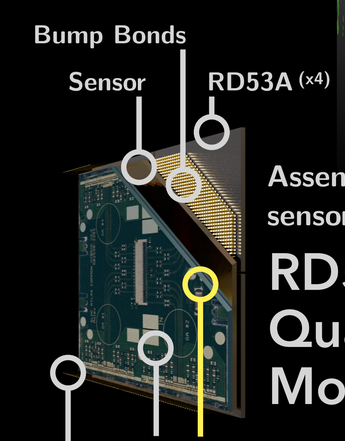
[1] ATLAS, *Expected tracking and related performance with the updated ATLAS Inner Tracker layout at the High-Luminosity LHC*, ATL-PHYS-PUB-2021-024

Pixel Interlock and DCS in SR1

for the Outer Barrel RD53A Demonstrator

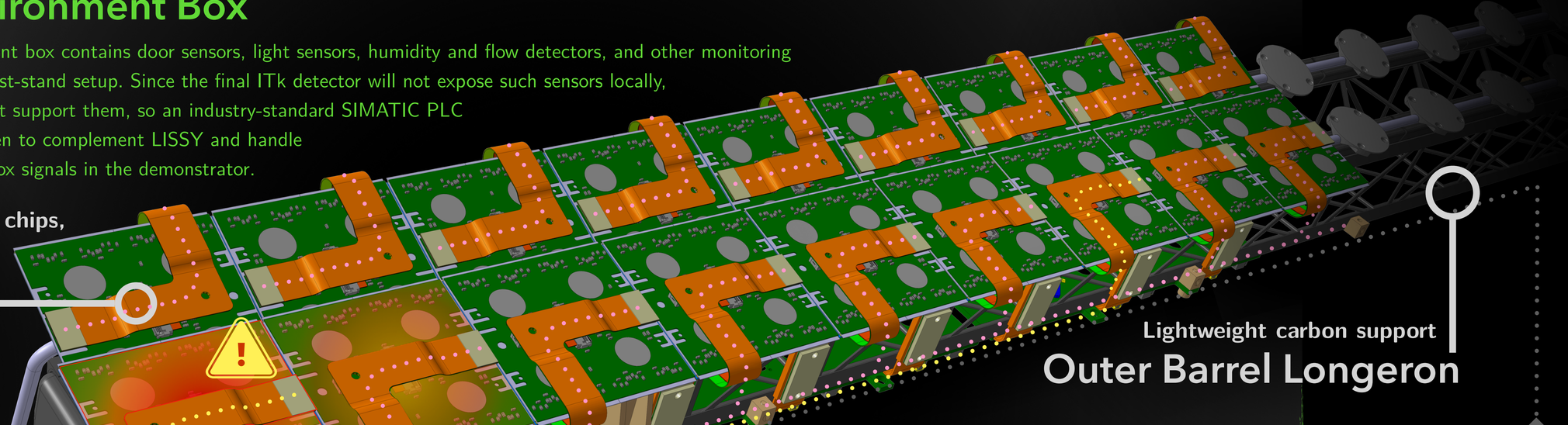
SR1 Environment Box

The environment box contains door sensors, light sensors, humidity and flow detectors, and other monitoring specific to a test-stand setup. Since the final ITk detector will not expose such sensors locally, LISSY does not support them, so an industry-standard SIMATIC PLC has been chosen to complement LISSY and handle environment box signals in the demonstrator.



Assembly of readout chips, sensor, flex PCB

RD53A Quad Module



Ti piping
CO_2 Cooling

Data and power, NTC data digitised via MOPS (*Monitoring of Pixel System*) chips

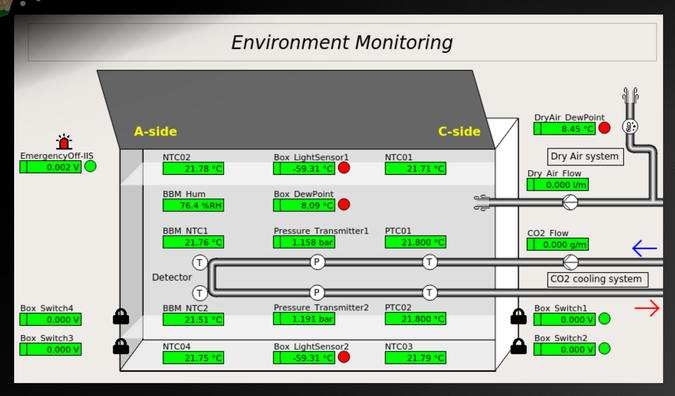
Patch Panel 0

The last module NTC in each serial powering chain is routed directly to the interlock crate.

Digital/analog data and LV/HV power transfer

Module Flex Cable

MOPS Digital NTC Data



Env. Box Signals

Power Distribution

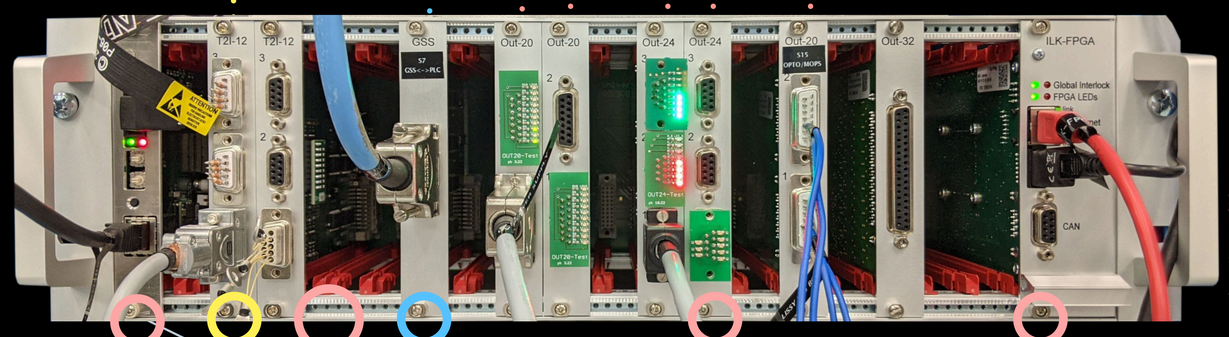
Analog NTC Temperature

Interlock Decision Signals

Env. Box Signals

CO_2 Plant

Cooling Control



NTC data for all non-interlock modules read out via MOPS chips

MOPSHub
for beginners
MOPS readout

Power Supplies
low + high voltage power

OPC-UA Server

Env. Box PLC
SIMATIC Programmable Logic Controller

The PLC has been developed to support *all* interlock functions; this alternate mode of operation will be used at outer barrel loading sites, since they will not receive a LISSY crate.

Monitoring FPGA

NTC inputs
Temperature 2 Input cards

Digital interconnect
Global Safety System card

Interlock signal outputs
OUT cards

Interlock FPGA
hot-swappable interlock matrix

OPC-UA Server

The OPC Unified Architecture (UA) data exchange protocol is used to standardise communication with hardware devices.

OPC-UA Server

ATLITPMOPSHUB4B

WinCC-OA distributed project
(**ATL**AS **IT**k **P**ixel **DEMO**nstrator)

ATLITPDEMO

OPC-UA Server

LISSY Crate
Local Interlock and Safety System

Interlock monitoring panels are provided as linked physical (crate-centric) and logical (demonstrator-centric) views for ease of operator use.

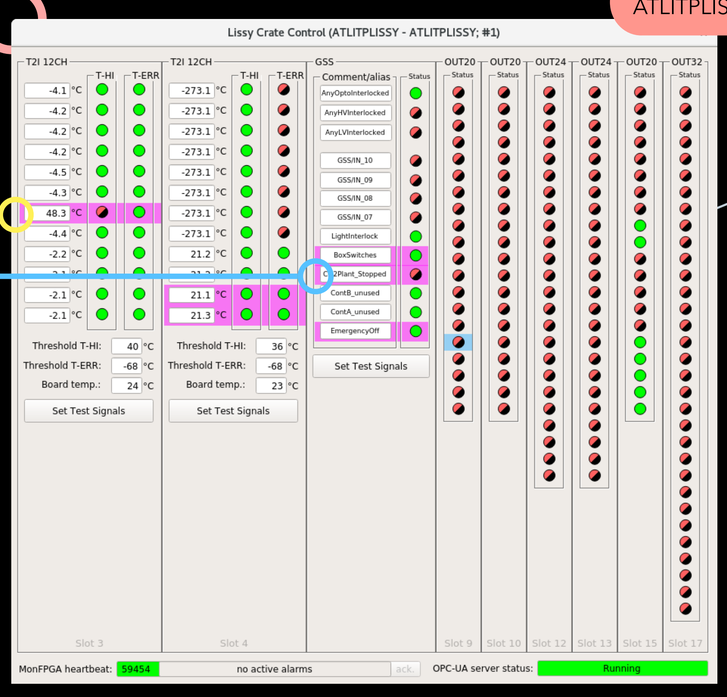
LISSY Panel
***Physical-view* control interface**

ATLITPLISSY

ATLITPENVBOX

The SR1 demonstrator uses the same WinCC-OA SCADA software, OPC-UA communication protocol, CERN JCOP framework, Final State Machine (FSM), and distributed project structure as the current ATLAS DCS system, allowing developments for the demonstrator to generalise for ITk, post-commissioning.

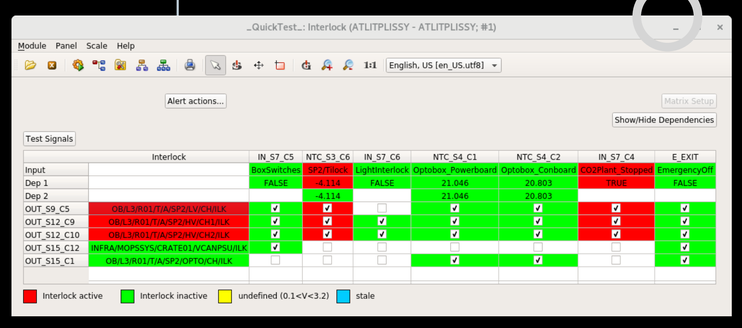
WinCC OA Distributed System



Temperature fault

Cooling/Env. Fault
(from PLC)

Interlock Panel
***Logical-view* control interface**



Status and Outlook

The LISSY + PLC solution will soon replace the current IBL interlock in use for the Pixel demonstrator, bringing the demonstrator in-line with the final ITk interlock solution. The LISSY DCS is complete, and physical integration is ready to go - only the actual swap remains.

References and Acknowledgements

Longeron render prepared by Diego Alvarez Feito (CERN)

Particular thanks to Hans Joos (U. Göttingen, CERN), Jarl Pettersen (CERN), and Nicola Pacifico (CERN) for their contributions to the demonstrator DCS system and development of the PLC interlock infrastructure.

CERN