Overview of the ATLAS High-Granularity Timing Detector: project status and results

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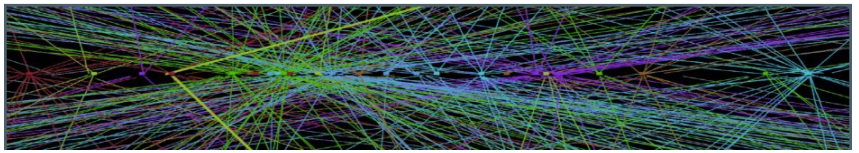
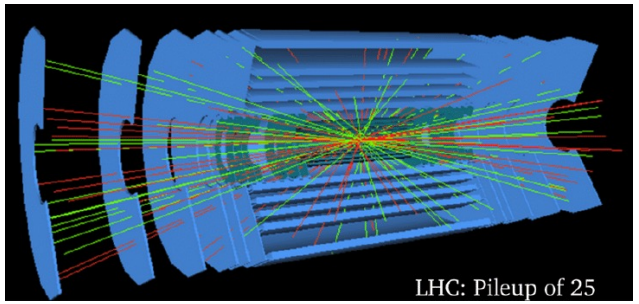
Challenges of HL-LHC

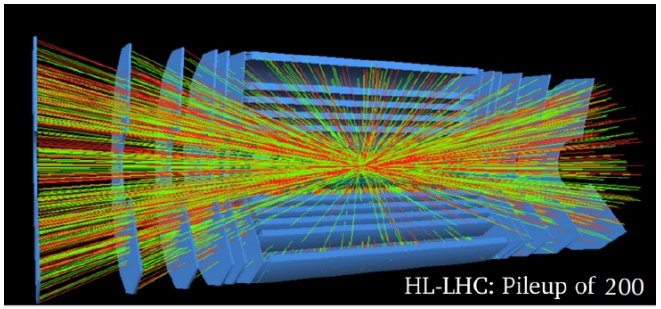
- In ~2029, LHC will run in **"high luminosity" , called HL-LHC**
  - The **instantaneous luminosity** will be a factor of ~5 – 7.5 higher than the LHC nominal values
  - 4000 fb^{-1}, collect ~**x10 more data than Run3** in the long term
  - *Pileup* of ~200 vertices per interaction
  - **Track reconstruction:** complexity increases **exponentially or worse with pileup**

On average 1.6-2.35 vertices per mm



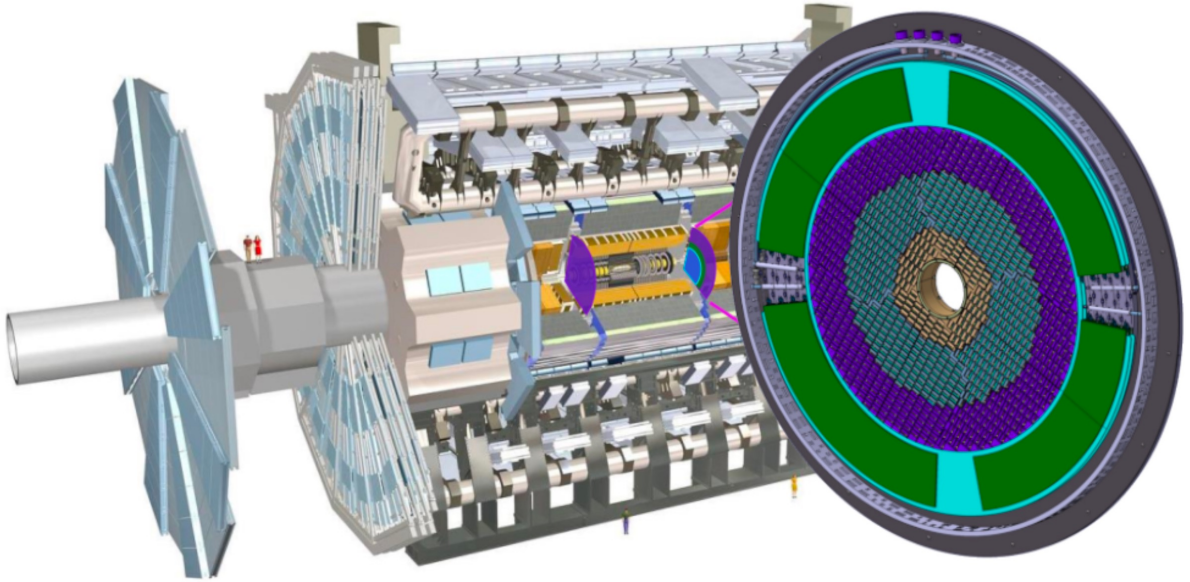


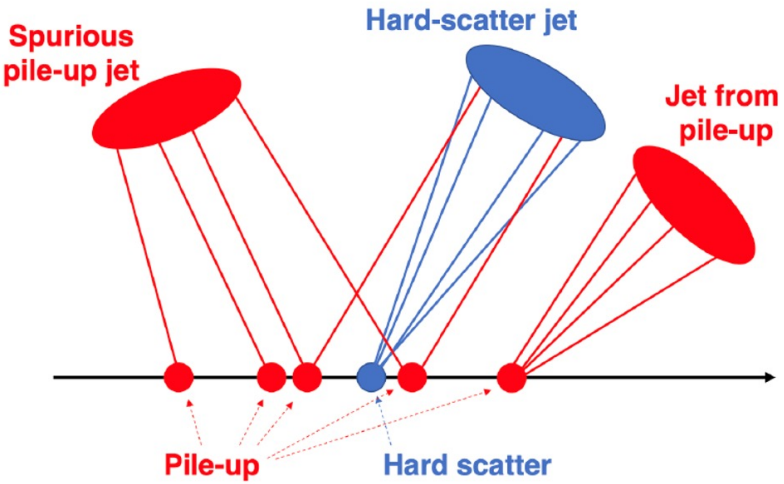
Pileup increases



High Granularity Timing Detector (HGTD)

- **HGTD aim to reduce pileup contribution at HL-LHC**
  - **Timing resolution is required to be better than 30 ps (start) - 50 ps (end) ps per track**
- **6.4 m^2 area silicon detector and ~ 3.6 × 10^6 channels**
- **High Granularity: Pixel pad size: 1.3 mm × 1.3 mm**
- **Radiation hardness : 2.5x10^{15} N_{eq} /cm^2 and 2 MGy**



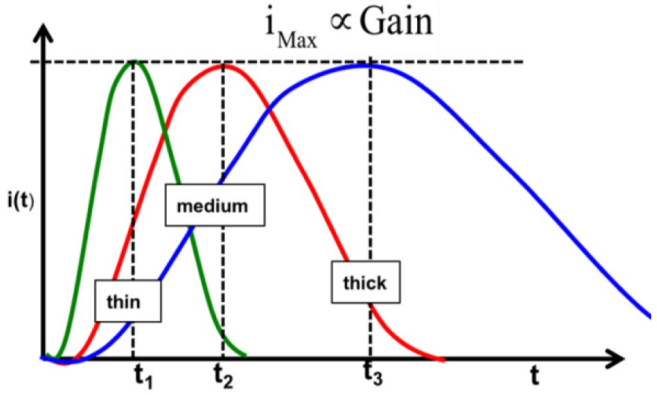


Low Gain Avalanche Detectors (LGAD)

- Compared to APD and SiPM, LGAD has modest gain (10-50)
- High drift velocity, thin active layer (fast timing)
- High S/N, no self-triggering

$$\sigma^2_{jitter} = \left(\frac{t_{rise}}{S/N}\right)^2$$

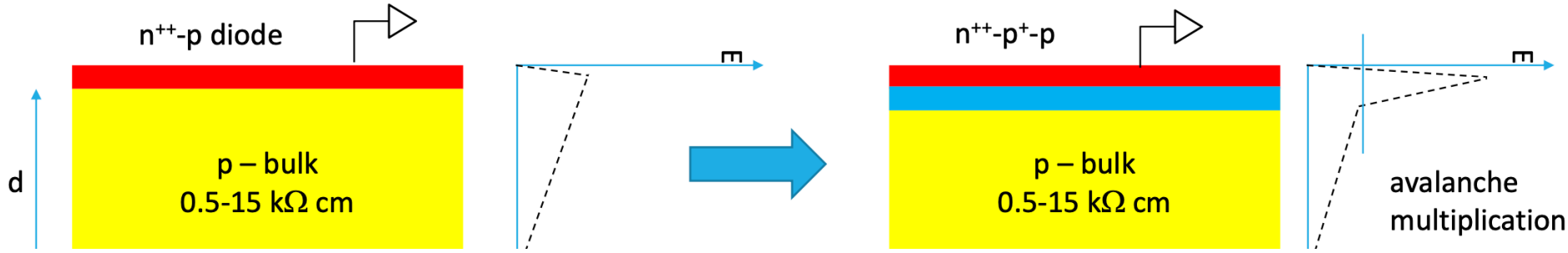
  - Modest gain to increase S/N
  - Need thin detector to decrease t_{rise}



LGAD

P+ gain layer on top of PIN diode

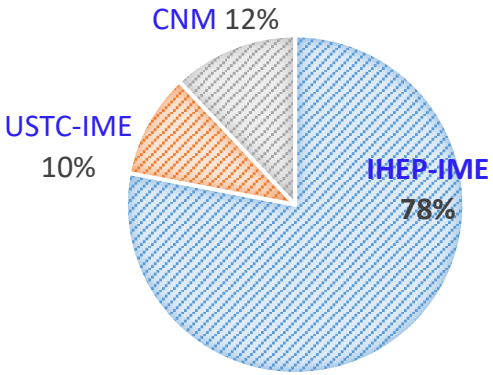
Conventional PiN diode

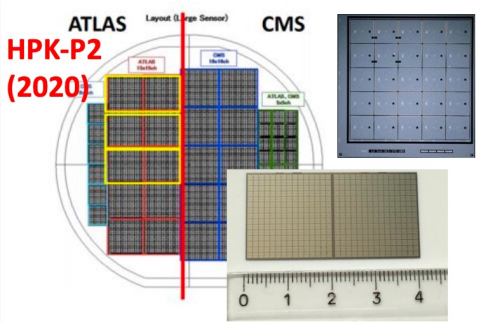


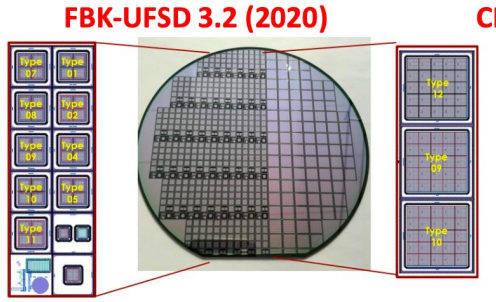
Latest prototypes produced by different vendors

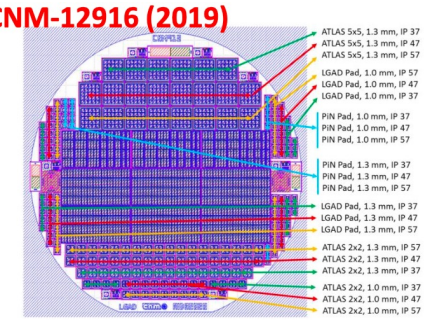
- Lots of prototypes R&D in LGAD in last few years, active vendors includes:
  - IHEP-IME (China), USTC-IME (China), IHEP-NDL(China), FBK (Italy), CNM (Spain), HPK (Japan) …
- HGTD just finalized the CERN tendering. The preliminary production plan:
  - IHEP-IME: 78% (54% from CERN tendering+24% in-kind contribution)
  - CNM: 12% in-kind contribution
  - USTC-IME: 10% in-kind contribution

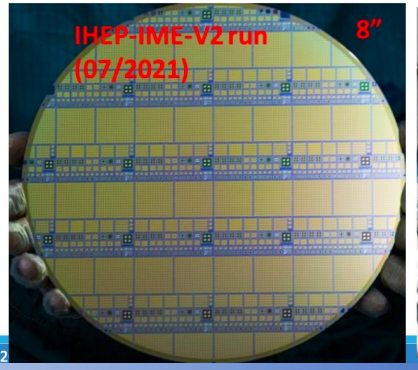
Share of production between vendors

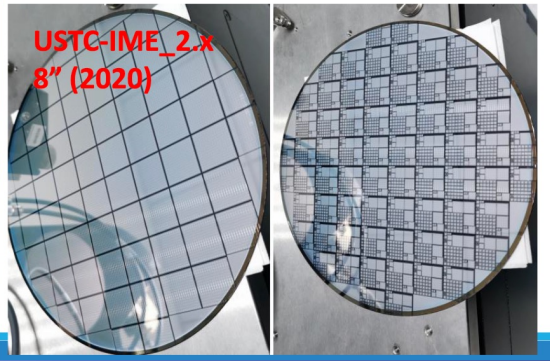


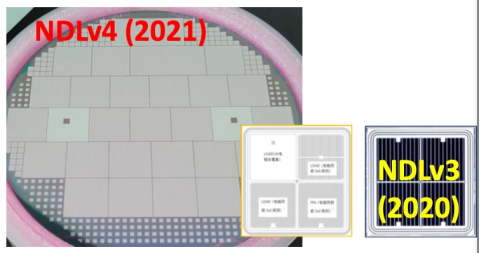








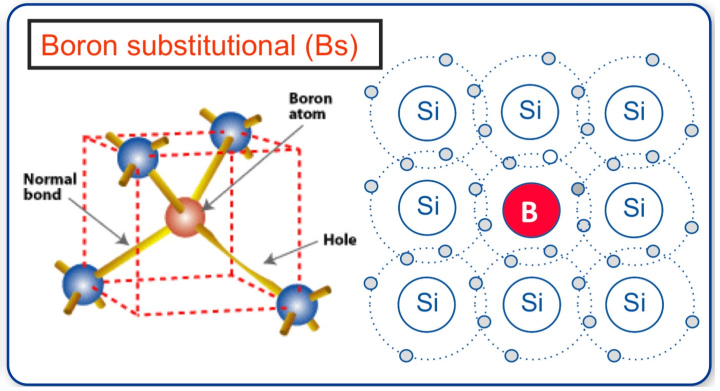




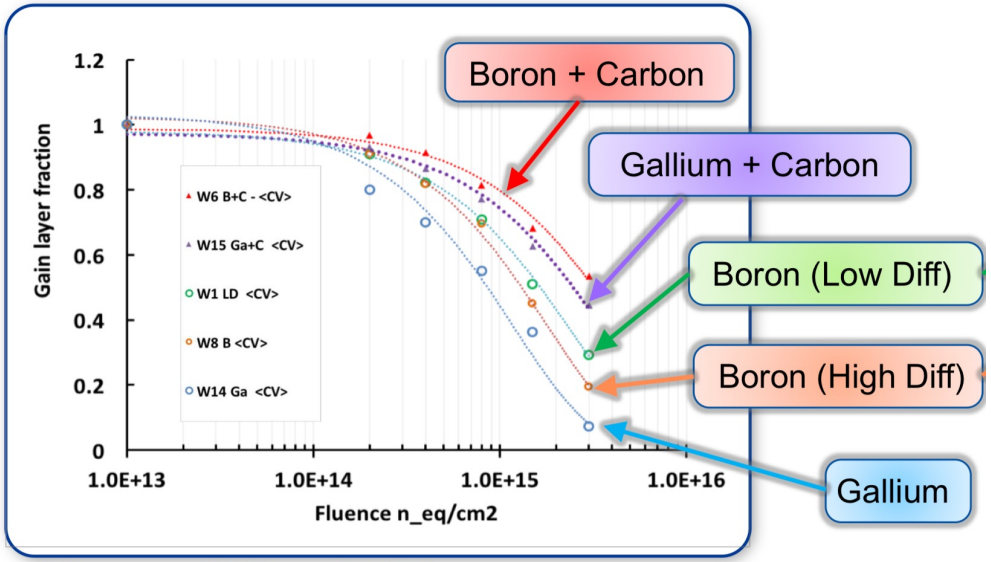
PLANAR TECHNOLOGY – more vendors (e2V, BNL, Micron …)

LGAD sensor after Irradiation

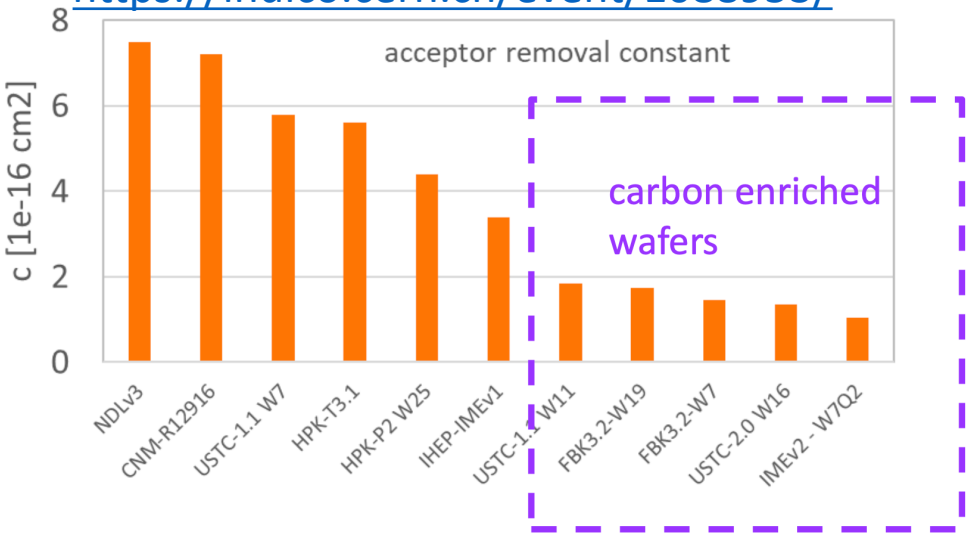
- After irradiation, Boron doping in gain layer became less active (Acceptor removal)
- Carbon-enriched LGAD is more radiation hard
  - Carbon "stabilized" boron doping
- IHEP-IME/FBK/USTC-IME LGAD with carbon
  - Significantly lower acceptor removal ratio
  - Significantly more radiation hard



See CERN Detector seminar
https://indico.cern.ch/event/1088953/



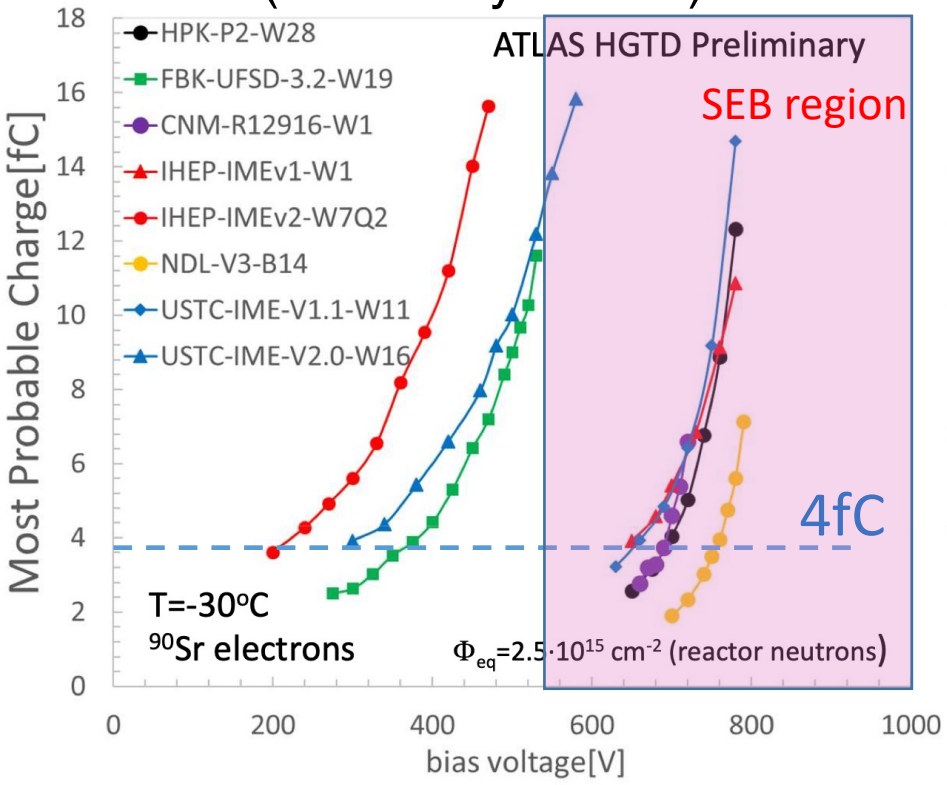
[G.Paternoster, FBK, Trento, Feb.2019]



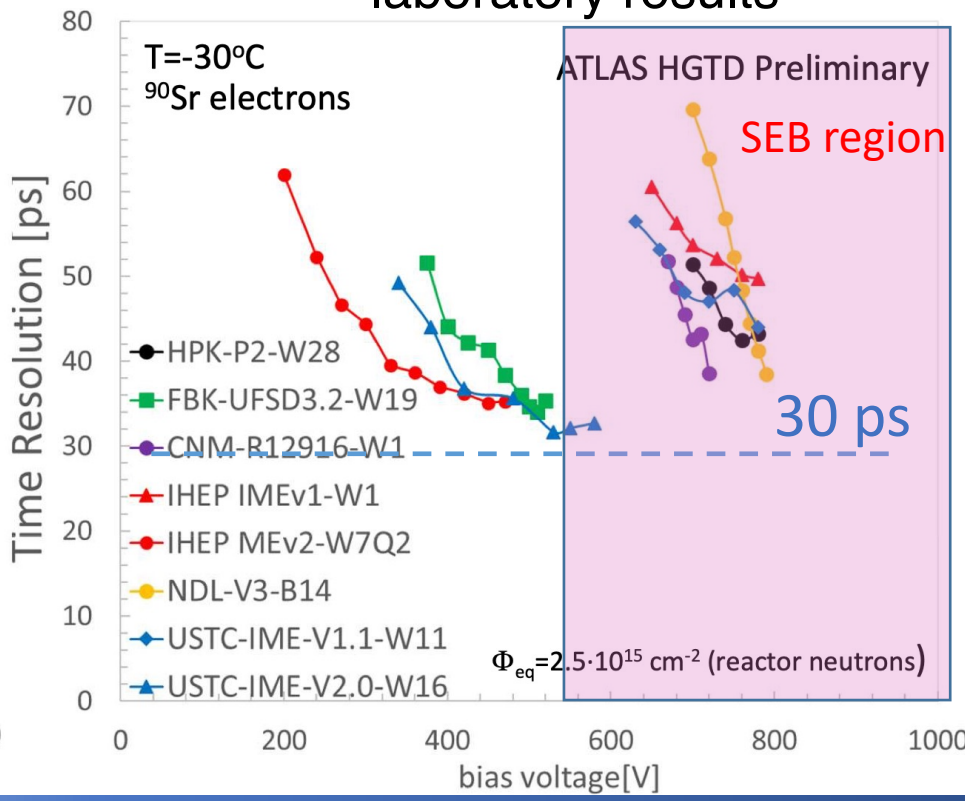
Performance of various LGAD prototypes at 2.5e15 cm^{-2} fluence

- Carbon enriched LGADs fulfil HGTD sensor requirements after irradiation
- Carbon-enrichment LGAD allows the sensors to be operated at low voltages
  - Single event break down (SEB) may happen if Operation Voltage >550V

Time resolution of LGADs Vs Bias Voltage
(laboratory results)

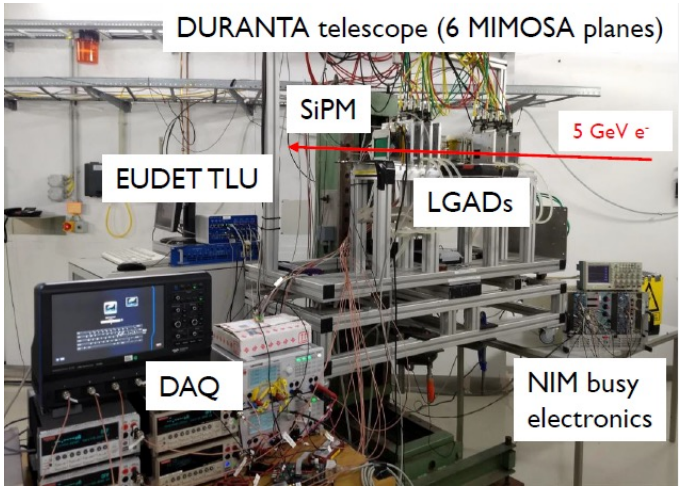


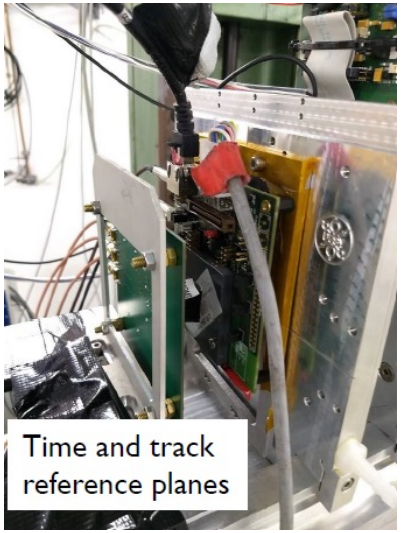
Charge collection Vs bias voltage
laboratory results

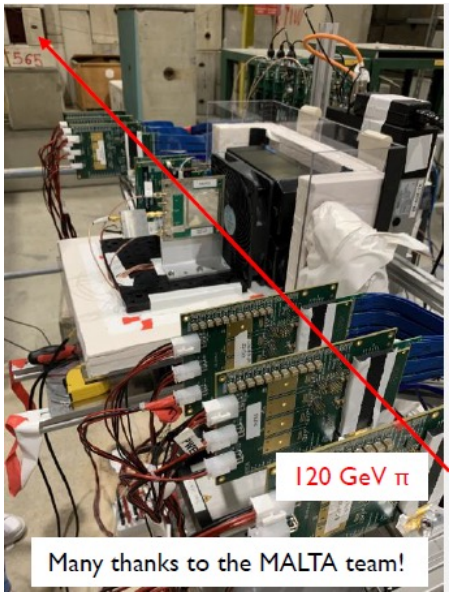


LGAD sensor Performance at test beam

- Test beam @DESY and @SPS in 2021 (setup)
  - CERN North Area SPS H6A beamline (120 GeV pion beam)
  - DESY T22 beamline (5 GeV e-beam)
  - Tracking Use of beam telescopes for tracking (EUDET-type 10 μm/MALTA 5μm)
  - Time reference： LGAD (CNM 0) used as a time reference in some tests (CERN SPS) as well as a SiPM device (DESY)



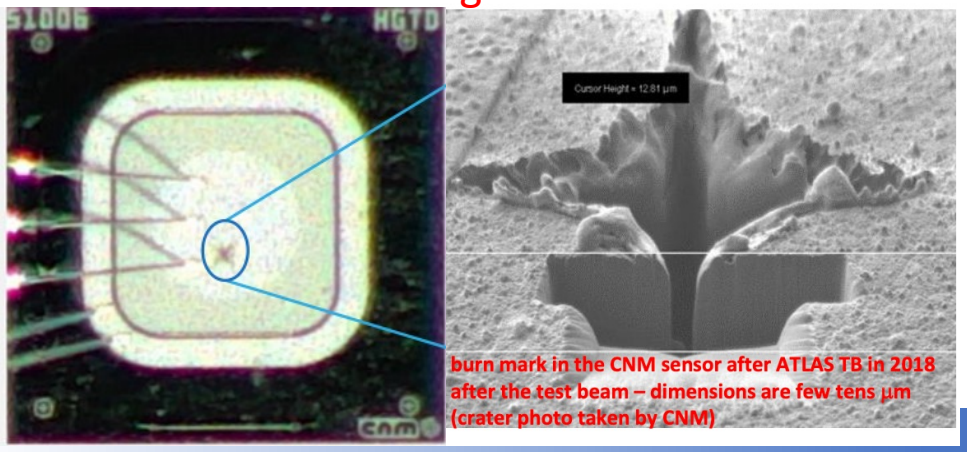




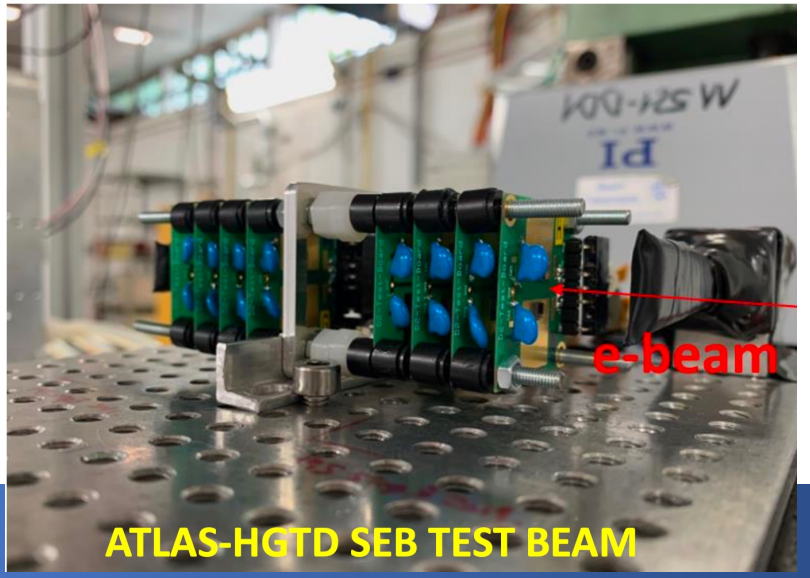
LGAD Single Event Burnout effect (HV stability in the beam)

- RD50, CMS and ATLAS confirmed Single Event Burnout (SEB) effect in testbeam
- The key to avoid burnout effect is to operate at low HV
  - Safe region: < 11 V/µm
  - Operate voltage needed to be <550 V (assuming 50 µm thick EPI layer)
- HGTD performed test beam at CERN and DESY
  - 120 GeV at CERN proton beam and 5GeV electron beam at DESY
  - Good performance for Carbon-enriched LGAD
  - Survived at Operation voltage

Burn mark of Single Event Burnout

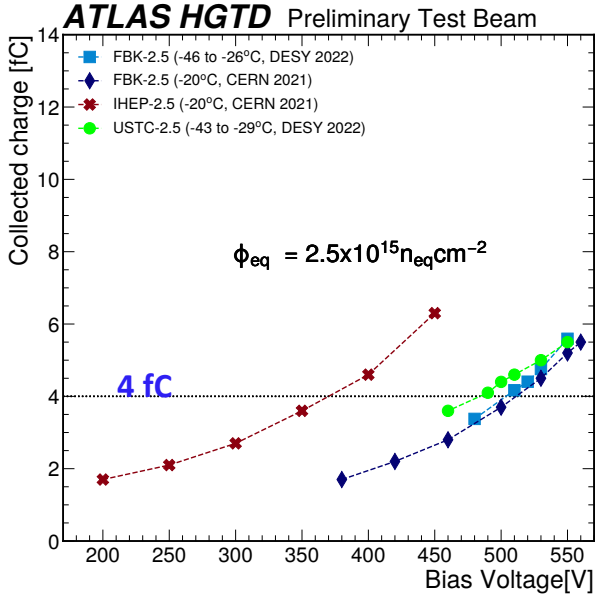


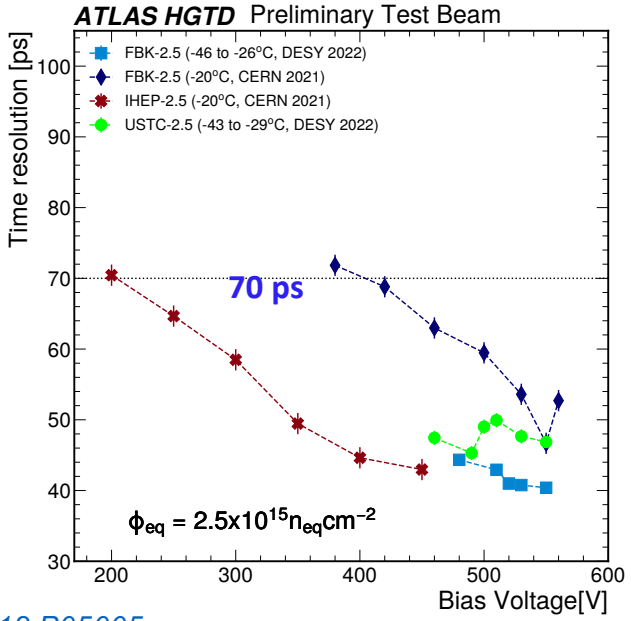
DESY test beam

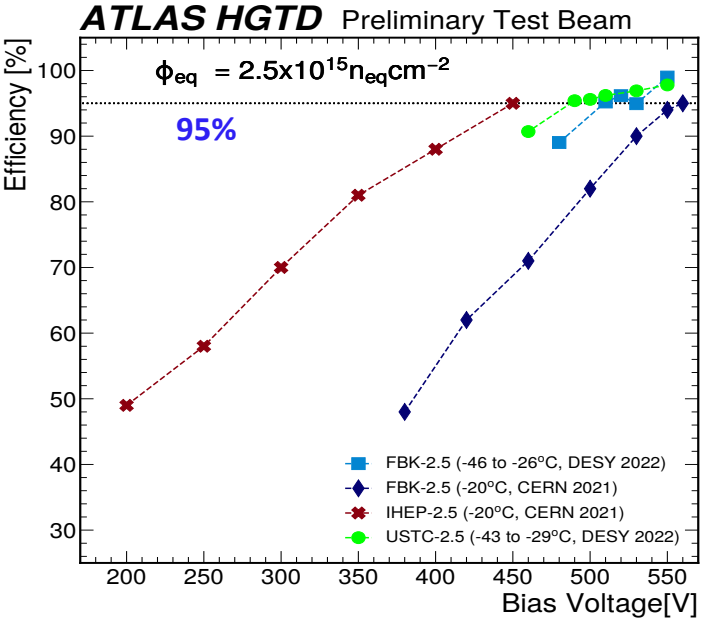


LGAD performance in the test beam

- After fluences of 2.5×10^{15} n_{eq}/cm^2, the LGADs were operated at voltages below 550 V
- Under these conditions, LGADs with shallow carbon achieved the objectives of:
  - Collected charge of more than 4 fC
  - while guaranteeing an optimum time resolution below 70 ps
  - An efficiency larger than 95% uniformly over sensors' surface is obtained
  - These results confirm the feasibility of an LGAD-based timing detector for HL-LHC



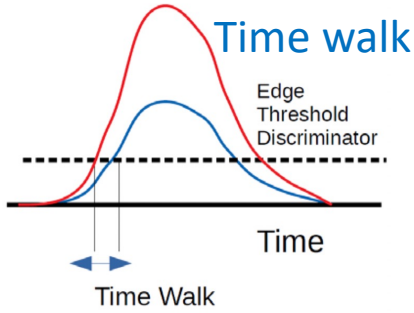




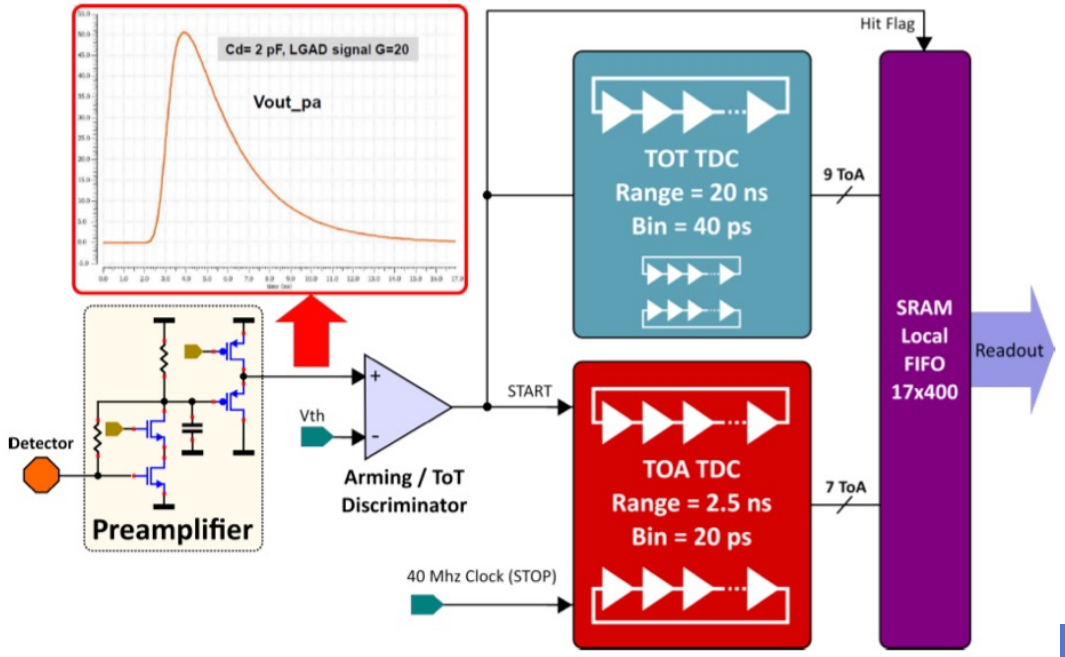
S. Ali et al 2023 JINST 18 P05005

ALTIROC : Fast Timing ASIC

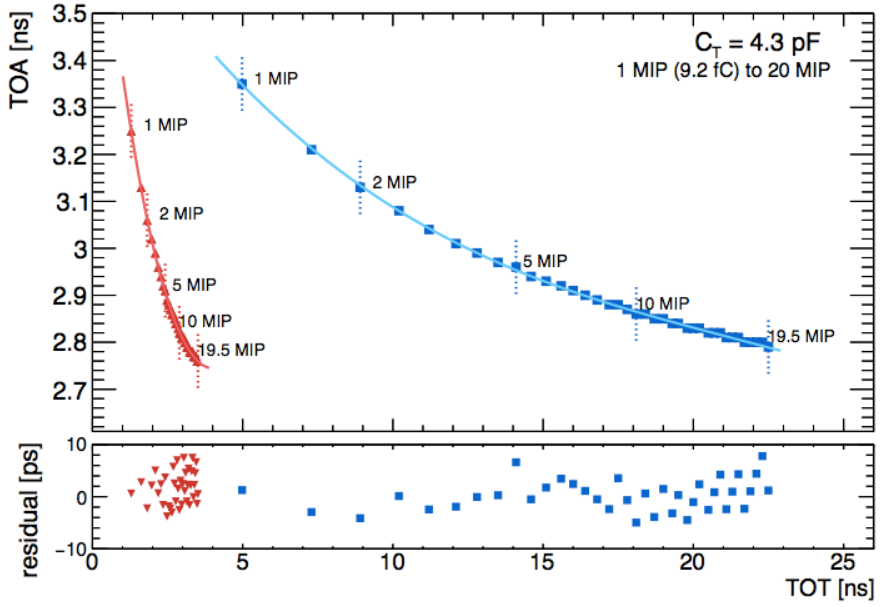
- 225 front-end channels in ALTIROC, each channel has
  - A preamplifier followed by a discriminator:
  - Two TDC (Time to Digital Converter) to provide digital **Hit data**
    - Time of Arrival (TOA) : Range of 2.5 ns and a bin of 20 ps (7 bits)
    - Time Over Threshold (TOT) : range of 20 ns and a bin of 40 ps (9 bits)
  - One Local memory: to store the 17 bits of the time measurement until L0/L1



ALTIROC timing ASIC in nutshell

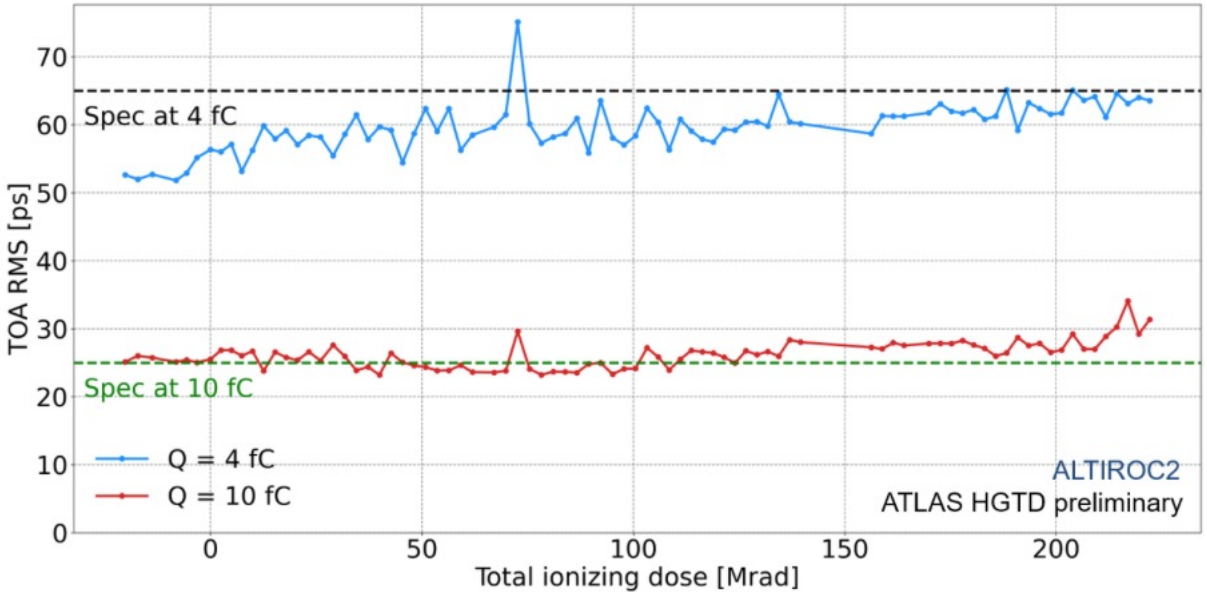


Time walk correction with TOT

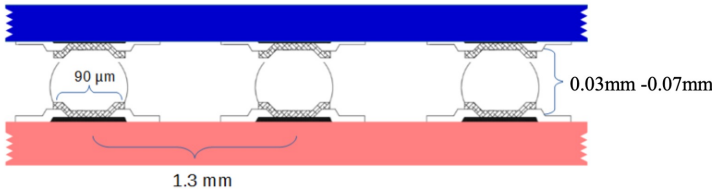


ALTIROC testing

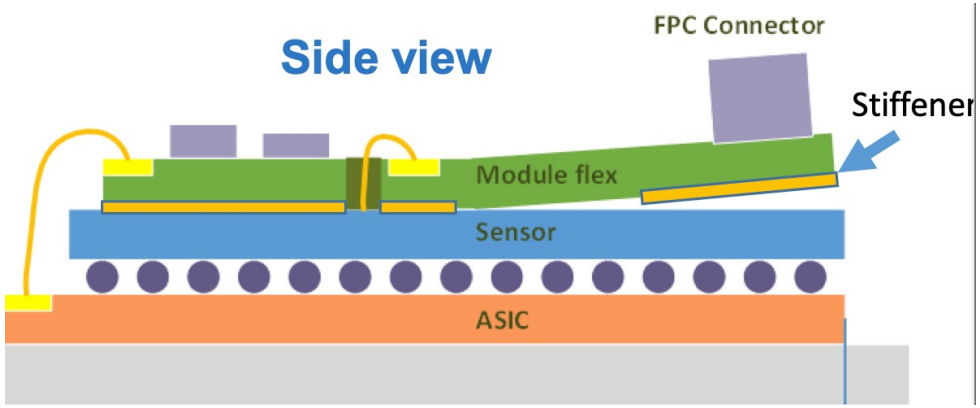
- Very demanding requirement of <70 ps time resolution @ 4 fC
  - LGAD collected charge >10 fC (>4 fC) before (after) irradiation
- Charge injection self-calibration test in ALTIROC
  - ~25 ps jitter @ 10fC
  - Better than 70 ps jitter@ 4 fC
  - Showing stability under radiation up to 220 Mrad total ionization dose

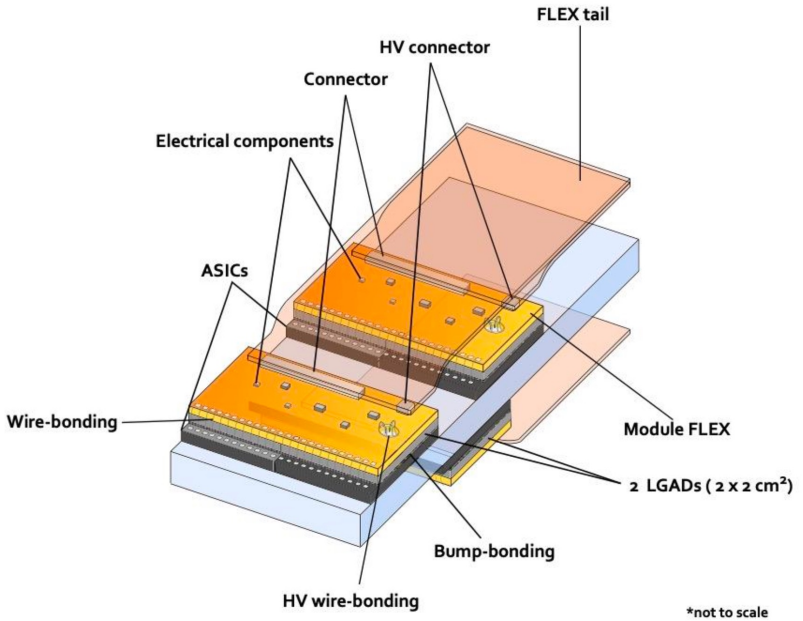


ALTIROC2 full-size hybrid

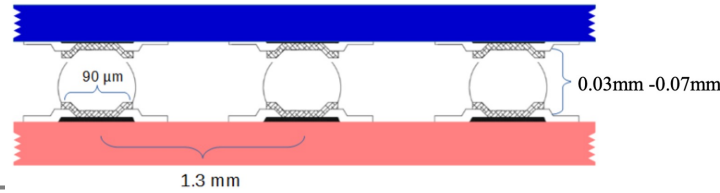


- HGTD has 8032 total modules, 3.6 M channels, 6.4 m^2
  - **A module consists of one module flex and two hybrids.**
    - There are six module production sites in HGTD project
  - **Hybrid: One LGAD sensor bump bonded to one readout ASIC (ALTIROC chip)**
    - **Low-Gain Avalanche sensors (LGAD) (15 × 15 pads of 1.3 x 1.3 mm^2)**
  - **One Flexible -PCB (module flex)** glued on top of two hybrids
  - Flexible tail connected module to outer radius electronics



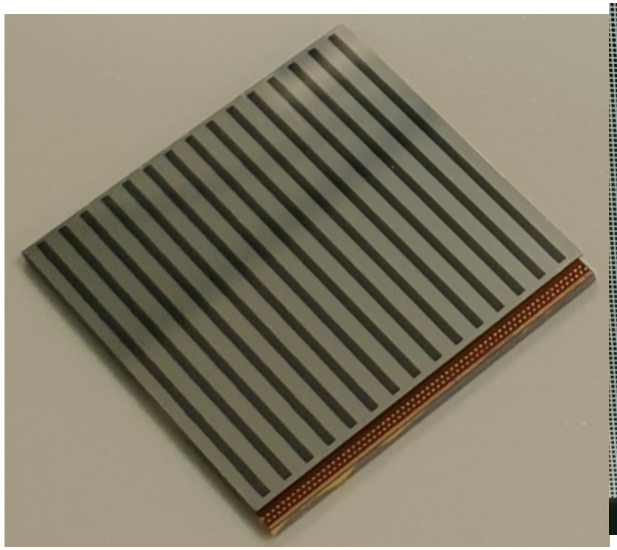


ALTIROC2 full-size hybrid

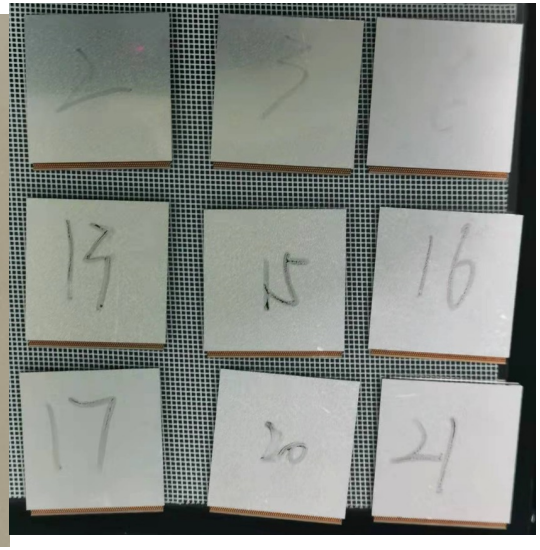


- Full Size ALTIROC2 full-size bare by different institutes and companies
  - IFAE already fabricated bare module prototype (ALTIROC2 + HPK LGAD, ALTIROC2 + FBK LGAD)
  - IHEP worked with NCAP company, made prototype with ALTIROC2 + IHEP-IME v2 LGAD
  - AEMtec (Germany) company made prototype with ALTIROC2 + FBK LGAD

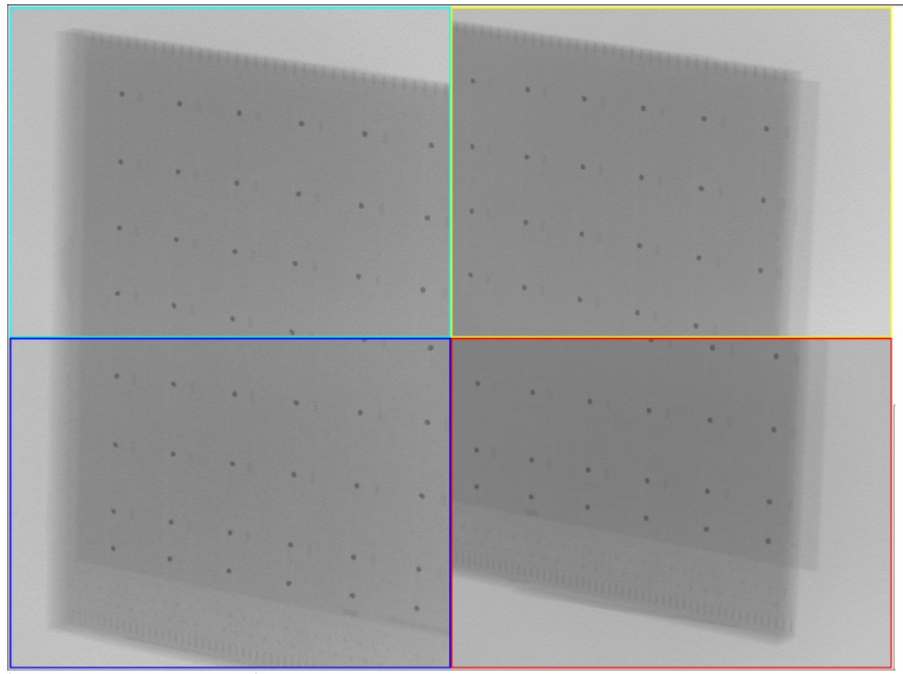
ALTIROC2 + HPK LGAD



ALTIROC2 + IHEP-IME LGAD

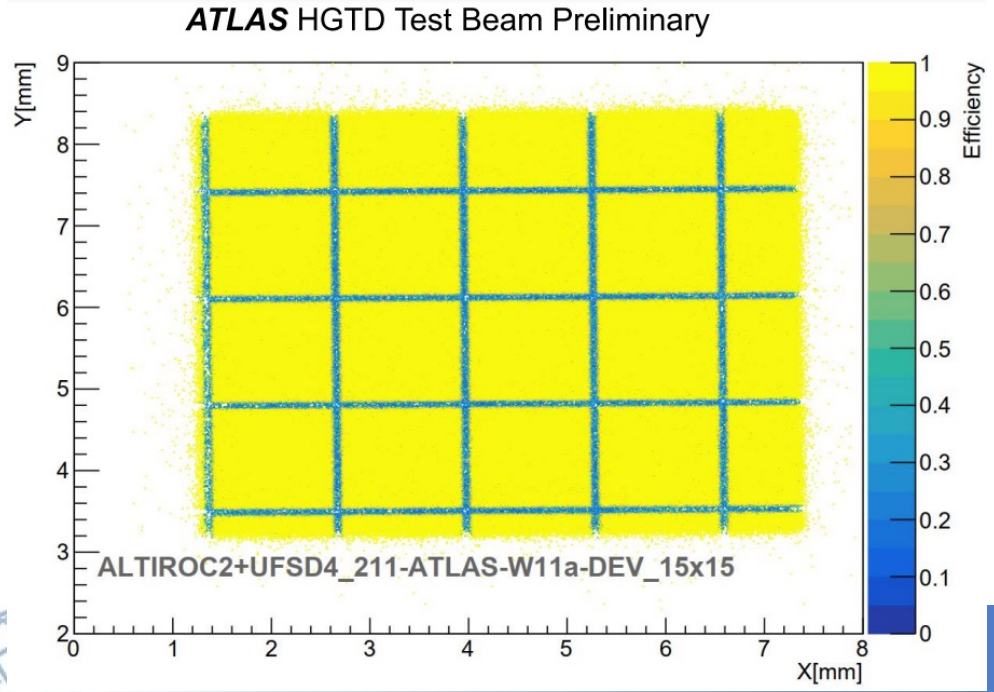


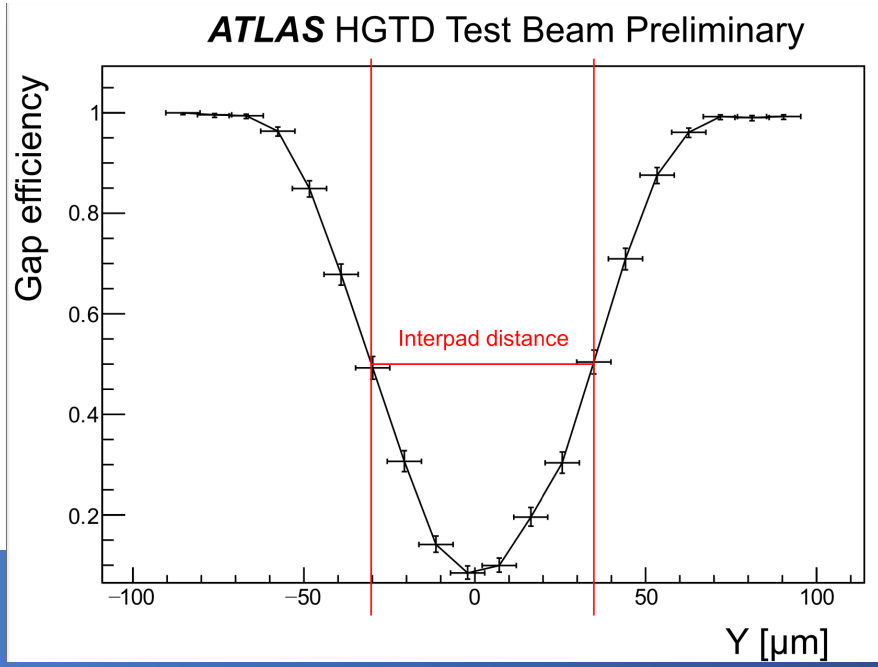
X-ray image of full-size hybrid



Hybrid test beam result

- Hybrid functionality was validated by test beam
  - The EUDET telescope is used for track reconstruction
  - Sensor bias voltage is -180 V, corresponding to a charge of ~20 fC
  - ASIC threshold 4.8 fC
- Close to 100% efficiency in the center of the pixel (pad)
  - The gap between pixels (pads) is about 50μm

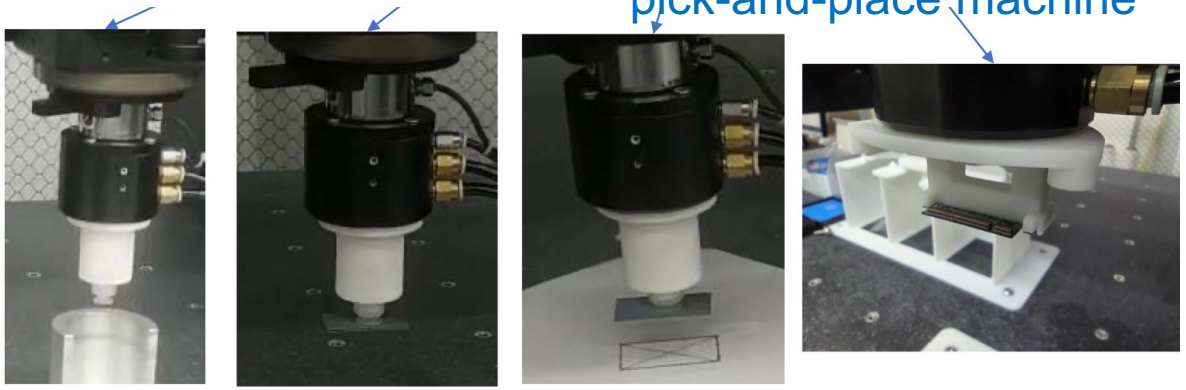




Module assembly

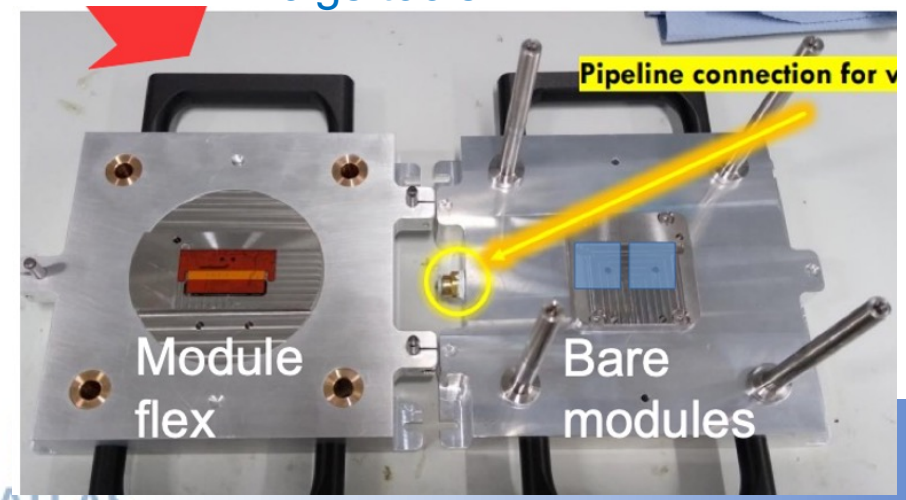
- Jigs tools and pick-and-place machine are in development

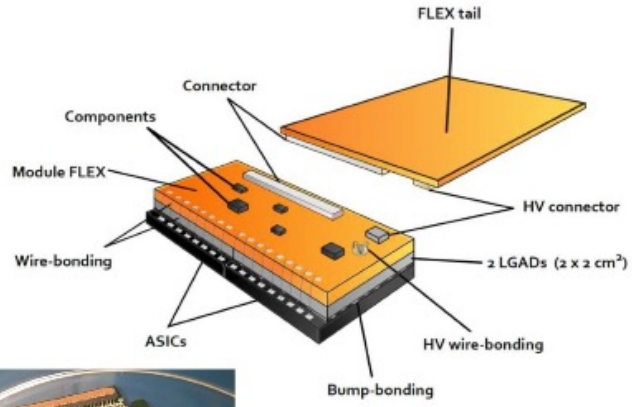
pick-and-place machine

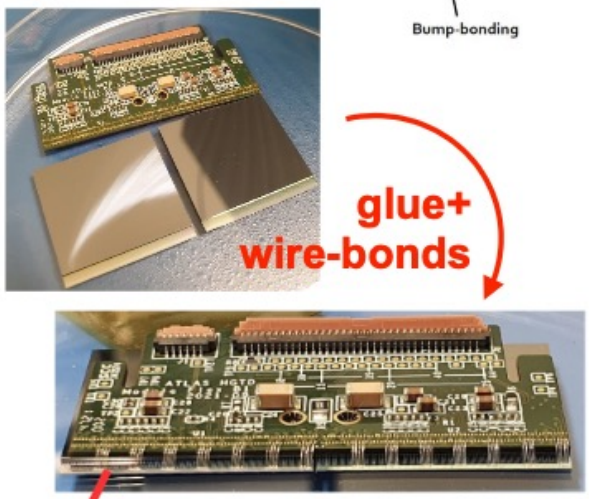


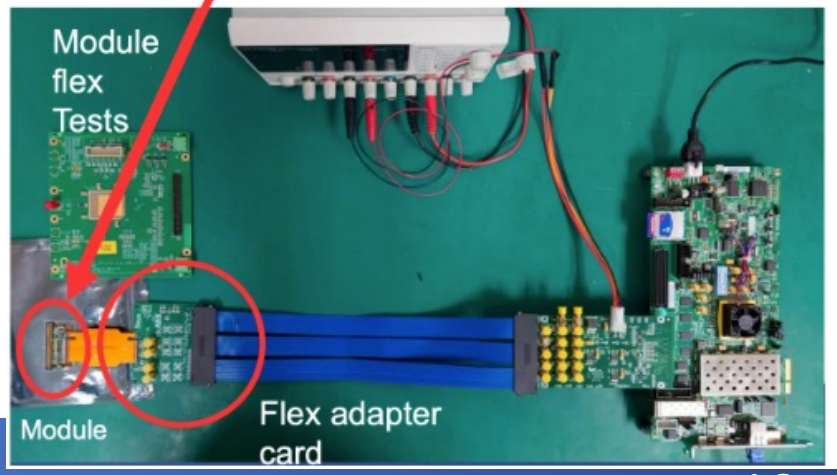
Picking tool | Picking dummy sensor | Placing dummy sensor | Picking flex

Jigs tools



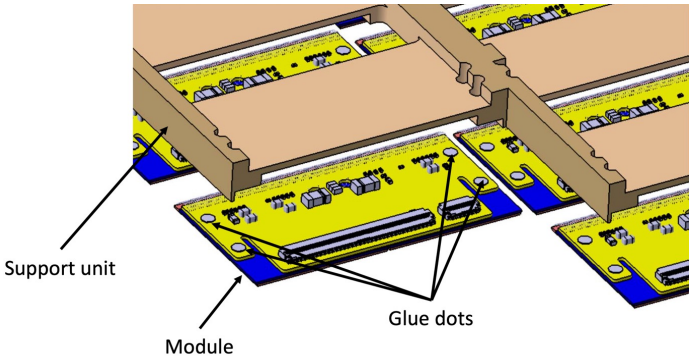




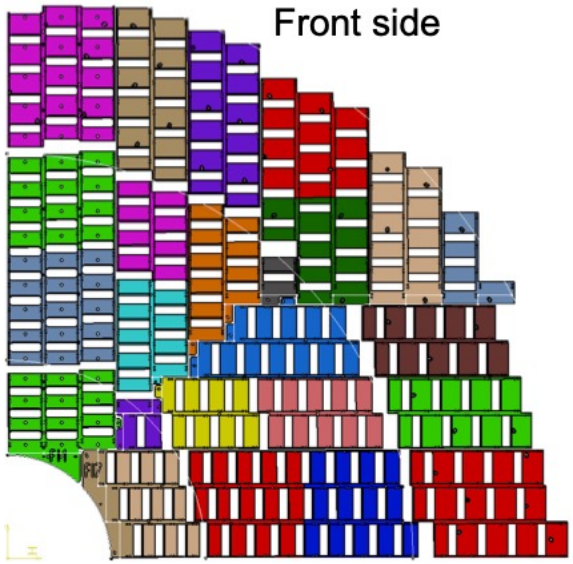


ALTIROC2 full-size hybrid

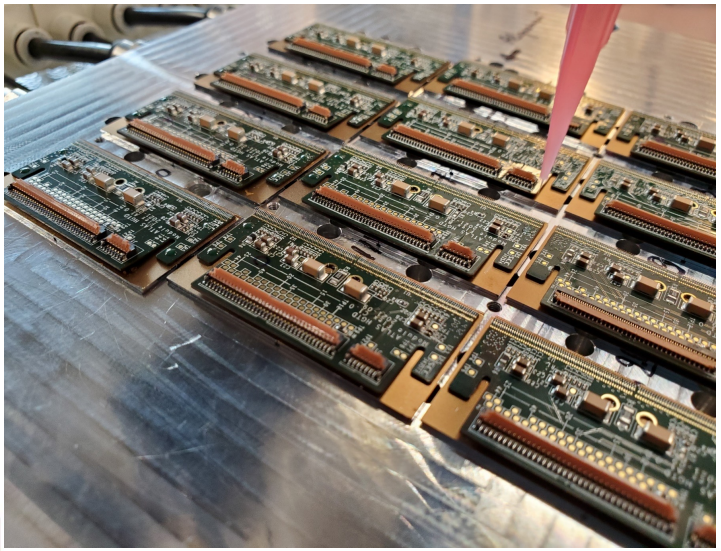
- Modules are installed and glued on support units
  - Challenges :machining of PEEK (flatness <200µm)



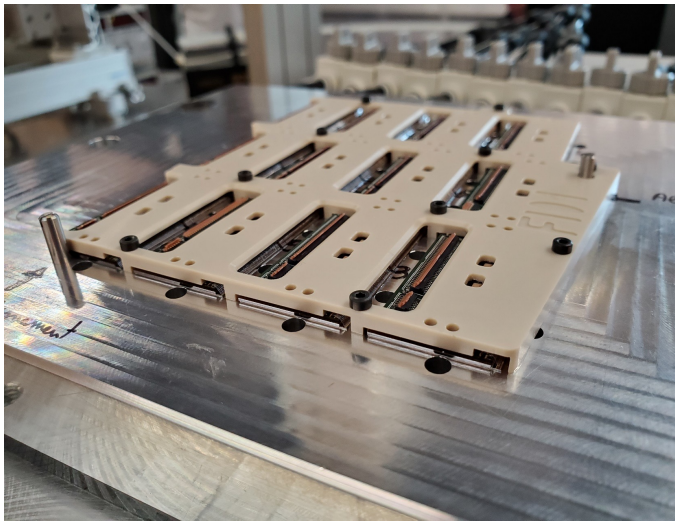
Different color represents different support units.



Gluing modules on support units



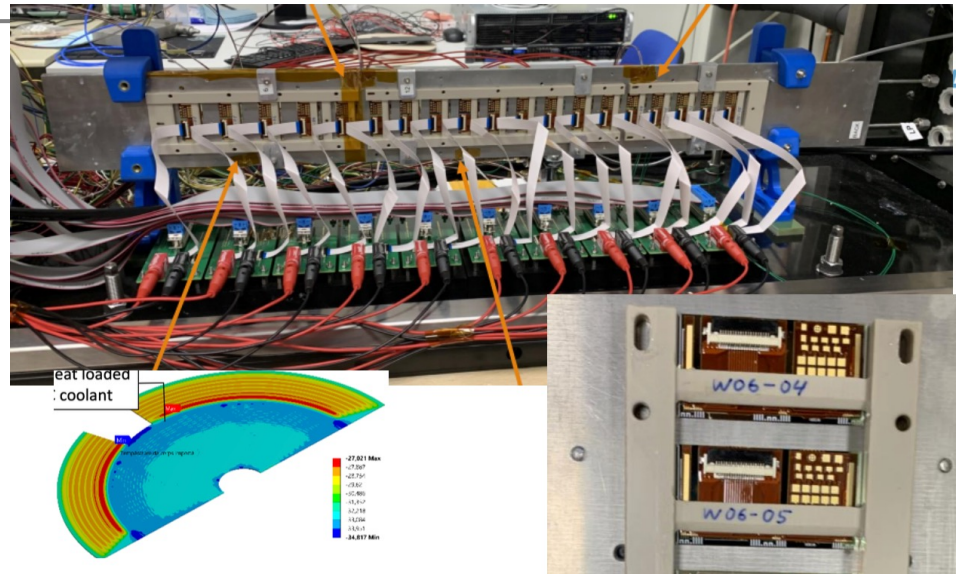
Loading modules on support unit



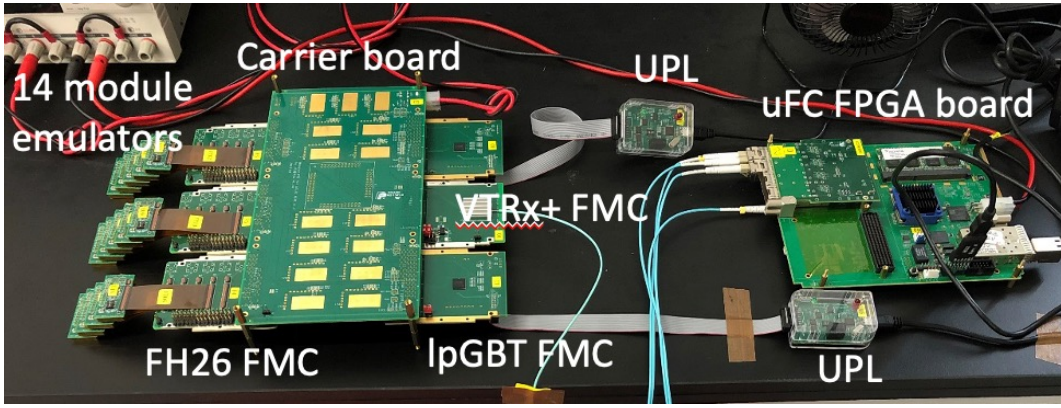
Demonstrator

- Heater demonstrator
  - 19 silicon heaters mounted on a single stave
  - Representing modules dissipating heat
  - on the cooling plate (CO2 cooling)
- DAQ demonstrator
  - Minimum system for full chain readout, from module emulator boards to FELIX board
  - Support up to 14 modules with two lpGBTs and one VTRx+
  - Timing
    - Up to 3 modules @ 1.28Gbps
    - Up to 7 modules @ 640Mbps
    - Up to 14 modules @ 320Mbps
  - Luminosity
    - 7 modules @ 640Mbps

Heater demonstrator



DAQ demonstrator

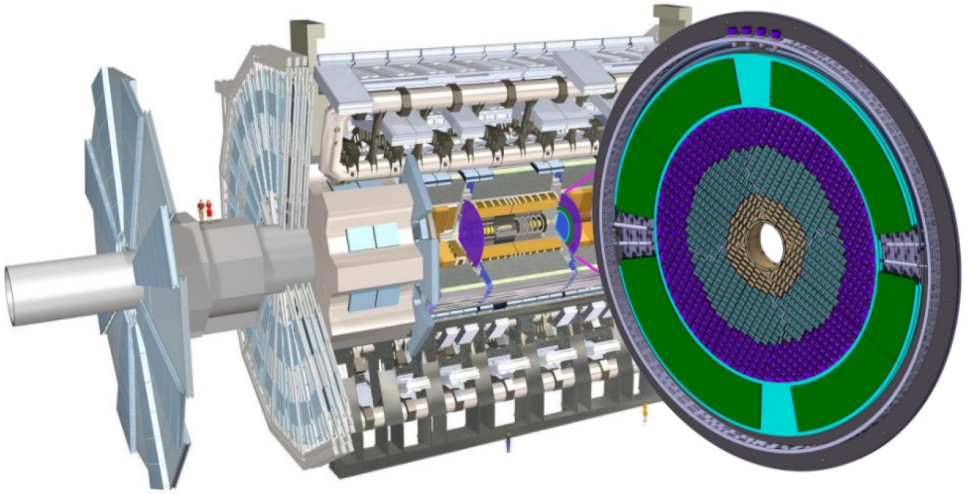


Summary: HGTD detector for ATLAS phase II upgrade

- Good progress in LGAD design fulfilling the radiation hardness requirements
  - Carbon enriched LGADs fulfil HGTD sensor requirements up to **2.5×10^{15} N_{eq} /cm^2**
  - Pre-production has started
- Two round of full-size ASICs have been prototyped, so far all blocks functional
- Concrete implementation of Peripheral electronics components are under test
- Full-size hybrids are in production and showed good results in functional tests
- Demonstrator activities ramping up
- Next milestones:
  - 2023: Peripheral electronics boards and LGAD sensors production started
  - 2024: ASICs, Modules and detector units production started
  - 2026-2027: HGTD detector Integration at CERN, installation

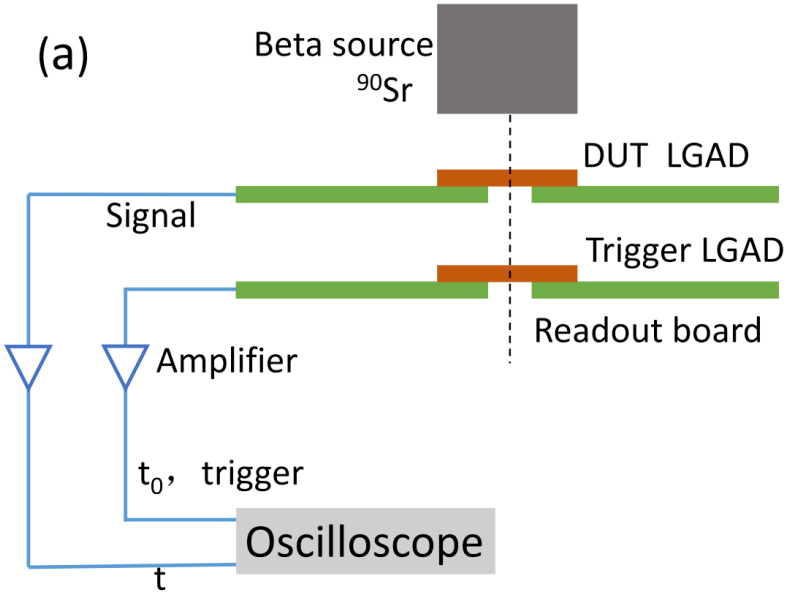
Backup: High Granularity Timing Detector (HGTD)

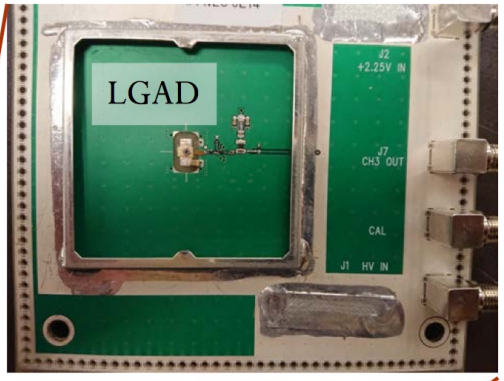
- High precision timing (per-track resolution of **35-50ps** up to 4000 fb-1) to mitigate pileup effects and improve the ATLAS performance in the forward region (**$2.4 \leq |\eta| < 4.0$**)
- Provide online and offline luminosity measurements by transmitting N_{Hits} per ASIC at 40MHz in outer region
  - 2 disks (one per endcap) outside of ITk volume, upstream of the fwd. calorimeters, consisting of **2 double-sided layers** each
  - Very limited space in z-direction ↠ overall thickness of 12.5 cm for each disk
- Silicon sensor technology (LGAD)
- Max expected fluence in "3-ring layout" is **2.5e15 neq/cm²** and sets the radiation hardness requirements for the sensors and electronics

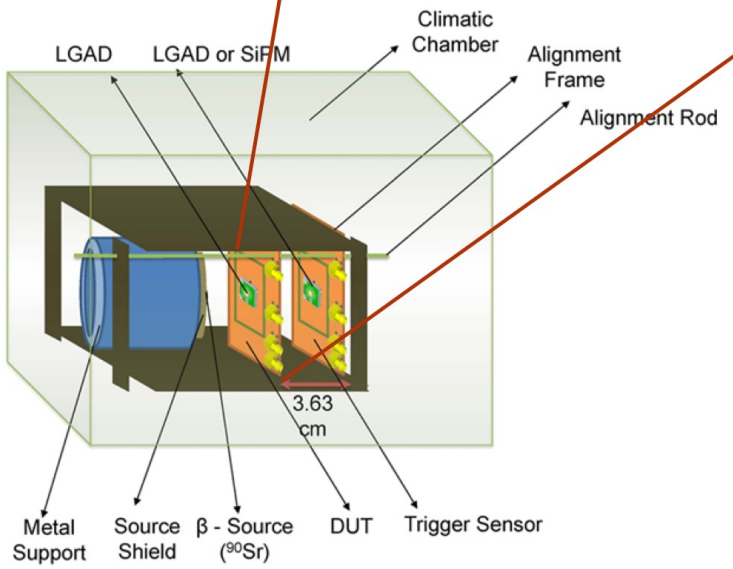


Beta source tests: LGAD timing resolution measurements

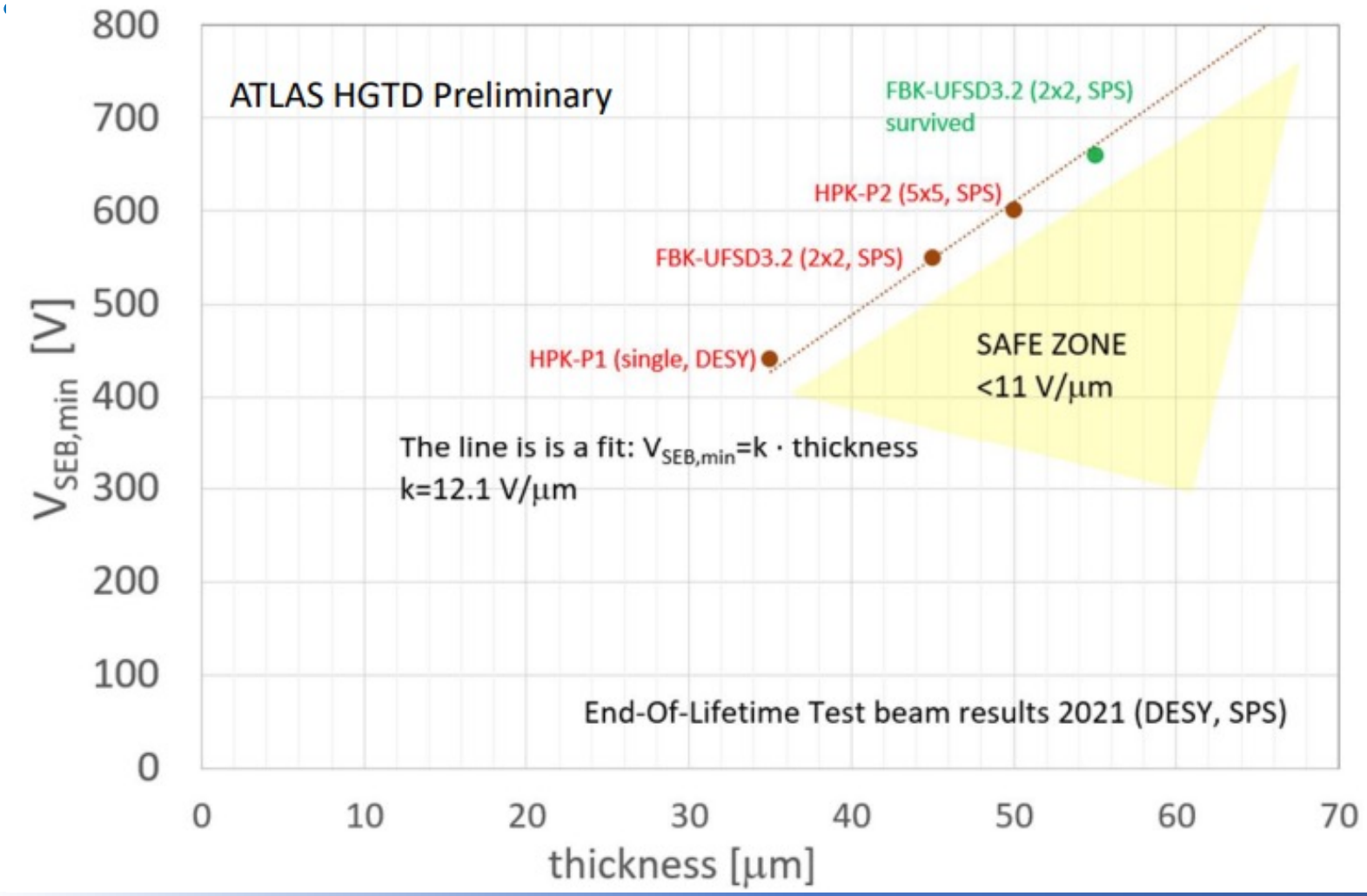
- Sr^{90} Beta telescope test (collected charge, gain, time resolution)
- UCSC boards with commercial amplifier and analog readout by Oscilloscope
  - Less constraints with respect to the ASICs – exploring the limits of the sensors.
- Two UCSC boards with two LGAD
  - One LGAD is device under test (DUT)
  - Another LGAD is used to trigger electrons events from Sr^{90}





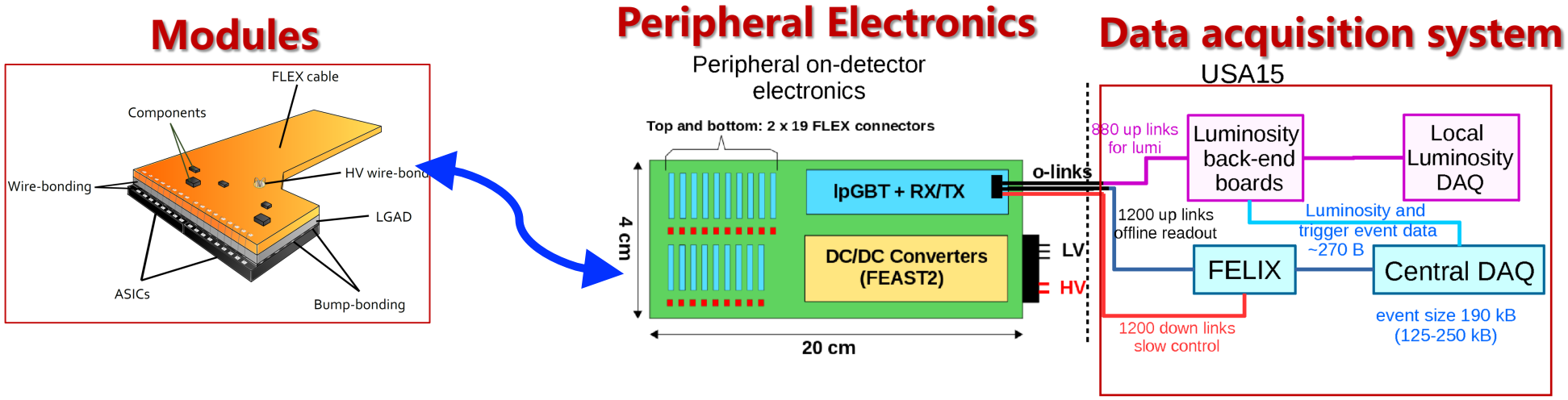


LGAD Single Event Burnout effect (HV stability in the beam)



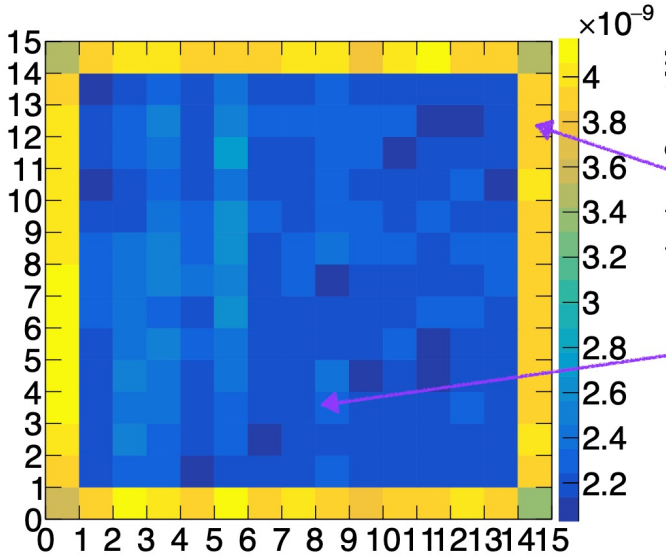
Peripheral board (PEB)

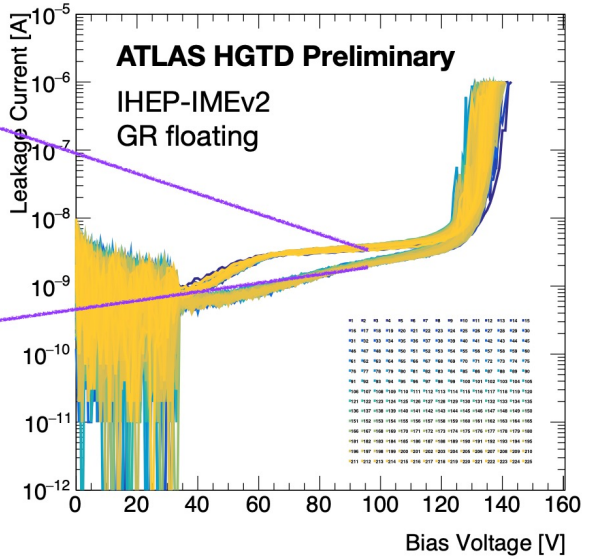
- PEB connects FE to the DAQ system, provides LV&HV to the modules

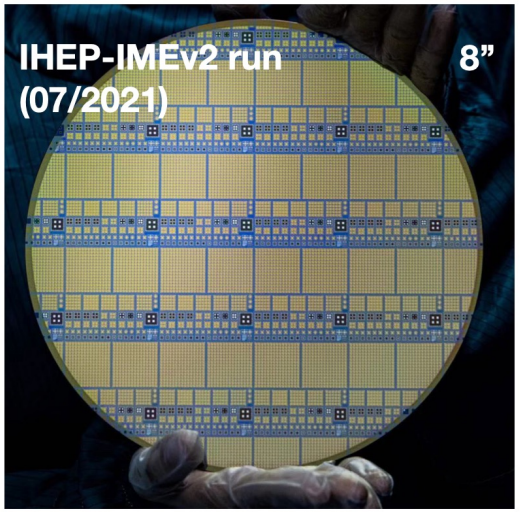


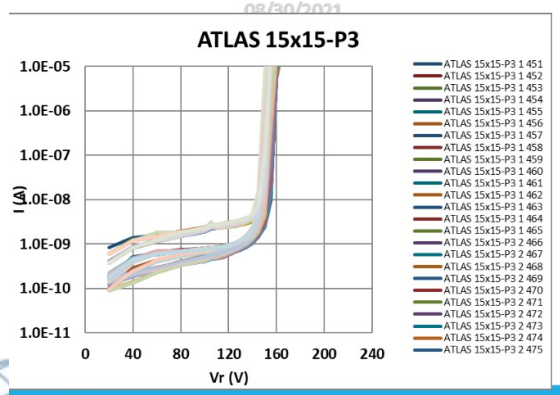
Full size LGAD sensor prototype

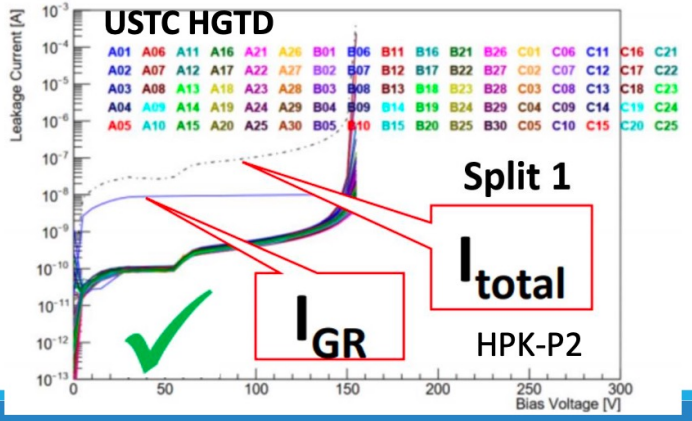
- Good uniformity of full size LGAD prototype (15*15 channels)
  - IHEP-IME, USTC-IME,HPK, FPK, CNM has produced good full-size LGAD prototype.

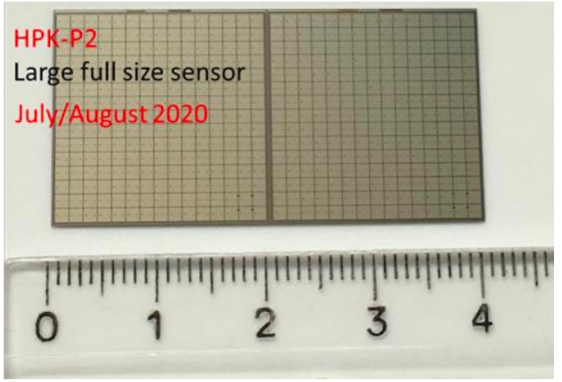










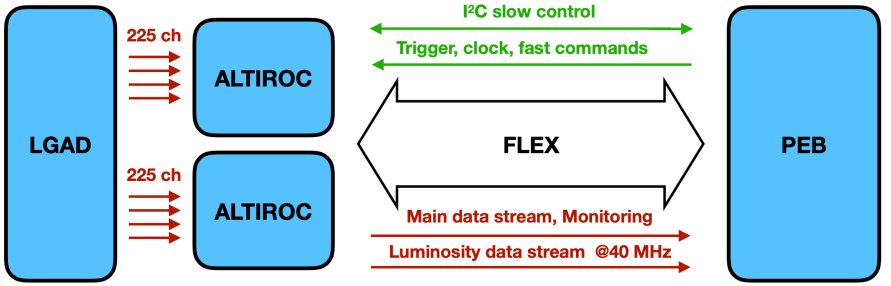


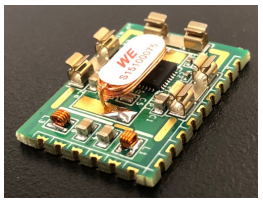
Peripheral electronics board (PEB)

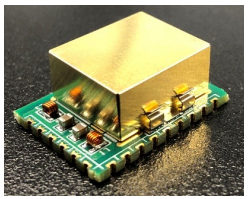
- Work on the characterization of all individual components, prototypes under production:
  - Detailed testing of the DC/DC converter (bPOL12V), different options under consideration

  ⇛ need to fulfil space constraints, power efficiency measured
  - Started tests on lpGBT with evaluation board
  - VTRX+: successfully tested 2.56G/10.24G communication, bit error rate ($<10^{-12}$), passed eye diagram test
  - MUX64: analogue multiplexer (for monitoring of ASIC power supply and temperature)

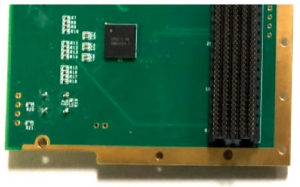
  ⇛ basic functionality confirmed, On-resistance larger than expected (further investigations necessary)



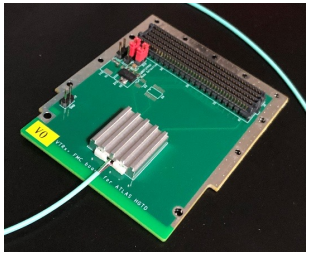




DC/DC converter



lpGBT eval. board



VTRx+ eval. board

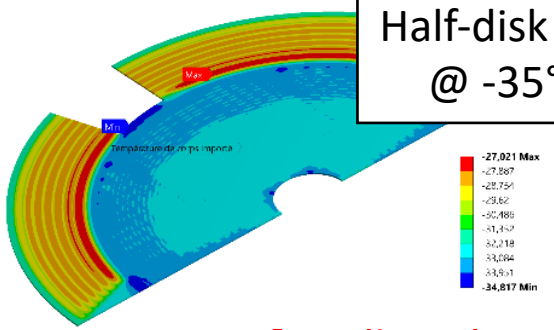
✓

MUX64 in QFN88

HGTD Mechanics and service

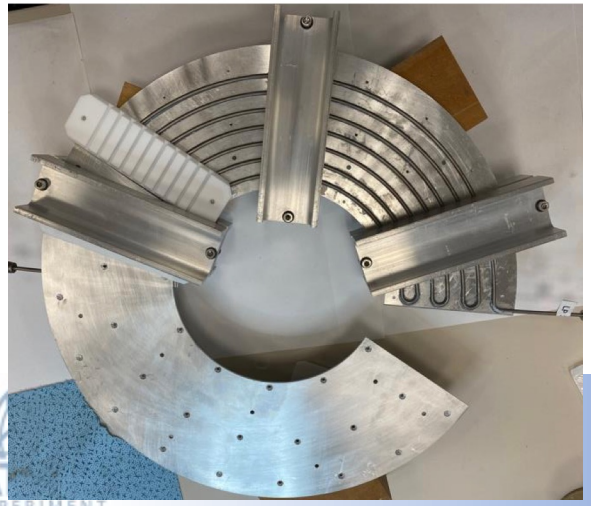
- Hermetic vessel and on-detector cooling passed SPR review
- Cooling plate with CO2 loops design and prototyping in good Progress
- Outer ring in progress: Challenging tight junction design with lots of feed-through

Thermal simulation of cooling system

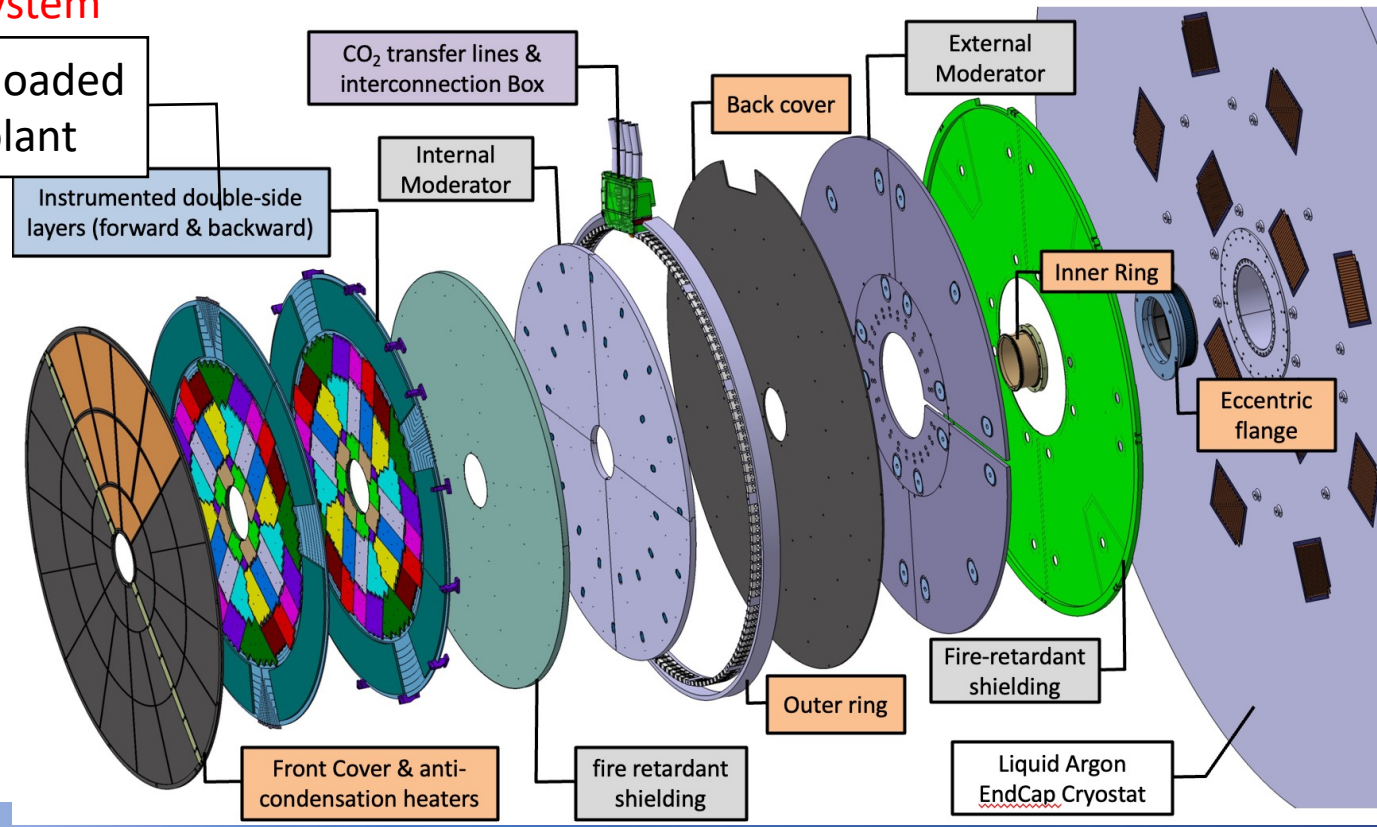


Half-disk heat loaded @ -35°C coolant

Prototype of cooling plate



Overall view with mechanics main items

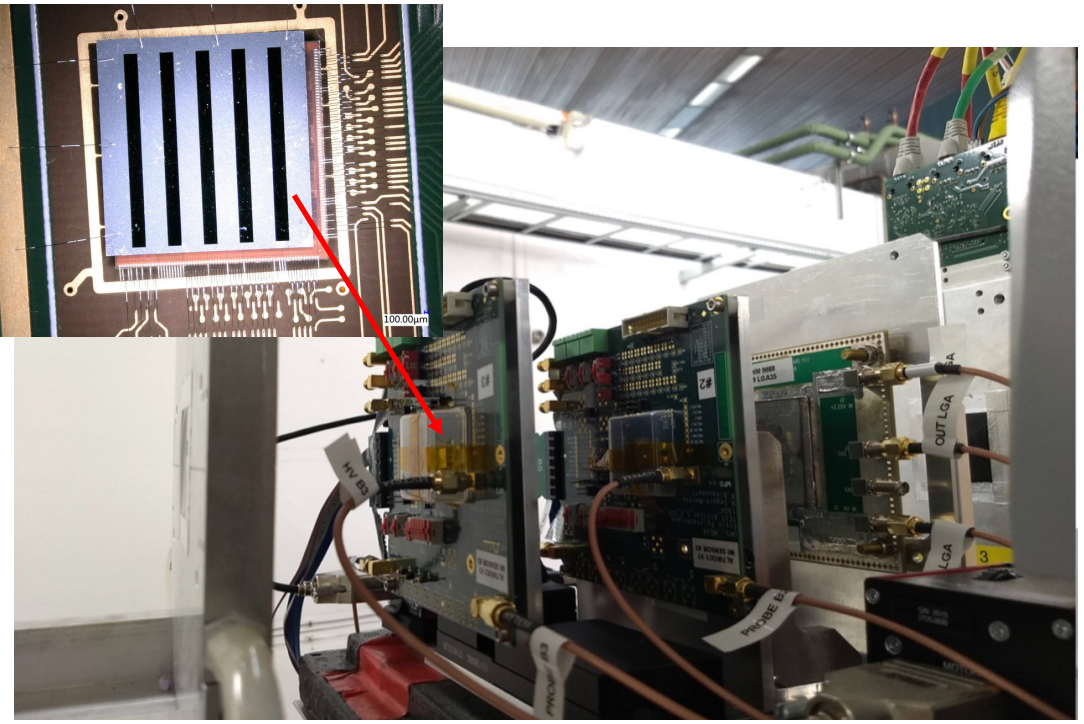


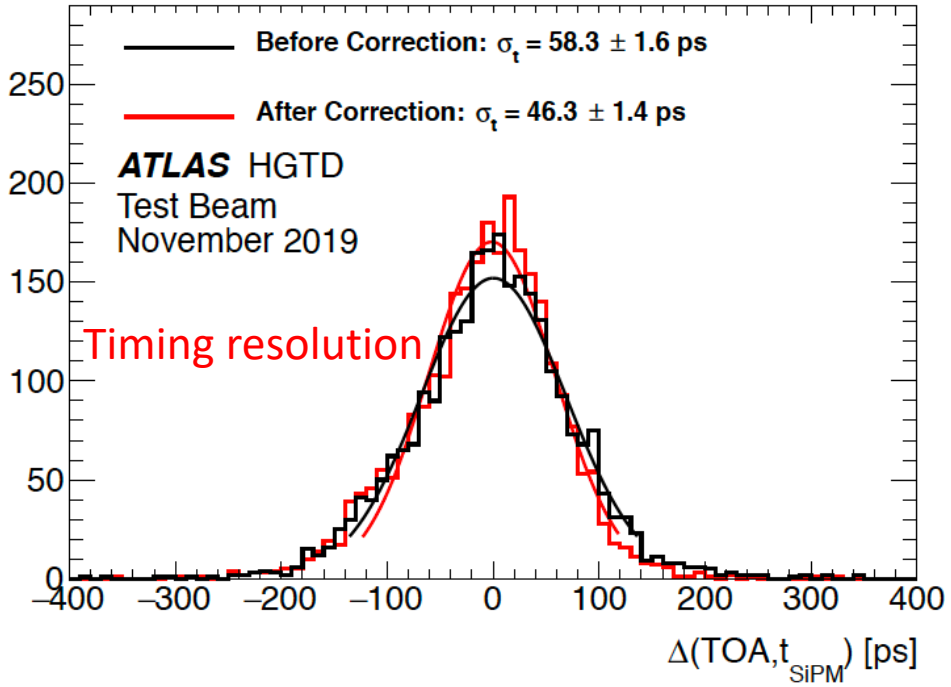
ALTIROC1 mini-modules performance at test beam

- 5*5 channels Mini-modules (ALTIROC1+LGAD) was tested at testbeam
  - 46ps timing resolution after time walk correction

LGAD Landau	25 ps	the reason for part of the high jitter found **26 (known reasons)**
Jitter+system/internal clock+time walk residual	37 ps	
TDC clock	7 ps	Total resolution: 36 ps (likely achievable for 20 fC)/ 70 ps for (4 fC)
Per hit total	46 ps	

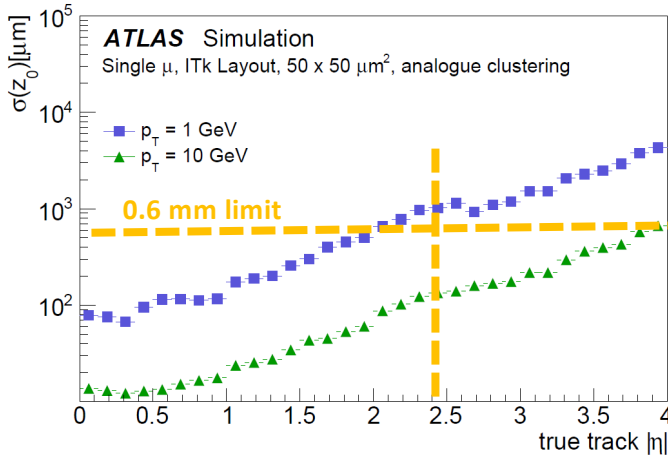
ALTIROC1 mini-modules @ test beam

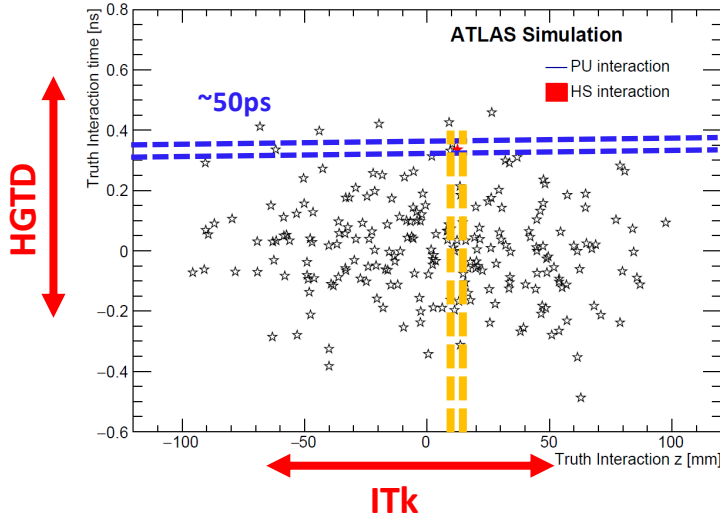




Why need the time information?

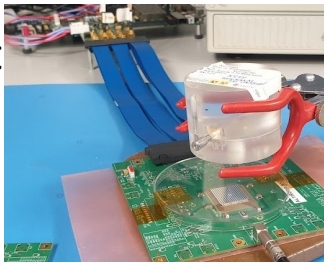
- At High Luminosity -LHC
  - Pileup: <μ>= 200 interactions per bunch crossing ~1.6 vertex/mm on average
- Problems of the vertex reconstruction in ATLAS
  - degradation significantly in the forward region compared to the central region
  - Need z_0 resolution < 0.6 mm
  - Liquid Argon based electromagnetic calorimeter has coarser granularity
  - New inner tracker (ITk) has poor z resolution in the forward region
- Using timing information easier to reconstruct vertices
- Timing information is necessary for the HL-LHC

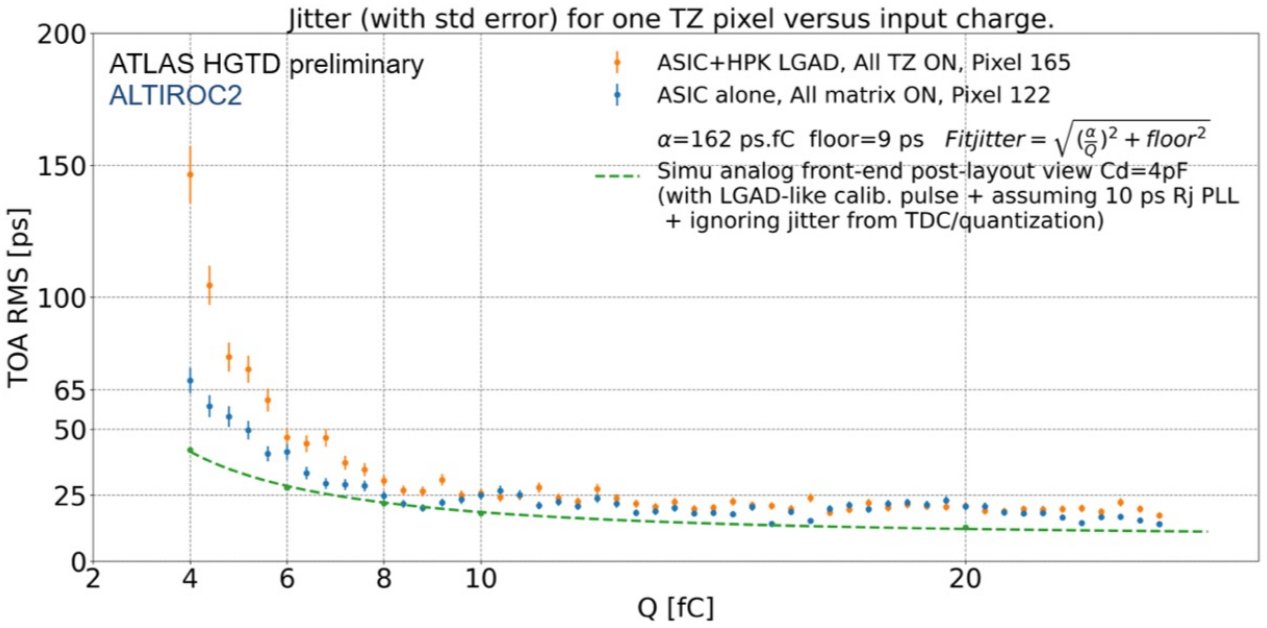


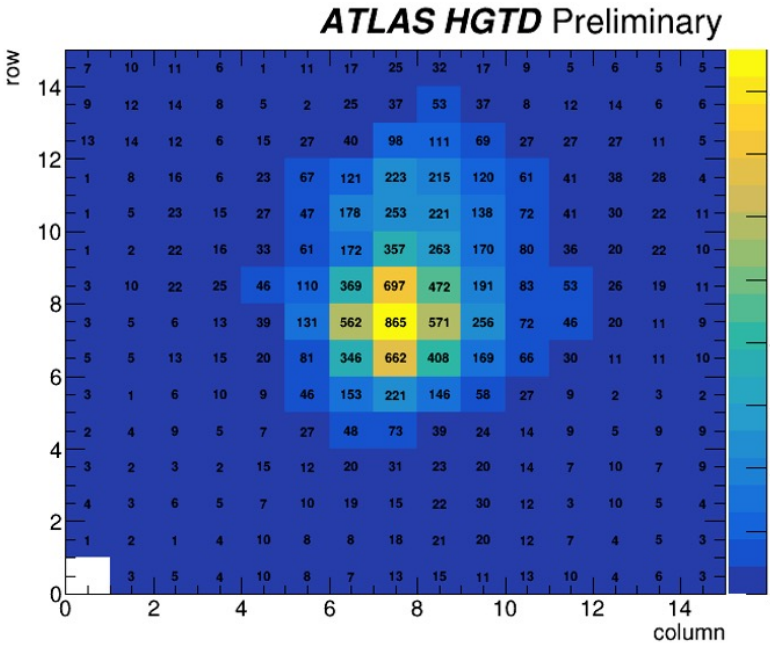


Hybrid tests

- Tests on-going of ALTIROC2 using dedicated PCB and interface board
  - ASIC-only and ASIC+LGAD tests after hybridization
  - Sr90 and testbeams performed with bare modules
  - Jitter as function of charge with ALTIROC2 ASIC alone and ASIC+LGAD with at least all TZ preamplifier channels enabled
  - Performance at low charge understood due to parasitic inductances separating sensor/ preamplifier grounds

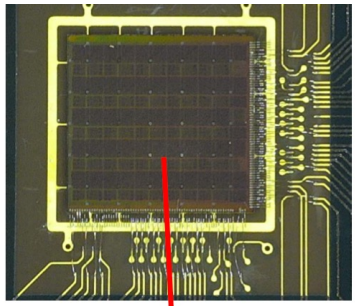


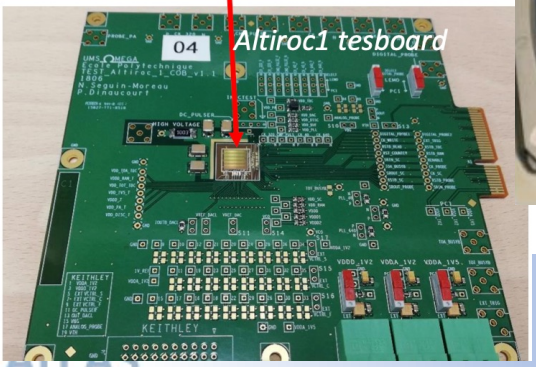




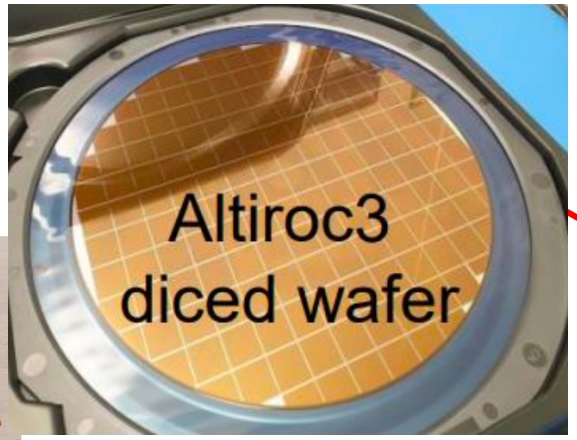
ALTIROC R & D

- ALTIROC0 – preamplifier + discriminator waveform sampling on the oscilloscope
- ALTROC1– 5x5 array with complete analogue front end (discriminator + TDC)
- ALTIROC2– 15x15 array with almost complete functionalities
  - First Full-size ASIC prototype ~2x2 cm^2 with 225 readout channels
- ALTIROC3- 15x15 array with complete functionalities
  - Digital-on top design, fix on TDC (TOT/TOA), radiation hard design





ALTIROC3 wafer



ALTIROC2 test bench setup