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Radiation hard true single-phase-clock logic for high-speed circuits in 28 nm CMOS

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Abstract: True Single-Phase-Clock (TSPC) dynamic logic is widely used in high-speed circuits such as high-speed SERDES (Serializer/Deserializer) and frequency dividers. TSPC flip-flops (FF) are known for their high operational speed and low power consumption, compared to static FFs. Due to the relatively high leakage currents in modern CMOS processes, the use of leakage protection techniques of the storage nodes in TSPC must be considered, especially at high radiation doses. In this paper, the limitations originating from Total Ionization Dose (TID)-induced subthreshold leakage currents are analysed and radiation-hardening-by-design (RHBD) circuit techniques are proposed. Additionally, Single Event Upsets (SEU) are investigated by quantifying the critical charge of the leakage protected TSPC FF. The results are compared to both the static and the TSPC FF without leakage mitigation.

Keywords: Digital electronic circuits; Radiation-hard electronics; Radiation calculations; Radiation damage to electronic components

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1 Introduction

The **D**emonstrator **A**SIC for **R**adiation-Tolerant **T**ransmitter in **28** nm (DART28) is an ASIC being developed in the context of the Experimental Physics research and development programme on technologies for future experiments at CERN [1]. Integrated circuits designed in this framework are implemented in a 28 nm CMOS technology and strive to improve radiation hardness up to TID levels of 1 Grad. The technology choice was motivated by the high-speed characteristics, high radiation robustness and low power consumption of the technology [2]. High-speed (multi-Gbps) data serializer circuits utilize dynamic True Single Phase Clock [3] flip-flops and latches, which inherently are characterized by fast operation, reduced area and lower power consumption when compared to static CMOS circuits [4]. Those benefits are expected from the dynamic circuit operation that stores information dynamically on node capacitance.

Although technology scaling offers many advantages, advanced CMOS processes suffer from relatively high leakage currents. Combined with small circuit node capacitances, excessive leakage current causes retention issues of the charge stored on dynamic nodes, thus corrupting the logic state. An example is shown in figure 1. This is an issue even at relatively high refreshing frequencies (multi-GHz values).

Prior research has shown that this subthreshold leakage current can significantly increase after irradiation to a Total Ionization Dose (TID) of 1000 Mrad, rendering the circuit even more prone to this problem. In order to improve the radiation robustness of a TSPC flip-flop, the use of leakage current protection is studied. Such circuit techniques have been investigated in a non-radiation context in [5]. To validate and compare the used architecture, a radiation and voltage dependent leakage current simulation model has been developed. The model was applied to the analysis of the FFs and latches implemented using three different circuit topologies: conventional TSPC,

TSPC with leakage protection and C^{2}MOS static architecture. The leakage current robustness and performance across TID are compared as well as the critical charge as an indicator of the SEU sensitivity.

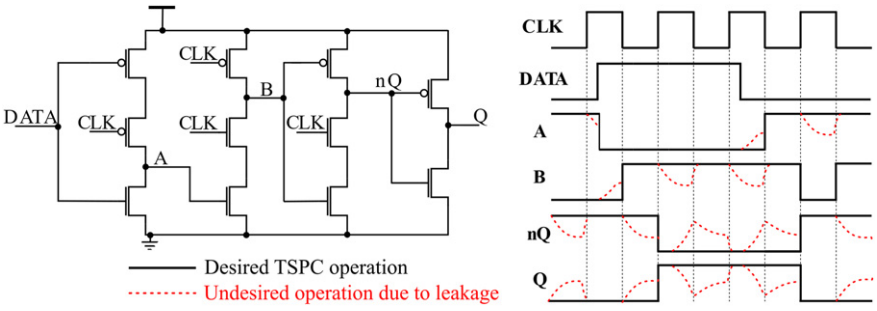

Figure 1. Schematic of the TSPC FF [4] with waveforms demonstrating the leakage problem.

2 Leakage current in 28 nm technology

The subthreshold leakage current is the dominant component of the transistor leakage (over gate oxide leakage) and it is properly modeled in the foundry transistor models. Even before irradiation, a strong temperature and corner dependency is present, with more than 2 orders of magnitude (100×) variation in the temperature range from 25 °C to 125 °C. However, the effects of radiation are not included in the foundry models. To address this shortcoming, we propose an extension of the foundry transistor models to account for TID-induced changes of the leakage current.

2.1 Modeling the TID-induced leakage current

The leakage simulation model has been developed based on the detailed characterization of the selected technology performed in [6–8]. It is shown that the TID-induced leakage current is caused by two main effects:

A **threshold voltage shift**, caused by the radiation-induced narrow channel effect (RINCE). The charge trapped in the lateral Shallow Trench Isolation (STI) oxide influences the electric field of the transistor channel, which reduces the threshold voltage (V_T) of the intrinsic channel [9, 10], thus increasing the off-state subthreshold current of the NMOS transistors. Due to lower V_T and the same I-V characteristic shape I_{DS} at $V_{GS} = 0$ V will increase.

Radiation-induced drain to source leakage is driven by enabling parasitic lateral devices. Charge built up in the STI oxide close to the channel will result in the creation of the conductive channels at the transistor edges, thus increasing the drain to source leakage current [9]. For the chosen technology this effect can be modelled using equation (2.1) [6]

$$I_{\text{Leakage}}(\text{Dose}) = I_{\text{pre-rad}}\left(\frac{\text{Dose}}{\text{TID}_{\text{crit}}}\right)^{k}, \tag{2.1}$$

where k is a length-dependent coefficient and TID_{crit} is the radiation dose at which the current from the parasitic devices is equal to the main channel leakage.

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Based on leakage I-V measurements from [2, 6, 8] a VerilogA model fitting the measured TID-induced leakage current was developed augmenting the foundry transistor models, as shown in figure 2(a). The characteristics were fitted with a polynomial to approximate $I_{\text{pre-rad}}$ for different V_{GS} values. The PMOS transistors have no radiation induced drain-source leakage current model because the oxide traps created by radiation in fact cause a leakage current decrease [10]. The threshold voltage shift (V_T-shift) model utilizes a look-up table based on measurement data of the V_T-shift for doses up to 1 Grad. For intermediate values of TID, a linear interpolation is performed to estimate the magnitude of V_T-shift. The proposed model was validated by comparing the simulation results with experimental data, that show less than 10% of error. An example for non-irradiated and irradiated NMOS transistors is shown in figure 2(b), showing a good agreement with the results showed in [6].

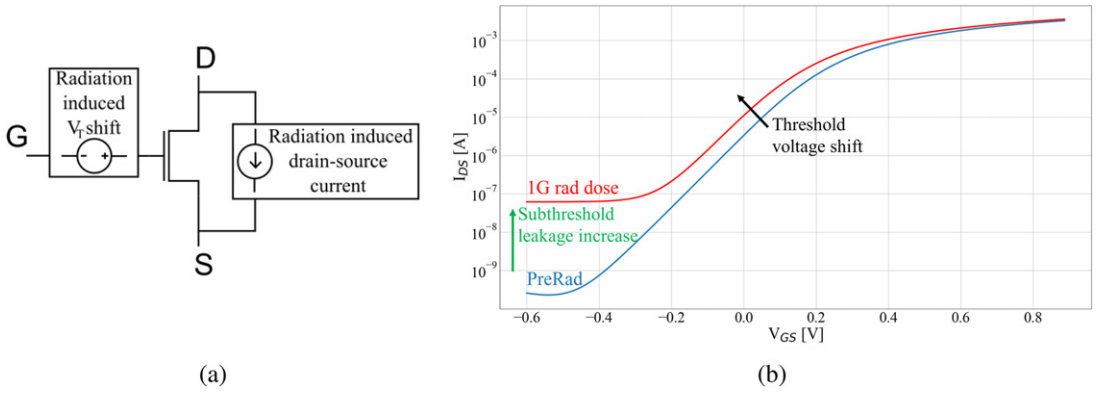

Figure 2. Designed transistor model (a) schematic diagram with TID-dependent VerilogA models and (b) drain current versus gate voltage characteristics of W/L = 3 µm/30 nm NMOS transistor obtained with the designed model for pre-rad and 1 Grad dose ($V_{DS} = V_{DD}$).

3 Analyzed architectures and sizing

The TSPC FF, as shown on figure 1, was designed using similar W/L used for static circuits, provided by the foundry. The TSPC circuit with leakage current mitigation uses state keepers based on gated inverters (GI) [5]. The core transistor sizing is equal but keepers are minimum sized (L = 30 nm, W = 100 nm), as indicated in figures 3(a) and (b). Transistors in all designs are minimum length devices (30 nm).

A similar mitigation strategy was applied to TSPC D-latches, however using a reduced number of transistors connected to the intermediate branch to not slow down the circuit, as shown in figure 3(b).

Flip-flops and latches of both TSPC flavours have been compared with widely used standard Master-Slave C^{2}MOS architecture to confront the performance and radiation robustness.

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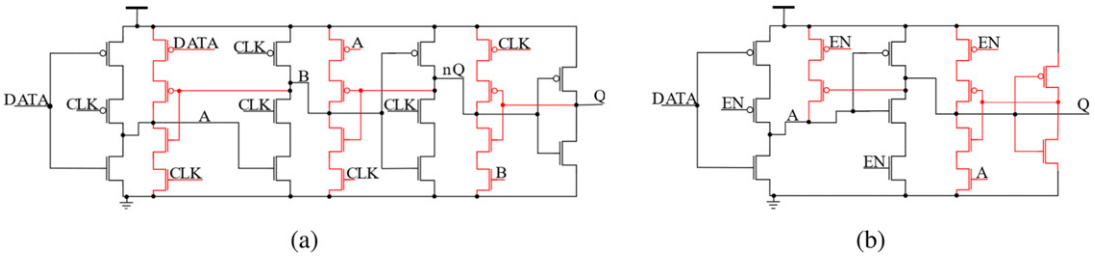

Figure 3. Schematic of (a) leakage protected TSPC flip-flop [5] and (b) leakage protected TSPC latch; both with leakage protection devices in red.

4 TID simulations

To compare the circuits in terms of radiation robustness and performance, they have been simulated with transistor models described in section 2.1 for radiation doses between 0 and 1 Grad. The minimum (F_{min}) and maximum operating frequency (F_{max}) and the power consumption of each circuit was measured. The F_{min} was defined as the frequency at which the FF is not able to retain the previously stored value due to the leakage current. The threshold values of 65% and 40% of the supply voltage were used for logic high ("1") and low ("0") levels, respectively. The results were obtained for nominal process, voltage, temperature (PVT) conditions (typical process, V_{DD} = 0.9 V, 25 °C) and the worst leakage corner (fast process, V_{DD} = 0.99 V, 125 °C).

Figure 4 presents the evolution of the F_{min} at which the TSPC FF operates reliably as a function of TID. It shows that the most significant increase of F_{min} occurs above 200 Mrad when the leakage current becomes significant, draining the stored charge. F_{min} of standard TSPC FF increases by 3× at 1 Grad. For worst case conditions, this frequency can reach 7.47 GHz. This significantly limits the application of the standard TSPC in radiation environments.

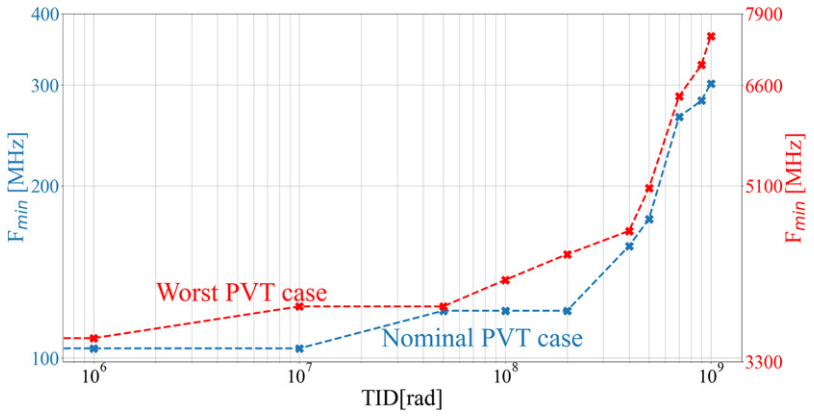

Figure 4. The minimum frequency (due to leakage current) with TID for non-protected TSPC FF.

The circuit with leakage protection is robust against radiation-induced leakage, retaining its data even at 1 Grad TID (even at 0 Hz). This is achieved at the cost of a moderate power and area

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penalty, as shown in table 1. Performance defined by F_{max} for protected circuits is still almost 50% higher than for static designs.

Table 1. Basic performance, power, area and leakage robustness results for simulated flip-flops and latches. Minimum frequency is an indicator reflecting leakage sensitivity of analysed circuit.

	Static		TSPC		TSPC protected	
Parameter	pre-rad	1 Grad	pre-rad	1 Grad	pre-rad	1 Grad
Flip-flops						
F_{min} (GHz) nominal PVT case	0	0	0.10	0.30	0	0
F_{min} (GHz) worst leakage PVT case	0	0	3.50	7.47	0	0
F_{max} (GHz)	50	50	95	87	73	73
Energy per bit (pre-rad) (fJ/bit)	6.86		4.26		4.85	
Area (μm^2)	3.04		2.53		3.88	
Latches						
F_{min} (GHz) nominal PVT case	0	0	0.30	0.97	0	0
F_{min} (GHz) worst leakage PVT case	0	0	3.78	7.75	0	0
F_{max} (GHz)	38	38	70	70	62	62
Energy per bit (pre-rad) (fJ/bit)	6.83		2.39		3.24	
Area (μm^2)	1.86		1.86		3.14	

5 Estimation of critical charge

TSPC logic is often more sensitive to SEEs. However, keeper logic can improve their resilience with weak feedback. To compare the SEU sensitivity of the topologies considered, the critical charge to upset the FF logic state was analysed [11]. In order to estimate this charge, a double-exponential current pulse [12–14] with time constants, t_{rising} = 15 ps, and $t_{falling}$ = 75 ps was injected into all nodes of the circuit at different times. The charge was gradually increased until an upset was detected at the output. Simulations have been performed for the nominal corner in pre-rad state.

Table 2. Critical charge results for flip-flops and latches.

	Architecture		
Parameter	Static	TSPC	TSPC protected
Critical charge for flip-flop [fC]	25.6	0.8	10.7
Critical charge for latch [fC]	23.1	1.6	10.8

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Results presented in table 2 show that the protected flip-flops and latches have a critical charge an order of magnitude higher than standard TSPC architecture, but still, these values are significantly smaller than for the static circuits. This difference comes from stronger feedback branches in C^2MOS circuits than in protected TSPC designs.

6 Conclusions

A modeling and simulation strategy for logic circuits affected by leakage currents induced by exposure to ultra-high radiation doses has been developed. The proposed method showed that TSPC flip-flops implementing leakage current protection are insensitive to TID-induced leakage up to 1 Grad, showing only a 23% decrease in speed, at the cost of 14% increase in power consumption, and a 53% increase in area compared with non-protected TSPC architecture. Nonetheless, the proposed circuits are still outperforming a static master-slave flip-flop, enabling their use in high-speed circuitry.

Based on the obtained results, leakage sensitivity and protection must be considered for high TID and high-temperature environments. Based on the estimated critical charges, the protected TSPC circuits provide additional SEU tolerance when compared with unprotected TSPC topologies using same device sizes. This further extends the range of applications of TSPC circuits in radiation environments.

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