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An lpGBT subsystem for environmental monitoring of experiments

lpGBT collaboration

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Abstract: In this paper, the Low Power Giga Bit Transceiver (lpGBT) built-in system for environmental monitoring of the LHC experiments is presented. Eight external analogue inputs and eight internal voltages are multiplexed into an instrumentation amplifier with selectable gain, whose output is digitised by a 10-bit SAR ADC. A programmable current source can be enabled for each external input to implement resistance measurements. Internal channels are used to monitor power supplies and the output of the temperature sensor. The environmental monitoring system includes a precise 1 V reference voltage source and a 10-bit voltage DAC. All blocks were designed and fabricated in 65 nm CMOS technology, fully characterised, and the pre- and post-irradiation measurement results are presented in this work.

Keywords: Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases); Radiation damage to electronic components; Radiation-hard electronics; VLSI circuits

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1 Introduction

Detection systems in modern particle physics experiments face similar challenges. One of the most common is data transfer from the detector to the Data Acquisition System (DAQ). Another indispensable part is the monitoring and control of environmental parameters. The idea of a common readout Application Specific Integrated Circuit (ASIC) for Large Hadron Collider (LHC) detectors, called the GigaBit Transceiver (GBT), emerged more than a decade ago during the planning of accelerator upgrade [1]. The project evolved over time into two complementary ASICs: GBTX intended for fast data transmission [2] and GBT-SCA for detector control and monitoring [3]. GBT ASICs were used in many readout systems developed for phase I of the LHC upgrade, such as [4–7]. These chips were also used in the Compressed Baryonic Matter (CBM) experiment at the Facility for Antiproton and Ion Research (FAIR) [8].

The Low Power Giga Bit Transceiver (lpGBT) is a successor of GBT and combines all required functions in a single ASIC designed in 65 nm CMOS process [9]. It is a radiation-tolerant chip that can be used to implement multipurpose high-speed bidirectional optical links [10]. It supports

2.56 Gb/s links in the direction from the control room to the detector and 5.12 or 10.24 Gb/s links in the direction from the detector to the DAQ in cooperation with the Versatile Link Plus (VL+) optical transceiver [11].

The lpGBT environmental monitoring and detector control is an integral subsystem of the lpGBT ASIC. This paper focuses on the main part of this subsystem — "Analogue peripherals" (see Chapter 13 of the lpGBT manual [10]). Section 2 describes the architecture and design, section 3 shows the measurement results of the key blocks, and section 4 shows the behaviour of the components in the radiation environment.

2 Architecture and design

The specifications of the lpGBT environmental monitoring and control system are presented in table 1.

Table 1. Specification of the lpGBT environmental monitoring and control system.

Block(s)	Parameter	Specification
General	Supply voltage range	1.08–1.32 V, nominal 1.2 V
	Radiation tolerance	up to 2 MGy
Precise voltage measurement block	Multiplexed inputs	16 (8 external)
	Operating modes	single-ended and differential
	Differential amplifier gains	×2, ×8, and ×16
	Differential input common mode	0.4–0.9 V
	Input bias current	below 250 nA
	Analogue to digital conversion	10-bit with $ENOB_{static}$ > 9 bits
	Maximum INL and DNL	< 1 LSB
	Conversion time	below 1 µs
Reference Source	Source type	voltage, 1 V internally calibrated
	Voltage outputs	external V_{ref} pad
Other	Programmable current source	0–900 µA (attached to any external input)
	Voltage DAC	0–1 V range with at least 8-bit precision
	Temperature sensor	−20°C to 40°C

The system provides the following functions: precise measurement of slow-changing analogue signals, generation of bias currents for external circuitry, and a configurable voltage source. The block diagram of the system shown in figure 1 addresses the specification requirements in the precision and resolution of various blocks. The system uses a nominal supply voltage 1.2 V with ±10% range.

A precise voltage measurement block (PVMB), the key element of the monitoring system, performs the measurement of analogue signals. It contains a fully differential instrumentation amplifier with three selectable gains (×2, ×8, ×16) and a fully differential 10-bit SAR ADC, which converts signals in the range 0–1 V. Through configuration, this block allows for single-ended and differential-mode measurements. The selectable gain enables measurements of input voltage in the differential range from ±500 mV down to ±70 mV (with the highest gain), in a wide range of input

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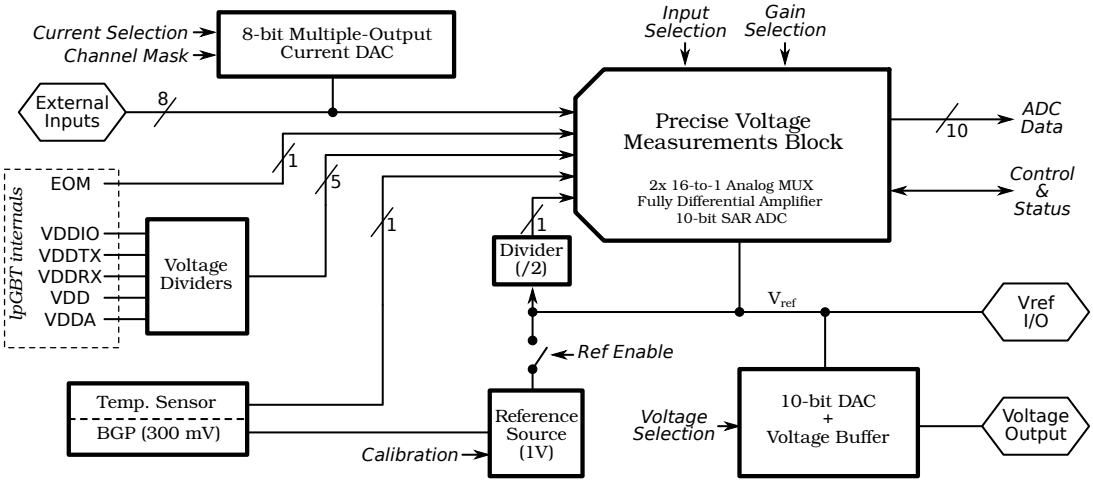

Figure 1. Block diagram of the lpGBT monitoring subsystem.

common mode voltages from 0.4 V to 0.9 V. Each of the external inputs is equipped with an internal current source (0–0.9 mA), controlled by an 8-bit multiple-output DAC that can be used to supply current to resistive sensors (such as a PT1000) or to bias analogue circuits. Internal inputs are used to measure the Eye Opening Monitor (EOM) voltage and power supply voltages for all lpGBT power domains, through voltage dividers.

The 1 V reference voltage for the PVMB is generated by an upscaled 0.3 V voltage source provided by a bandgap circuit [12]. The bandgap circuit also generates a PTAT signal that is used as an internal temperature sensor. The reference voltage can also be used to bias external circuits and guarantees a stable voltage with capacitive loads of up to 10 nF. To work with such a large load, a dedicated amplifier was developed that buffers the reference voltage. Moreover, to complete the functionality, a 10-bit voltage DAC is included that provides an accurate voltage in the range of 0–1 V.

All blocks are calibrated during production testing to allow correction of process variation effects. The calibration constants are stored in a dedicated on-chip non-volatile memory.

2.1 Precise voltage measurement block

The block diagram of the PVMB is presented in figure 2. It consists of two independently controlled analogue multiplexers, a fully differential amplifier with switchable feedback resistors that works as an instrumentation amplifier, and a 10-bit SAR ADC. The multiplexers are connected to the instrumentation amplifier (one to the positive and one to the negative input). Both multiplexers receive the same 16 signals. Seven of them are internal signals used to monitor the supply voltages, temperature, and other parameters of the lpGBT [10]. One signal provides 0.5 V from the reference voltage source to perform single-ended ADC conversions. The remaining eight are external inputs connected to the lpGBT pads.

2.1.1 Fully differential amplifier

A fully differential amplifier is one of the key blocks for PVMB. A simplified schematic of the amplifier is shown in figure 3. It is a two-stage amplifier with a recycling folded Cascode (RFC)

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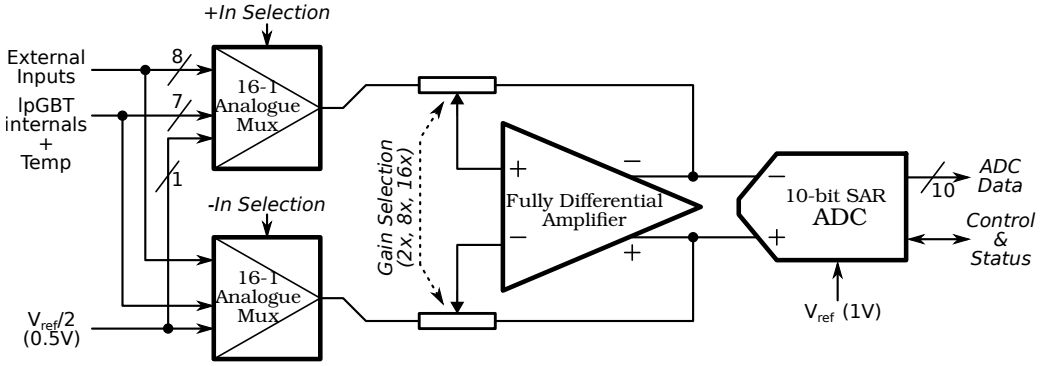

Figure 2. Block diagram of the precise voltage measurement block.

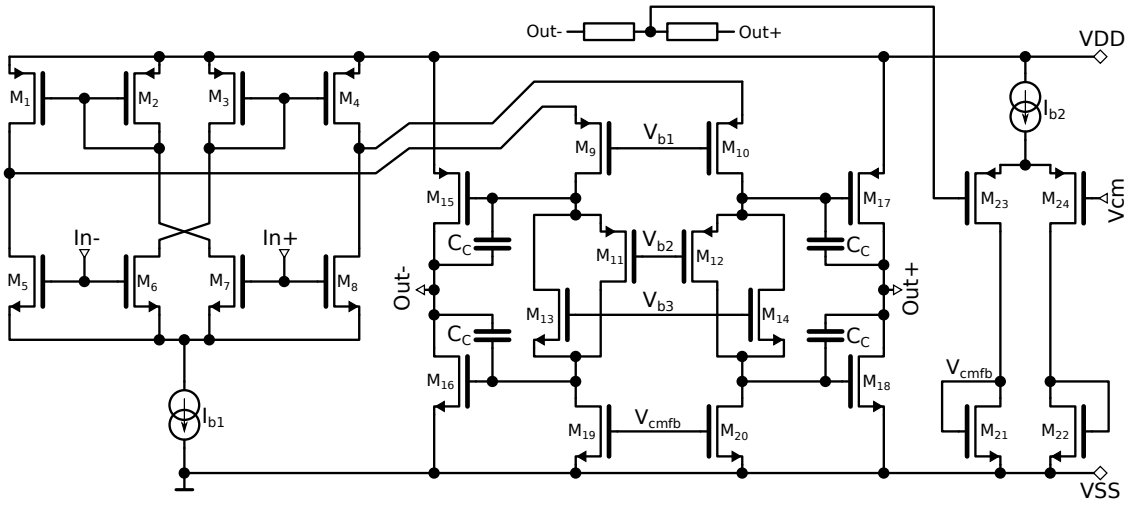

Figure 3. Simplified schematic of a fully differential amplifier.

differential input stage [13] and an AB class rail-to-rail differential output stage [14]. This architecture was chosen for the lowest power consumption at the highest power efficiency and to obtain rail-to-rail output. As shown on the right-hand side of figure 3 a simple amplifier with a PMOS pair provides common-mode feedback.

2.1.2 10-bit SAR ADC

Figure 4 shows the block diagram of the ADC architecture. Differential segmented/split DAC operating in the merged capacitor switching (MCS) scheme [15] is used to achieve ultra-low power consumption. For the same reason, a dynamic comparator was implemented to eliminate static power consumption. Bootstrapped input switches ensure that the required linearity is attained over the full input voltage range. The design of the above blocks is similar, apart from the CMOS process used, to the previous work [16]. To improve the radiation immunity of the ADC core, a fully triplicated synchronous control logic is implemented. Although the goal is static measurement, because of the chosen SAR architecture, the ADC can convert signals at a speed of several MSps. In the lpGBT, the speed of the ADC is limited by the operation of the control interface used (I^2 C or Serial Control),

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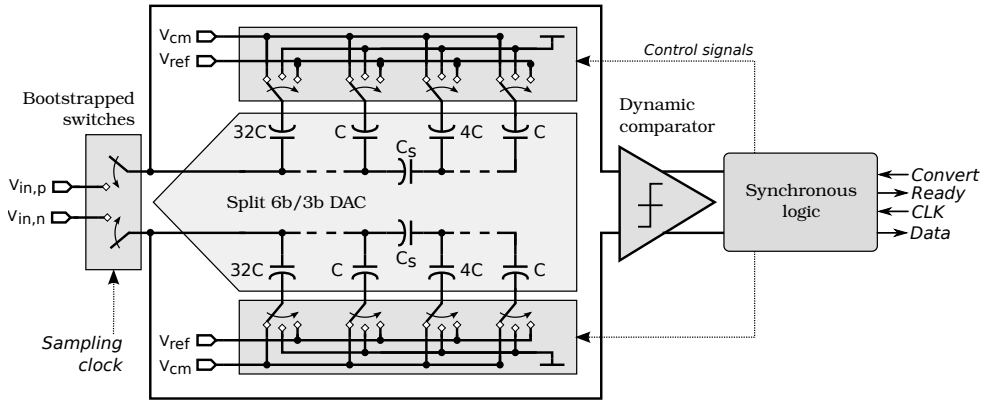

Figure 4. Architecture of the 10-bit SAR ADC.

which initiates the conversion and fetches the results. Serial Control is a dedicated serial interface over the high-speed link used to communicate with the lpGBT.

2.2 Reference voltage source

The block diagram of a reference voltage source, with a nominal value of 1 V, is shown in figure 5. The circuit uses an operational amplifier in a non-inverting configuration, together with the 300 mV voltage reference bandgap circuit (BGP). The non-inverting amplifier architecture, thanks to the

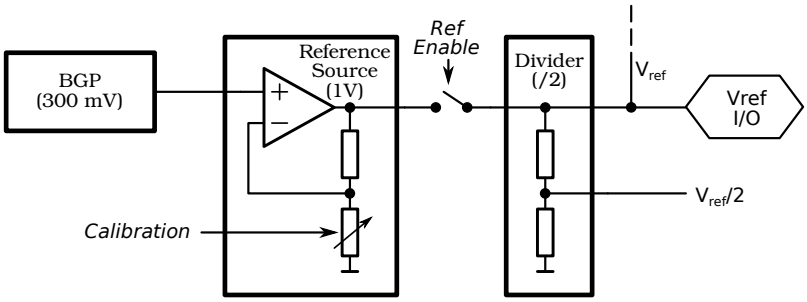

Figure 5. Block diagram of the reference voltage source.

variable gain in the range 3.2–3.4, can compensate for the bandgap circuit voltage variations and amplifiers offset, caused by the process variations and irradiation effects. The gain can be digitally tuned with 8-bit precision during the calibration process.

The operational amplifier used in the reference source has the same two-stage architecture as the amplifier described above for PVMB. However, in this case, the first RFC input stage is PMOS, while the second rail-to-rail class AB output stage is single-ended and designed to improve efficiency. This allows the 1 V reference output to drive external loads with currents up to 5 mA and voltage drops below 0.1%.

2.3 8-bit current and 10-bit voltage DACs

All lpGBT external inputs are internally connected to an 8-output current mirror (see figure 6) controlled by an 8-bit current DAC. Although only the single output current value in the range

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0–900 µA with LSB of about 3.5 µA can be defined, the block configuration is quite flexible, since each current output is activated independently. This circuitry allows biasing of resistive sensors such as a PT1000 without additional external components.

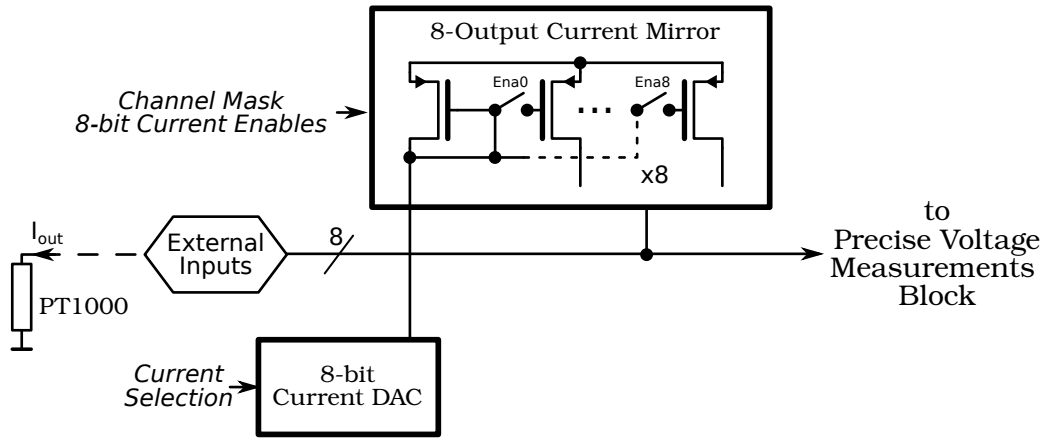

Figure 6. Block diagram of the 8-bit current DAC.

The second DAC in the lpGBT monitoring subsystem accessible directly to the user is the 10-bit DAC with a voltage buffer. The simplified block diagram is shown in figure 7. This DAC is based on the typical R-2R architecture with a reference voltage taken either from on-chip 1 V calibrated reference source or delivered from an external pad. The output of the DAC resistor ladder is buffered to improve its current efficiency. An existing design with 12-bit input control and non-rail-to-rail output buffer was used to achieve the requested 10-bit resolution [17].

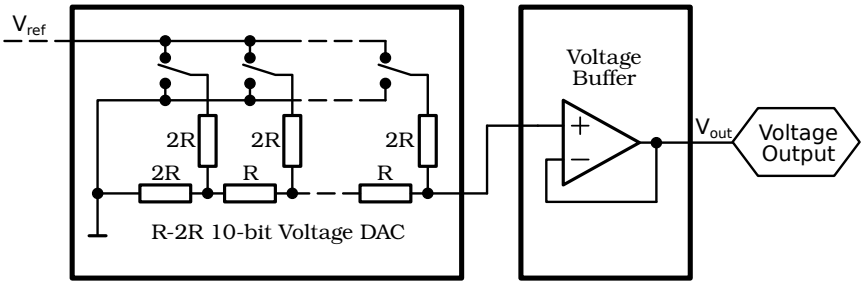

Figure 7. Simplified block diagram of a 10-bit voltage DAC.

3 Measurement results

Systematic measurements of key parameters of the lpGBT environmental monitoring subsystem were made to verify and quantify its performance. In particular, the precise voltage monitoring block, the DACs, the reference voltage source, and the temperature sensor were tested using the setup shown in figure 8. It is based on a Xilinx VC707 FPGA evaluation board connected to a custom mezzanine card linked to the main board via an FMC (FPGA Mezzanine Card standard) connector. The FMC card, equipped with a socket for hosting the lpGBT ASIC, provides connections

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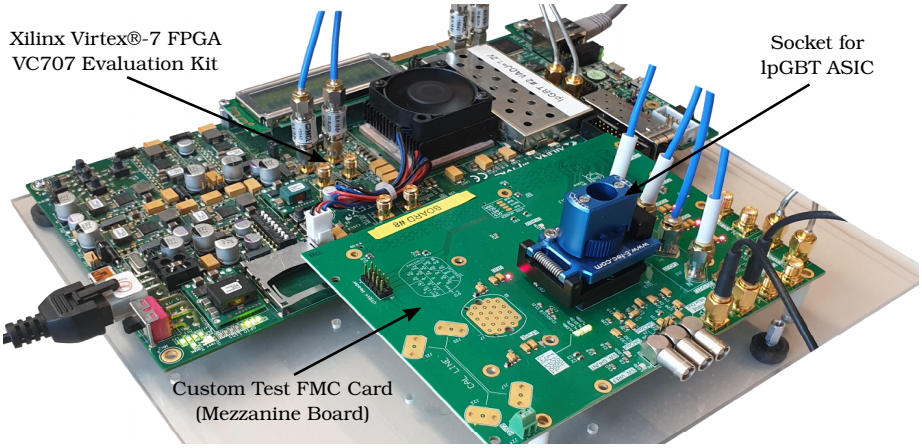

Figure 8. Photograph of the lpGBT measurement setup, based on the Xilinx VC707 evaluation board with a custom mezzanine card connected to the main board via an FMC connector.

to all lpGBT communication interfaces, delivers power supply, and controls its value. Additionally, it also contains 16-bit ADC (AD7682), 16-bit DACs (AD5686), and a high accuracy (±0.25°C) temperature sensor ADT7420 to test analogue sub-circuits of the lpGBT [18].

3.1 Reference voltage source

The reference voltage V_{ref} tuning characteristic, measured at room temperature, is shown in figure 9 (left). The curves measured at different supply voltages almost overlap, and the nominal value 1 V is in the middle of the available tuning range. Obviously, for the lowest supply voltage of 1.08 V the reference voltage saturates for the highest codes. The stability of the reference voltage in the temperature range from −20°C to 50°C, obtained after tuning of V_{ref} to 1 V, is shown in figure 9 (right). The drift of the reference voltage with temperature is almost the same for different supply voltages, with a slope of about 0.3 mV/K. These variations are due to the operation of the bandgap circuit (and multiplication from 0.3 V to 1 V). For the following measurements, V_{ref} was tuned to 1 V separately for 1.08 V, nominal 1.2 V, and 1.32 V supply voltages.

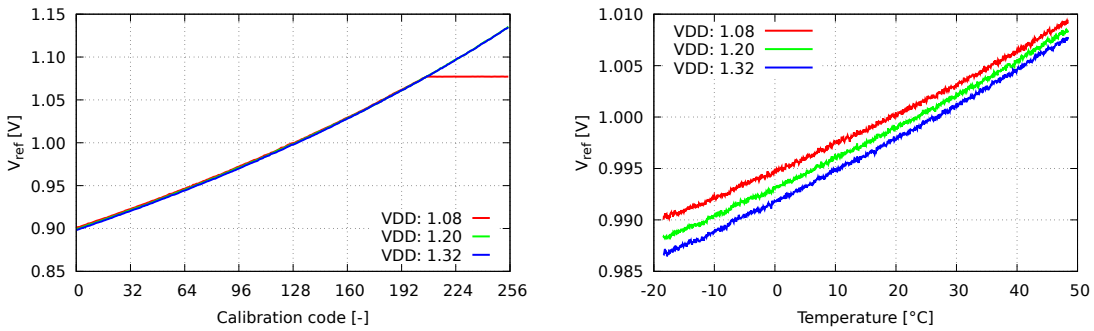

Figure 9. Reference voltage calibration curve for different supply voltages obtained at room temperature (left) and temperature stability of the reference voltage for different supply voltages measured for the calibration value of V_{ref} set to 130 (right).

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3.2 Precise voltage measurement block

Measurements of the PVMB transfer function, made for a typical gain ×2, for the entire input voltage range, at three different supply voltages, are shown in figure 10 (left). They show good performance throughout the full input signal range, from 0 to 1 V. These results were obtained in single-ended operation mode with the internal 0.5 V reference (1 V on-chip reference divided by two). Since the three curves are almost indistinguishable, for better visualisation, figure 10 (right) shows a zoomed plot near the centre codes of the ADC range.

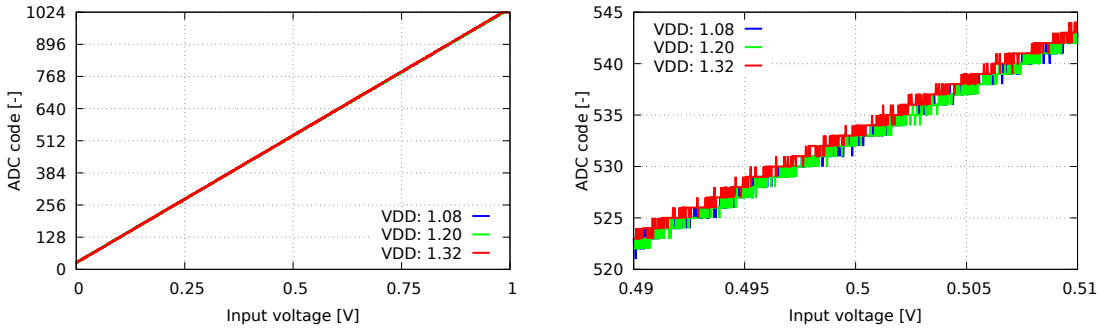

Figure 10. Measurement results of the PVMB transfer curves for different power supply voltages for the default gain ×2 (left) and its zoom for the middle codes (right).

For precise linearity quantification, integral (INL) and differential (DNL) nonlinearity, errors were measured as shown in figure 11. These results were obtained in differential mode for the external differential input signal. The PVMB achieves good linearity with a maximum DNL error

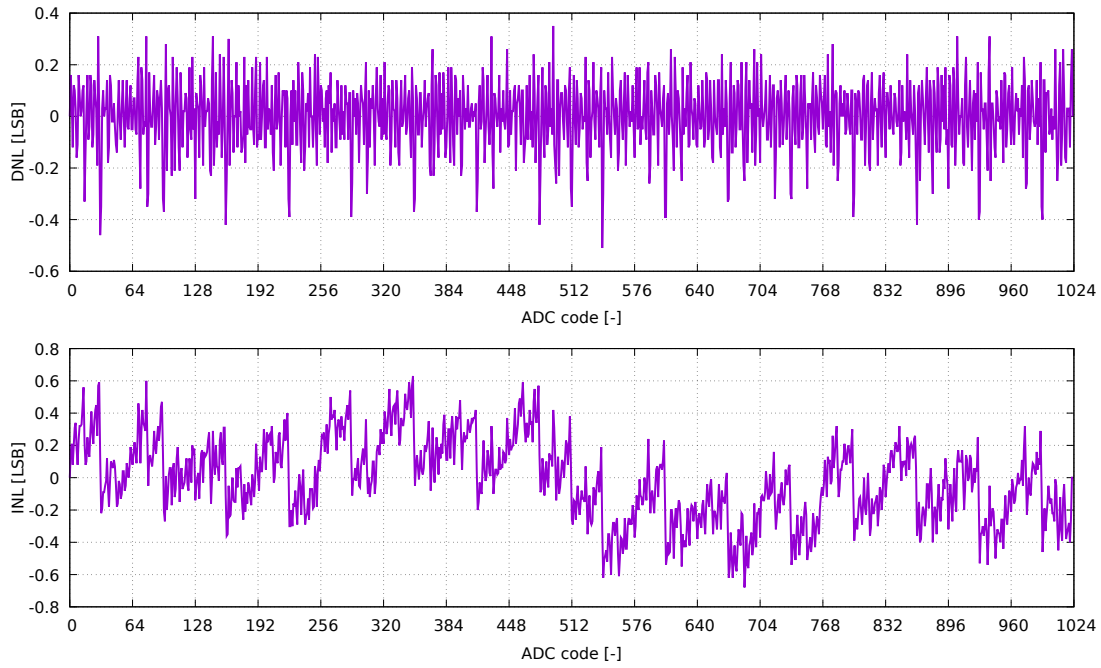

Figure 11. Static DNL (top) and INL (bottom) non-linearity errors of PVMB.

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below 0.5 LSB and maximum INL error below 0.7 LSB. On the basis of the INL results, one can calculate a static effective number of bits ($\mathrm{ENOB_{static}}$) [19]:

$$\mathrm{ENOB_{static}} = \log_2\left(\frac{N}{\sqrt{12 \cdot \left[12^{-1} + (N-2)^{-1} \cdot \sum_{k=1}^{N-2} \mathrm{INL}_k^2\right]}}\right),$$

where N is the number of ADC codes. The equivalent resolution is $\mathrm{ENOB_{static}} = 9.60$ bits.

Measurements of the PVMB transfer function, made in single-ended operation mode with the internal 0.5 V reference, for gains ×8 and ×16 are shown in figure 12 (left); gain ×2 is added for comparison.

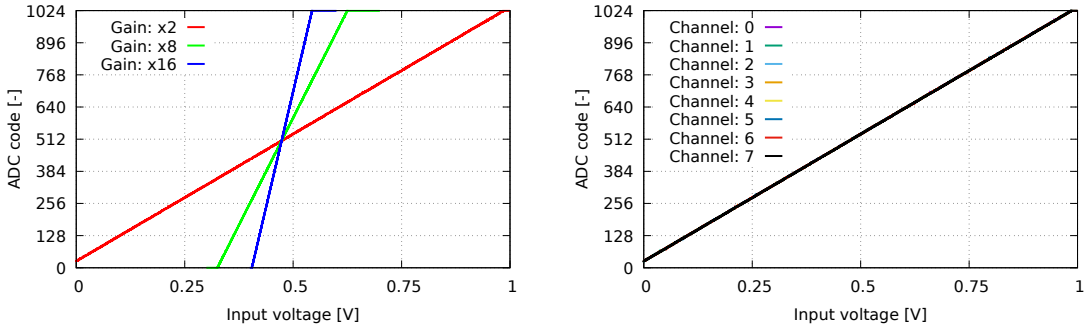

Figure 12. Transfer curves of the PVMB for different gains (left) and transfer curves for all external channels at gain ×2 (right).

Very good linearity is seen for all three gain configurations. For verification, the same measurement was performed for gain ×2 using the eight external channels, giving the same results, as presented in figure 12 (right).

3.3 8-bit current DAC and 10-bit voltage DAC

The measurement results of the transfer function of the 8-bit current DAC for different power supply voltages are shown in figure 13 (left). The plot presents the output voltage obtained with 1 kΩ shunt resistor (connected from the input to the ground) versus the DAC code. The value of 1 kΩ corresponds to the nominal resistance of a PT1000 temperature sensor, which is one of the typical applications of measurement blocks. Measurements were made for all current mirror outputs (see figure 6) but since there were no significant differences between them, the plot shows the results only for the selected one.

It can be seen that the output current does not depend on the power supply. The curve is not perfectly linear, but it was not the main goal for the DAC serving to bias the analogue circuits. On the other hand, monotonicity and good differential non-linearity (DNL) were a requirement. The measured DNL of the DAC is presented in figure 13 (right). Very good performance with DNL below ±0.5 LSB is observed.

Figure 14 (left) shows the voltage DAC transfer function and its INL (right) for different supply voltages. The DAC INL is within ±1 LSB for 87% of the operational range (0–1 V) at the worst case

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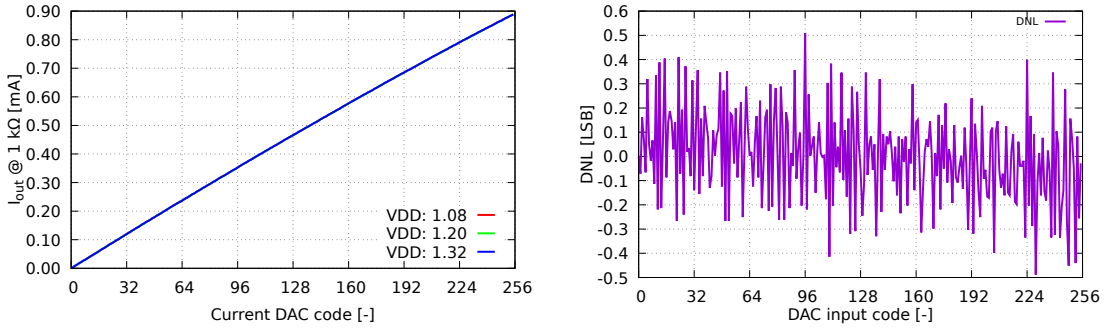

Figure 13. Example of the results of the current DAC measurement. Transfer curves with 1 kΩ load at different supply voltages (left) and DNL at a nominal power supply (right) for the selected current mirror.

supply voltage of 1.08 V. The linearity degrades on the edges, as expected, due to the output buffer, which architecture does not provide rail-to-rail capability.

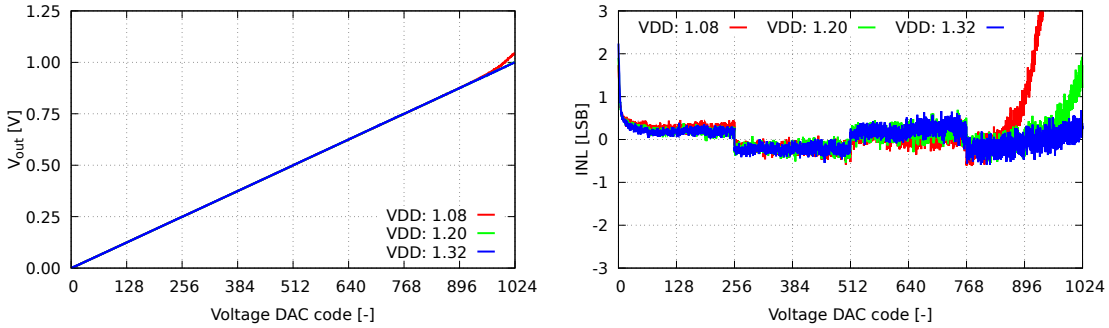

Figure 14. Voltage DAC measurement results. Transfer curves for different supply voltages (left) and INL for different supply voltages (right).

3.4 Temperature sensor

The internal temperature sensor was characterised in a temperature range from −25°C to 50°C, as shown in figure 15 (left). The measurements give a voltage-to-temperature conversion factor of 2.12 LSB/°C. The conversion factor is constant for different supply voltages, but small offset changes are observed. Figure 15 (right) shows the INL of the temperature sensor — the precision is about ±0.5°C in the full temperature range from −25°C to 50°C.

4 Radiation measurements

To study the operation of the environmental monitoring and control subsystem during irradiation, measurements of its key blocks as a function of the received dose were performed at a high X-ray beam intensity of about 24.5 kGy/h, up to 3.8 MGy, with the setup presented in figure 16. The main difference from the setup used for the previous measurements is the X-ray tube and an additional cable (blue cable in figure 16) between the FPGA and FMC boards. The reference voltage of the chip was set to 1 V at the beginning for the nominal 1.2 V power supply and kept unchanged during all

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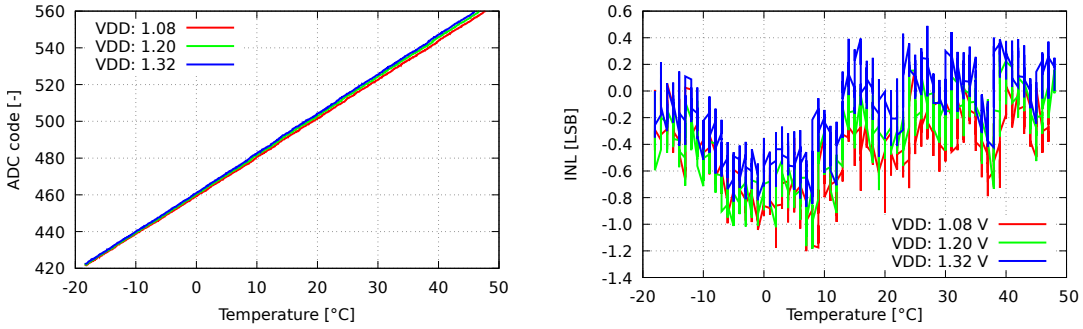

Figure 15. Transfer curve of the internal temperature sensor (left) and INL (right) for different supply voltages measured with PVMB.

measurements. It is the most typical and expected use case for the lpGBT ASIC during monitoring of LHC detectors. The use of V_{ref} tuned for the nominal supply only explains small differences in the results for different power supply voltages, which were not present in the measurements that were discussed in the previous section, for which V_{ref} was always tuned.

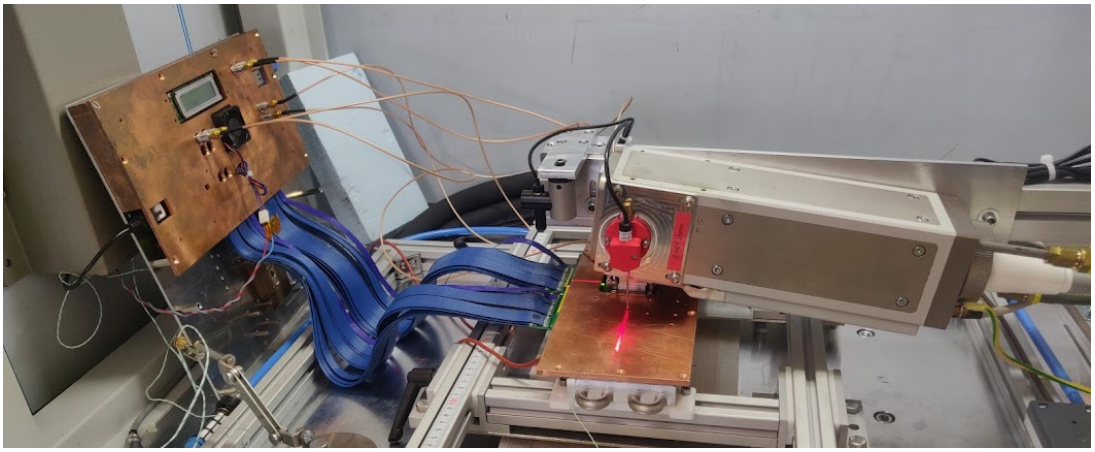

Figure 16. Photograph of the measurement setup during irradiation. FPGA board behind the copper plate on the left. The board is connected through blue cables to the FMC card located in the centre and is covered by the second copper plate. X-ray tube is just above the second copper plate.

All blocks were always fully functional during the entire irradiation time and only subtle changes in the analogue characteristics were observed (except for the temperature sensor). The detailed behaviour of the various blocks is discussed below.

4.1 Reference voltage source

Figure 17 shows the drift of the reference voltage output from the starting nominal setting versus the received dose, for different supply voltages. The output decreases slightly with the received dose with almost no dependency on the supply voltage. The maximum drop in the reference voltage is less than 18 mV (< 1.8%) and is observed in the flat part of the curve for doses between 2–3.8 MGy.

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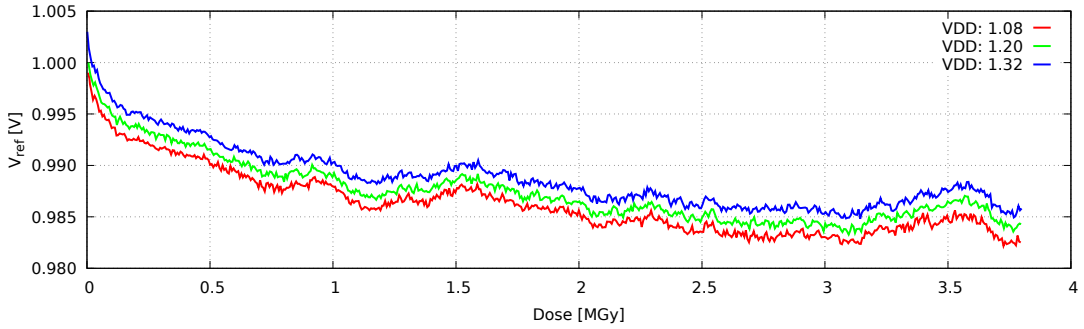

Figure 17. Reference voltage as a function of the received dose.

4.2 Precise voltage measurement block

Figure 18 presents the change in slope (top) and offset (bottom) of the transfer curve (see figure 10 (left)) of the PVMB as a function of the received dose, obtained for different supply voltages. Each slope and offset point comes from the linear fit of the transfer curve measured at a given irradiation dose. The differences in the results obtained for different power supplies are quantitatively negligible. The offset is stable within about ±2 LSB along the whole irradiation dose, while the slope increases slightly during irradiation by 15 LSB/V (1.5%) for doses above 2 MGy.

It is interesting to understand how the effect of V_{ref} change with irradiation (figure 17), affects the behaviour of the PVMB slope in figure 18 (top). When plotting the slope of the PVMB for the input voltage normalised to V_{ref}, a flat curve is obtained as seen in figure 19. It may be concluded

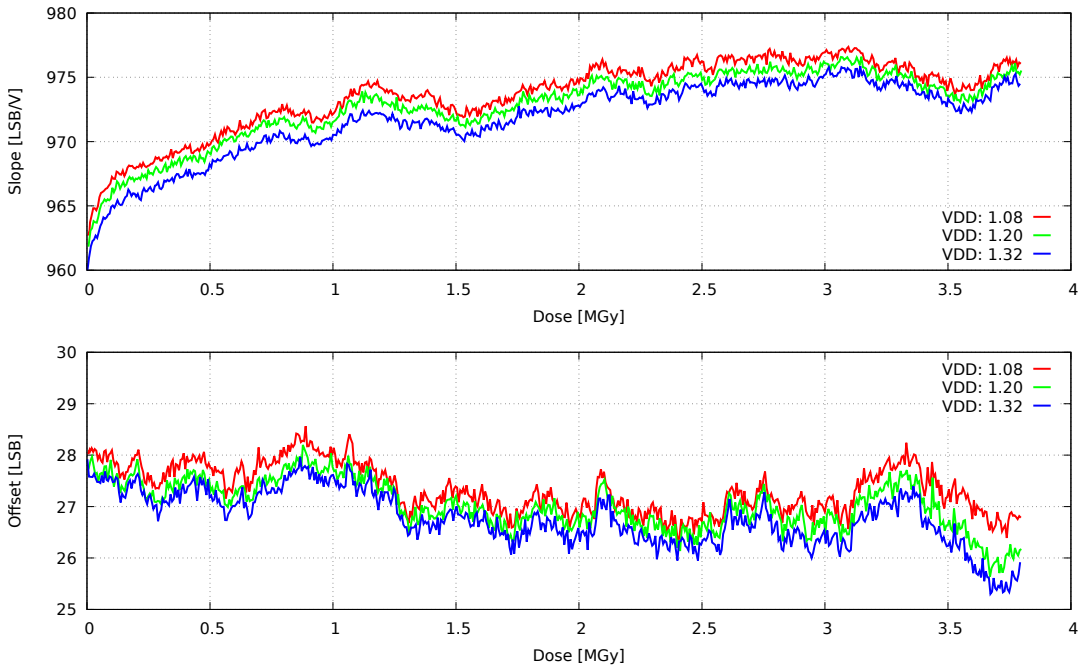

Figure 18. Transfer curve slope (top) and offset (bottom) parameters of the PVMB during irradiation up to 3.8 MGy dose, measured for a default gain ×2.

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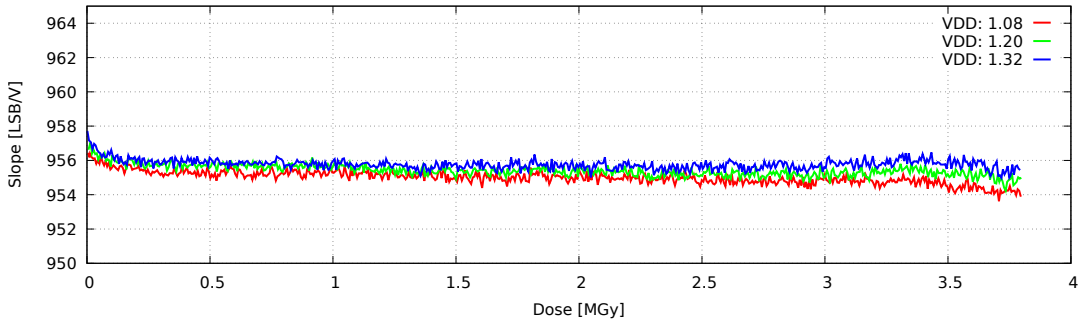

Figure 19. Transfer curve slope parameter of the voltage monitoring block during irradiation up to 3.8 MGy dose normalised by V_{ref} drift, for a default gain ×2.

that the change in slope of the transfer curve is mostly due to the change in the reference voltage generated by the bandgap circuit.

4.3 8-bit current DAC and 10-bit voltage DAC

During irradiation, the transfer curves for both the 8-bit current DAC and the 10-bit voltage DAC were measured periodically with approximately 6 Gy steps. Figure 20 (left) shows the maximum current of the 8-bit current DAC as a function of the received dose, for different supply voltages. The DAC is still fully operational after a dose of 3.8 MGy, although the output current at maximum dose drops by approximately 5% for a given supply voltage.

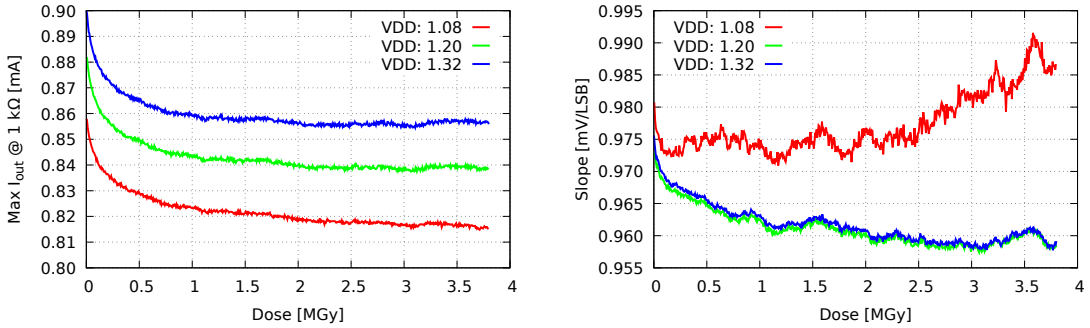

Figure 20. DACs performance during irradiation. Maximum current for the 8-bit current DAC (left) and transfer curve slope of the 10-bit voltage DAC (right).

Figure 20 (right) shows the slope of the transfer curve of a 10-bit voltage DAC as a function of the received dose, for different supply voltages. The maximum slope change at the highest dose is approximately 4% for the default and highest supply voltage. For the lowest supply, it is even less, but the curve has a different shape.

4.4 Temperature sensor

The internal temperature sensor was characterised as a function of the received dose at room temperature, for different supply voltages, as shown in figure 21. The drift in temperature with dose is linear (except for very small doses) with a slope around 22 LSB/MGy. For very small doses,

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below 5 kGy, a rapid change from 520 LSB to around 540 LSB at nominal supply voltage, was observed. The temperature sensor is affected by radiation and cannot be relied upon for precise absolute temperature monitoring in a radiation environment. However, it can still be used to detect temperature changes (transients) caused by events such as the failure of the cooling system, which is the main application for the sensor.

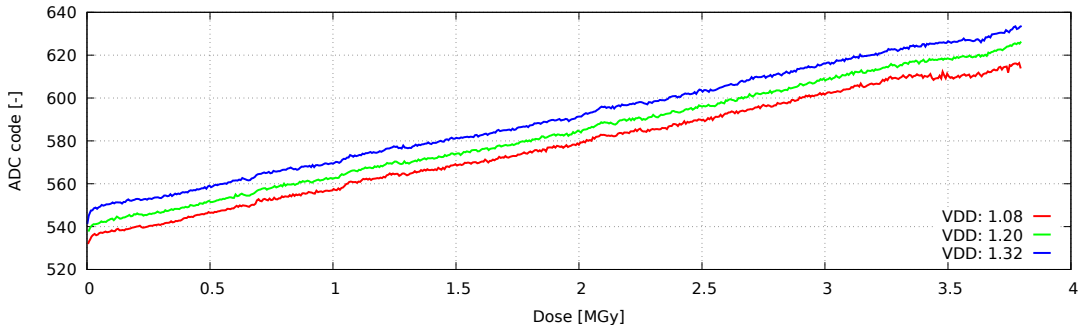

Figure 21. Internal temperature sensor values as a function of the received dose.

5 Conclusions

The design, measurement results, and behaviour after irradiation of the lpGBT system for environmental monitoring and control of experiments were presented. The system supports needed detector monitoring functions. In particular, it includes precise voltage monitoring composed of an instrumentation amplifier and a 10-bit SAR ADC. The measurement results match the system requirements.

The performance of the system was studied as a function of the irradiation dose up to 3.8 MGy. The circuit was fully functional during and post irradiation and no significant performance decrease was observed (except the temperature sensor), even after 3.8 MGy dose.

The lpGBT ASIC has already been adopted by some sub-detectors planned for Phase II of the LHC upgrade [20–23]. Other users are expected in the near future [24].

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