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Radiation-tolerant all-digital clock generators for HEP applications

S. Biereigel,[a,b,c,*] S. Kulis,[a] E. Mendes,[a] P. Hazell,[a] P. Moreira[a] and J. Prinzie[b]

[a] *European Organization for Nuclear Research (CERN), Espl. des Particules 1, CH-1211 Meyrin, Switzerland*
[b] *ESAT-ADVISE Research Lab, KU Leuven, Kleinhoefstraat 4, B-2440 Geel, Belgium*
[c] *Electronics and Sensor Systems, Brandenburg University of Technology, Siemens-Halske-Ring 14, D-03046 Cottbus, Germany*

E-mail: stefan.biereigel@cern.ch

Abstract: The emergence of high-precision timing systems in High Energy Physics motivates new developments in the domain of clock generation and distribution. Particularly, when considering the challenges arising from adopting advanced deep-submicron CMOS technology nodes, all-digital PLL and clock and data recovery (CDR) architectures constitute a promising option for future high energy physics (HEP) experiments. Both LC oscillator and ring oscillator-based all-digital PLL/CDR blocks for front-end ASICs were studied, designed, manufactured and characterized. Their design, the hardening considerations, as well as the performance obtained with these circuits are presented in this article.

Keywords: Digital electronic circuits; Radiation-hard electronics; Analogue electronic circuits; Timing detectors

*Corresponding author.

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1 Introduction

The adoption of advanced CMOS technology nodes imposes significant restrictions on the design of high performance PLL and CDR circuits. To remedy the associated design difficulties, all-digital clock generator architectures have been proposed and studied extensively. They have since been widely adopted in many commercial applications [1]. As the high energy physics domain continues to exploit more advanced deep sub-micron CMOS nodes, the same concerns become relevant in addition to the persistent challenges of radiation-tolerant circuit design. For digital circuits in particular, systematic radiation hardening approaches against single-event effects (SEEs) and total ionizing dose (TID) degradation have found widespread adoption in the HEP community. Conceptually, applying these techniques to digital PLL and CDR architectures promises significant improvements to their radiation tolerance over conventional clock generator circuits.

To evaluate the merits of all-digital phase-locked loop (ADPLL) and CDR circuits for high energy physics environments, two radiation-tolerant macro blocks were developed. As a study case, front-end ASIC applications are considered. Typical requirements for these applications in the High Luminosity LHC (HL-LHC) context are the use of reference clock frequencies of 40, 80, 160 or 320 MHz or an equivalent CDR input data rate of 80, 160 or 320 Mbps. The ability to synthesize frequencies up to 1.28 GHz constitutes a further requirement, compatible with the eLink specifications of the low power Gigabit Transceiver (lpGBT) ASIC [2], which is nowadays considered the mainstream data aggregator at the HL-LHC experiments. To explore relevant design trade-offs, two types of all-digital clock generators were designed, manufactured and tested. A ring oscillator PLL/CDR may target area-constrained general purpose applications, while LC oscillator ADPLLs cover precision timing use cases, for example in timing detector front-end ASICs.

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2 Circuit description

The basic architecture of the developed macro blocks is outlined in figure 1. Since only integer-N PLL/CDR operation of the clock generator circuits is desired, a bang-bang loop architecture is chosen. Compared to time-to-digital-converter-based phase detectors, such an architecture is preferable in terms of power consumption and area requirements. Further, it has been shown that such phase detectors provide intrinsic SEEs robustness [3]. For PLL operation, a custom D-flip-flop is used as a bang-bang phase detector (BBPD), while an Alexander phase detector [4] enables CDR operation. The digital loop filter (DLF) is implemented using a proportional-integral structure with programmable coefficients. A data path word length of 16 bit is used, which supports operation of the digital PLL with both types of digitally controlled oscillator (DCO). The six most significant output bits of the DLF directly drive control bits of the DCO frequency tuning word, while the ten least significant bits are fractionally interpolated by a digital MASH-1-1 sigma-delta modulator (ΣΔM) [5].

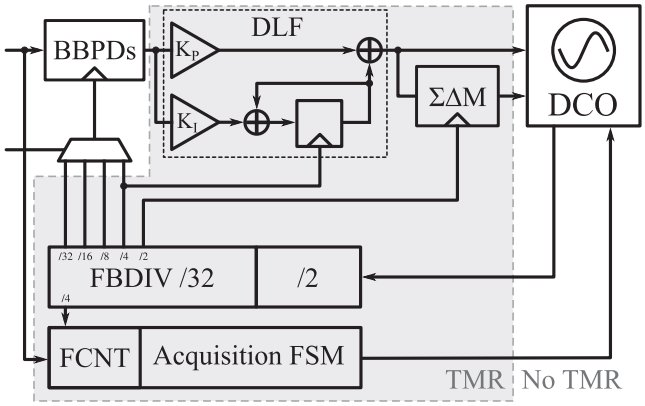

Figure 1. Block diagram of the studied radiation-tolerant ADPLL macro blocks.

2.1 Digitally controlled LC oscillator

A low-jitter 2.56 GHz LC DCO was implemented using the basic architecture shown in figure 2. A current-reuse cross-coupled amplifier topology with an NMOS tail current source is used, allowing an implementation using only thin-oxide devices to reduce TID sensitivity. A two-turn 1.6 nH spiral inductor together with three banks of digitally controlled capacitor cells are used to control the oscillation frequency. A coarse process, voltage and temperature (PVT) bank (ΔC_{LSB} = 12.5 fF), an acquisition bank (ΔC_{LSB} = 600 aF) and a fine tracking bank (ΔC_{LSB} = 65 aF) are implemented. While the PVT bank uses binary-weighted cells to minimize area, the acquisition and tracking banks are implemented using identical unit cells to ensure optimal matching. The tracking cell layout in particular was extensively simulated using a 3D planar electromagnetic simulator to ensure accurate prediction of its capacitance. During operation, the tuning range of the tracking bank is initially centered by means of a frequency counter (FCNT) and an acquisition finite state machine (FSM) using the PVT and acquisition banks. Subsequently, only the tracking bank is used during closed-loop operation. Further design details can be found in [6].

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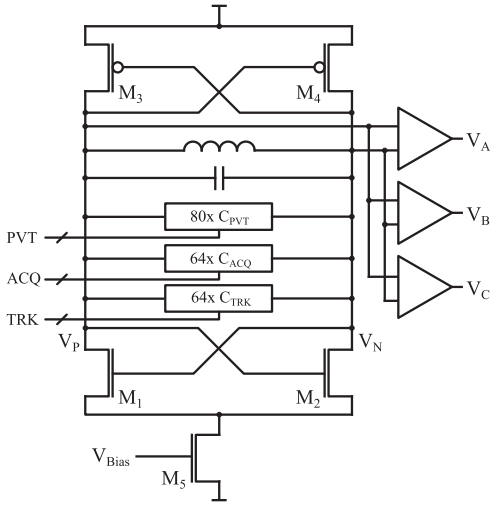

Figure 2. LC DCO architecture.

2.2 Digitally Controlled Ring Oscillator (DCRO)

A five-stage DCRO was designed for a target center frequency of 1.28 GHz. A previously proposed architecture [7] promising high immunity against SEE has been selected, in which each ring oscillator stage is composed of multiple tri-state-inverter cells driving one common node, as shown in figure 3. Oscillator frequency control is obtained through varying the number of enabled unit cells in the oscillator. This segmentation distributes devices sensitive to charge collection spatially, causing only a small subset to be affected by any given SEE. To further suppress the phase displacement from SEEs, we proposed to add an additional series resistor in series with the output of each unit cell, which provides additional decoupling of unit cells from one another, as reported in [8]. The oscillator provides 9 bit frequency control range with linear tuning characteristics at an LSB size of 3.5 MHz. Its tuning range is sized to cover PVT variations plus a 15% margin reserved for TID degradation of the active devices.

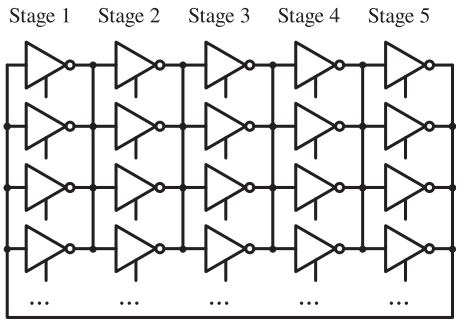

Figure 3. DCRO architecture.

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2.3 Implementation and radiation hardening considerations

While the oscillator circuits were designed using a custom design flow, the remainder of the ADPLL designs were completed using a highly automated digital design workflow. Hence, the majority of digital circuitry was synthesized from Verilog RTL code. The TMRG tool [9] was used to automate the insertion of triple modular redundancy (TMR)-based SEE protection into the DLF, ΣΔM, feedback divider and control logic. During the place-and-route process, precautions to preserve signal integrity of clock signals were taken. Placement guidance constraints as well as manual cell placements were used to maintain spacing between critical paths and less critical logic. Custom, high-density decoupling cells were inserted throughout the digital core area to improve power integrity and reduce deterministic jitter due to digital switching activity. To ensure effectiveness of the TMR protection, instance spacing constraints were used to enforce a minimum distance between redundant sequential cells. Fault injection simulations were performed to verify SEE protection.

3 Experimental characterization

Both circuits were manufactured using a commercial 65 nm CMOS technology which was extensively characterized for its radiation tolerance previously [10, 11]. Aspects of circuit performance and radiation hardness of the developed circuits were studied experimentally.

3.1 PLL and CDR performance

All foreseen modes of operation, reference clock frequencies, input data rates and output clock frequencies were characterized. Across these configurations, the macro blocks individually consume between 10 and 13 mW of power at a nominal supply voltage of 1.2 V. Full functionality was validated within a ±10% supply voltage range. The PLL figure of merit (FOM)[1] was obtained during operation of the PLLs locked to a low-jitter 320 MHz reference clock. A jitter performance of 520 fs rms (LC PLL, FOM: −235 dB) and 1.6 ps rms (DCRO PLL, FOM: −225 dB) was achieved. Performance measurements in a chain comprised of a field programmable gate array (FPGA) back-end emulator, a VTRX+-based optical link [12] and an lpGBT were performed to assess the system level performance of the developed circuits. A 40 MHz eClock and a 80 Mbps eLink were used to operate the ADPLL clock generators in PLL and CDR modes respectively. The measured jitter performance for each of the tested configurations is summarized in table 1 below.

In all tested scenarios, the ADPLL blocks were able to provide a front-end level jitter performance in line with requirements of contemporary timing detectors (i.e. better than 5 ps rms). The LC ADPLL consistently provides better jitter performance than the ring oscillator circuit as a result of the better phase noise performance of its local oscillator. Its lower loop bandwidth efficiently suppresses the broadband phase noise originating from the FPGA back-end, which propagates through the lpGBT CDR when it is operating in transceiver mode.

[1] $\mathrm{FOM_{PLL}} = 20\log_{10}\frac{\sigma_{\mathrm{PLL}}}{1\,\mathrm{s}} + 10\log_{10}\frac{P_{\mathrm{PLL}}}{1\,\mathrm{mW}}$.

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Table 1. Jitter performance measurements obtained using a front-end demonstrator setup.

	lpGBT TX mode 40 MHz eClock	lpGBT TRX mode 40 MHz eClock	lpGBT TRX mode 80 Mbps eLink
Reference jitter	1.9 ps rms	1.9 ps rms	
LC ADPLL jitter	2.2 ps rms	1.1 ps rms	1.5 ps rms
DCRO ADPLL jitter	2.6 ps rms	2.8 ps rms	4.8 ps rms

3.2 Single-event effects testing

The SEE sensitivity of the manufactured ADPLL circuit blocks was experimentally tested using the Heavy Ion Facility (HIF) at the Cyclotron Resources Center (CRC) in Louvain-La-Neuve, Belgium. Both circuits were operated in PLL mode using a 40 MHz reference clock while being irradiated with ions of LET_{Si} up to 62.5 MeV cm^2 mg^{-1}. A fluence of at least 1×10^7 cm^{-2} was collected for each of the PLL circuits per ion species. A transient phase measurement instrumentation system offering picosecond-level resolution and sub-picosecond rms jitter performance was used to detect and record excursions of 80 MHz clock signals produced by either of the clock generator circuits. The detection threshold for single-event effect responses was limited by the random jitter of the PLL circuits, to about ±15 ps and ±10 ps for the ring and LC ADPLL circuits respectively.

In both ADPLL circuits, no SEE signatures pointing to any of the digital circuit components protected by TMR (feedback divider, DLF, ΣΔM, state machines) were identified. This highlights the significant advantages of systematic SEE hardening techniques that can be applied to digital PLL circuits. All sensitivities found in the circuits could be traced back to SEE responses stimulated in their respective oscillator circuits. Comparing the heavy ion cross section of both circuits for the same event magnitude (peak phase error within a single transient), the ring oscillator PLL circuit was found to be significantly less sensitive. The distributed-element nature of the ring DCO combined with the resistive decoupling scheme was found highly effective at suppressing charge collection effects. Combined with the much larger bandwidth of this PLL during operation, phase and frequency transients in the oscillator are quickly counteracted by the feedback of the tracking loop. Only at the highest LET_{Si} could transients exceeding the random jitter of the PLL be detected [8]. The cross section of the LC ADPLL is much larger in comparison, and the root causes for this sensitivity in the LC DCO have been identified in the used inductor geometry and the switched-capacitor cells used in the PVT and acquisition banks, as discussed in [6, 13].

3.3 Total ionizing dose testing

The developed ADPLL circuits were irradiated at the CERN X-ray facility. A dose rate of 8.94 Mrad h^{-1} was used to irradiate the devices up to a total dose of 1.5 Grad at a temperature of −15 °C. During the irradiation, the PLL circuits were electrically characterized for supply voltages of 1.2 V ± 10%. The open-loop center frequency, tuning curve and power consumption of both types of DCO was measured in a first phase of the test routine. Both PLL blocks remained functional up to a TID of 1.4 Grad. Different individual failure mechanisms were identified for the two circuits. As expected, the ring DCO circuit suffered from a significant reduction in free-running oscillation frequency. A total reduction of 15% with respect to the pre-irradiation condition was

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found for this circuit at the point of failure. The DCRO ADPLL hence failed to obtain lock as soon as the maximum oscillation frequency became insufficient to provide the desired value [8]. The LC DCO in comparison showed a radiation-induced frequency shift of less than 1%. The LC ADPLL failed to operate reliably at a dose of 1.4 Grad due to a failure of its divide-by-two prescaler circuit [6].

4 Conclusions

Radiation-tolerant all-digital PLL and CDR macro blocks have been designed and manufactured in a commercial 65 nm CMOS technology. A ring-oscillator PLL/CDR for general purpose clock generation applications and an LC-oscillator PLL/CDR for precision timing applications have been presented in this article. The digital nature of these clock generator circuits enabled the application of proven radiation hardening techniques that are highly effective against SEEs. Further, exploiting an RTL-driven digital implementation flow for a majority of the circuit allows them to remain flexible in the face of changing functional requirements, area constraints and technology scaling. An extensive experimental characterization has confirmed the performance of these clock generators to be in line with the requirements of HL-LHC experiments in terms of their jitter performance, power consumption as well as their state-of-the-art SEE and TID tolerance.

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