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Measurements of total ionizing dose effects in TPSCo 65 nm and influence of NMOS bulk bias

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Abstract: The CERN EP R & D WP 1.2 aims to develop state-of-art monolithic pixel detectors using modern CMOS processes. The TPSCo 65 nm process is a suitable candidate and its radiation tolerance and sensor performance are therefore being studied. The impact of the back bias on the transistor behavior has also been measured to provide the designers with accurate models. This process shows sensitivity to radiation and degradation mechanisms similar to previously studied 65 nm CMOS technologies, strongly dependent on the geometry of the transistors. This paper presents preliminary characterization results of this technology that can serve as a guideline for designers.

Keywords: Radiation damage to detector materials (solid state); Analogue electronic circuits; Radiation-hard electronics; Particle tracking detectors (Solid-state detectors)

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2023 JINST 18 C02036

Contents

1 Introduction 1

2 First measurements up to 1 Grad (SiO2) TID 2

3 Transistor dimension related effects 2
  3.1 Leakage current 4

4 Influence of nMOS bulk bias 4

5 Conclusion 5

1 Introduction

One of the main objectives of the EP R & D Work Package (WP) 1.2 is to develop monolithic active CMOS pixel sensors for vertex measurements at a high rate and hostile environments at the HL-LHC (High Luminosity-Large Hadron Collider). The higher luminosity leads to a maximum expected Total Ionizing Dose (TID) of up to 1 Grad (SiO_2). The move to more advanced nodes with smaller feature sizes should allow for reducing power consumption and more sophisticated signal processing. Moreover, the thinner gate oxide which comes with the downscaling of the transistor size increases the tolerance to TID [1, 2]. During phase 1, WP1.2 intends to evaluate different nodes and their performance for radiation tolerance and sensor performance. At the moment TPSCo 65 nm process is the main candidate.

Several Transistor Test Structures (TTS) including both pMOS and nMOS have been designed and tested. Some of these TTS include core CMOS devices (rated at 1.2 V) distributed into two arrays of transistors, where either the width or the length varies, allowing to test the radiation response on different transistor dimensions. TID tests up to 1 Grad (SiO_2) on core 1.2 V devices confirm the reliability of these transistors under irradiation, showing similar radiation response to other 65 nm technologies [3, 4]. Post-irradiation high-temperature annealing revealed the presence of two well-known radiation effects: RISCE (Radiation-Induced Short Channel Effects) and RINCE (Radiation-Induced Narrow Channel Effects) [5]. These are directly related to the radiation-induced charge trapped in the spacers and the Shallow Trench Isolation (STI) oxide.

Another topic of study was the effect of bulk bias on the transistor performance. This is relevant as there are certain pixel designs where the nMOS on the pixel matrix are biased with their bulk at voltages down to −6 V. This is done to fully deplete the sensor in order to improve the charge collection [6, 7]. However, significant reverse bulk bias might induce a considerable threshold voltage shift due to the body effect and therefore a decrease of the maximum drain current [8]. This study aims to analyze the behavior of nMOS transistors at an unusual operating point at which

2023 JINST 18 C02036

the models provided by the foundry are not longer valid. Measurements at different negative bulk bias showed the impact of the body effect.

2 First measurements up to 1 Grad (SiO_2) TID

We performed a first measurement up to 1 Grad (SiO_2) to test the performance of this technology at the maximum TID level expected at HL-LHC. Figure 1 shows the measured degradation of the maximum drain current ($\%I_{ON}^{sat}$) for both nMOS (left) and pMOS (right). For nMOS transistors I_{ON}^{sat} drops ~15% while for the pMOS decreases by ~80%. The behaviour seen on both nMOS and pMOS matches with the results shown in [4], from the same technology node but different foundry. For both nMOS and pMOS, there is a correlation between the drain current drop and the size of the transistor (smaller sizes are less resilient to radiation). This points out the presence of both RISCE and RINCE [5], further discussed below.

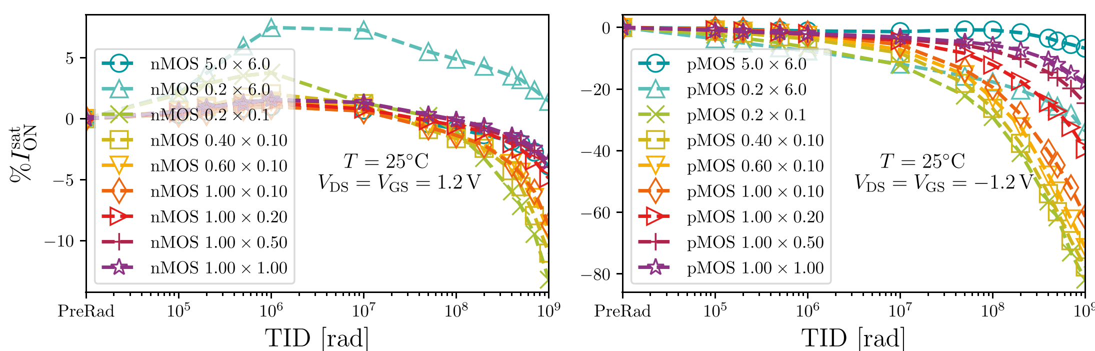

Figure 1. Variation of I_{ON}^{sat} for nMOS (left) and pMOS (right) transistors with widths from 0.2 µm to 5.0 µm and lengths from 0.1 µm to 6.0 µm. The transistors were biased with $|V_{DS}| = |V_{GS}| = 1.2$ V.

3 Transistor dimension related effects

After these measurements up to 1 Grad (SiO_2), we performed a second irradiation on a new TTS1 up to 300 Mrad (SiO_2) followed by 85 h annealing at 100 °C. This allowed us to study in detail the effects of RINCE and RISCE on this 65 nm technology. RINCEs are related with the charges accumulated in the STI which generates an electric field, narrowing the effective channel. nMOS transistors and pMOS transistors are affected differently by TID. In nMOS devices, at the beginning of irradiation, the positive charges accumulate in the STI lowering the threshold voltage and increasing the drain current. As we increase the TID level, the negative charges accumulate at the STI/Si and compensate for the field generated by the trapped holes [9]. These two compensating effects cause the non-monotonic behaviour visible in figure 2. On the other hand, the behaviour of pMOS shown in figure 2 is monotonic. This is due to the fact that both the charges at the STI and at the STI/Si interface have the same positive sign, increasing V_{TH}, and causing the maximum drain current to decrease.

2023 JINST 18 C02036

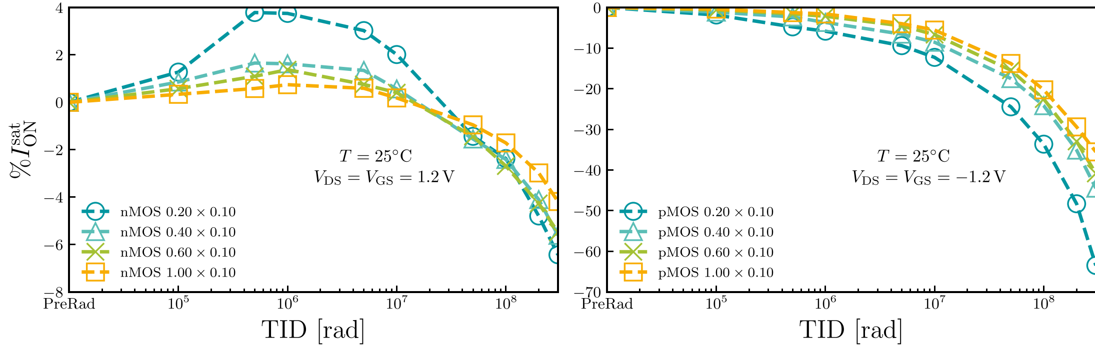

Figure 2. Variation of I_{ON}^{sat} during irradiation of nMOS (left) and pMOS (right) for transistors with width from 0.2 µm to 1.0 µm and length 0.1 µm. The transistors were biased with $V_{DS} = V_{GS} = 1.2\,V$ for the nMOS and with opposite sign of the pMOS.

As expected from studies performed on other 65 nm technologies from different manufacturers [5], this node also shows the presence of RISCEs; making the short channel transistors less radiation hard. RISCE can be described as [10]: (i) an increase of resistivity on the sides of the transistor induced by the accumulation of positive charges in the spacers and (ii) temperature-induced transport of hydrogen ions H^+ from the spacers to the gate oxide. On pMOS transistors, these two processes are visible during irradiation and annealing respectively. In the case of the nMOS, both processes are visible already during irradiation, making its study more difficult. We will focus on the pMOS as it is possible to separate the effect due to irradiation from temperature.

In order to study RISCEs table 1 shows, for a short pMOS device, maximum drain current ($|I_{ON}^{sat}|$), threshold voltage ($|V_{TH}^{sat}|$) and the transconductance (K_U^{sat}) together with their shift from their pre-irradiation value. Variations on the latter one are directly related with variations on the series resistance. The values are extracted before irradiation, at 300 Mrad (SiO_2), and at 25 °C after annealing. As mentioned before, during irradiation, there is an increase on the series resistance due to the positive charges trapped in the spacers. This is visible at 300 Mrad (SiO_2) where I_{ON}^{sat} drops 36% while K_U^{sat} decreases by ~20%. On the other hand, the temperature-activated transport of H^+ in pMOS devices is visible at 25 °C after annealing. At this point, the V_{TH} increases ~175 mV from its value before irradiation while K_U^{sat} almost recovers its pre-irradiation value. This temperature-dependent behaviour matches with the results obtained from similar studies performed on other 65 nm technologies [3].

Table 1. Maximum drain current ($|I_{ON}^{sat}|$), threshold voltage ($|V_{TH}^{sat}|$) and the transconductance (K_U^{sat}) before irradiation together with their shift from their pre-irradiation value, at 300 Mrad (SiO_2), and at 25 °C after annealing for a 1.0 µm × 0.1 µm pMOS transistor.

	PreRad.	300 Mrad (SiO_2)	After Ann.
$\|I_{ON}^{sat}\|$ [µA]	252.0	163.0 (−36.0%)	176.0 (−30.0%)
K_U^{sat} [mA/V]	40.9	32.8 (−19.9%)	38.11 (−6.85%)
$\|\Delta V_{TH}^{sat}\|$ [mV]	275.1	288.8 (13.8)	450.9 (175.8)

2023 JINST 18 C02036

3.1 Leakage current

nMOS devices are known to suffer radiation-induced leakage current increase ($I_{\rm OFF}^{\rm sat}$) [11, 12]. Figure 3 shows the evolution of $I_{\rm OFF}^{\rm sat}$ during irradiation up to 300 Mrad (SiO_2). $I_{\rm OFF}^{\rm sat}$ increase less than an order of magnitude from its pre-radiation value. The minimum size device shows a lower pre-radiation leakage current and higher increase of $I_{\rm OFF}^{\rm sat}$ during the exposure. This leads to assume that transistors with high nominal pre-radiation leakage current will see a lower increase in $I_{\rm OFF}^{\rm sat}$ than transistors with a smaller initial leakage current. Nevertheless it is not possible to correlate the increase of $I_{\rm OFF}^{\rm sat}$ with the length of the transistor, as it could be expected from previous studies [13]. Regarding the post-annealing values, there seems to be a good recovery of the leakage current values, almost going back to their pre-radiation nominal values before TID exposure.

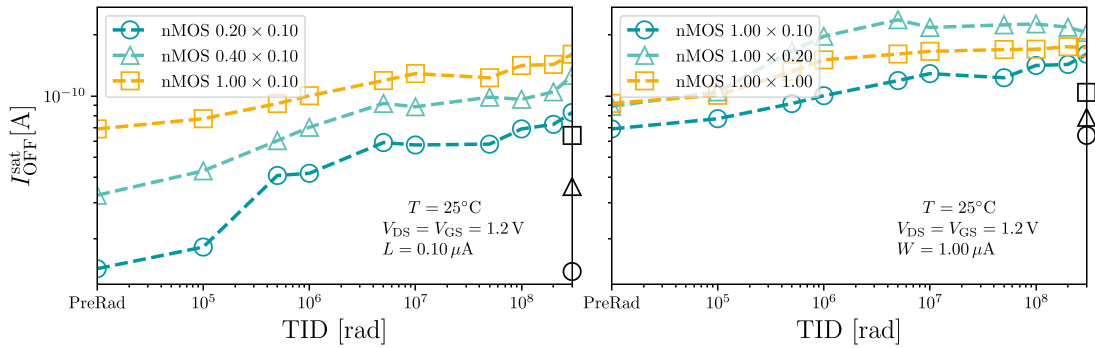

Figure 3. Evolution of $I_{\rm OFF}^{\rm sat}$ during irradiation up to 300 Mrad (SiO_2). On the left, for nMOS transistors with lengths of 0.10 µm and widths ranging from 0.20 µm to 1.0 µm. On the right, for nMOS transistors with widths fix to 1.00 µm and lengths ranging from 0.10 µm to 1.0 µm. The black markers at the end of each plot corresponds to the values of $I_{\rm OFF}^{\rm sat}$ measured after 85 h of annealing at 100 °C.

4 Influence of nMOS bulk bias

In order to study the influence of negative bulk biasing on nMOS devices, we measured the $I_{\rm D}$ vs. $V_{\rm G}$ curves for maximum and minimum size devices, with their bulks biased at 0, −1.2, and −6 V. The results are plotted in figure 4. The extracted values of $V_{\rm TH}$ and its respective shift from the nominal value (at $V_{\rm PWELL} = 0$ V) are shown in table 2. Measurements of nMOS transistors with a pwell biasing of −6 V show an increase of the nominal $V_{\rm TH}$ of ∼260 mV together with a ∼40% drop of $I_{\rm ON}^{\rm sat}$.

In order to test the accuracy of the models, we compared the measurements with the simulations using typical (TYP) corner. The extracted values of $V_{\rm TH}$ and $I_{\rm ON}^{\rm sat}$, together with their shift and percentage of variation from the nominal value (at $V_{\rm PWELL}$ = 0, −1.2 V, −6 V), can be found on table 2. Figure 4 reports the simulated $I_{\rm D}$ vs. $V_{\rm G}$ characteristics in grey color to ease the comparison with the measurements. In the case of the maximum size device, at a bias of −6 V, the measured $V_{\rm TH}$ error w.r.t. the simulation reaches ∼160 mV. Regarding the minimum-size device, for both the $V_{\rm TH}$ and $I_{\rm ON}^{\rm sat}$ there is a significant error compared with the simulation, but on the same

2023 JINST 18 C02036

order of magnitude for the three biases. However, the V_{TH} shift is overestimated for maximum size devices and underestimated for minimum size devices, in both cases not accurate at large reverse biases.

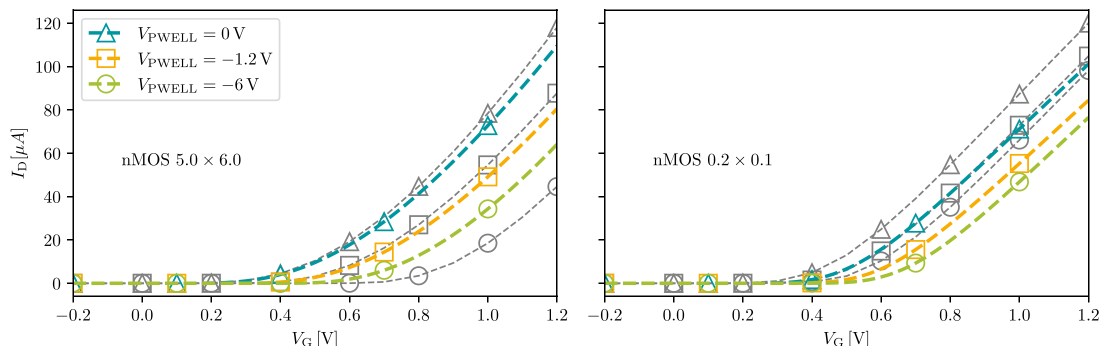

Figure 4. I_D vs. V_G of a maximum size 5 μm × 6 μm device (left) and a minimum size 0.2 μm × 0.1 μm device (right) measured at $V_{PWELL} = 0\,V$ (blue triangles), at $V_{PWELL} = -1.2\,V$ (orange squares) and at $V_{PWELL} = -6\,V$ (green circles). Grey colored curves correspond to their equivalent simulations (TYP corner).

Table 2. Extracted values of V_{TH} and I_{ON}^{sat} from the measurements and simulation (TYP corner) showed at figure 4 for $V_{PWELL} = 0, -1.2\,V, -6\,V$. The respective V_{TH} shift and percentage of variation of I_{ON}^{sat} from the nominal value (I_{ON}^{sat} and V_{TH}^{sat} measured at $V_{PWELL} = 0, -1.2\,V, -6\,V$) is shown in parenthesis with the same color coding as in figure 4.

Size	V_{PWELL} [V]	$\lvert V_{TH}^{sat}\rvert$ [mV]	$\lvert V_{TH,\,TYP}^{sat}\rvert$ [mV]	I_{ON}^{sat} [μA]	$I_{ON,\,TYP}^{sat}$ [μA]
	0	223.4	223.1 (−0.4)	109.5	118.4 (7.75%)
5.0/6.0	−1.2	354.7	352.5 (−2.2)	80.5	87.7 (8.93%)
	−6	487.1	650.5 (+163.5)	64.6	44.6 (−30.4%)
	0	315.2	241.1 (−74.1)	101.2	120.0 (18.60%)
0.2/0.1	−1.2	413.7	321.8 (−91.1)	84.4	104.8 (24.12%)
	−6	483.2	371.3 (−111.9)	76.5	98.2 (28.35%)

5 Conclusion

We presented the irradiation response of TPSCo 65 nm transistors together with the performance degradation study of nMOS transistors under negative bulk biases.

Irradiation results up to 1 Grad (SiO_2) proof the resilience of nMOS transistors to irradiation (max. ∼15% I_{ON}^{sat} drop) while pMOS transistors show similar degradation (max. ∼80% I_{ON} drop) to other 65 nm studies. Irradiation test up to 300 Mrad (SiO_2) and subsequent annealing at 100 °C confirmed the presence of RISCE and RINCE. We measured V_{TH} shifts up to −200 mV, followed by a fast recovery of K_U and V_{TH} after annealing. Small and monotonic radiation-induced leakage current increase on nMOS transistors of less than one order of magnitude. Minimum size devices show a higher increase of I_{OFF} during irradiation.

2023 JINST 18 C02036

Regarding bulk biasing, measurements of nMOS transistors with a pwell biasing of −6 V shows an increase of the nominal V_{TH} of ∼260 mV. For bulk biases down to −1.2 V, the measured V_{TH} matches the simulation. But this is not the case for a bias of −6 V, where the error concerning the simulation reaches ∼160 mV.

This paper offered a preliminary characterization of this technology, but this subject requires further studies. Increasing the number of measured transistors will allow to quantify the device-to-device variability. More irradiation tests will lead to reliable statistics and the understanding of radiation induced variability. Lastly, a more detailed study of performance degradation due to body effect and its correlation with transistor sizing would be beneficial for the designers, to provide an accurate model to assist on analog circuit design.

Acknowledgments

These results are the product of the team-work. Geun Hee Hong and Wenjing Deng are the designers of the TTS and collaborated on the initial measurements. Giulio Borghello and Gennaro Termo took care of performing the irradiation and the annealing, as well as a first processing of the results. Ana Dorda performed pre-radiation measurements, analyzed the data and was the responsible of the measurement and characterization of the transistor performance under several bulk biases.

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2023 JINST 18 C02036