First bent wafer-scale sensor in truly-cylindrical geometry for the ALICE ITS3 detector

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Abstract. An upgrade of the three innermost layers of the ALICE ITS, intended to be installed during the LHC Long Shutdown 3, is under development. The detector concept foresees the usage of curved, wafer-scale Monolithic Active Pixel Sensors. Extensive characterization studies of bent single ALPIDE chips (used for the current ITS), have been carried out to evaluate their performance under the mechanical stress involved in the bending process. These tests on small sensors have opened the way to the investigation of a large scale sensor: a full size demonstrator of a half-layer in a truly cylindrical shape based on so called super-ALPIDE chips. Such activity has required the development of special tools and procedures dedicated to bend and read out the new pixel matrix.

1 Introduction

A pillar of the ALICE upgrade program is the improvement of the Inner Tracking System (ITS2) performance by the replacement of its three innermost layers during the next/third long shutdown of the LHC (LS3) . The proposal is based on a vertex detector consisting of three cylindrical layers composed by curved wafer-scale silicon sensors, with the first layer positioned at 18 mm radial distance from the interaction point [1]. The new detector will present a significant reduction of the material budget, down to only 0.03% of an interaction length, thus improving the spatial resolution of the reconstructed charged tracks.

Currently ALPIDE MAPS sensors, the same as used in the ITS2, are being used for preliminary bending studies. The primary goal is testing the chips performance under the mechanical strain involved in the bending process. Since silicon is a piezoresistive material, when a mechanical stress is applied on the crystal, the internal energy structure changes, causing a change in electron mobility and, in turn, electrical resistance [2]. Moreover it has to be verified that the electronic circuitry on the chips preserve its functionalities after the mechanical stress of the bending.

Under these premises, extensive test campaigns, devoted to the electrical characterization of bent single ALPIDE chips and the evaluation of their performance in a test-beam environment, have been carried out.

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2 Electrical characterization in laboratory tests

The setup for the electrical tests was composed by a single ALPIDE chip wire bonded to a flexible printed circuit (FPC), this component is extended by coupling it to an I-board, used both as noise filter and to release mechanical stress from the setup. The last is connected through a cable to an adapter board (Flex2daq) for the communication between the chip and the DAQ board (Fig.1). The whole setup was placed inside a black box in order to isolate it from any light source.

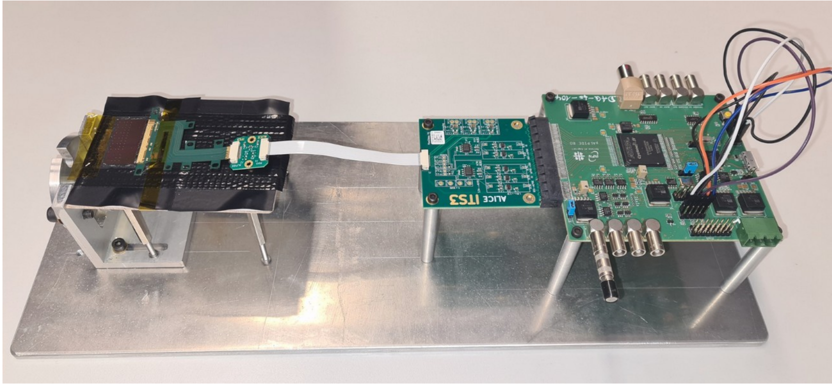

Fig. 1. Setup assembled for the electrical tests with flat ALPIDE.

The tests were performed with the ALPIDE both in flat and bent positions. For the bending procedure a cylindrical jig made of Aluminum was designed and realized to assure a good control of the shape and it is attached to the platform holding the setup (Fig. 2 left). The radius of the jig is r=18 mm, this corresponds to the intended radius for the innermost layer of the ITS3. The chip is positioned on top of this tool, such that the bent axis is parallel to its long side and is bent carefully forcing it to follow the curved shape by using a piece of kapton foil. Starting at one of the short sides and then moving on towards the other one in a rolling fashion, the chip bends gradually and is fixed in the final position by screwing the kapton to the jig at both extremes (Fig. 2 right).

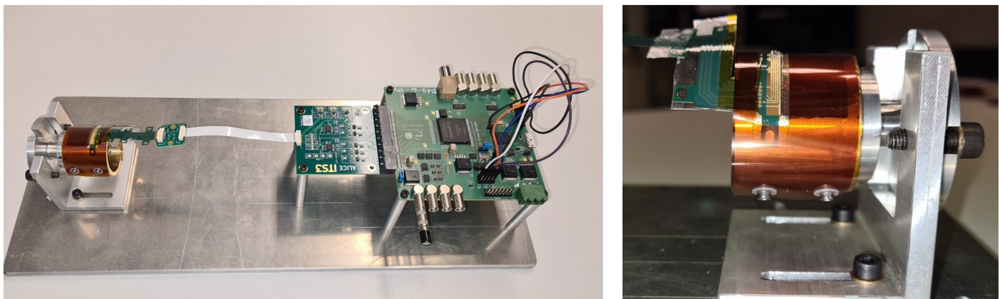

Fig. 2. (left) Setup assembled for the electrical tests with the ALPIDE bent over a cylindrical jig. (right) Closed view if the ALPIDE bent along its long side over the cylindrical jig and held in position with a kapton foil screwed at the edges.

The ALPIDE chip was characterized mainly in terms of threshold and fake-hit rate.

The charge threshold is the key parameter leading the chip performance. It is defined for every pixel by three front-end parameters: ITHR, VCASN and IDB. The effective value is increased by increasing ITHR or IDB and decreased by augmenting VCASN. For a given set of these parameters, pixel charge threshold can be determined using the analogue

pulsing. The measurement consists in injecting N_{inj} times a range of test charges Q_{inj} via pulsing capacitance C_{inj} such that

$$Q_{inj} = C_{inj}\,(VPLSE_HIGH - VPLSE_LOW) \qquad (1)$$

VPLSE_HIGH and VPLSE_LOW maximum value is 1.8 V and are set via on-board 8-bit DACs. For each test charge Q_{iinj} , out of N_{inj} injections, N^{i}_{hit} pass the threshold i.e. result in pixel hits. The plot of N^{i}_{hit} / N_{inj} as a function of Q^{i}_{inj} is often referred to as s-curve measurement as its shape resembles the letter S. The threshold is defined as charge at which pixel fires in 50% of cases (injections).

The fake-hit rate of a sensor is defined as the number of hits per pixel per event in absence of any external stimulus. It is measured by sending a number of triggers (N_{trg}) to the chip without providing any charge injection, and recording the number of hits N_{hits}

$$FHR = N_{hits} \,/\, (N_{pix} \cdot N_{trg}) \qquad (2)$$

where N_{pix} is the number of pixels in the sensor.

A similar test was done by bending the chip along its short side [3]. In this procedure, the long edge, hosting the bonding pads and the periphery logic, was glued onto a carrier board. The bonding area remained flat, and the rest of the sensor was left unattached and lightly compressed between two layers of polyimide film, which were tied to two lateral wheels that could be moved along the bending direction (Fig. 3). Following this method the chip was bent up to curvature radius of less than 18mm.

Here, the sensor was also characterized in terms of threshold and fake hit rate before and after bending. The distribution of thresholds over the pixel matrix, showed only negligible variations between both positions.

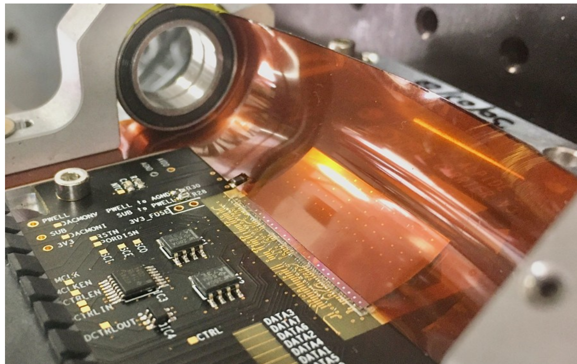

Fig. 3. ALPIDE sensor bent along the short edge to a radius of 18 mm.

3 Performance of bent ALPIDEs in a test-beam

In a previous study [3], curved ALPIDE MAPS have been characterized in a test beam environment, using 5.4 GeV electrons. In this case, a sensor was bent along the short side as described above and taken as device under test. It was placed between reference flat detector planes in a telescope configuration.

An important component of the analysis was the measurement of the detection efficiency as a function of the beam position and local inclination angle. The inefficiency as a function of threshold for different rows and incident angles can be seen in figure 4.

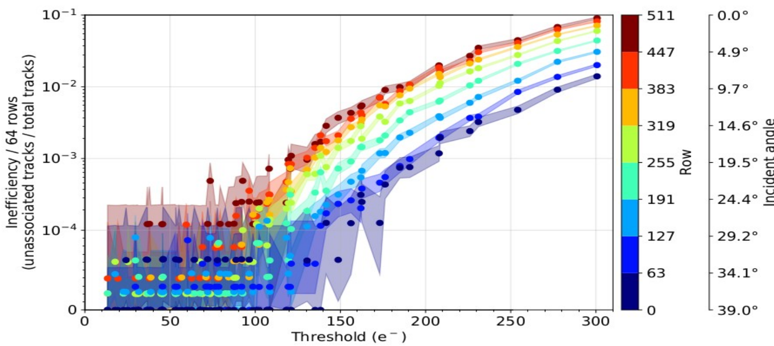

Fig. 4. Inefficiency as a function of threshold for different rows and incident angles. The dark circles represent the calculated efficiency and the shaded areas the statistical uncertainty. Each data point corresponds to at least 8k tracks.

For thresholds above 100 electrons, which is the nominal operating point of ALPIDE, the efficiency increases with increasing beam incident angle, this is, decreasing row number. Below 100 electrons, the inefficiency is generally lower than 10^{-4}, showing that the sensors maintain their excellent performance after bending to radii of about 2cm, with detection efficiencies above 99.9% at typical operating conditions.

More recently, during a beam test campaign realized at CERN SPS facility in July 2021 a beam telescope featuring six flat ALPIDE chips as reference detectors was used to measure the performance of other six ALPIDE chips, bent at the foreseen ITS3 layer radii, composing the so called micro-ITS3. A picture of the resulting DUTs, forming the μ-ITS3 and a top view of the DUTs mounted within the ALPIDE beam telescope can be seen in figure 5.

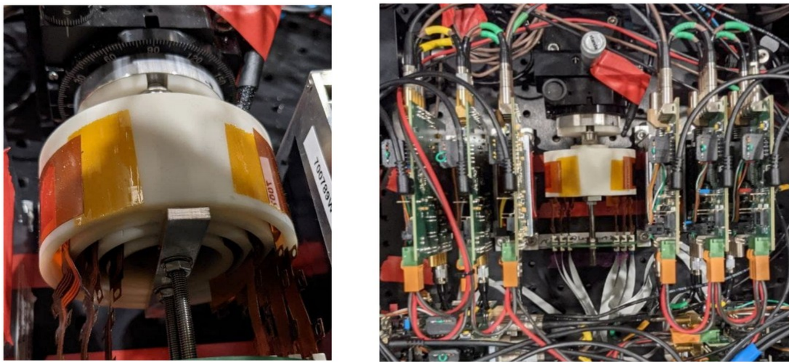

Fig. 5. (left) Image of the six DUTs used in the test-beam campaign, bent over three cylindrical jigs at different radii, forming the μ-ITS3. (right) Top view of the bent DUTs mounted within the ALPIDE beam telescope.

4 Beyond the single-ALPIDE

An important part of the R&D activities dedicated to the detector performance upgrade of the Inner Tracking System is focused on the prototyping and testing of bending techniques, the mechanics, and the integration into the detector.

A full size (1:1 scale) demonstrator of a half-layer in a truly cylindrical shape has been produced, based on so called super-ALPIDE chips. Wafer-scale bending tests have also been carried out on dummy silicon wafers. A bending technique was developed and

bending down to a radius of 18 mm can be carried out in a reliable and repeatable way. For this purpose, a dedicated tool was designed (Fig. 6). In this case a tensioned mylar foil is attached by one extreme to a cylindrical mandrel of the desired radius. The silicon wafer is placed between both objects, then the mandrel is rotated, allowing the mylar to wrap it down and to bend the wafer around it. The mechanical components for the bending and electrical assembly of this demonstrator, as shown in figure 6, are being completed in 2022. Once assembled, the detectors will be characterized in the laboratory and eventually on a test-beam.

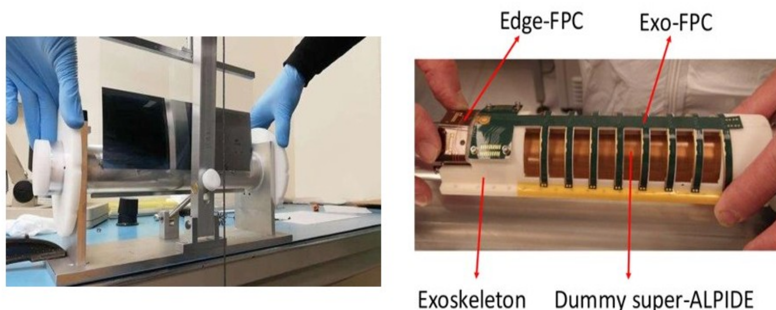

Fig. 6. Mechanical tool developed for bending the super-ALPIDE (left) and main components designed for the electrical assembly (right).

Forward activities will be dedicated to the testing and characterization of the newest chip designs, specifically the test chips contained in the MLR1, which stands for Multi Layer Reticle 1. This is the first submission of a chip fabricated with the TowerJazz 65nm technology, featuring many devices for technology exploration, including transistor test structures for radiation hardness, various diode matrices for charge collection studies, and both digital and analogue test structures.

5 Conclusions

Looking towards the realization of the new ITS3, which envisages a detector consisting of three truly-cylindrical layers, composed only by wafer-scale silicon sensors, several test with bent ALPIDE chips have been carried out, to evaluate the consequences of bending. These studies have included the electrical characterization of a bent single ALPIDE chip, through the measurement of the main parameters steering the chip functioning. On the other hand, the evaluation of in-beam performance has been realized in different test-beams, including the one carried out at CERN SPS with a telescope of six flat ALPIDE chips as reference detectors used to measure the efficiency of other six ALPIDE chips, bent at the foreseen ITS3 layer radii, composing the so called micro- ITS3.

The results obtained up to now, exhibit the expected behavior of the bent chips with respect to that when they are flat, demonstrating that the functionalities of the ALPIDE are not affected by the curvature effect.

References

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