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Full Length Article

TDCpix pixel detector ASIC with 100 ps time stamping

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ABSTRACT

The TDCpix pixel read-out ASIC contains 1800 pixels arranged in 40 columns and 45 rows with the dimension of 300 μm x 300 μm. Each pixel contains a preamplifier and shaper circuit with a dynamic range of 0.8 to 10 fC and a rise time of 5 ns, followed by a Leading-Edge discriminator with Time-over-Threshold correction. The discriminator outputs of each pixel are connected to time-to-digital converters (TDC) measuring the time when the input signal has exceeded the threshold and the pulse width with a binning of 97 ps. The electronics noise of pre-amplifier/shaper is 170 e^- or 2.7 mV rms with a gain of 65 mV/fC. The jitter of the entire processing chain for an electrical input signal of 2.4 fC is lower than 60 ps rms. The ASIC has been designed to work in radiated environments of 6 * 10^4 Gray per year and 2 x 10^{14} 1 MeV neutron equivalent cm^{-2}.

1. Introduction

The TDCpix is a read-out ASIC for hybrid pixel detectors with emphasis on timing [1,2]. It was designed for the read-out of the GigaTracker (GTK) sensors of the NA62 experiment at CERN [3,4]. The GTK detector has three tracking stations, each containing a hybrid pixel module placed in vacuum and orthogonally across a high intensity hadron beam. Each tracking station time stamps the hits of all incoming particles with a time resolution better than 200 ps RMS. The silicon pixel sensors are 60 mm × 27 mm and 200 μm thick. The pixel size of 300 × 300 μm^2 provides the required position resolution. Each sensor is read out by 2 × 5 TDCpix chips, connected by flip-chip bonding to the sensor. The peripheral regions of the chips extend out of the sensitive area by 6.7 mm.

The TDCpix has been in use since 2014 in the GTK of NA62, achieving a timing resolution of 115 ps RMS [3]. At the time of production the TDCpix was the first pixel read-out ASIC featuring such time resolution. It is noted that the timing resolution ultimately achievable with the TDCpix depends also on the pixel sensor connected to it. The sensor, the TDCpix and their interplay contribute to the final timing resolution error. The characteristics of the sensor (material, geometry, bias voltage) bonded to the TDCpix dictate if the contribution to the error from the chip dominates over the one of the sensor or vice-versa.

This paper aims at giving a comprehensive description of the design of the TDCpix ASIC and of its development process, together with key results and performance measurements obtained during the validation of the chip. The remainder of this introduction provides an overview of the chip main characteristics and a description of the prototyping and development phases. Section 2 describes in details the architecture of the TDCpix ASIC and the design of the building blocks, as well as their integration in the final die. Section 3 provides experimental results and performance figures. Section 4 provides a discussion of some lessons that were learned, alternative design choices deserving consideration in retrospective and a description of the fundamental mechanisms limiting the timing resolution achievable with the TDCpix chip in combination with planar silicon pixels.

1.1. Overview of TDCpix

Fig. 1 shows a simplified block diagram of the TDCpix chip. The chip contains 1800 front-end channels arranged in a matrix of 40 columns of 45 pixels. The dimensions of the pixel channels match the ones of the sensor pixels (300 × 300 μm^2). Each pixel column is connected to a TDC bank. The ASIC is read-out by four read-out processors. Fig. 2 shows the top-level layout with overlaid indications of the main sections. Table 1 gives a summary of its main characteristics.

The architecture completely decouples the sensitive analog front-ends in the pixel matrix from the digital TDCs, read-out processors and serialisers circuits of the End of Column (EoC) region. Each pixel channel of the matrix contains an integrating amplifier followed by a threshold discriminator and a differential line driver. Only the discriminated pulses are transmitted to the peripheral circuits on dedicated differential lines, one per pixel. There are no synchronous digital circuits in the pixel matrix. In this way, the design provides a sharp separation between sensitive analog and noisy digital domains, both for

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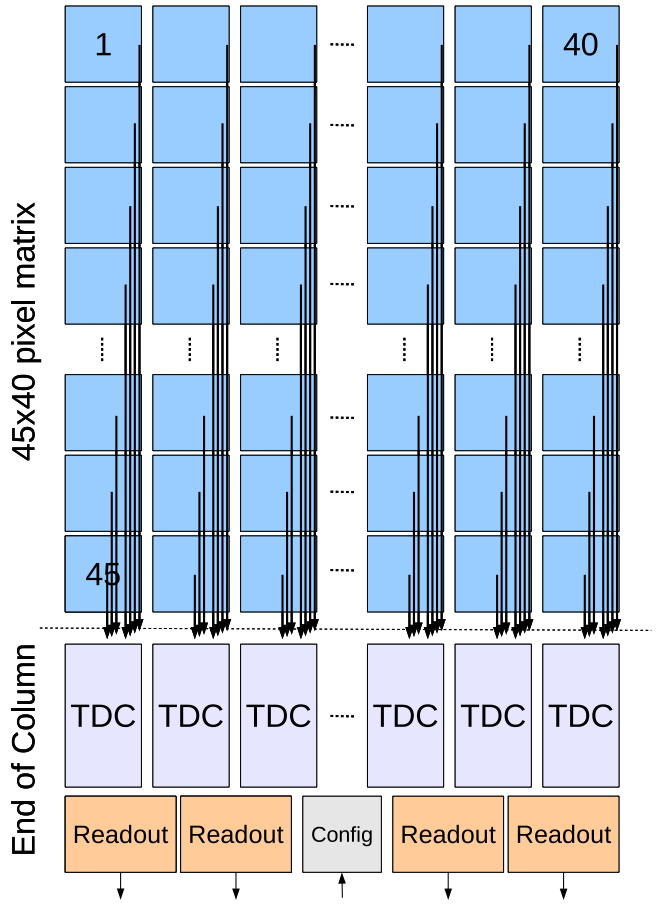


Fig. 1. Block diagram of the TDCpix ASIC.

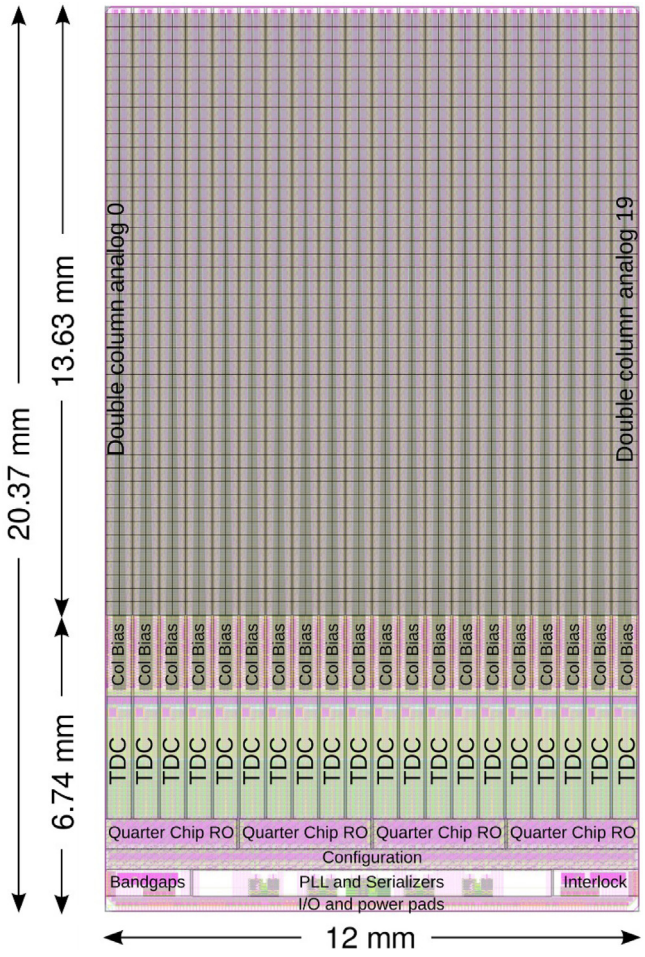


Fig. 2. Layout of the TDCpix ASIC.

power routing and signal routing. Biasing DACs providing the voltage references that are needed by the pixels front-ends are implemented at the end of columns.

The EoC region contains an array of Time to Digital Converters (TDCs) with 97 ps bin width and Time over Threshold (ToT) capabilities. The internal timing references in the TDCs are generated by 20 independent Delay Locked Loops (DLL), shared by the TDCs of adjacent column pairs. Data aggregation and formatting are made in four digital Quarter Chip read-out Units. Each one serves 10 columns of pixels and transmits the data off chip on a 3.2 Gb/s serial link, for a total output rate of 12.8 Gb/s over 4 high speed output interfaces. The data transmission line clock is generated by an on-chip Phase Locked Loop (PLL) circuit. Alternative serial and parallel read-out interfaces operating at lower bit rates are also available.

The periphery also includes on-chip band-gap references and a temperature sensing circuit. The control of the pixels, biasing DACs, TDCs, read-out blocks, serial transmitters, PLL and auxiliary blocks is handled by distributed custom configuration logic, interfacing to the external world by serial synchronous communication at 320 Mb/s on differential I/O ports. The nominal frequency of the main input clock is 320 MHz.

The data acquisition works in a continuous fashion. After an initial configuration phase the chip is continuously sensitive and the read-out is entirely data driven. The discrimination of a hit above threshold in a pixel is an event which initiates the transmission of a data packet with hit position and timing information, without the need of a trigger. The design can sustain pixel hit rates up to 130 MHz/cm^2 or 212 MHz over the full matrix.

Table 1
Specifications of the TDCpix chip.

Number of pixels per chip	1800 = 45 × 40
Size of pixels	300 µm × 300 µm
Active area	12 mm × 13.5 mm = 162 mm^2
Dynamic input range	5000–60 000 e^-/0.8–10 fC
TDCs	360 dual TDCs, 97 ps binning
Read-out	Trigger-less, 12.8 Gb/s
Max. hit rate per ASIC	212 MHz, 130 MHz/cm^2
Power dissipation	2.6 W
Total dose in 1 year	6×10^4 Gy
Neutron flux in 100 days	2×10^{14} 1 MeV neutron equivalent cm^{-2}

The TDCpix chip is 12 mm × 20.37 mm and it is implemented in 130 nm IBM/GF CMOS technology. The operating supply voltage is 1.2 V. The total power consumption of the pixel matrix is about 0.6 W corresponding to a power density of 0.45 W/cm^2 in the active region. The peripheral circuits consume 2 W corresponding to a power density of 2.5 W/cm^2 over the EoC region. The power consumption density averaged over the full chip area is about 1 W/cm^2. The pads for the supplies and communication are available as wire bond pads on the south edge of the ASIC, whereas the 1800 signal inputs are applied to an array of pads over the pixels for flip-chip bump bonding interconnection to pixel sensors.

A prototype demonstrator circuit containing all principal building blocks with the exception of the serializer has been produced and tested before the final size and full functionality TDCpix ASIC was developed.

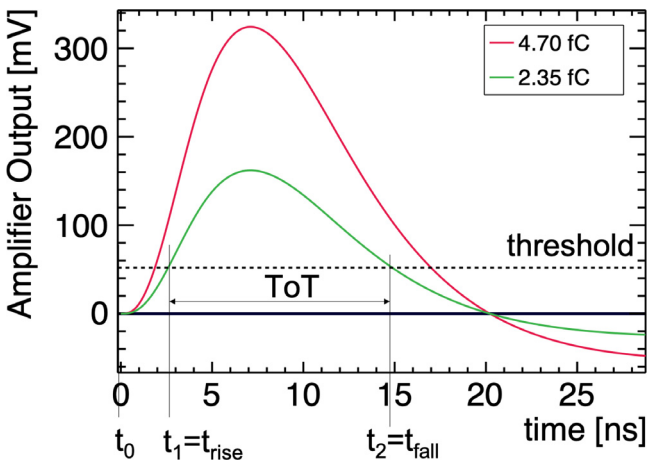


Fig. 3. Illustration of the time-walk effect and of the Time-over-Threshold measurement. The time of when the discriminator threshold is exceeded on the rising edge of the signal is referred to as t_1. The time the signals decreases below the threshold during the falling edge is referred to as t_2. The actual particle arrival time compensated using t_1 and t_2 is referred to t0. The difference between t_2 and t_1 is the Time-over-Threshold (ToT) width.

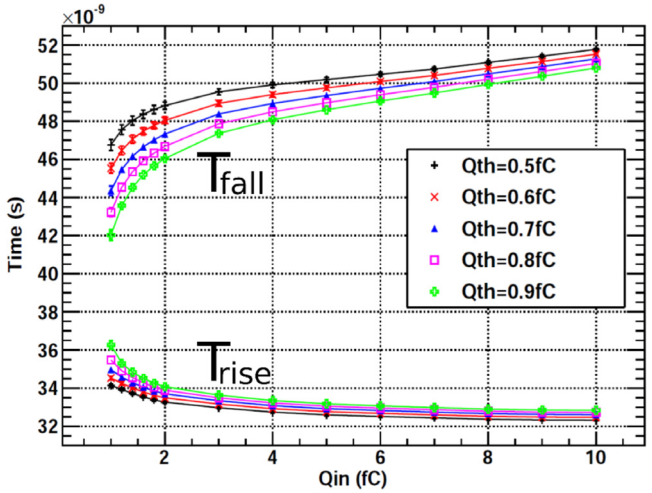


Fig. 4. Timing of the rising and falling edges as a function of input charge.

1.2. Principle of operation of the timing functionality

As illustrated in a simplified way in Fig. 3, the time delay of the rising and falling edges of the discriminated pulse with respect to the particle hit change with the total charge of the input pulse integrated by the front-end. The plot in Fig. 4 shows timing measurements of the rising and falling edges as a function of the input charge. These measurements were made on the prototype circuit demonstrator. It is noticed that the delay between particle hit and rising edge can vary by more than 2 ns in the range of interest. Therefore an accurate determination of the particle hit timing requires a compensation of the time-walk of the discriminated signal edges related to the randomness of the collected input charge.

The Time Over Threshold (ToT), the duration of the time interval between the rising and falling edges, is a monotonic function of the charge. Therefore, the input charge can be estimated knowing ToT and the time-walk of the rising edge compensated, determining the timing of the hit with better accuracy. It is noted that the Time-over-Threshold measurement also provides an estimate of the deposited charge.

The TDCs in the EoC of the TDCpix chips are designed to time stamp both the rising and the falling edges of the discriminated pulses, with respect to the time reference provided by the main input clock. The Time Over Threshold is calculated and inserted in the hit data packet.

1.3. Challenges and development phases

The development of the TDCpix chip was divided in two phases. The first phase addressed the most challenging requirements and served as validation of the key concepts. Most of the building blocks thought to be critical for the target timing performance were integrated and tested in a small scale TDCpix Prototype chip. This first chip addressed in particular the following points:

- the performance of the analog front-end for fast timing resolution, time-walk and immunity to noise;
- the effectiveness of techniques foreseen to isolate the sensitive front-ends from the noise generated by the fast switching circuits of the periphery;
- the possible detrimental effect on the timing resolution of the transmission of the discriminated pulses over long lines from the pixels to the TDCs at the periphery.

Thus, in addition to test structures for most of the critical sub-blocks, the prototype integrated a full length column of 45 pixels arranged in a folded layout and connected to a prototype TDC via transmission lines with a maximum length of 15 mm, equal to the one needed for the final chip.

The 3.2 Gb/s output serialisers were notably not implemented in the TDCpix Prototype. The read-out of the chip was done with serial transmitters operating at 320 Mb/s only and using a simplified read-out processing logic.

The experimental evaluation of the prototype validated the simulation models, verified the key building blocks and showed a measured performance exceeding the specifications [5–8]. This ensured that the timing performance was achieved by the front-end and it was not degraded by coupled noise nor by the significant length of the pulse transmission lines.

Due to the increase of the rise time of the signal at the receiving end in the EoC, it also became evident that an acceptable performance could be maintained only if the level of noise in the larger and more complex final ASIC would remain as low as in the prototype. Additionally, due to the reduced set of circuits, die size and given the availability of a pad ring with pads on all the four sides of the die, the supply distribution in the TDCpix Prototype was simpler than it was expected for the full-scale chip. The final TDCpix chip has to allow abutting on three-sides and thus power supply and I/O pads can be implemented only at one side of the die. The power integrity performance and the risk of coupling noise from the digital periphery to the analog front-ends of the pixels could not be addressed in thorough manner with a small scale prototype.

It was concluded that a second prototype of intermediate size and with a partial set of features would not yield any significant additional information, nor address reliably the concerns on noise immunity and power integrity when integrating a large matrix and a fully featured periphery.

Therefore, the second stage of the project targeted directly the design and production of the full scale final ASIC (TDCpix), integrating all the final features and addressing all the physical implementation requirements.

2. Implementation

2.1. Architecture and data flow

Fig. 5 shows the full block diagram of the TDCpix. The top left block in the figure show the 45 pixels in a column containing the front-end, discriminators and transmission line drivers. Each column is connected to a 4-bit bias DAC, setting the DC operation points of the front-end, and an 8-bit threshold DAC, setting the global threshold range of all

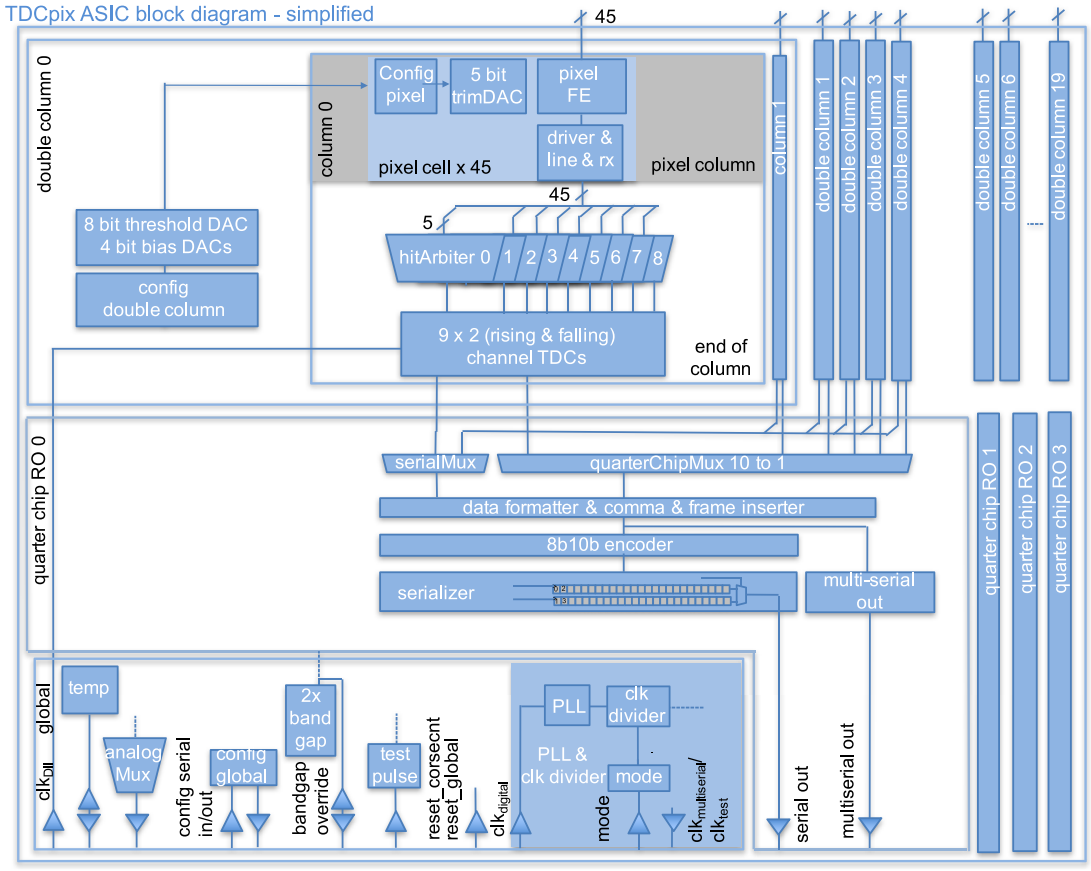


Fig. 5. Block diagram of the TDCpix ASIC.

pixels in that column. Each pixel can be individually configured with a 5-bit fine range discriminator threshold DAC and binary configuration settings allowing to mask pixels and to set the polarity of negative or positive input signals. Each of the 45 pixels in a column has a line driver connected to an up to 15 mm long transmission line, depending on the location of the pixel along the column.

The transmission lines are routed to the end-of-column (EOC) region at the bottom periphery of the ASIC outside the pixel matrix. In order to minimise the needed silicon area each 5 pixels are connected to one dual channel TDC, each channel measuring rising and falling discriminator outputs times, respectively. Thus, for the 45 pixels in one column 9 dual channel TDCs are used, and 360 dual channel TDCs are implemented in the full TDCpix ASIC. The 5 pixels sharing one TDC are connected to a hitArbiter circuit which forwards the address and the digital signal of that channel whose discriminator pulse arrived first to the TDC. As long as the signal of the first channel is above threshold all other four inputs are blocked. However, the address of the blocked signals are registered and are forwarded to the read-out for applications where hit position without timing information can be useful. As a consequence, the timing of the blocked signals cannot be read out, but the addresses of the blocked channels are known. In the NA62 Gigatracker application, the loss of timing data due to the sharing of TDC channels by 5 pixels is less than 0.6% assuming Poisson distributed signal arrival times and 132 MHz/TDCpix hit rate.

The TDC data of one column are multiplexed into a column FIFO. Each 10 columns are connected to one of four quarter-chip read-out processors. The quarter-chip reads the column FIFOs in a round robin based fashion, formats the data and applies an 8b10b encoding scheme before the 3.2 Gb/s serializer sends the data off chip. The quarter-chip data encoder inserts each 6.4 μs a frame word containing a frame counter which extends the dynamic range of the TDCs of 6.4 μs to 1718 s.

The TDCpix ASIC contains a temperature probe which acts on a binary output once a predefined temperature threshold has exceeded and contains on-chip band-gap reference cells which allow operation without the need of external reference voltages. Test pulses can be transmitted to each single pixel either by programming the control interface or via an external input. A configurable clock manager allows the operation of the ASIC with only one single input clock of 320 MHz. All other internal clocks are derived from this master input clock.

2.2. Front-end

The block diagram and schematic of the in-pixel circuits are shown in Figs. 6 and 7 respectively. The front-end signal processing chain consists of a preamplifier, a differential amplification and integration stage, a three-stage discriminator and a differential transmission line driver to transmit the discriminated pulse to the End of Column. The preamplifier, differential amplifier and integration stage contribute to the overall shaping function with roughly the same time constants implied by the bandwidth limitation of those blocks which are optimised for low power. In consequence, the overall response of the preamplifier and shaper corresponds to a CR-RC3 shaping function.

The front-end circuit can process either positive or negative polarity signals from p-on-n or n-on-p type detectors. Any pixel input not connected to a sensor does not affect the performance of other pixel channels.

The peaking time is around 5 ns and the overall gain is 65 mV/fC.

The simulated Equivalent Noise Charge is given in Fig. 8 as a function of the capacitance of the sensing junction and for a maximum input leakage current of 20 nA. For a nominal pixel capacitance of 250 fF, the calculated ENC is below 200 e^-.

The INL is better than 10% in the range 0 to 5 fC.

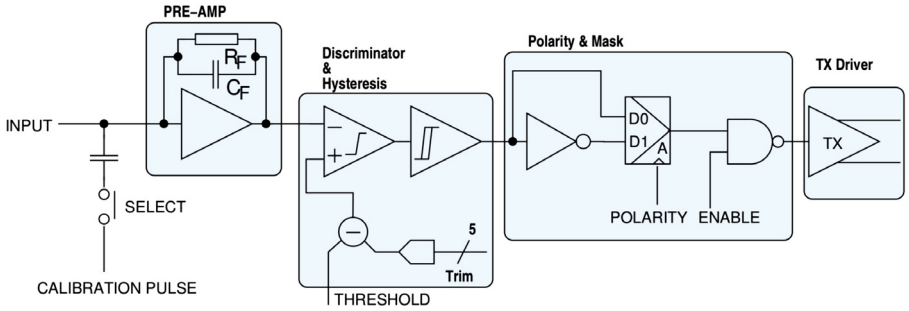


Fig. 6. Block diagram of pixel cell.

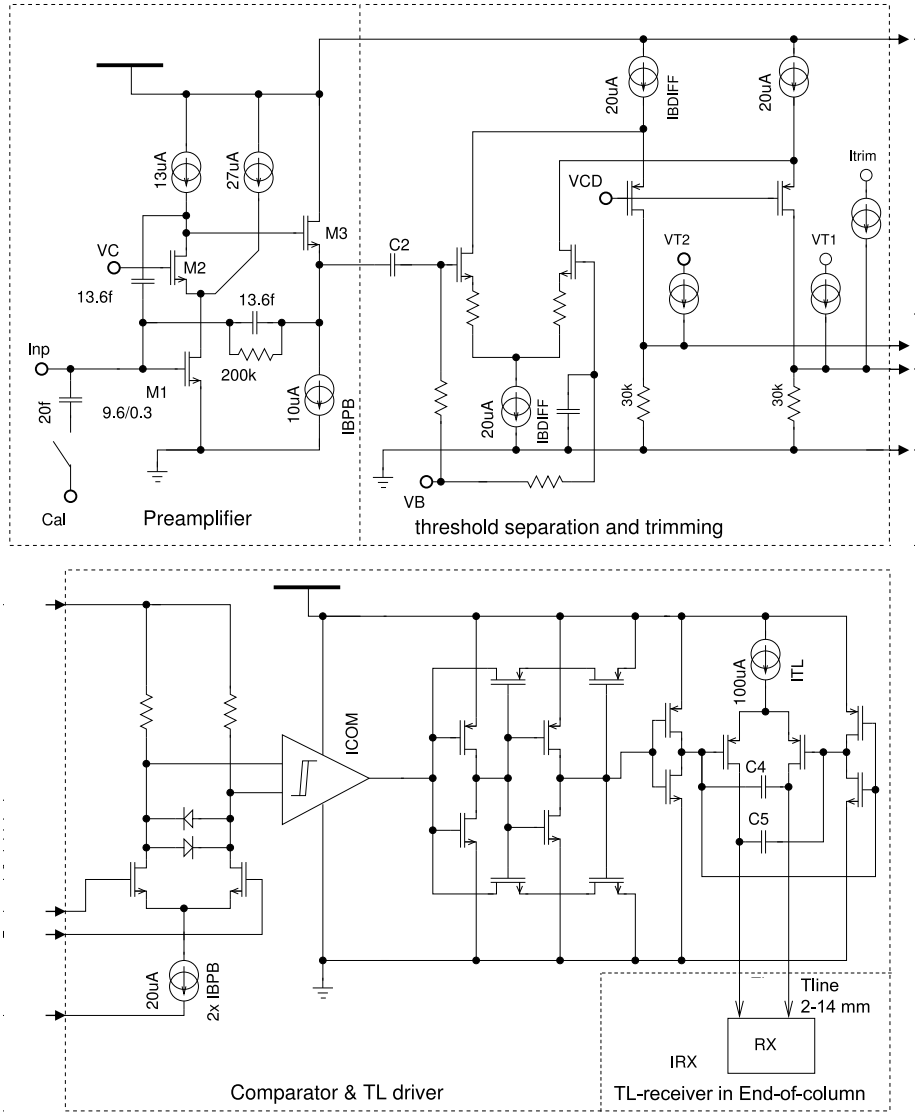


Fig. 7. Schematics of TDCpix front-end (divided in two rows for better readability).

The sensitivity of the gain with respect to analog supply variations is <1%/100 mV for 1 fC input pulses. The power supply rejection ratio under nominal biasing conditions is shown in Table 2.

A trade-off between maximising signal collection and limiting the cross-talk to neighbouring pixels sets the requirements on the input impedance of the preamplifier. An inter-pixel capacitance of 50 fF was estimated due to the geometry of the pixel sensor. The input impedance of the preamplifier is in the range of 1 to 2 kΩ within a 1 GHz bandwidth. This is sufficiently low to maintain an efficient collection of charge in the front-end, while at the same time limiting the cross-talk between neighbouring pixel channels to less than 3%.

Table 2
Power supply rejection ratio under nominal biasing conditions.

Frequency range	PSRR [dB]
10 Hz to 10 kHz	40
10 kHz to 1 MHz	20
1 MHz to 10 MHz	2
10 MHz to 500 MHz	10
500 MHz to 1 GHz	10

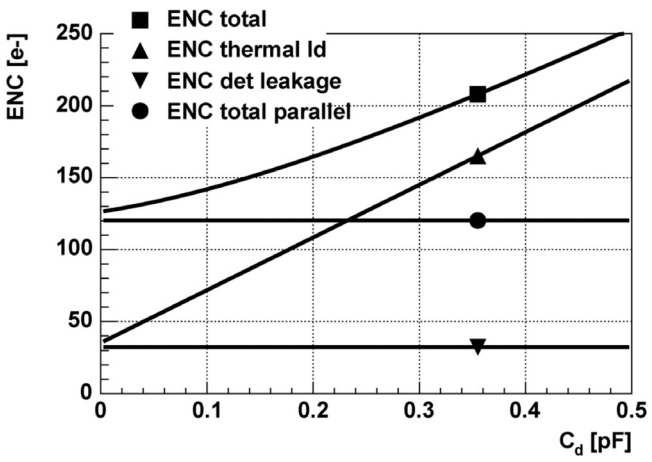


Fig. 8. Calculation of the ENC performance of the TDCpix front-end as a function of input capacitance for 40 μA input transistor bias and assumed maximum detector leakage current of 20 nA.

Extensive analog simulations were made to characterise the timing behaviour at the output of the discriminator. Transient noise simulation of the full signal processing chain including front-end and discriminator showed a jitter of the rising edge of the discriminator of the order of 30 ps RMS, for a constant input signal charge of 3 fC. This agrees well with the expectation based on the rising time of the discriminator input and the ENC value.

The delay between an input pulse and the discriminator transition depends on the input pulse charge. For input signal charge from 1 fC to 5 fC and a typical threshold setting of 0.7 fC, the duration of the discriminator pulse, namely the Time Over Threshold, ranges from 5 ns to 15 ns. Under the same assumptions, the time-walk of the rising edge, i.e. the variation of delay between the input pulse and the asserting transition of the discriminator, is less than 3 ns.

Two distinct input pulses with the same charge of 2.4 fC are resolved if their time separation is at least 18 ns. In the limiting case of an input pulse of 80 fC followed by a typical pulse of 2.4 fC, the latter gets distinctly resolved if the separation is of 250 ns.

The complete analog section (preamplifier, shaper and trim DAC) consumes 140 μA. The digital section, including the discriminator the transmission line driver and the corresponding line receiver, consumes 160 μA. The current consumption in the analog part is driven by the input device and defined by the noise and speed requirements. The current consumption in the transmission line drivers is defined by the jitter and signal slope specifications based on current signals to provide minimum interference to the pixel front end.

The rather low value of the input capacitance allowed the usage of a simple buffered cascode topology for the preamplifier stage. This offers a very large bandwidth (1 GHz gain-bandwidth product) at an affordable power consumption. The dimensions of the NMOS-input transistor are 9.6 μm × 0.3 μm. The open loop gain is ≈45 dB. The input transistor is loaded with a common source amplifier with source degeneration with a resistive (200 kΩ) and capacitive feedback (transimpedance configuration). The resulting closed-loop gain of the preamplifier is 30 mV/fC. The nominal bias current of the input stage is 40 μA for a power consumption of 60 μW.

The threshold is applied as a differential voltage offset VT_1-VT_2 in the differential shaping stage, ahead of the comparator stage. The first stage of the comparator translates from differential to single-ended, makes the crossing from the analog to digital supply domain and provides hysteresis. A differential comparator stage improves the rejection of common signal noise on the digital supply rails and provides good threshold uniformity. The following 3 stages of the comparator provide high sensitivity and very high switching speed. The total power consumed by the discriminator is 50 μW.

The threshold voltage is generated from an internal DAC in a range from 0 to 376 mV with 256 steps of 1.46 mV. This corresponds to input charge range 0 fC to 5.4 fC and threshold resolution of 0.02 fC. The typical threshold setting is at 0.7 fC. The threshold spread before trimming is expected to be less than 15 mV RMS (0.2 fC RMS). Each pixel has a local 5-bit threshold trim DAC allowing fine tuning of the pixel threshold in the range 45 mV–180 mV (0.6 fC to 2.6 fC).

The discriminated signals are transmitted to the TDC circuits at the EoC region using differential transmission lines. The cross-coupled capacitors C4–C5 of 1 pF in the transmitter switching pair are used to enhance the edges of the differential current signal (100 μA nominal). The differential current signal is sensed in the pixel receiver at the EoC across a terminating resistor of 1.5 kΩ and converted to single ended CMOS signal.

The transmission lines are built with metal traces surrounded by conducting strips and vias connected to digital ground, acting as shields. The routing utilises minimum width and spacing. The resistance of the line traces reaches 1.3 kΩ in the case of the maximum length of about 15 mm. This is comparable to the resistance of the line terminating resistor. Therefore, for the maximum length lines, the amplitude of the signal reduces of about 50%. This amplitude loss does not degrade the timing performance as the clock-free in-matrix electronics propagates the signals with a minimum of noise added.

2.3. Time-to-digital converter (TDC)

2.3.1. Overview of TDC and sub-components

For the TDC it was important to design an architecture scalable over the pixel matrix columns and injecting a minimum of noise towards the analog front-end. Thus, a delay-locked-loop (DLL) based circuit has been selected with a reference clock frequency of 320 MHz [9]. The DLL has 32 delay elements dividing the clock period 3.125 ns into 32 timing bins of 97.7 ps each. The DLL acts like a 32-bit shift register filled with 16 '1' followed by 16 '0' for 50% duty cycle. Every TDC time bin of 97.7 ps, the two edges advance by one position. Thus, registering the 32 bit output of the DLL allows the time measurement with a binning of 97.7 ps. At the same time, this means that only two bits per DLL toggle their values, reducing the digital noise. Digital registers store the value of the DLL state only when a signal needs to be registered and are otherwise inactive.

The TDCpix chip has an array of 20 identical TDC blocks (see Fig. 2). These are located at the end-of-column region of the ASIC, immediately below the pixel matrix region. They receive the discriminated hit signals from the pixels. Each TDC block processes the signals from 2 adjacent columns, namely 2 * 45 = 90 pixels. A block diagram of one of the TDC units is shown in Fig. 9. The main functions of the circuit are the generation of data words including a time stamp code and a ToT field for each incoming hit and the buffering of these words waiting for their read-out by the quarter-chip read-out circuits. The timing codes are generated by storing the value present on the 32-bit bus driven by the DLL circuit in dedicated registers at the time of arrival of rising and falling edges of the discriminated hit pulse.

The main data flow is from the top to the bottom of the block diagram. The inputs of the discriminated pulses are shown on the top side of the unit. The main digital read-out clock is labelled Sync clk. The DLL input clock, which acts as timing reference is labelled DLL clk and it is independent from 'Sync clk'. Hit pulses are received by 18 hitArbiters, 9 per column. These are digital multiplexing units used to share the timing circuits between groups of 5 pixels. The hitArbiters include asynchronous, synchronising and clock synchronous logic circuits. They buffer and forward the hit pulses to the timing code latching registers and detect collisions of pulses inside a pixel group. They also act as synchronisers, generating latch enable signals synchronous with the main read-out clock upon detection of an input pulse.

The 32-stage DLL circuit is the fine resolution time code generation unit. The DLL is a custom layout circuit. The DLL is monitored and

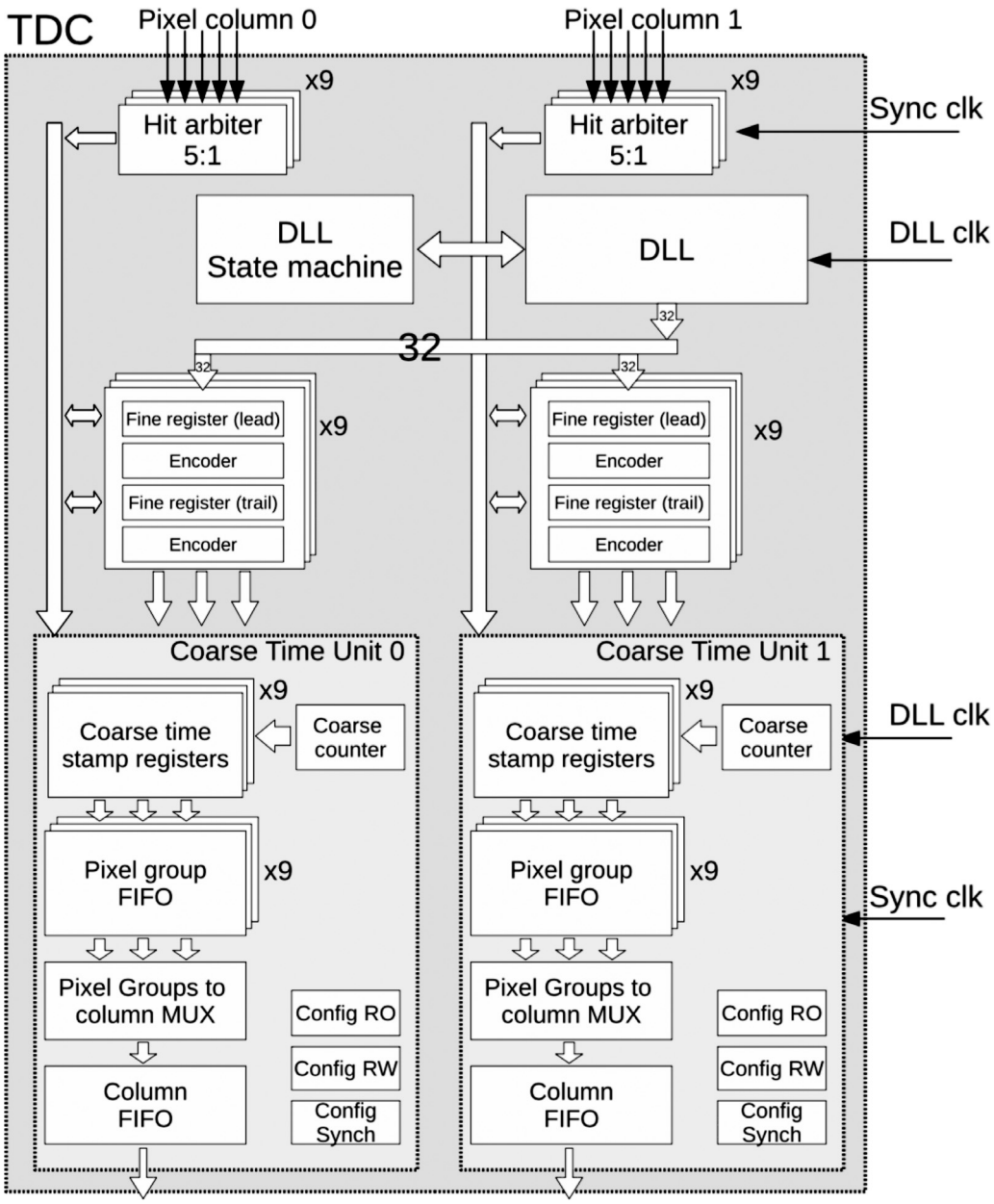


Fig. 9. Block diagram of one TDC block.

controlled by a state machine circuit and the fine time code is distributed on a 32-bit bus to two identical banks of latching registers, one bank per column. Each bank features 9 pairs of 32-bit Fine Code Registers, one pair per hitArbiter. One register of the pair latches the DLL code on the rising edge of the hit pulse, the second one latches the code on the falling edge. Each register is immediately followed by a dedicated encoder circuit. The encoders translate the 32-bit fine code values stored in the registers into a 5-bit code. The encoding is based on the detection of the rising edge of the signal along the 32 fine code wires. The position of the edge is encoded as a 5-bit canonical Gray code.

The latched and encoded codes are provided to two instances of the Coarse Time Unit block, one instance per column. Inside each one of these blocks, coarse time codes are associated with the hit pulse edges inside the Coarse Time Registers block. The coarse time stamping extends the TDC dynamic range to 6.4 μs by recording the code of a local coarse counter advancing at the frequency of the DLL input clock. On arrival of the synchronous enable from the hitArbiter all data relative to a hit are processed, combined in a data word and stored into a Pixel Group FIFO corresponding to the source hitArbiter. The nine Pixel Group FIFOs are 2 stages deep. Data words from these FIFOs are then tagged with a pixel group identifier (group of 5 pixels belonging to one hitArbiter) and multiplexed into a single, 10 stages deep, Column FIFO. The Column FIFOs are polled by the top level read-out blocks.

The output parallel data word is 46 bit wide. It is noticed that these data are further processed by the quarter-chip read-out circuits and only some of the fields are directly available as constituents of the chip output data words.

Dictated by the pixel matrix column size the TDC for one column needed to fit within 300 μm. In a trade-off between routability, buffer needs and used silicon area one DLL is shared between the TDC registers of two columns instead of routing and buffering the DLL outputs to more or all columns. Thus, the TDC block was designed for a column pair and was replicated 20 times. Fig. 10 shows the layout of one of the dual-column TDC blocks of the size 2700 μm × 600 μm.

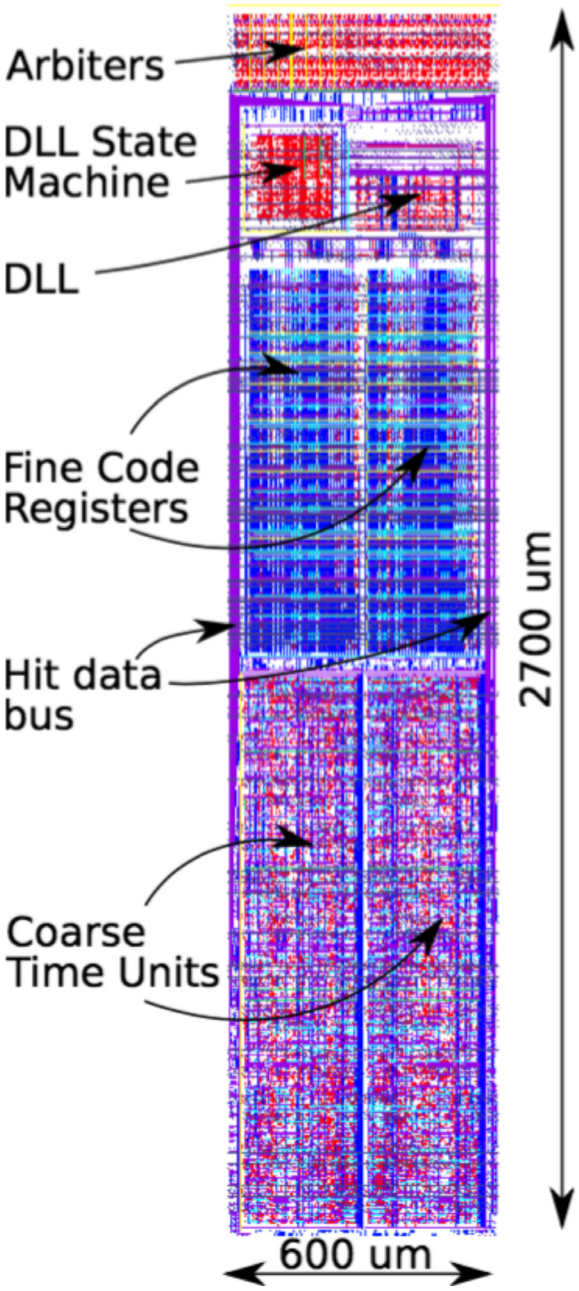


Fig. 10. Layout of the TDC block.

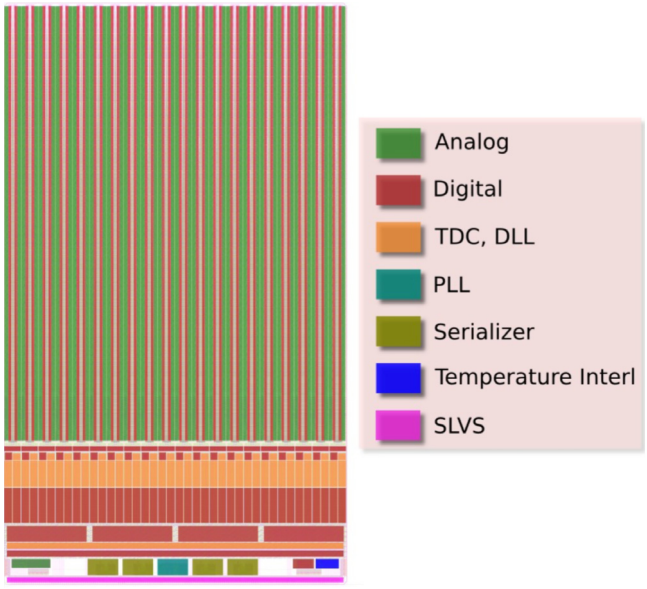


Fig. 11. TDCpix power domains.

2.4. Read-out processor and serializer

Fig. 5 shows the full TDCpix block diagram. The layout of the columns is arranged in 20 identical double columns. The read-out processor is divided into four identical functional blocks, the quarter-chip, which polls the 10 column FIFOs in a round robin basis for available data, applies an 8b10b encoding and multiplexes the data into one of four 3.2-Gb/s serializers. For applications without high speed serial links the data can be read via a 10-bit bus. For test purposes a slow read-out chain of the TDC registers has been implemented allowing the read out of the intermediate TDC registers in a fashion similar to a scan-chain. The four serializers share one PLL and a clock manager which distributes the high speed serial clock of 1.6 GHz and the digital clocks to the four quarter-chips, the configuration blocks and the TDCs. The 4 serializers were spread out over the full width of the end-of-column logic (12 mm) which required the layout of the serial clock distribution to be done manually with appropriate shielding techniques. In retrospective the authors argue that an approach where each quarter-chip would contain one PLL for the high speed serial clock generation might be preferable, avoiding the need of transmitting and regenerating the clock signal over long distribution traces.

The read-out processor allows a maximum signal input rate of 212 MHz per TDCpix or 5.3 MHz per pixel column corresponding to 1.3 MHz/cm^{-2}.

The serializers and the clock managers have been made single-event-upset (SEU) resistant by using block-level triple modular redundancy.

2.5. Configuration and additional features

In addition to the analog front-end and the transmission line driver, each pixel contains a 5-bit fine resolution trim DAC and a triple redundant SEU protected configuration register. Each double column contains an 8-bit threshold DAC and a 4-bit bias DAC, which is controlled by the double column configuration unit. All double column configuration units can be accessed individually from the global configuration unit. A test pulse can be sent to each pixel from an external pad or be sent from the internal configuration unit. The ASIC does not need any external analog reference voltage thanks to two internal band gap reference cells, one for the analog and digital domain each to improve the separation between the domains. A built-in temperature sensing block can be used to protect the chip against over-heating. A threshold on the temperature can be set via an external resistor. An open-drain output asserts if the threshold is exceeded and can be used for interlock.

2.6. Layout

2.6.1. Power domains

As the suppression of noise propagation from the read-out processor or the TDC to front-end was of utmost importance, high effort has been invested in the design of power supply distribution and decoupling. Fig. 11 shows the location of the different power domains. The high number of supply domains allowed the connection of front-end, TDC/DLL, PLL, serializer and output drivers to be individually supplied from external pins. The internal decoupling network and distribution network was adapted to each of the functional elements. It should be

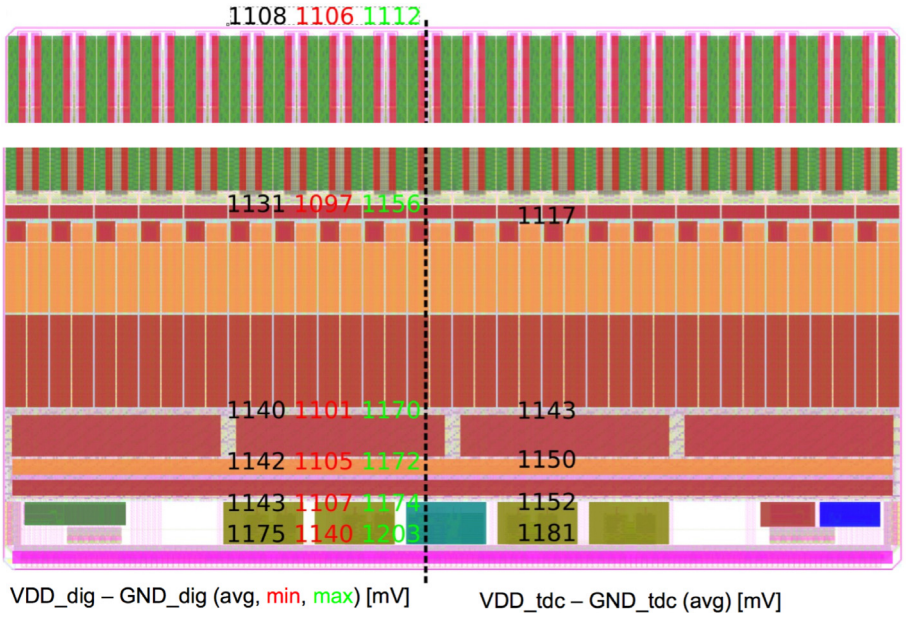


Fig. 12. Power rail drop simulations for digital and TDC domain. The numbers show the available power voltage for the average or typical case, the minimum and maximum simulation models. At the typical case the 1200 mV input voltage is degraded to 1108 mV, corresponding to an acceptable 92 mV voltage drop at the end of the pixel matrix.

VDD/GND domain	Nom. Current [mA]	%		Power pad *pairs*		
				Main row	Staggered	Total
Analog	272	12.6%		12 +	4	16
Digital	940	43.5%		8 +	5	13
TDC	568	26.2%		7 +	2	9
PLL	92	4.3%		2 +	0	2
Serializer	292	13.5%		12 +	0	12
Temp. Interlock				1 +	0	1
SLVS				5 +	0	5
	2164					58

Fig. 13. Power domain consumption and number of power pad pairs.

noted that power supply and any other external signal can be supplied only from the bottom side of the ASIC. Thus, the dimensioning of the length and width of the metal and the placement and size of the internal decoupling capacitors was critical. Intensive simulations were performed to obtain a balanced power rail drop between the domains. Fig. 12 shows the power drop of the digital power for the read-out processor and the TDC power domain for the TDC and DLL. Fig. 13 shows a table with the power consumption of the different domains and the number of power pad pairs used for each domain. The wire bond pads have been arranged in two rows in a staggered arrangement to increase the number of bondable power pads and prevent electro-migration effects.

In total, these power consumptions lead to a power density of 0.4 W/cm^{-2} for the pixel matrix and 2.5 W/cm^{-2} for the digital end-of-column region for a total consumption of 2.6 W. The high power consumption is due to the application of single-event-upset hardening techniques especially in the serializer, read-out processor and the TDC.

On the printed circuit board level, all power domains with the exception of the analog domain were connected to a single supply source. The temperature interlock sensor was also supplied individually in order to allow the temperature sensor to remain powered even if the remaining blocks and the system cooling are not powered.

2.6.2. Clock domains

The clock manager can run in different modes allowing the switch between 3.2 Gb/s and 2.4 Gb/s serial read-out and between 320 Mb/s and 480 Mb/s parallel read-out. In any of these modes, the TDCpix receives one master clock of 320 MHz and the clock manager is programmed via external hardwired pins. The precision clock to the DLL is supplied independently to the TDC and DLLs. Nominally, it is 320 MHz, but it can run up to 420 MHz decreasing the time bin size to 70 ps.

The TDCpix contains 5 different clock domains: clk_sync for the general digital processing, clk_dll connected to the DLL, clk_serial connected to the serializer, clk_multiserial connected to the parallel read-out and clk_config which drives the configuration units.

2.7. Integration

The integration of the full chip has been done with a digital-on-top methodology, using a fully scripted workflow. The individual building blocks such as pixel cell and matrix, TDC, quarter-chip, PLL and serializer were individually verified in simulation and together with their interfacing building blocks in functional, gate-level and spice representations. After the full ASIC assembly, the entire ASIC was functionally verified using RTL and time back-annotated gate-level descriptions for the digital circuits. For the analog circuits verilogAMS models were used. During these full system simulations the ASIC was virtually configured via the models of the configuration interface instead of pre-loading simulation parameters. Simulated test pulses were injected, the TDC time stamps were read out and their values were verified against a golden model. The verification test bench was written

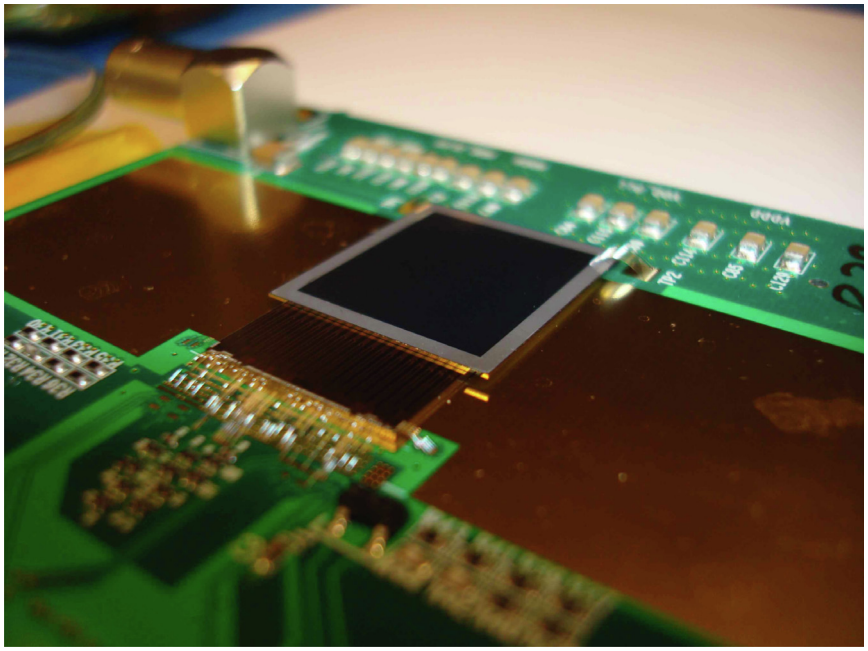


Fig. 14. Photograph of a single TDCpix chip connected to a sensor and wire bonded to a read-out card.

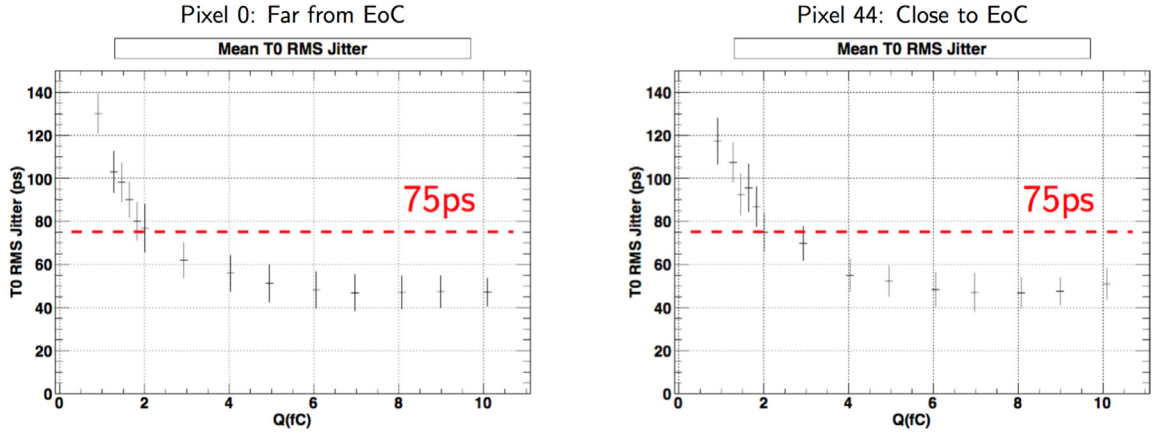


Fig. 15. Jitter of time-walk compensated arrival time t_0 over input charge for pixel far from (left) and close to EoC (right) in the TDCpix demonstrator.

in C++ and VHDL and imported into the simulation environment. Another important advantage of this approach was that the test bench was fully available and could be reused during the ASIC acceptance test and for the read-out of the ASIC in the target application.

These intensive testing phase paid off as until now still no single implementation error was found in the silicon device.

3. Measurements

3.1. Method — electrical pulse, laser, beam

The test configurations for the TDCpix prototype and the final size ASIC were identical and involved tests without a sensor attached and with a planar silicon 200 μm thick p-in-n detector connected. Three different setups were used.

- the electrical injection of test pulses via an internal injection capacitor without and with a planar silicon 200 μm thick p-in-n detector connected;
- a laser setup with a 1060 nm laser with a spot size of 7 μm mounted on an xy-table with automatic scanning of the pixel matrix and within a pixel;
- particle beam setup in a test beam for the demonstrator and in the target application, NA62, of the TDCpix ASIC.

Fig. 14 shows a photograph of a single TDCpix chip connected to a sensor and wire bonded to a read-out card.

3.2. Prototype results

One of the challenges of the TDCpix ASIC is the integration of all building blocks into a mixed mode ASIC without degradation of the analog circuit performance. Fig. 15 shows the jitter performance of a pixel far from (in the fig. left) and close to (in the fig. right) the noise generating end-of-column (EoC) circuit over the input charge with sensor. These tests have been performed with a detector bias voltage of 300 V and use the focused laser pulse shone on the pixel centre. For the most probable signal amplitude of 2.4 fC a jitter of 75 ps was measured.

3.3. TDCpix results from electrical measurements without a sensor connected

3.3.1. Front-end

Fig. 16 shows the transfer curve and Fig. 17 shows the gain distribution over all pixels of 62 mV/fC with a RMS spread of 1.1 mV/fC. Fig. 18 shows the noise in equivalent noise charge (ENC) of 170 e^- (RMS spread of 3.7 e^-) obtained with an S-curve scan.

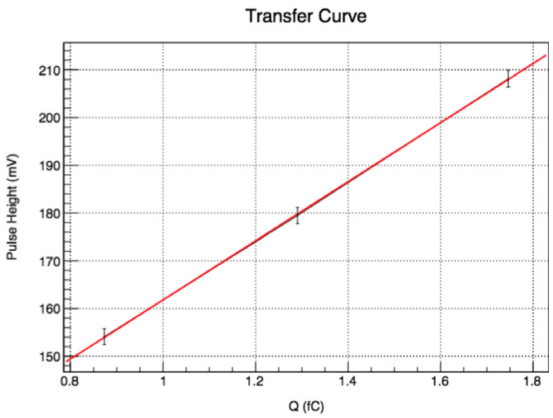


Fig. 16. TDCpix transfer curve with electrical input pulses and without sensor showing the front-end gain (mV/fC) in the linear operation region. As the measurement time is a factor for production testing, only 3 points were taken to demonstrate the process.

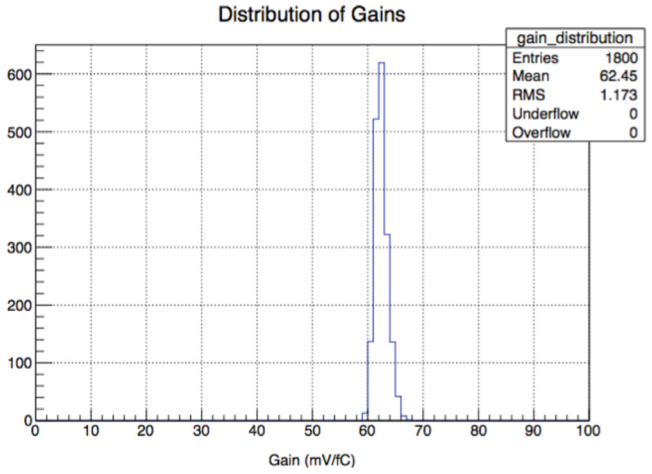


Fig. 17. TDCpix gain distribution with electrical input pulses and without sensor.

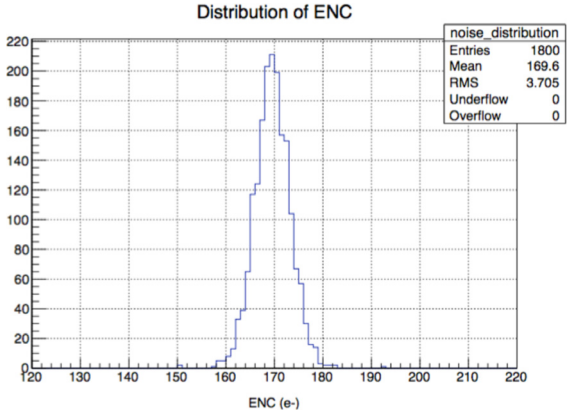


Fig. 18. TDCpix noise with electrical input pulses and without sensor.

Each pixel can individually be trimmed. Fig. 19 shows the turn-on curves of untrimmed (left) and trimmed pixels (right). Before/after trimming a peak-to-peak spread of 85/6 mV was achieved, which correspond to the simulated 15 mV RMS value.

After the transmission line the discriminator output of 2 pixels are available to external pads which allowed direct testing of the jitter bypassing the TDC. Fig. 20 shows the pixel jitter measured via the test output. For the most probable input charge of 2.4 fC in the target application the jitter is 60 ps. This value includes the pre-amplifier shaper, discriminator performance, the transmission line driver and receiver, the digital hitArbiter, a buffer in the EoC region, the test pulse generation with a jitter contribution of 30 ps and an unknown contribution from the test pulse distribution in the ASIC, and thus the measurement presents an upper limit. Removing the quadratic term of the test pulse generation allows to set an upper limit of the pixel jitter to 52 ps.

Fig. 21 shows the jitter versus the distance from the EoC region. Fig. 22 shows the jitter versus the input signal frequency. In both cases no degradation due to the transmission line length or the input frequency can be observed.

3.3.2. TDC

Figs. 23 and 24 show the integrated non-linearity (INL) for the rising and falling edge TDC measurements respectively. The plots combine all 360 TDC channels and show an RMS INL value less than 0.15 LSBs.

Fig. 25 shows the rising edge TDC transfer curve. For column 0 a test pad is available as 6th input to the hitArbiter and thus gives direct access to the TDC input. The plot is obtained by scanning the delay of the test inputs through the full dynamic range of 6.4 μs of the fine time measurements. For each delay setting 30.000 test pulses were sent and are separated from the next delay setting by 10 ps. This small step size allows taking the quantisation error due to the bin size of 97 ps into account as the expected jitter or resolution is less than the bin size. Thus, scanning through the dynamic range with a larger step size and depending on the applied delay would result in a histogram filled only with one bin if the applied delay is centred within one TDC measurement bin or result in two filled bins if the test pulse arrival time is close enough to a TDC bin boundary so that the arrival time with TDC jitter overspans two TDC bins. For these measurements the analog front-end was bypassed and digital test pulses were directly injected to a test input of the hitArbiter.

Fig. 26 shows the Time-over-Threshold measured by the TDC for a fixed-width digital input pulse with a duration of 14.5 ns that is swept through two clock periods. An ideal TDC would digitise this as a flat line. The undulations seen are the interplay of the INLs of the leading edge and trailing edge TDC channels, and naturally shows a periodicity of one DLL period of 3.125 ns.

When entering all obtained jitter values for all 626 delay settings (2 * 3.13 ns/10 ps) into a histogram one gets the jitter or resolution histogram as shown in Fig. 27. From this histogram the effective resolution of 58 ps is taken because it is the most probable value of the distribution. This value again contains a contribution of 30 ps from the clock/pulse generator and the unknown contribution from the test pulse distribution in the ASIC. Thus, removing the quadratic term, the upper limit of the TDC resolution can be set to 50 ps.

3.3.3. Read-out without sensor

The full chain including the analog pre-amplifier/shaper, discriminator, transmission line driver/receiver, transmission line, hitArbiter and TDC read out via the high speed serial interface has been evaluated by sending 10,000 test pulses for each of 32 delay phases and 14 charge values separated by 97.7 ps without a sensor attached to the TDCpix.

The resulting histogram in Fig. 28 shows a rising edge jitter of 65 ps for 2.4 fC input charge including the TDC quantisation error of $97/\sqrt{12} = 28$ ps, the clock/signal generator jitter of 30 ps and the unknown contribution from the test pulse distribution inside the ASIC. Consequently, a maximum jitter value of 50 ps can be calculated.

Fig. 29 shows the time-walk compensated time measurement for equally weighted input charges from 1 to 7.5 fC using the electrical test pulse input without a sensor connected. The TOT correction curve was measured individually for each pixel, and then a statistically separate data set was acquired and the t_0 values calculated from the raw data without knowledge of which charge was being injected. The histogram shows 72 ps RMS resolution including the clock/pulse distribution of

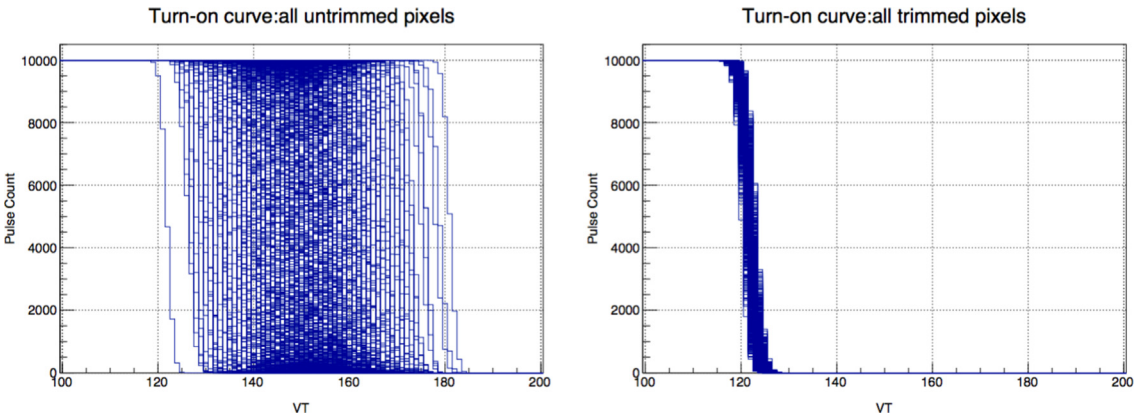


Fig. 19. TDCpix turn-on curves for untrimmed (left) and trimmed (right) pixels.

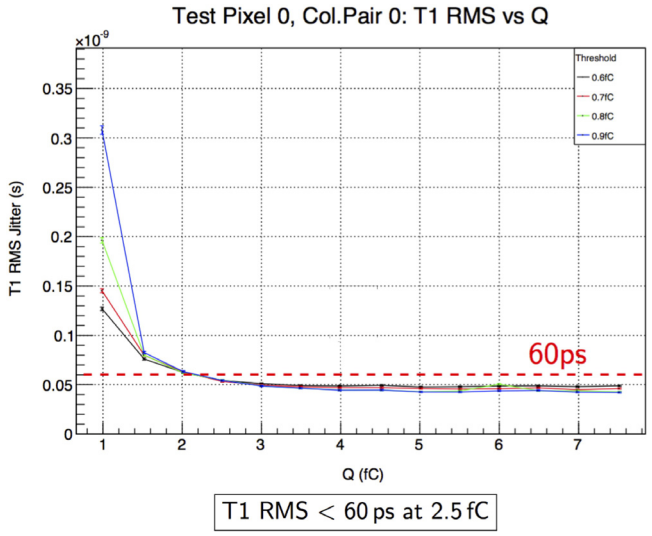


Fig. 20. Pixel jitter vs. input charge measured via the test output.

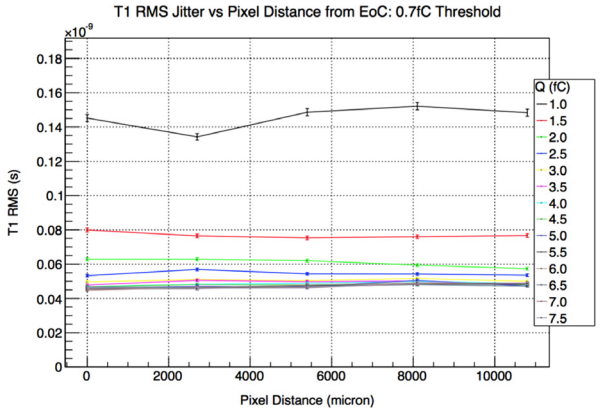


Fig. 21. Rising time signal t_1 jitter versus distance from the EoC region.

30 ps and the TDC quantisation error. Subtracting the clock/pulse distribution contribution one obtains 65 ps and when also subtracting the TDC quantisation error one obtains 59 ps. Of course, the quantisation error will add to the measurement uncertainty and subtracting the contribution only serves as demonstration that the analog front-end and the TDC linearity performance would also be compatible with a TDC system with a smaller bin size.

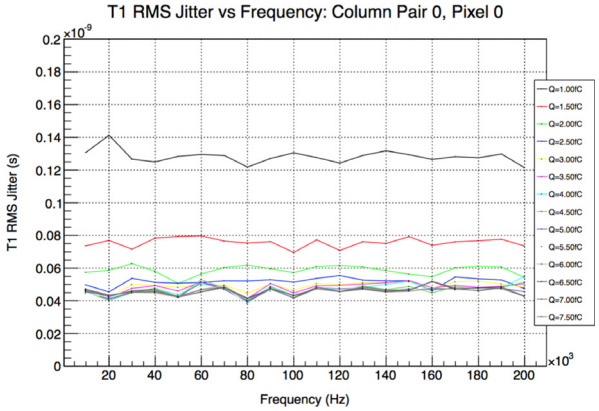


Fig. 22. Rising time signal t_1 jitter versus pixel signal input frequency.

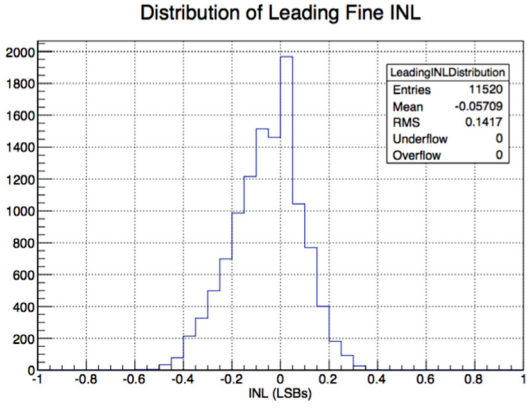


Fig. 23. INL for the rising edge TDC measurement.

3.4. TDCpix results with sensor connected using the laser

3.4.1. Laser setup

The laser setup consists of a 1060 nm pulsed laser with a microfocal lens and a beam size of ≈7 μm. The laser driver has ≈10 ps RMS jitter and ≈50 ps full-width-half-maximum pulse length. It is driven by an external pulser and the total system jitter is ≈30 ps RMS.

A programmable optical attenuator allows automatic adaptation of the signal input amplitude and an xyz-motion stage with a precision of ≈0.5 μm allows automatic scanning over the full pixel matrix and within one pixel. Fig. 30 shows a picture of the laser setup with a test card containing a TDCpix ASIC connected to a planar silicon p-in-n sensor

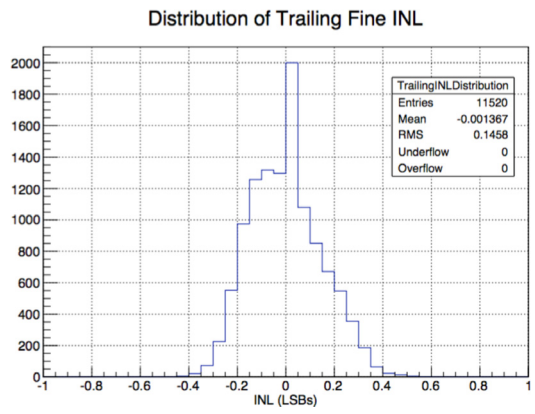


Fig. 24. INL for the falling edge TDC measurement.

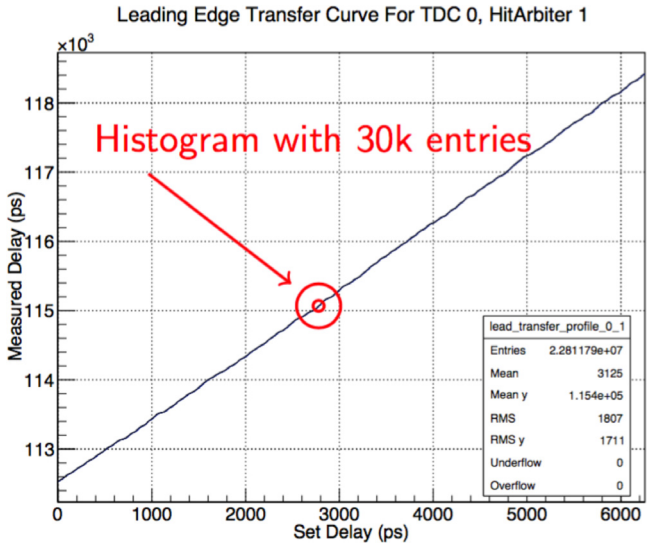


Fig. 25. Transfer curve for the rising edge TDC measurement.

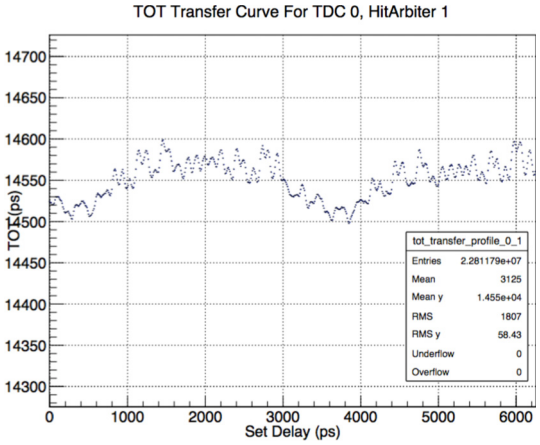


Fig. 26. Transfer curve for the Time-over-Threshold measurement.

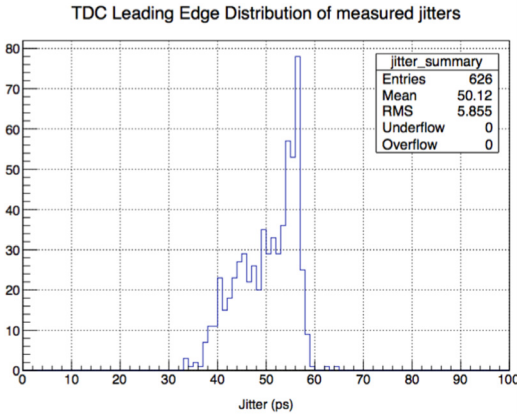


Fig. 27. Rising edge distribution of all measured delay settings.

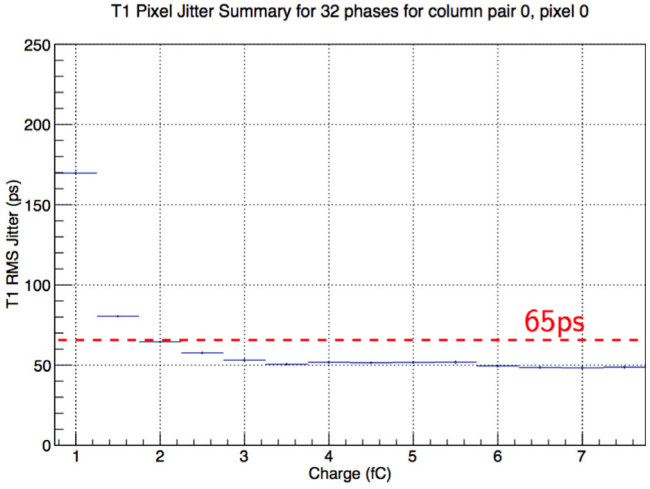


Fig. 28. Full chain rising edge t_1 jitter versus input charge.

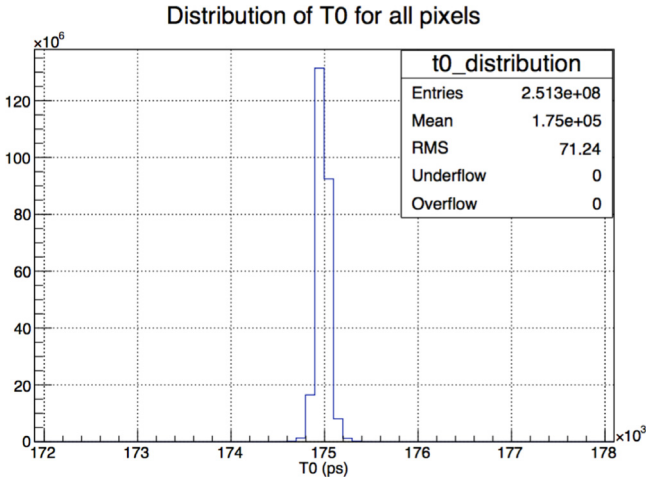


Fig. 29. Time-walk compensated full chain TDCpix resolution of t_0 without sensor.

of 200 μm thickness. The ASIC sensor assembly is cooled with a custom made water cooling and connected to an FPGA-based read-out card.

Fig. 31 shows a block diagram of the laser setup. Dedicated care has been taken to setup the laser system to allow correct synchronisation of the laser pulse with respect to the precision clock sent to the delay locked loop in the TDC. This synchronisation allowed the detailed TDC characterisation with a precision beyond the 97.7 ps TDC bins.

The 320 MHz precision reference clock used by the TDCPix was generated by an external precision clock generator (Stanford Research Systems CG635). The 10MHz laboratory reference output clock generated by this instrument was connected to the external clock reference

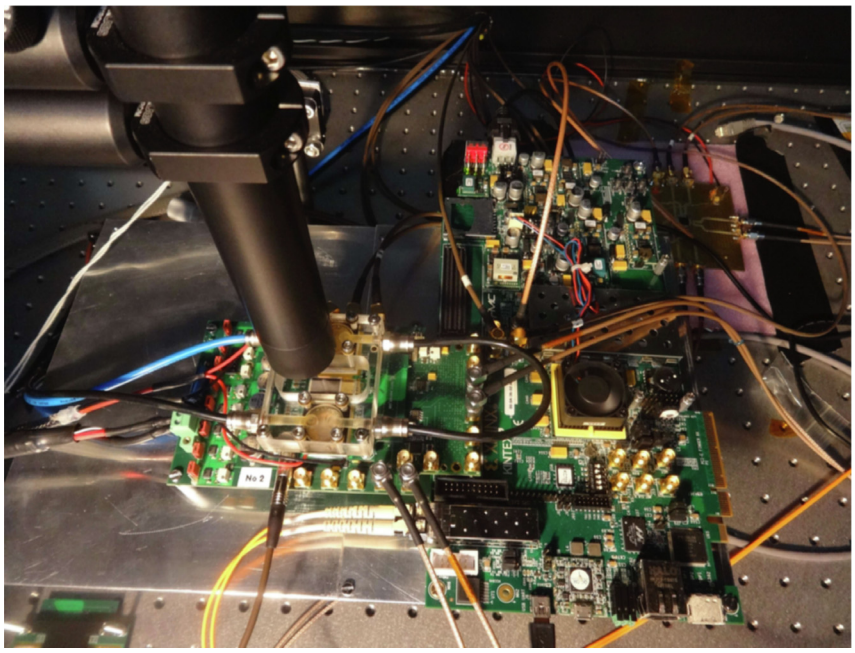


Fig. 30. Photograph of the laser setup.

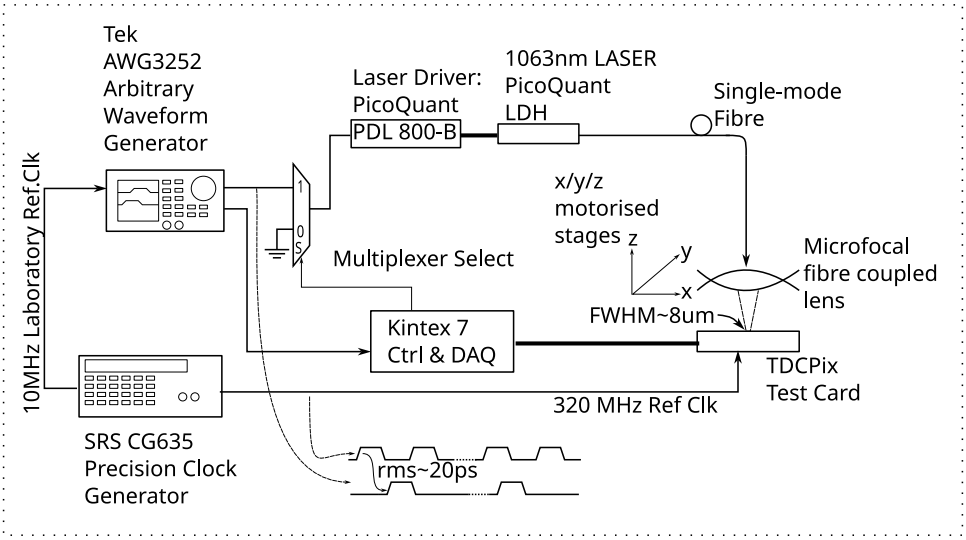


Fig. 31. Block diagram of the laser test setup.

input of an arbitrary waveform generator (Tektronix AWG3252) and used as its base reference clock. This phase locked the two instruments together. The arbitrary waveform generator was used to generate two equivalent trigger signals. As long as the repetition rate of the trigger was judiciously selected to be a multiple of the 3125 ps clock period, the two instruments remained phase locked, with an RMS jitter between them of approximately 20 ps. A high-performance multiplexer controlled by the DAQ FPGA was used to enable the trigger signal to the LASER driver and to allow a certain number of pulses through. The second output of the arbitrary waveform generator was sent to the FPGA and used to synchronise the select signal to the inter-trigger gap. The arbitrary waveform generator was under software control to allow automated sweeping of the trigger rate and phase relative to the 320 MHz reference clock. In all connections, high-quality coaxial cables and correct signal termination were used to maintain the signal quality between the various instruments.

In order to achieve precise mechanical alignment of the laser setup to allow automatic xy-scans over the full pixel matrix and scans within a pixel and the pixel borders, the setup was precisely aligned on x–y and in z direction.

Precise alignment between the laser and the TDCpix test system allowed automated xy-scans over the full pixel matrix and within the pixel itself. The laser spot was scanned from one pixel to its neighbours in both x- and y-directions and repeated for each corner of the pixel matrix. Using this method, the axes were aligned with a precision of $10\,\mu m$. Z-axis alignment allowed optimisation of the beam spot size and lateral spread of the charge injection point. A beam spot of around $8\,\mu m$ was attained, compatible with the micro-focal lens connected to the optical fibre.

The optical input amplitude was calibrated using the programmable optical attenuator. In a first step, the threshold setting of the ASIC was calibrated using the electrical input pulse, where each pixel threshold was trimmed. In a second step, the laser attenuator setting was calibrated for 6 discrete threshold values. Fig. 32 on the left shows the turn-on curves for one pixel for different thresholds and the plot on the right shows the resulting optical transfer curves for one pixel of each

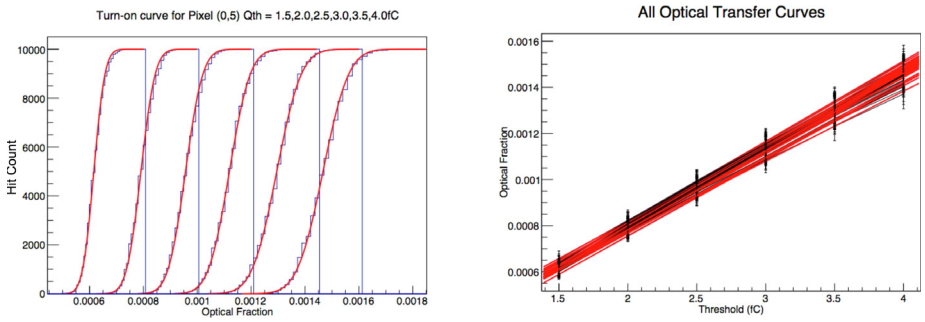


Fig. 32. Laser calibration.

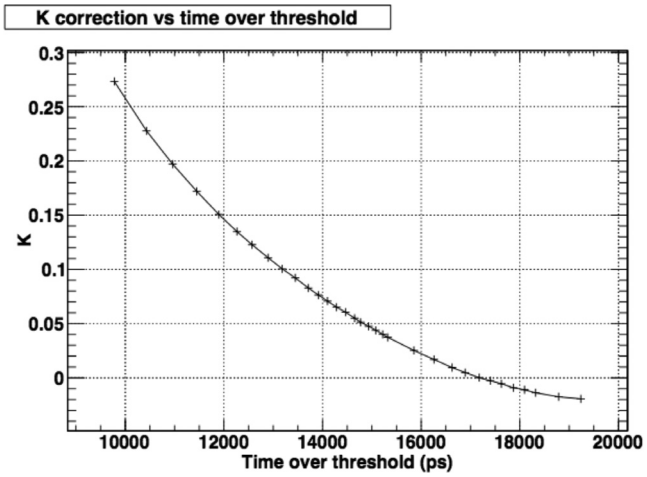


Fig. 33. Correction factor K versus Time-over-Threshold.

Table 3
Summary of TDCpix electrical and laser measurements.

Parameter	Jitter [ps]
Electrical measurements without sensor	
Front-end jitter t_1 @ 2.4 fC (pre-amplifier/shaper/discriminator/transmission line/ driver/receiver/hitArbiter/buffer)	<60 ps
TDC+read-out jitter contribution	<50 ps
Front-end+TDC+read-out t_1 jitter @ 2.4 fC Front-end+TDC+read-out t_0 jitter @ 1–7.5 fC (flat) (pre-amplifier/shaper/discriminator/transmission line/ driver/receiver/hitArbiter/TDC/high speed serial read-out)	<65 ps <72 ps
Measurements with laser into pixel centre with p-in-n sensor	
Front-end+TDC+read-out t_0 jitter @ 1–7.5 fC (flat) Front-end+TDC+read-out t_0 jitter @ 1–7.5 fC (Landau) (Sensor/pre-amplifier/shaper/discriminator/transmission line/ transmitter/receiver/hitArbiter/TDC/high speed serial read-out)	71 ps 81 ps

column. For the laser operation the average of all pixels were taken and a look-up-table was created and used.

3.4.2. Laser measurements

For all tests, the TDCpix was connected to a 200 μm thick planar p-in-n sensor. The procedure to measure the time resolution was divided into two steps. In the first step, a data set of 10.000 triggers was used to calibrate the time-walk compensation scheme using the Time-over-Threshold measurement. For this calibration the charge was scanned from 1 to 10 fC in 33 steps and a look-up-table for the correction of the rising edge time using the Time-over-Threshold measurement was created for each pixel. In the second step of the actual measurement, 10.000 input pulses were scanned from 1.5 to 10 fC in 16 steps. In both procedures the light was shone directly into the pixel centre. The results shown are for 5 complete columns containing 225 pixels.

Fig. 33 shows the obtained calibration curve where $K = (t_1\text{-}t_0)/(t_2\text{-}t_1)$ and corrects for offset and time-walk. Fig. 34 shows the resolution plots obtained by this procedure for time-walk corrected arrival time, t_0. The plots on the top show the resolution of 71 ps for all pixels. These plots assume a flat probability distribution for each input charge values. In order to take into account the target application where the input charge probability follows a Landau distribution the plots on the bottom show the resolution plots (82 ps) following a Landau distributed charge distribution.

Table 3 shows the summary of the electrical and laser test performance.

3.5. Application in CERN-NA62 experiment

The TDCpix has been qualified bump bonded to 200 μm thick planar p-in-n and n-in-p CMOS sensors in the beam line of the NA62 experiment in the Giga Tracker detector. A resolution of 115 ps per detector station containing 10 TDCpix ASIC bump bonded to a n-in-p sensor biased at 250 V was achieved in the experimental beam line [3].

3.6. Limitations of sensor

As mentioned before, the TDCpix achieves a timing resolution of 115 ps with a planar 200 μm thick CMOS sensor in the target application (NA62 GigaTracker). This is larger than the resolution obtained in laboratory conditions with the laser measurements. The additional uncertainty is explained by the fluctuations of the signal created in the silicon sensor when detecting charged particles.

The entity of the contribution to the uncertainty from the sensor can be estimated by subtracting in quadrature the time resolution measured in the lab (81 ps) from the total resolution with particles (115 ps) and this results in a value of the order of 80 ps. This reveals that effects in the pixel sensor gives a significant contribution to the dispersion of the time of arrival measurements and that the combination of the planar sensor with the TDCpix does not profit fully from the timing capabilities of the chip. No specific development was done on optimising the timing properties of the sensor itself, e.g. optimising the thickness of the sensor.

In a planar pixel sensor two main effects lead to fluctuations of the shape of the induced current signal seen at the front-end, in addition to the randomness of its amplitude. The first is charge straggling. The second is due to the variations of the induced signal depending on where the primary charge deposit and carrier transport happen inside the pixel cell, which is customarily modelled through a weighting field determined by the pixel geometry. Whereas the TDCpix can effectively compensate the time-walk due to the amplitude fluctuations of the signal using the Time-over-Threshold measurement, this correction technique cannot effectively compensate the non-uniformity of the induced current signal shape. An in-depth treatment and quantitative

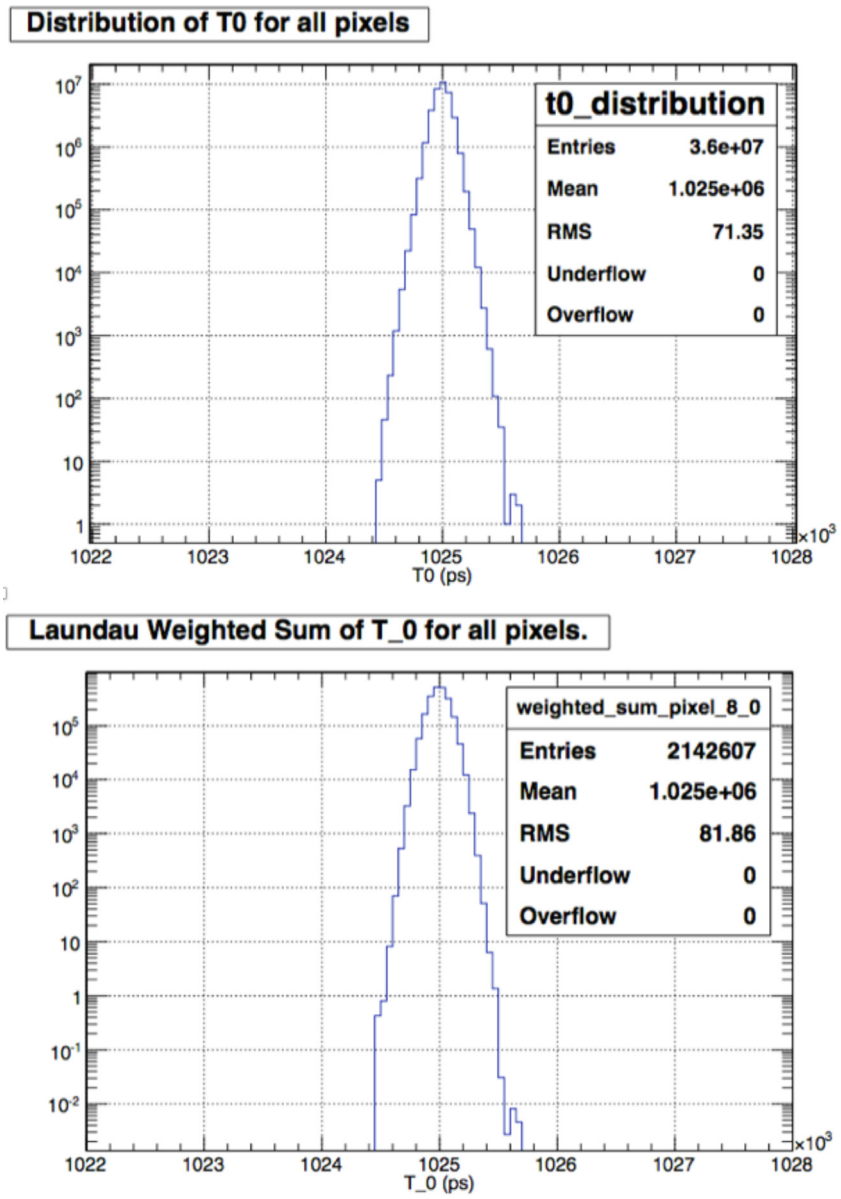
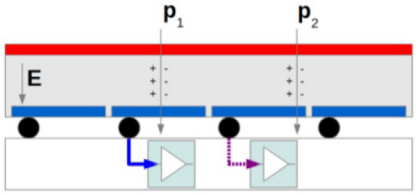


Fig. 34. Distribution of time-walk compensated arrival time t_0 resolution.

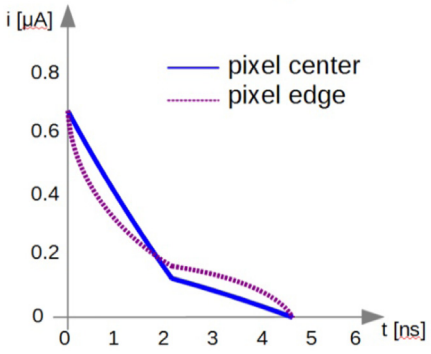
discussion of the impact on the full-chain timing resolution of the signal formation in the sensor can be found in [10]. This reference includes a discussion on the NA62 GigaTracker sensor and the effect of the weighting field is expected to be dominant over the one of charge straggling given its pixel geometry.

To provide insight, Fig. 35(a) illustrates the cases of two particles crossing two pixels with normal incidence but at different displacement from the centre of a pixel. Even assuming constant and uniform charge release, the two events induce different current pulses at the input of the front-end. Fig. 35(b) illustrates qualitatively the different shapes of the pulses corresponding to the two events. These were obtained using an analytical model of the weighting field, which was feasible for the planar pixel geometry of the GTK sensor. The centroid of the induced current pulse of the event off-centre is shifted to a later time with respect to the case of the hit close to the centre of the pixel. The response of the amplifier, the convolution of its pulse response with the input current pulse, reflects that time shift in most of its features, including a delay of its rising edge.

The effects on the full chain response due to the weighting field could be revealed directly with laser pulse injection experiments. An xy-scan of the laser beam position over the pixel array was performed. The stepping size was 10 μm, the laser pulse energy was set to produce a constant charge injection of 4 fC, and the bias voltage applied on the p-in-n sensor was 300 V. Fig. 36 shows the time-walk compensated arrival time t_0 as a function of the y-offset and x-offset from the pixel centre of the laser focusing point. The plot shows that laser shots close to the pixel periphery are assigned a larger arrival time and this is attributable to the effect of the weighting field discussed above. The peak-to-peak variations of the data set are of 340 ps and the RMS is of the order of 100 ps. While this value of uncertainty is of the expected order of magnitude, it remains difficult to extrapolate accurately to the full chain performance with particles due to the interplay of numerous effects such as the actual deposit of carriers, transport, lateral diffusion, sharing across pixels and inclined incidence of incoming particles.



(a) Two sample events: particle p_1 hits the pixel in the center, particle p_2 towards the edge.



(b) Illustration of the signal shapes from the hit at the center of the pixel (blue,solid line) and close to its edge (red, dashed line).

Fig. 35. Illustrations of the effect of the point of incidence on the response due to the weighting field in the sensor volume.

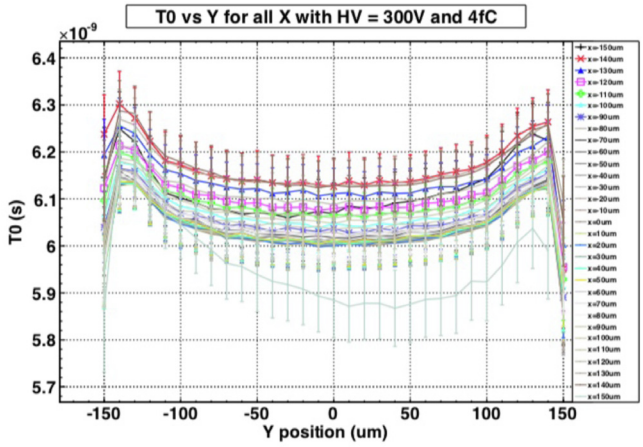


Fig. 36. Time-walk compensated arrival time t_0 over y-position along the pixel cell with x-positions as parameters.

4. Considerations

The ASIC fully fulfilled the NA62-Gigatracker target application specifications. During the design phase, several observations were made. The measurements revealed that the noise separation between the digital and analog domains was effective. Even though it was found that the transmission lines are lossy and the signal rise time from far pixels is high (order of nanoseconds), the signals from pixels close to the noisy end-of-column region compared to those close did have similar performance. This is an indication that no significant noise was injected in those lines as noise would have degraded the timing performance. The designers concluded that the timing signal transmission from the pixels to the end-of-column region could have been done without transmission lines. In the present implementation, the pixel width of 300 μm is consumed by the transmission lines. With traditional connections, this width could have been reduced to 150 μm or less allowing for pixel sizes of 150 μm × 150 μm still maintaining the general implementation architecture.

In the target application, the hit rate and hit topology allowed the use of the hitArbiter to reduce the number of TDC channels. However, in the design phase, the designers noted that it would have been possible to suppress the hitArbiter and implement a sufficient number of TDC channels by enlarging the end-of-column area by acceptable sizes. The clock distribution from one PLL to all 4 serialisers required considerable design and layout effort. In retrospect, taking the effective noise separation between the power domains into account, an approach with 4 PLLs, each for one serializer, instead of one might have been the better choice.

5. Summary

The TDCpix ASIC has been designed in 130 nm IBM/GF technology to provide a 1800-pixel read-out chip with 97.7 ps bin size time tagging capability and a triggerless read-out. The electronics channel loaded with a 250 fF, 200 μm thick, planar sensor including the TDC and 3.2 Gb/s read-out has an ENC of 170 e^-. The front-end contributes to the overall jitter with 60 ps for an input signal of 2.4 fC. The TDC and read-out chain contribute with 50 ps. Measurements with the planar silicon sensor and a laser shone into the centre of a pixel qualified the full electronics chain to provide a time resolution of 71 ps considering a flat input charge distribution. The TDCpix is successfully in operation in NA62 since many years. During the design and production period only one single small scale prototype was produced before the final size ASIC was produced. Before production intensive functional ASIC-level and system level simulations were conducted which resulted in an ASIC without any known errors and allowed immediate mass production without the need of a re-spin.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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