PS/RF Note 95-12
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The G64 Interface used to control the Radio Frequency equipment in the PS

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This technical note describes the interface system used to control the RF equipment of the Booster C08, C16, BTKRF, the PS C01, C02, C10, EPPHINJ and the EPA CRF in the PS division.

Based on a G64[1]-Europa chassis connected to a DSC[2] -VME chassis via a MIL1553 bus, this application follows the basic rules (see reference note [1]), defined in the "Control Protocol"[3] already applied for Vacuum, Power Converter, Stepping Motors and Instrumentation remote control.

As identical functionalities plus some enhancements were required to control RF equipment. This technical note replaces the PS/RF Note 94-26 which described the first implementation on the Booster machines.

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[1] G64, GESPAC are trademark of GESPAC S.A. Geneva, Switzerland.

[2] DSC stands for Device Stub Controller: an industrial VME chassis which executes the distributed processes of the Cern Control system.

[3] The Control Protocol, a model based, uniform access procedure to accelerator equipment from a control system, has been proposed at CERN. More than 300 equipment belonging to different families are now in normal operation: this includes Power Converters, Vacuum Systems, Beam Instrumentation Devices, RF Equipment, etc.

LIST OF CONTENTS

1. INTRODUCTION.

The RF stations in the PS are (see Appendix 1,2,3,4,6) :

- the PSBC08 Cavities (set of 4)
- the PSBC16 Cavities (set of 4)
- the PSBBTKRF or Dipole
- the PSC10 10 MHz cavities (set of 11)
- the PSC02 200MHz cavities (set of 8)
- the PSC01 114 MHz cavities (set of 2)
- the EPPHINJ
- the EPA 19 Mhz cavity.

For these equipment, the operator wants to remotely:

a) control:
- the amplifier actuation (OFF, STANDBY, ON, RESET)
- the RF Enable

and from cycle to cycle (PPM[4]),
- the RF actuation
- the RF phase of the Dipole BTKRF, EPPHINJ and EPACRF
- the RF voltage amplitude of the Dipole BTKRF and EPACRF

b) acquire:
- the amplifier status (OFF, STANDBY, ON)
- the RF Enabled status

and from cycle to cycle (PPM),
- the RF actuated status
- the RF phase of the Dipole BTKRF, EPPHINJ and EPACRF
- the RF voltage amplitude of the Dipole BTKRF and EPACRF

Figure 1 shows where the G64 chassis stands between the operator and the equipment.

This document describes the G64 interface chassis (hardware and software: intelligent part only - see section 2.1.), it links with the equipment layer and details the messages exchanged with the Front End Computer (DSC). Special behaviours will also be explained.

Diagnostic facilities have been included to help the equipment specialist PS/RF or the PS/CO Maintenance team in trouble shooting. These will be described at the end.

[4] Pulse to Pulse Modulation

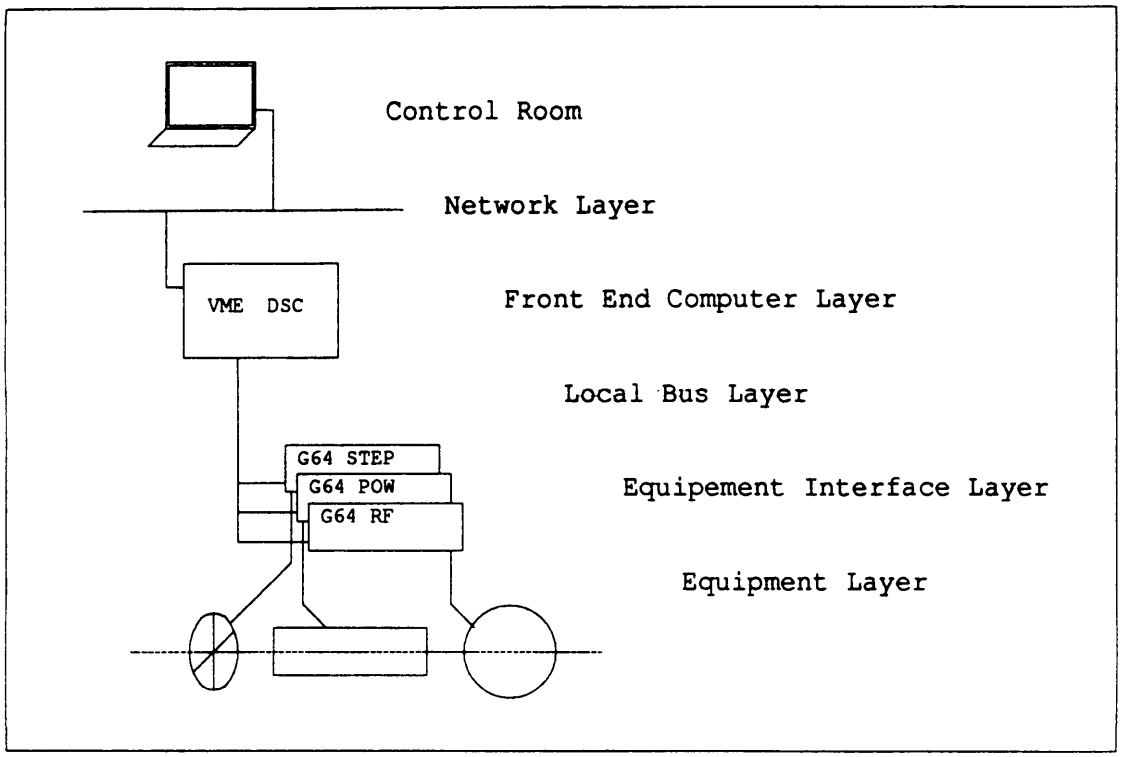


Figure 1: Layers between Operator and accelerator components.

2. SYSTEM DESCRIPTION.

2.1. Generalities.

The 2 functionalities of this interface are :
- to receive control message (high level protocol) sent by the DSC and set the correct bits or analog signal for the equipment.
- to acquire status and data from the equipment and make it available for the DSC.

The interface system is built with a 3 Units height Europa chassis with (see figures 2):
- in the front a G64 bus that receives the local processor and the programmable modules
- and in the rear, power feeds the specific interface modules.

The following hardware modules are used:
- Gespac CIO-1A as Input/Output module for the Status/Actuation of the Amplifier
- Gespac INP-2A as Input module for the fault memory acquisitions
- DAC (j14512) 12 bits Cern/PS made module for analog signal control.
- QADC[5] (j14945) 12 bits Cern/PS made module for analog signal acquisition.
- CE3000 (j1000) Cern/PS made module with the 6809 CPU for the local processor
- RTI[6] MIL1553 Cern/SL made module to communicate with the DSC.

[5] Quadruple Analog to Digital Converter
[6] Remote Terminal Interface

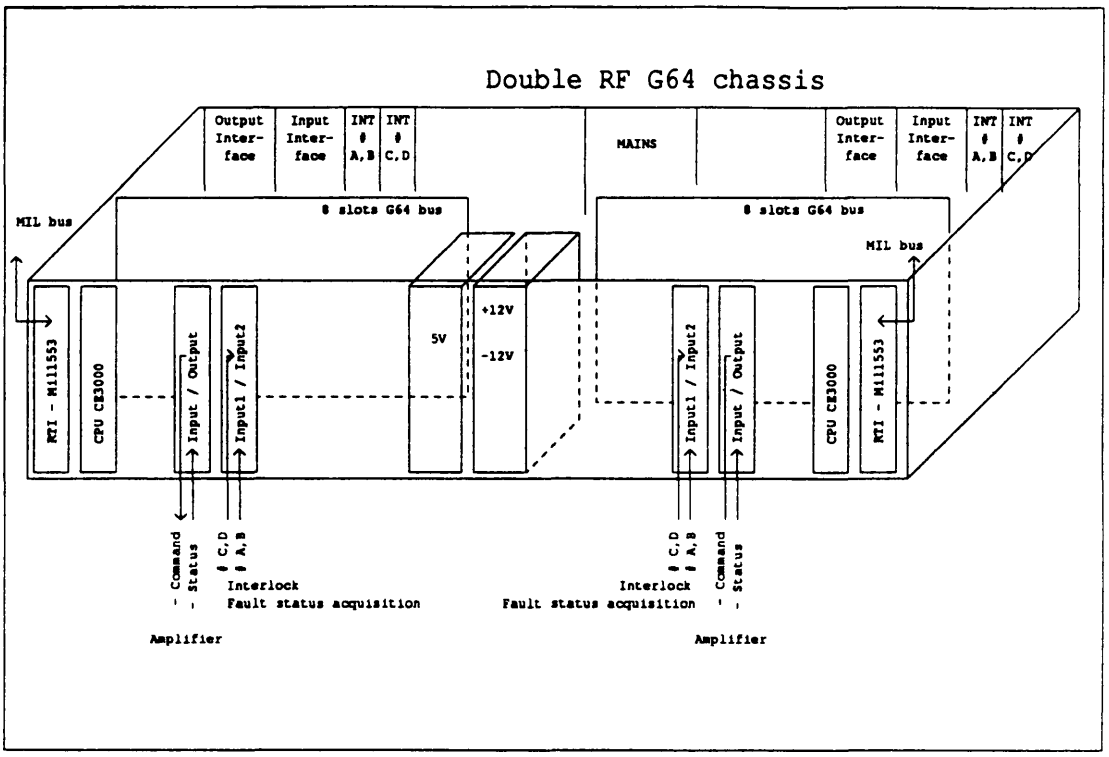


Figure 2: 114 MHz & 200 MHz RF cavities G64 chassis interfacing in PS .

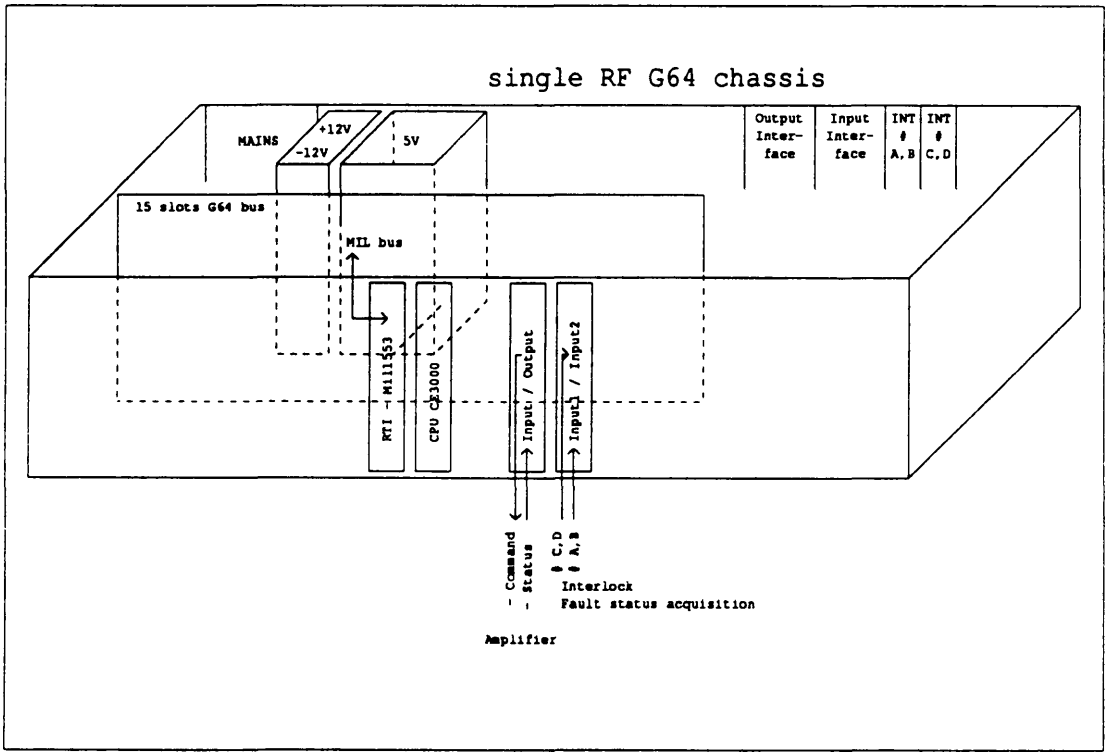


Figure 2 bis: PS 10 MHz RF cavities G64 chassis interfacing .

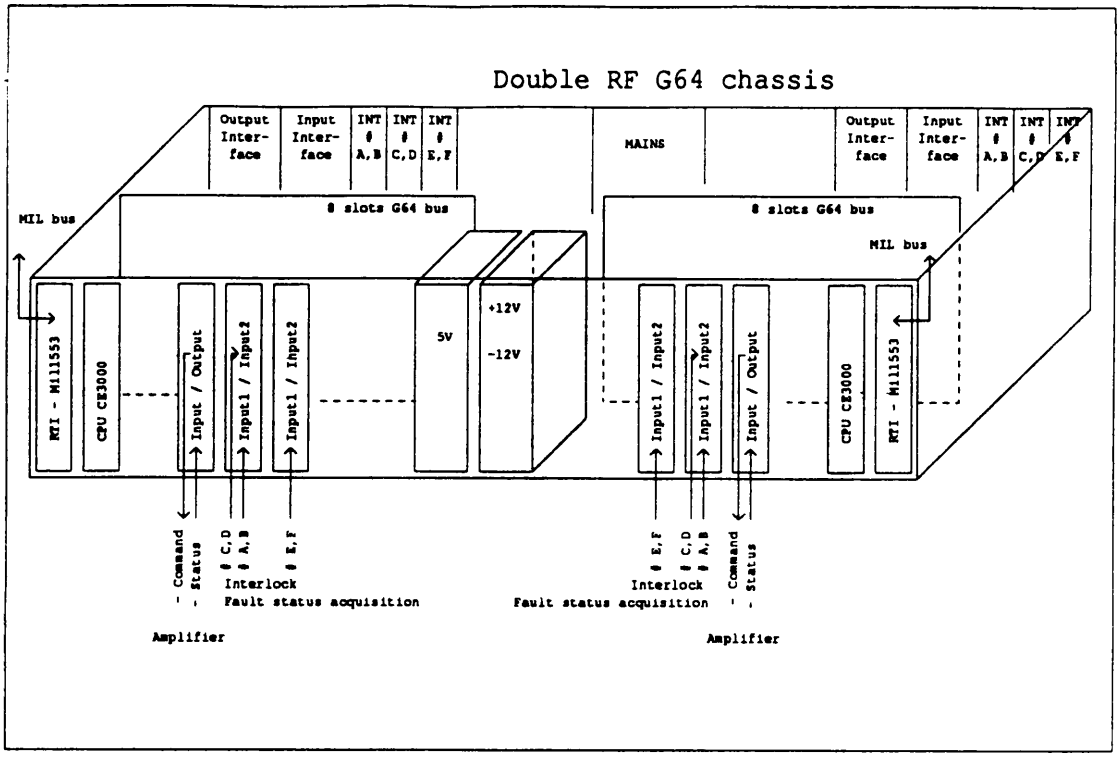


Figure 2 tiers: Booster C08, C16 RF cavities G64 chassis interfacing .

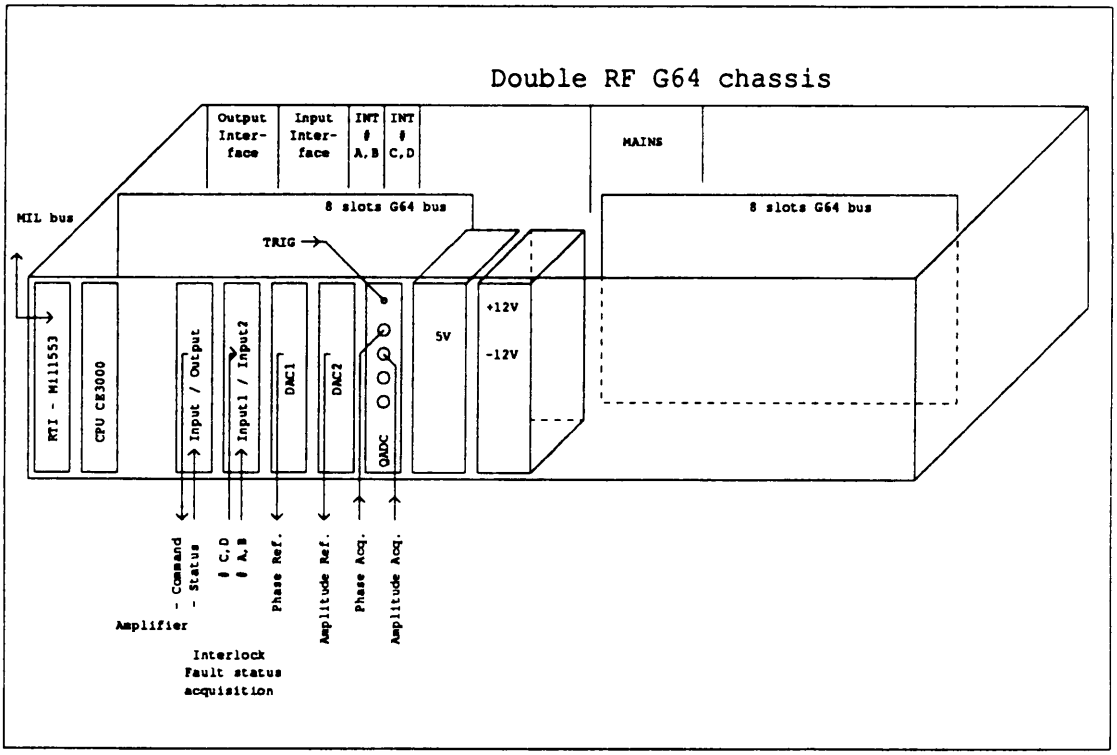


Figure 2 quat: BTKRF, EPA RF cavity G64 chassis interfacing .

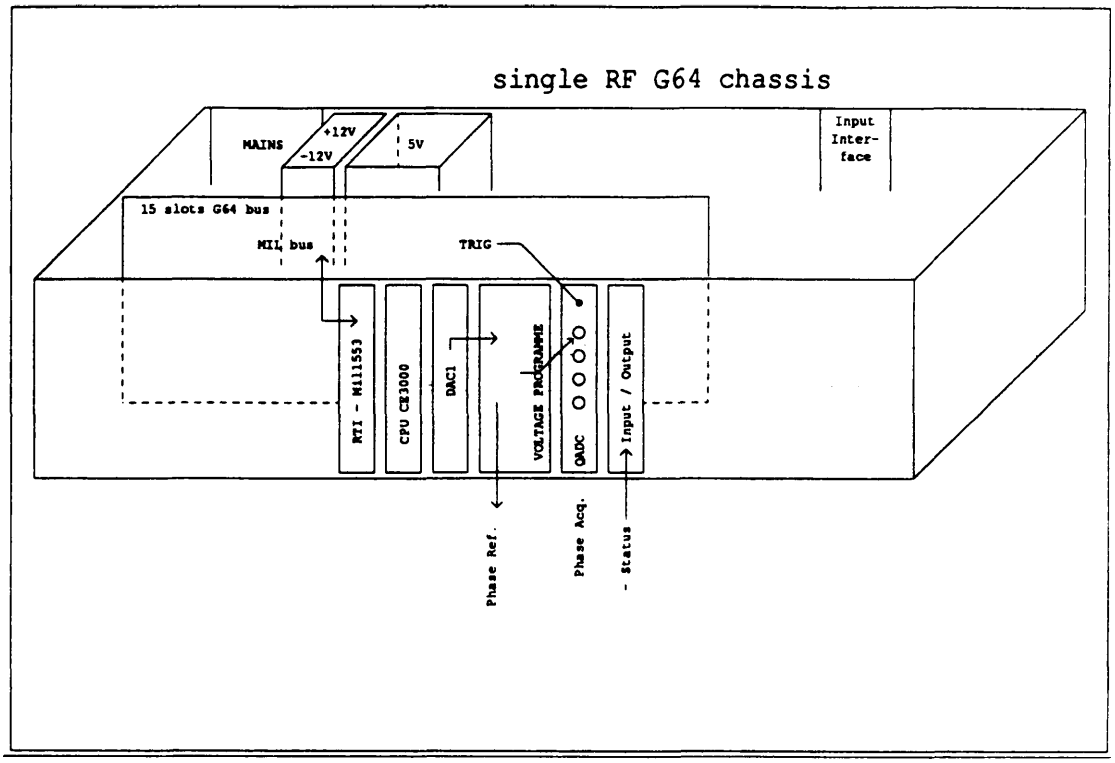


Figure 2 cinq: EPPHINJ G64 chassis interfacing in PS .

2.2 Details of the hardware modules

2.2.1 The Input/Output module

Generalities.

This module gives 16 inputs and 16 outputs isolated by opto-couplers and is designed with Darlington type circuits on the outputs in order to supply up to 100 mA. Input and output voltage can vary in the range between 12 and 24 volts.
The I/O signals are connected via two 26-pins connectors on the front panel to the specific input, output interfaces at the rear panel.
For more details, the reader will refer to the Gespac data sheets (GESC-IO1A/B).

Amplifier Status/Actuation.

The bit allocation for the Input register and Output register are given in the following table.

Bit number	Input Level high *	Output Darlington saturated
1	Level 1 Survey on	Level 1 ON
2	Level 1 Ready	Level 1 OFF
3	Level 1 Fault	Level 2 ON
4	Level 2 Survey on	Level 2 OFF
5	Level 2 Ready	System RESET
6	Level 2 Fault	-
7	RF Enabled	RF Enable
8	RF Disabled	RF Disable
9	RF ON Status	RF ON
10	RF OFF Status	RF OFF
11	SYS Remote	-
12	SYS Local	-
13	RF fault	-
14	Power Interlock Fault	-
15	-	-
16**	Diagnostic flag	-

* 0/1 is the value read from the G64 bus
**The 16th one enables (0) or disables (1) special outputs to the RS232 port on the processor module.

The base address setting of the module is indicated in Appendix 7.

2.2.2 The 2 Input registers modules

These modules give 32 inputs, isolated by optocouplers which can work on 12, 24 and 48V, with a maximum input current of 15 mA.
The input signals are connected via two 26-pin connectors (16 inputs each) on the front panel to the input interfaces at the rear panel.
For more detail, the reader will refer to the Gespac data sheets (GESINP-2A).

The base address setting of the modules is indicated in Appendix 7.

2.2.3 The DAC module for the Amplifier reference

Designed in the CERN/PS-PO group for the Power Converter interface [1], it is used in the 12 bits version and can supply a reference voltage in the range of - 10 V to + 10 V Output reference is available on a 3M - 10 pins connector.

The base address setting of the module is indicated in Appendix 7.

2.2.4 The QADC module

Designed in the CERN/PS-CO group [2], it can simultaneously convert 4 analog signals to four digital values (12 bits). The input signal range can be set on the board by jumpers but is fixed to -10V to +10V for this application.

Digital conversion can be started either from the G64 bus or with an external trigger connected to the front panel (TTL inv. or BLO). In our case, the latter will be used.

When a trigger occurs, the 4 channels are converted. Maximum 25 µs later, digital values are stored in registers.

On the front panel, the green LED lights when an external trigger occurs; the red LED goes ON when the digital conversion is completed and goes back to OFF when the local processor reads the converted values in the QADC.

From the 8 dip switches on the board, the first 6 ones are used to set the base address (see Appendix 7).

2.2.5 The processor module

This is either the new release CPU RAM-ROM PS/PO 24168P or the CE 3000 module. It is also used for the Power Converter and the Stepping motor interfaces:

- IC2 (48K or 32Kbytes Eprom) contains the application program,
- IC9 (4Kbytes Eprom) contains the Start Program and the IRQ Routine addresses,
- IC13 (8Kbytes) is the static RAM used by the application program.

The push button on the front panel allows to reboot the system. It also generates a reset on the G64 bus.

The 3M 26 pins connector is mainly used for diagnostic facilities (see chapter 4).

The memory map of the processors is shown in Appendix 8.

2.2.6 The Remote Terminal Interface module

It allows connection to the multidrop bus based on the MIL-STD-1553-B standard; its address on the MIL bus is set with dip switches located near the Cannon 9 pins connector on the front (see jumpers setting in Appendix 10).

Up to 30 RTI modules can be connected to the MIL bus.

For more detail, see section 2.4.

2.3 Interfaces with the RF station

To interface signals between the front part of the chassis and the equipment, some non industrial modules, designed by the PS/RF group, are plugged in the rear of the chassis.

See Appendices 12, 13, 14.

2.4 Interface with the Control system

2.4.1 Generalities

The next figure shows the MIL bus architecture and its different components. One Bus Controller (in our case, the VME module) can be present at a time on the bus and up to 30 RTI slave modules can be connected to it.

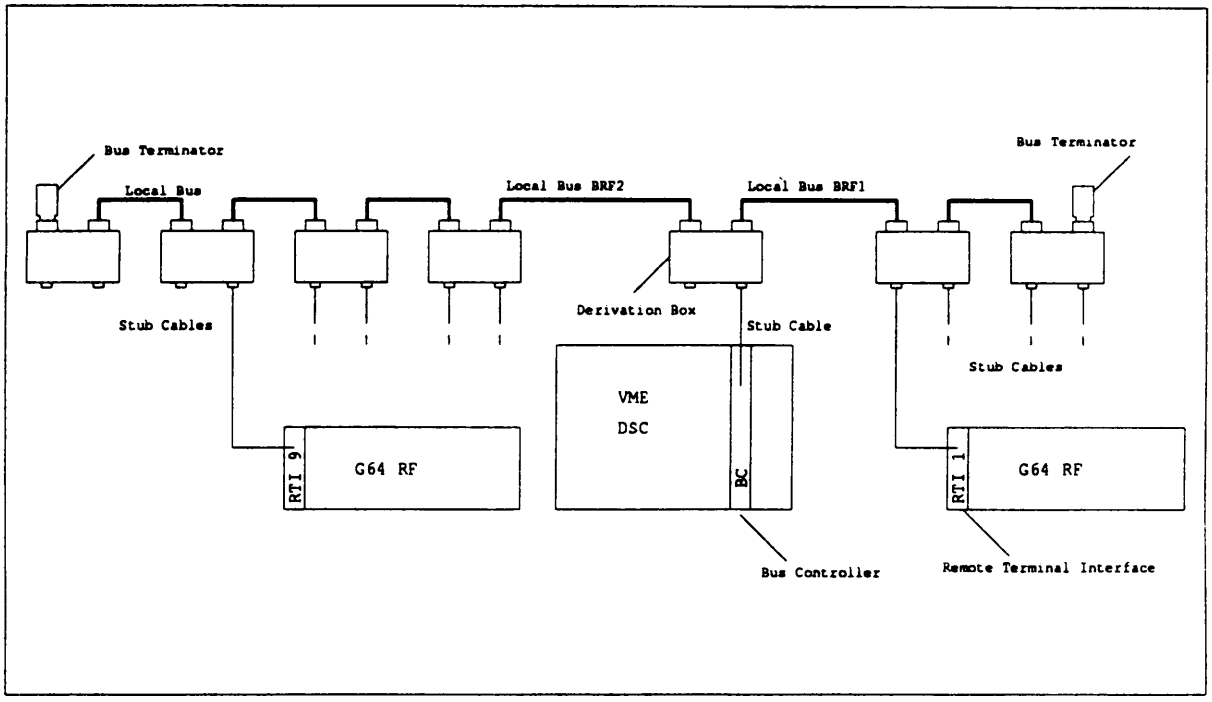


Figure 3: MIL bus architecture used in PS Booster.

2.4.2 The RTI module on the G64 side

The front panel of the RTI module has a 5 pins Cannon connector to plug the Stub cable.

5 green LEDS (LD1 to LD5) indicate its MIL address which can be set with the SW2 dip-switches.

About the other 6 LEDS, LD6 (yellow) lights when a MIL-1553 cycle is executed (ex: for PPM equipment, every 1.2 sec). LD9 (green) should always be ON (Service Request OK). LD11 (red) lights on system initialisation (Bus Controller mode) then goes off.

Message reception:

The message (containing new Actuation or new Control values as defined in the Control Protocol - see 2.5.1.), sent by the Bus Controller, generates an interrupt on the G64 bus. The local processor clears the interrupt and executes its routine call sequence (see Appendix 5). It first reads the message in the Reception Buffer.

Message transmission:

During its routine call sequence, the processor checks the requested service content in the control message and writes the correspondent acquisition message into the Transmit Buffer . Afterwards it executes the new control.

For more detail on the RTI module itself, please refer to note [4].

2.4.3 The MIL1553 Bus Controller VME module on the Front End Computer side

The BC number, the IRQ Vector and the VME address must be set according to the driver installation [5]. Appendix 9 shows how to set the jumpers for Index 0 (BC=1).

2.5 Software modules

2.5.1 Control protocol

Introduction

Messages defined in the 'Control Protocol' [6] and exchanged on the MIL bus between the Bus Controller and an RTI module contain:

- the Quick Data packet header where one can find the BC address,
- the RTI address, the Quick Data type, etc. (see reference note [7]), which are 'low level' protocol data,
- the Control Protocol header,
- the Control Protocol data (if any).

The Control messages

- The asynchronous Normal Control message PPM (AMM=0):

sent, by the BC module to an RF station and from cycle to cycle, when the VME interrupt occurs (see the Real Time process in section 2.5.2.).

Table 4.1 details its different data.

	Byte Number	Field	Type	Number of Bytes	EM Property
Header	1-2	Family Number	Integer(16)	2	---
	3-4	Type, Subtype	Integer(16)	2	---
	5-6	Serial Number	Integer(16)	2	---
	7-8	Req. Service	Integer(16)	2	---
	9-12	Ident.Event	2xInteger(16)	4	---
	13-20	Date	2xLong(32)	8	---
	21-22	Spec.Facil.	Integer(16)	2	TBIT
Body	23	Change Act.	Byte	1	---
	24	Actuat.	Byte	1	CCSACT
	25-28	First CCV	Real	4	CCV
	29-32	Second CCV	Real	4	CCV1
	33-36	Third CCV	Long	4	ENABLE
	37-40	Fourth CCV	Long	4	RF_ACT
	41	Ch. 1st CCV	Byte	1	---
	42	Ch. 2nd CCV	Byte	1	---
	43	Ch. 3rd CCV	Byte	1	---
	44	Ch. 4th CCV	Byte	1	---

Table 4.1.: The RFPS Normal Control message. (Total size: 44 bytes)

with

Family Number	= 173 (Equipment module number for RFPS),
Type	= classification seen from the operation point of view,
Subtype	= classification seen from the specialist point of view,
Serial Number	= the equipment number in the respective family,
Request Service (AMM)	= 0,
Ident. Event	= PLS line number,
Date	= the date,
Spec.Facilties (TBIT)	= 0,
Change Act.	= 1 if CCSACT has changed since previous cycle else 0,
CCSACT	= 1 for OFF, = 2 for STBY (Level 1 ON), = 3 for ON (Level 2 ON), = 4 for RESET,
CCV	= Phase reference (degree),
CCV1	= Amplitude reference (V or dBV),
Ch. CCV flags	= 1 if value has changed since previous cycle else 0.

- The synchronous Control messages:

will only have an header where the Requested Service variable (AMM) is equal to:

- 1 for a Read Back message,
- 2 for a Synchronous Acquisition message (not used in this application),
- 3 for a stored acquisition message (not used in this application),
- 4 for a Status Fault message,
- 5 for a Hardware Specialist Data message.

The Acquisition messages.

- The asynchronous Normal Acquisition message PPM (AMM=0):

is available in the RTI module when the G64 processor has read the equipment status, the digital and analog data and has filled up the RTI Transmit buffer. The following table details the different data.

	Byte Number	Field	Type	Number of Bytes	Property
Header	1-2	Family Number	Integer(16)	2	---
	3-4	Type, Subtype	Integer(16)	2	---
	5-6	Serial Number	Integer(16)	2	---
	7-8	Prov. Service	Integer(16)	2	---
	9-12	Ident.Event	2xInteger(16)	4	---
	13-20	Date	2xLong(32)	8	---
	21-22	Spec.Facil.	Integer(16)	2	TBIT
Body	23	Physical Stat.	Byte	1	PSTAT
	24	Static Stat.	Byte	1	STAQ
	25	Extern.Asp.	Byte	1	ASPEC
	26	Stat.Qualif.	Byte	1	QUALIF
	27-28	Busy Time	Integer	2	BSYTIM
	29-32	First AQN	Real	4	AQN
	33-36	Second AQN	Real	4	AQN1
	37-40	Third AQN	Long	4	st_ENABLE
	41-44	Fourth AQN	Long	4	st_RF_ACT

Table 4.2.: The RFPS Normal Acquisition message.(Total size: 44 bytes)

with:

Header = identical to the last Control message,
PSTAT = 1 for 'Operational', 2 for 'Partially Operational', 3 for 'Not Operational', 4 for 'Needs Commissioning'
STAQ = 1 for 'OFF', 2 for 'STBY', 3 for 'ON'
ASPEC = 1 for 'Not Connected', 2 for 'Local', 3 for 'Remote'
QUALIF = 8 non-exclusive bits with b8 set for ' log bit ',b5 set for the 'Interlocks', b4 set for the 'Non Resettable Faults', b3 set for the 'Resettable Faults', b2 set for the 'Busy' status, b1 set for the 'Warnings'
BSYTIM = not used,
AQN = Phase acquisition (degree),
AQN1 = Amplitude acquisition (V or dBV),

- The synchronous Read Back message (AMM=1):

When the G64 processor receives a control message with a Requested Service (AMM) equal to 1, it fills the Transmit buffer with the last Normal Control message (AMM=0) sent by the DSC, except that the Requested Service value is changed to 1.

- The synchronous Status Fault message (AMM=4):

it contains the status faults of the equipment.

	Byte Number	Field	Type	Number of Bytes	Property
Header	1-2	Family Number	Integer(16)	2	---
	3-4	Type, Subtype	Integer(16)	2	---
	5-6	Serial Number	Integer(16)	2	---
	7-8	Prov. Service	Integer(16)	2	---
	9-12	Ident.Event	2xInteger(16)	4	---
	13-20	Date	2xLong(32)	8	---
	21-22	Spec.Facil.	Integer(16)	2	---
Body	23-26	Warnings	Long(32)	4	FAULT
	27-30	Res. Faults	Long(32)	4	FAULT
	31-34	Non Reset. Faults	Long(32)	4	FAULT
	35-38	Interlocks	Long(32)	4	FAULT

Table 4.3.: The RFPS Synchronous Status message (AMM=4).(Total size: 38 bytes)

Once the system failed in a hardware level 1 or 2 fault, the G64 directly fills a buffer with the date and the fault registers and put the QUALIF in Resettable Fault status. It also fills this buffer if the hardware can not switch On after a software time-out. In that case the QUALIF will indicate a Non Resettable Fault.

In order to tell the upper control level to read this memorized buffer, the G64 puts the MSB of QUALIF high (the so called " log bit").

And in between two normal PPM operations, an application program asks for this synchronous message and puts the fault memory record in a file containing the last 100 failures.
In the application layer one can display these fault messages by means of several sorting and searching procedures and see the detailed fault once the message has been extracted from the fault list database.[10]

- The synchronous Hardware Specialist Data message (AMM=5):

it contains the status faults of the equipment (raw status bits - used by the equipment specialist).

	Byte Number	Field	Type	Number of Bytes	Property
Header	1-2	Family Number	Integer(16)	2	---
	3-4	Type, Subtype	Integer(16)	2	---
	5-6	Serial Number	Integer(16)	2	---
	7-8	Prov. Service	Integer(16)	2	---
	9-12	Ident.Event	2xInteger(16)	4	---
	13-20	Date	2xLong(32)	8	---
	21-22	Spec.Facil.	Integer(16)	2	TBIT
	23-42	Hardw.Registers	20xBytes(8)	20	SAQD

Table 4.4.: The RFPS Synchronous Status message (AMM=5).(Total size: 42 bytes)

2.5.2 The Application Program in the G64 chassis

Generalities

To benefit from many routines already available in the Power Converter and the Stepping Motor G64 applications (MIL driver, Control Protocol), the application program has been written in Pascal language (Flex Omegasoft) .

Once the processor on the CPU card is powered up or receives a manual reset, it begins the main application program (p1.txt). It consists of a continuous loop always looking at the RF status fault after some initializations. This loop is interrupted for the time to execute the routine call sequence (shown in Appendix 7) after each MIL card interrupt.

One can find the up-to-date software modules on the Nice Server in H:database\pcad\rf\hc\ catalog\g64
Appendix 15 lists all routines used and the corresponding module filename.

Some special routines are explained below.

MIL RTI Interrupt routine: INT1.

It is executed when a control message, sent by the Bus Controller in the DSC, has been received in the RTI module (see flow chart in Appendix 5).

As previously mentionned, the assembler routines (MILIN and MILOUT in the 'pe1.ps' file) are indentical to those used in the Power Converter applications.

Equipment status routine: r_stat and chk_st.

The routine *'r_stat'* reads the Amplifier status bits (address pointed by the variables *aml lbr* and *aml hbr i.e the input register of the I/O module*)

According to these bits, the routine *chk_stat* produces the 4 status values (PSTAT, STAQ, ASPEC and QUALIF) which will be put in the Normal Acquisition message.
The four following tables show which of the status bits are used to determine the value for those.

L2 Ready (b5)	L1 Ready (b2)	STAQ Value	STAQ meaning
-	0	1	Off
0	1	2	Standby
1	1	3	On

System Local (b12)	System Remote (b11)	ASPEC Value	ASPEC meaning
1	1	1	Not Connected
0	0	1	Not Connected
1	0	2	Local
0	1	3	Remote

Intk (b14)	RFft (b13)	RF (b9)	En (b7)	L2f (b6)	L2r (b5)	L2s (b4)	L1f (b3)	L1r (b2)	L1s (b1)	QUALIF bit set	QUALIF meaning
-	-	-	-	-	-	-	-	-	-	8	Logbit
0	-	-	-	-	-	-	-	-	-	5	Interlock
-	-	-	-	-	-	-	-	-	-	4	Non Resetable Fault
-	-	-	-	1	-	-	-	-	-	3	Resetable Fault
-	-	-	-	-	-	-	1	-	-	3	Resetable Fault
-	-	-	-	-	-	-	-	0	1	2	Busy
-	-	-	-	-	0	1	-	-	-	2	Busy
-	1	-	-	-	1	-	-	-	-	1	Warning
-	-	-	0	-	1	-	-	-	-	1	Warning
-	-	0	-	-	1	-	-	-	-	1	Warning

ASPEC	QUALIF	PSTAT Value	PSTAT meaning
Remote	No bit set	1	Operational
Remote	Busy	1	Operational
Remote	Warning	2	Partially Op.
-	Interlock	3	Not Operational
-	Non Resetable Fault	3	Not Operational
-	Resetable Fault	3	Not Operational
Local	-	3	Not Operational

Actuation routine: s_act.

When a new actuation is received, **the command sent to the equipment depends on the present status of the amplifier and this new actuation,** as shown in the next table.
Note that:
' Equipment OFF ' means : L1= OFF and L2= OFF;
' Equipment STBY ' means : L1= ON and L2= OFF;
' Equipment ON ' means : L1= ON and L2= ON.

Present State (input register)				New Actuation	Pulsed Com. sent (output register)				
L2 r (b4)	L2 so (b3)	L1 r (b2)	L1 so (b1)		RESET (b5)	L2 OFF (b4)	L2 ON (b3)	L1 OFF (b2)	L1 ON (b1)
-	1	-	-	OFF		1			
1	-	-	-	OFF		1			
0	0	-	1	OFF				1	
0	0	1	-	OFF				1	
-	1	-	-	STBY		1			
1	-	-	-	STBY		1			
-	-	0	0	STBY					1
-	-	0	0	ON					1
0	0	1	-	ON			1		
-	-	-	-	RESET	1				

N.B : when a reset actuation is asked, the G64 first generates one reset hardware pulse to the equipment, then executes the memorized actuation preceding the reset command.

2.5.3 Front end computer side

The Real Time process (see Figure 4).

It reads the PLS telegram when this has been received in the FPIPLS VME module.

When an interrupt occurs on FPI1 on the same hardware module, it:
- sends, for the next PPM cycle, the corresponding new Normal Control message from the Equipment Module Data Table to each RTI module connected to the MIL Bus Controller VME module
- waits approximately 100 ms
- reads, for the current PPM cycle, the Normal acquisition message in the Transmit Buffer of each RTI module connected to the MIL Bus Controller VME module
- stores it in the Equipment Module Data Table.

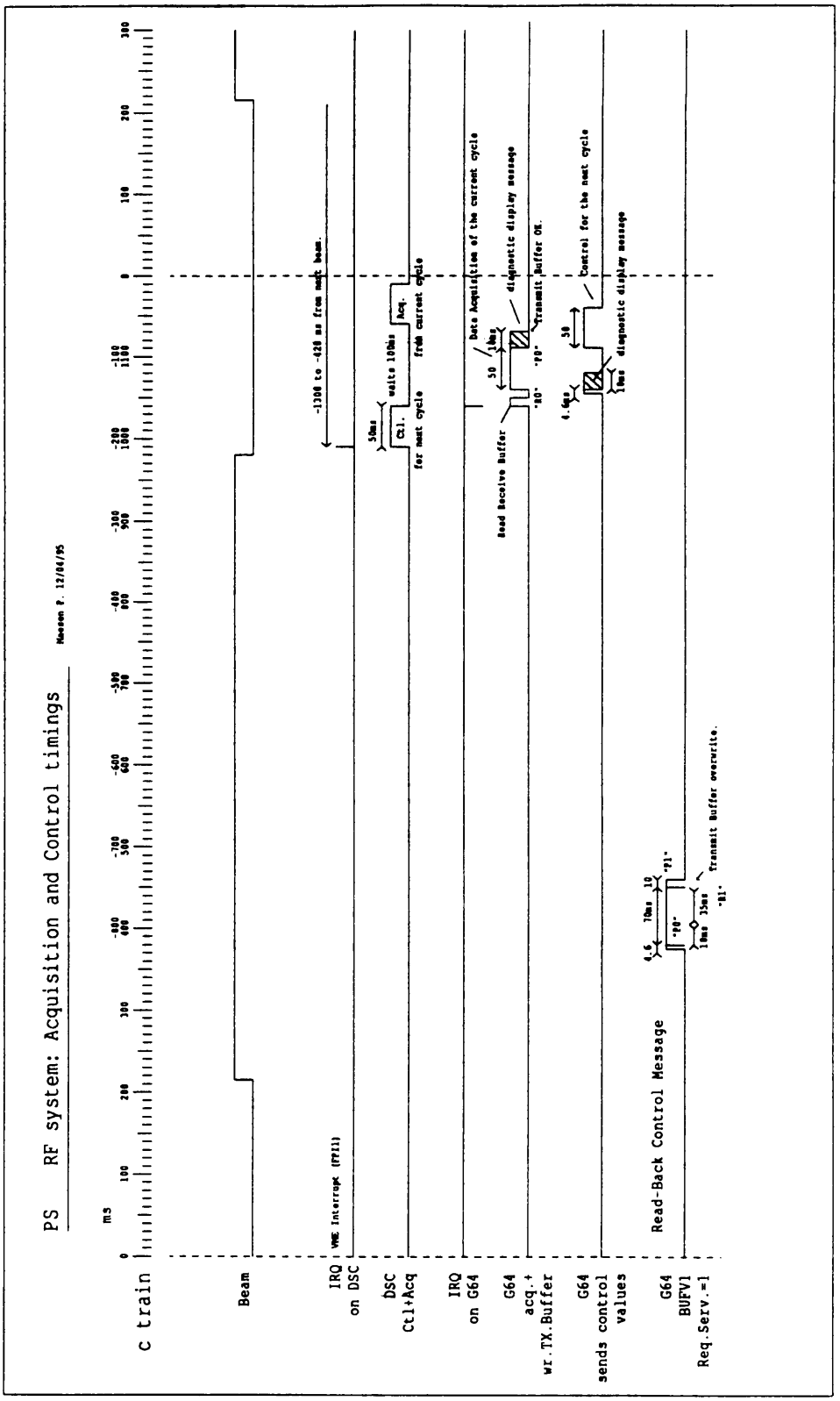


Fig.4: Chronology of events during Control, Acquisition and Read Back messages in the PS.

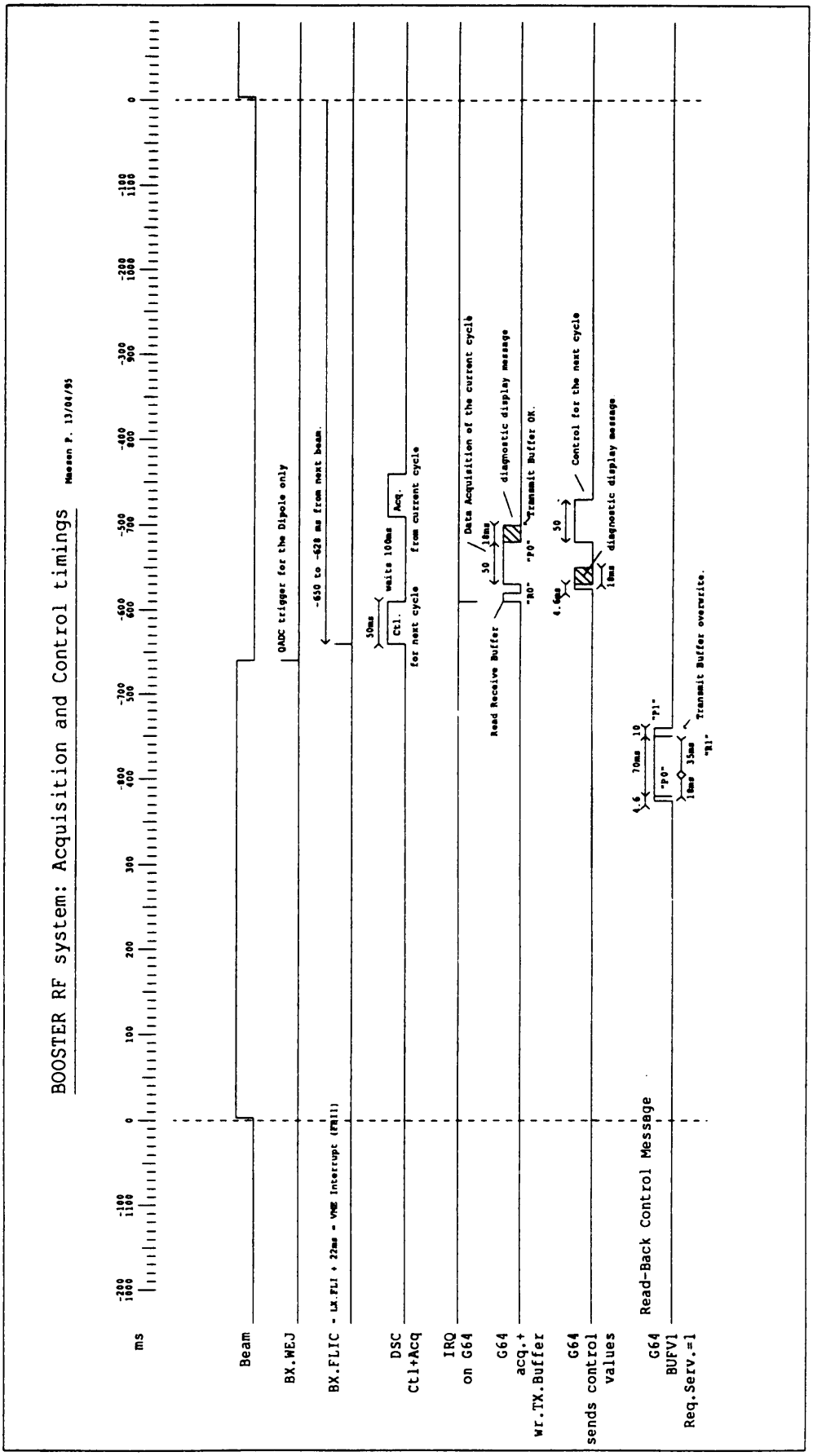


Fig.4 bis: Chronology of events during Control, Acquisition and Read Back messages in the PSB.

3. STAND-ALONE CONTROL

3.1 Basic ideas

As shown in Figure 1 at the beginning of this document, the control of an equipment requires a lot of hardware and software modules.

Moreover, these are designed and maintained by different teams (ex: CO, RF, POW, .. groups).

In this context, tools which can replace or emulate some parts of the system are very useful for new design, maintenance and troubleshooting.

For this purpose, the 'Mil-trotinette', based on the very useful 'STE trotinette' has been designed by Abtamu Abie and Gérard Coudert.

As it was specially made for the Power Converter specialist, it has been extended for other equivalent equipment : Step, RF LIN station, RF PSB station, DC motor [8].

3.2 Control of an RTI equipment with the MIL-trotinette

In this case, the G64 equipment interface is disconnected from the MIL bus and connected to the MIL-trotinette which replaces the control part of the system (stand-alone control).

This allows to manually:

- send actuation and control values to the equipment (Normal Control message),
- read acquisition from the equipment (Normal Acquisition message),
- execute some specific MIL diagnostic functions.

3.3 Emulation of an RTI equipment with the MIL-trotinette

For the control interface point of view, it is now easy to emulate the equipment (in this case, the RF station) interfaced with the MIL bus and controlled with the Control Protocol.
The functions implemented in the emulator are:

- to accept standard control messages from the DSC,
- to write standard acquisition messages to the transmit buffer,
- to allow the user to specify values to be written in:

• the header of the acquisition message (Family, Type, Subtype, Ser.Numb.,...)
• the body of the acquisition message (PSTAT, STAQ, ASPEC, QUALIF, BSYTIM, and AQNs)

For this application, the MIL-trotinette is connected directly to the local MIL bus and replaces the G64 equipment interface (Do not forget to set the same address for the RTI module in the MIL-trotinette).

4. DIAGNOSTIC FACILITIES

4.1 System Configuration

Since one uses the MIL-trotinette, the G64 equipment interface is disconnected from the control system which is not useful for PPM diagnostic.

Some extra diagnostic facilities have then been installed to give information on the messages exchanged between the BC VME module in the DSC crate and the RTI module in the G64 chassis.

This information is sent to the RS232 port on the local processor module and can be displayed when one connects a terminal to it.

As the write access to this IO port takes CPU time, only a few characters are displayed in normal operation.

In case of serious problems and if more information is required on the MIL data, the bit 16 on the I/O card will be set to OPEN (0) and the G64 system will be rebooted; this bit is only checked at system initialisation.

Note that as many characters are displayed, the PPM process in the G64 can be disturbed.

4.2 Diagnostic displays

Short diagnostic message.

Characters displayed are:

'Rx' when a correct (MIL and Control Protocol conformities) message has been received in the Receive Buffer of the RTI module. The second character indicates the requested service type (AMM).

'Px' when a reading routine has been executed, meaning that the G64 CPU has written data to the Transmit Buffer in the RTI module. The second character indicates the provided service type (AMM)

'NoChAct' or *'NoCHCcv xx'* when a correct (MIL and Control Protocol conformities) message has been received in the Receive Buffer of the RTI module; but the 'change flag indicator' is zero. No action will be taken for the corresponding parameter (Actuation or CCVs).

'Réception non encore identifiée' when a message has been received by the RTI module but does not conform with the QuickData packet.

'Message is not for RFPS EM' when a correct (MIL and Control Protocol conformities) message has been received in the Receive Buffer of the RTI module but the Family Number is not correct. This can occur:

- when data in the message are wrong or,
- when different kind of equipment are connected to the MIL bus and when 2 RTI modules have the same MIL address.

One equivalent long message is written with the detailed status interlock when the system fails in resetable or non-resetable fault.

Long diagnostic messages.

The following displays appear when:

a) a new message is received in the RTI module. This shows the raw data in hex format. For a Normal Control message , the data can be related to table 4.1. in section 2.5.1.

Message received:
00 AD 01 02 17 7F 00 00 00 04 00 08
00 7E B4 20 91 BC 04 A0 00 00 01 03
42 34 00 00 44 9C 40 00 00 00 00 01
00 00 00 00 01 01 00 00

b) the message conforms to a Normal Control message. Data for the next cycle are decoded and can be related to the table 4.1. in section 2.5.1. As the Change Flag indicator for Val3,4 is zero, Val3,4 are not significant (NoChCcv3, NoChCcv4).

The CCVs are displayed in real format.

Req.Serv.= 0
CONTROL:

Eq.Mod.	= 00 AD				
Type	= 01				
Sub-type	= 02				
Eq.Numb.	= 17 7F				
Req.Serv.	= 00 00				
Id.Event	= 00 04				
Pulse Ev.	= 00 08				
Date	= 00 7E B4 20 91 BC 04 A0				
Spec.Fac.	= 00 00			*[Means:*	
Ch.Act.	= 0001	Actuat.	= 0003	*[Actuation*	*= ON*
Ch.Val1	= 0001	Val1	= 4.500000E+01	*[CCV Phase*	*= 45 degree*
Ch.Val2	= 0001	Val2	= 3.600000E+01	*[CCV Amplifier*	*= 36dBV*
Ch.Val3	= 0000	Val3	= 1.000000E+00	*[Enable*	*= ON*
Ch.Val4	= 0000	Val4	= 0.000000E+00	*[RFact*	*= OFF*

R0
NoChCcv3
NoChCcv4

c) the reading routine has been executed, meaning that the G64 CPU has written data of the current cycle to the Transmit Buffer in the RTI module.

```
P0
ACQUISITION:
Eq.Mod.        = 00 AD
Type           = 01
Sub-type       = 02
Eq.Numb.       = 17 7F
Prov.Ser       = 00 00
Id.Event       = 00 03
Pulse Ev.      = 00 02
Date           = 00 7E B4 24 E3 45 12 9B
Spec.Fac.      = 00 00
Phys.St.       = 2  (1-OPERAT, 2-PARTLY, 3-NONOPERAT, 4-NEEDSCOM)
Stat.St.       = 3  (1-OFF  , 2-STBY  , 3-ON     , 4-RESET)
Ext.Asp.       = 3  (1-NOTCON, 2-LOCAL , 3-REMOTE)
St.Qual.       = 00 (10-INTERLOCK,8-NRFAULT,4-RFAULT,2-BUSY,1-WARNG)
1  4.763000E+01
2  3.596400E+01
3  0.000000E+00
4  0.000000E+00
```

4.3 Interrupt diagnostic

An additionnal diagnostic test is available when one plugs a GESINP-1A&B module with the base address $E102 (see Appendix 7 - Test Card) to the G64 chassis.
Data are written to this test module when the interrupt routine is executed.

By observing the 4 LSB on it (with a scope or, better with the special diagnostic module), one can verify if this process works correctly.

REFERENCES

[1] Final report on the uniform equipment access at CERN, the USAP, CERN/ps 93-16 (CO).

[2] DAC16_RLP, G. Coudert, PS/PO/GC 13/11/89

[3] QADC G64 module, Cl. Dehavay, PS/CO/ Note 93-79.

[4] MIL-1553-b Multidrop Bus for controlling LEP and SPS equipment - User's Manual, D. Francart, M. Pressevot, R. Rausch, J.M. Sainson, O. van der Vossen and R. Wilhelm, SPS/ACC/Note 85-26.

[5] The MIL-1553 VME driver. SL/CO/Note
The FPI-PLS VME driver. C.Dehavay, A. Gagnaire, PS/CO/Note 93-48.

[6] Generalities on the Operational Control Protocol, G.Benincasa, PS/CO Note 91-01.

[7] Interface message MIL-1553 a transfert par tampons, P. Charrue - SPS/ACC/Note 87-02.

[8] The RFPS Equipment Module documentation. U.Davydenko, L. Merard, PS/CO.

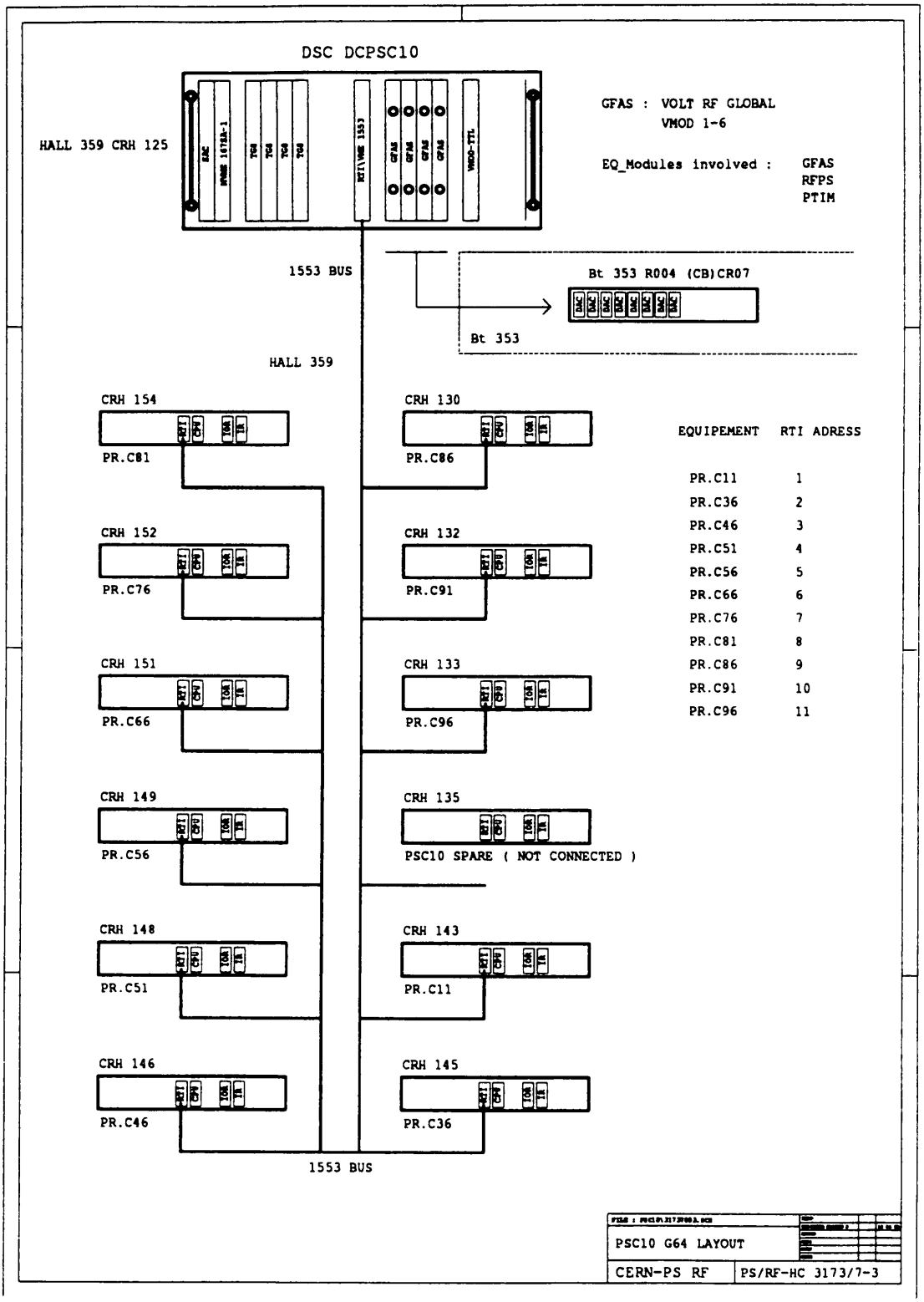
[9] Standalone facilities to control PS G64 equipment connected to the MIL-1553 bus. C. Dehavay PS/CO/Note 93-72.

[10] The fault history report facility, Mark Beharrell, to be published, PS/CO/Note 95-.

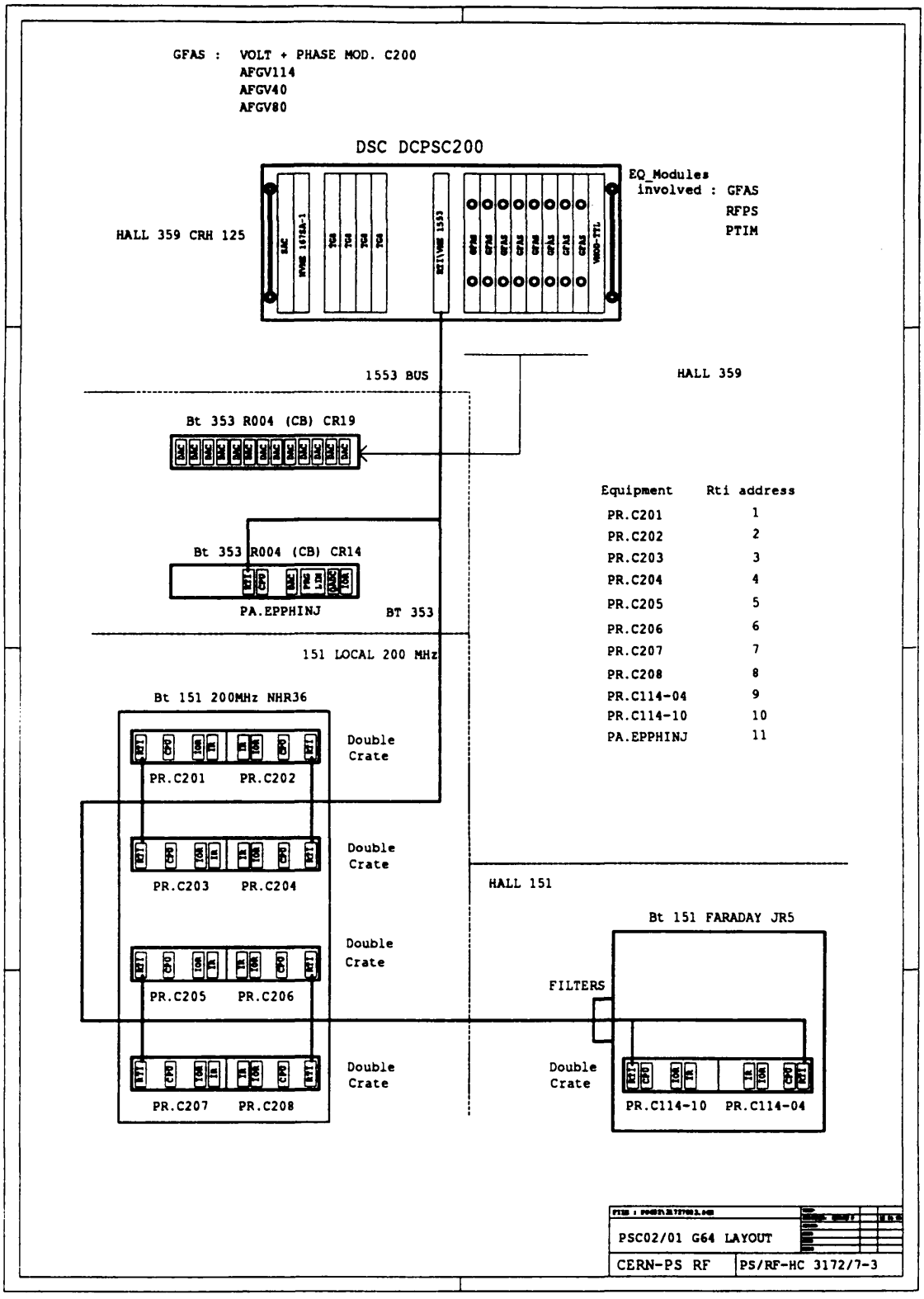
Distribution

PS/RF-HC section
PS/RF-LL section
G.P. Benincasa
G. Daems
C. Dehavay
F. di Maio
R. Garoby
W. Heinze
L. Merard
F. Perriollat

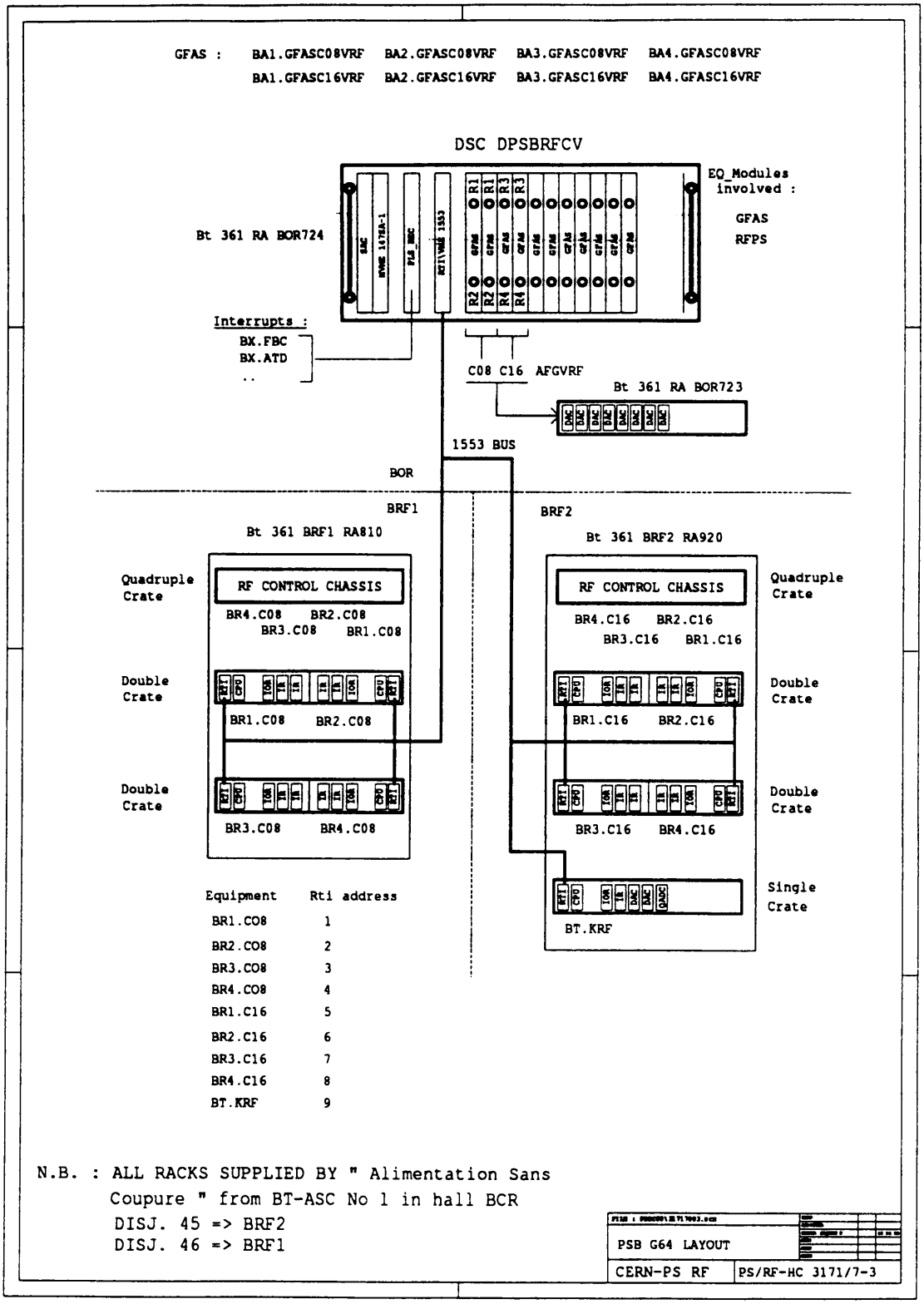
Appendix 1: PSC10 G64 layout.



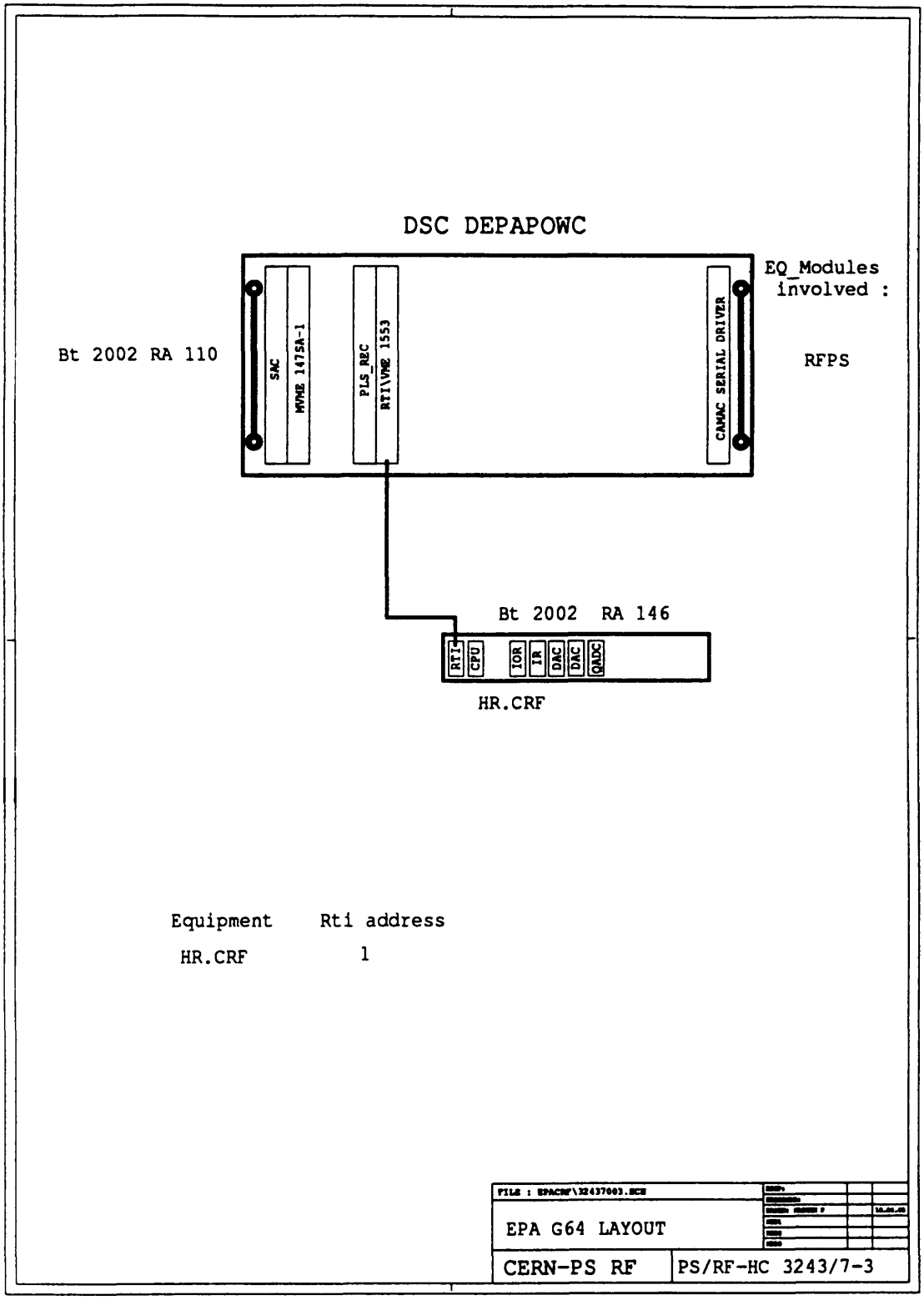
Appendix 2: PSC01-02 G64 layout.



Appendix 3: PSB G64 layout.



Appendix 4: EPA G64 layout.



Appendix 5: Routine call sequence after a MIL card interrupt.

INT 1

```
-mil_read
          -milin
          -milin
          -msg_rcpt
          if AMM=0 =>   [ lg_cmsg ]
                        " R0 "
                        -s_amsg      (the current cycle)
                                     -acquis
                                                  -rstat
                                                  -chk_st
                                                  if fault =>   -flt_rec
                                                  -r_aqnd
                                                  -cv_acq
                                     -send_acqmsg
                                                  -send_msg
                                                                -swap_header
                                                                -milout
                                                                -milout
                                                                " P0 "
                                                  [lg_amsg ]
                        -control     ( the next cycle)
                                     -s_act
                                                  -rstat
                                     -s_ccvs
                                                  -phr_cv
          if AMM=1 =>                             -amr_cv
                        " R1 "
                        -send_msg
                                     -swap_header
                                     -milout
                                     -milout
          if AMM=4 =>                " P1 "
                        -s_aq04
                                     " RS4 "
                                     -send_msg
                                                  -swap_header
                                                  -milout
                                                  -milout
          if AMM=5 =>                             " P4 "
                        -s_aq05
                                     " RS5 "
                                     -send_msg
                                                  -swap_header
                                                  -milout
                                                  -milout
end                                               " P5 "
```

One finds in between [ ] the executed routines when the diagnostic flag is active.
One finds comments in between ( ).
And one finds in between " " the message sent to the RS232 port when normal operation is active.

Appendix 6: RFPS family number classification.

EQUIPMENT MODULE : RFPS
FAMILY NUMBER : 173 or AD hexa

SERIAL NUMBER	EQUIPMENT	DSC	BC	RTI	TYPE	SUBTYPE
3001	BR1.C08	DPSBRFCV	1	1	1	6
3002	BR2.C08	DPSBRFCV	1	2	1	6
3003	BR3.C08	DPSBRFCV	1	3	1	6
3004	BR4.C08	DPSBRFCV	1	4	1	6
3005	BR1.C16	DPSBRFCV	1	5	1	7
3006	BR2.C16	DPSBRFCV	1	6	1	7
3007	BR3.C16	DPSBRFCV	1	7	1	7
3008	BR4.C16	DPSBRFCV	1	8	1	7
3009	BT.KRF	DPSBRFCV	1	9	2	8
6001	PR.C11	DCPSC10	1	1	1	1
6002	PR.C36	DCPSC10	1	2	1	1
6003	PR.C46	DCPSC10	1	3	1	1
6004	PR.C51	DCPSC10	1	4	1	1
6005	PR.C56	DCPSC10	1	5	1	1
6006	PR.C66	DCPSC10	1	6	1	1
6007	PR.C76	DCPSC10	1	7	1	1
6008	PR.C81	DCPSC10	1	8	1	1
6009	PR.C86	DCPSC10	1	9	1	1
6010	PR.C91	DCPSC10	1	10	1	1
6011	PR.C96	DCPSC10	1	11	1	1
6015	PR.C201	DCPSC200	1	1	1	2
6016	PR.C202	DCPSC200	1	2	1	2
6017	PR.C203	DCPSC200	1	3	1	2
6018	PR.C204	DCPSC200	1	4	1	2
6019	PR.C205	DCPSC200	1	5	1	2
6020	PR.C206	DCPSC200	1	6	1	2
6021	PR.C207	DCPSC200	1	7	1	2
6022	PR.C208	DCPSC200	1	8	1	2
6024	PR.C114-04	DCPSC200	1	9	1	3
6025	PR.C114-10	DCPSC200	1	10	1	3
6026	PA.EPPHINJ	DCPSC200	1	11	3	4
9001	HR.CRF	DEPAPOWC	1	1	4	5

Appendix 7: Adresses settings for the PS interfaces modules.

RF IO-Cards addresses configuration

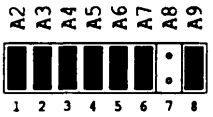
Maesen P.11/04/94

Test Card:

Type : GESINP-1A&B

Address: $E100-$E103

Jumpers:

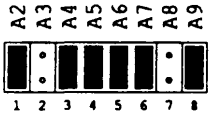


Amplifier (Act.+ Stat.):

Type : GESINP-1A&B

Address: $E108-$E10B

Jumpers:

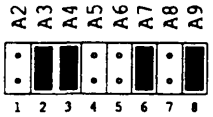


Fault memory 1-4 (Acq.):

Type : GESINP-2A

Address: $E164-$E167

Jumpers:

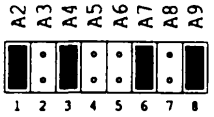


Fault memory 5-8 (Acq.):

Type : GESINP-2A

Address: $E168-$E16B

Jumpers:

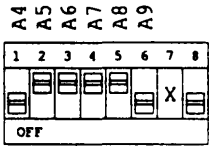


ADC 1 (Amplifier Acq.):

Type : Cern-QADC-J14945

Address: $E210-$E21F

Jumpers:

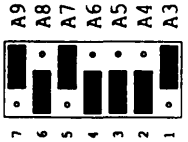


DAC 1 (Amplifier Ctl.):

Type : Cern-DAC-J14512

Address: $E170-$E177

Jumpers:

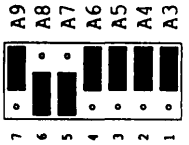


DAC 2 (Amplifier Ctl.):

Type : Cern-DAC-J14512

Address: $E180-$E187

Jumpers:



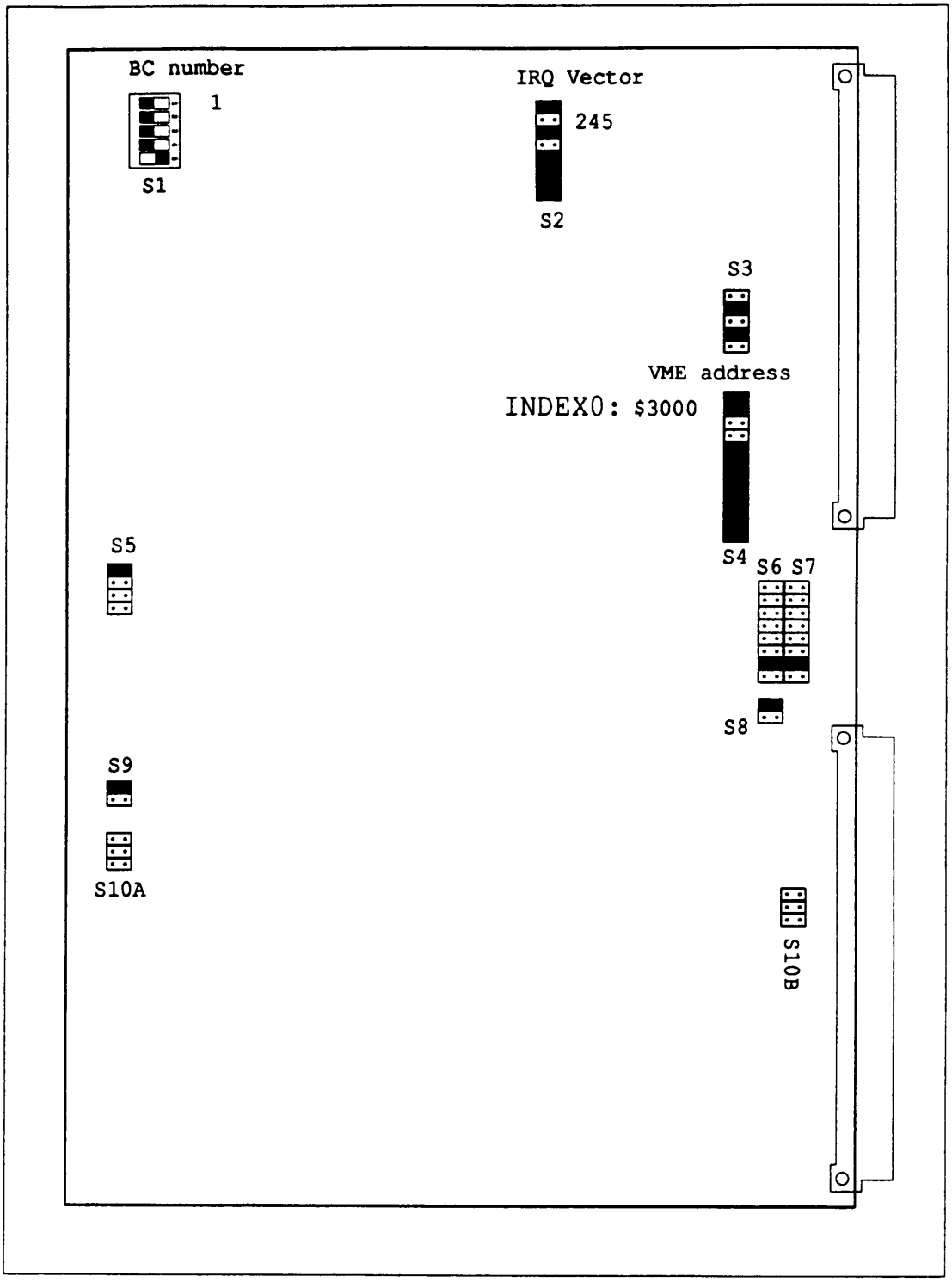
Appendix 8: Memory map for the CE3000 module.

Address (Hexadecimal)	Chip	Function	Value
FFFE-FFFF FFF8-FFF9 .. F000	 EPROM 4K 2732 IC9	Start Program Pointer Interrupt Routine Pointer	$4000 $BFF8
EFFF .. E000	Input/ Output VPA	See Appendix 7	
DFFF .. C000	RAM 8K HM6264 IC13	Variables	
BFFF BFF8 4000	 EPROM 32K 27256 IC2	Interrupt Routine address Application Program	
3FFF .. 0000	EPROM 16K 27128 IC6	Not used	

Appendix 8 bis: Memory map for the CPU RAM-ROM PS/PO 24168P module.

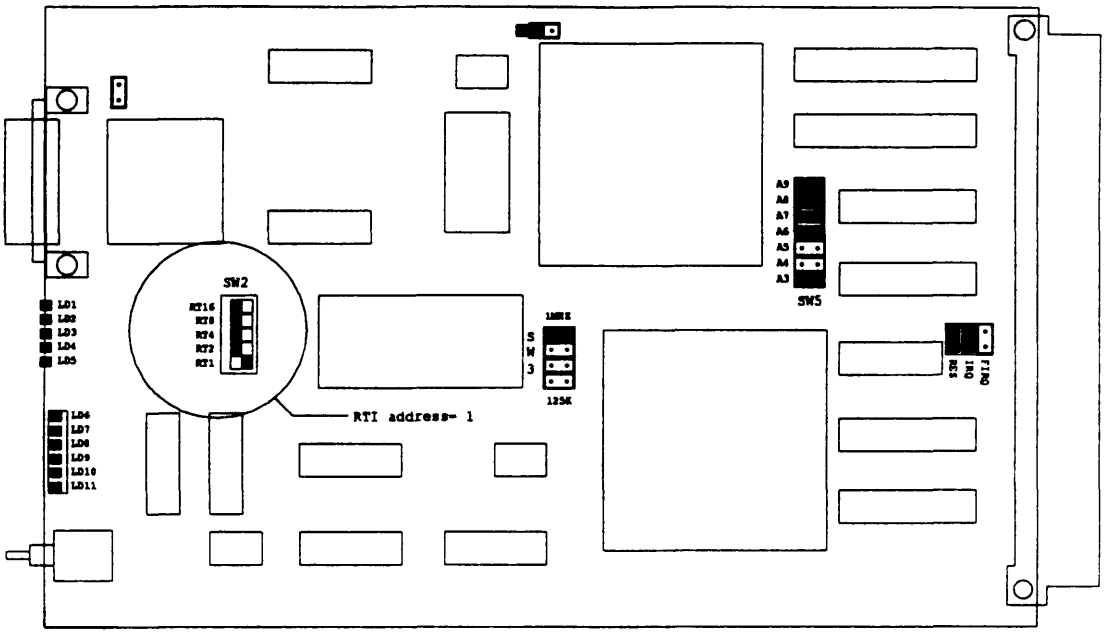
Address (Hexadecimal)	Chip	Function	Value
FFFE-FFFF FFF8-FFF9 .. F000	 EPROM 4K 2732 IC9	Start Program Pointer Interrupt Routine Pointer	$4000 $BFF8
EFFF .. E400		Not used	
E3FF .. E000	Input/ Output VPA	See Appendix 7	
DFFF .. C000	RAM 8K HM6264 IC13	Variables	
BFFF BFF8 4000	 EPROM 48K 27C512 IC2	Interrupt Routine address Application Program	
3FFF .. 0000		Not used	

Appendix 9: Jumpers settings for the MIL1553 Bus Controler VME module.

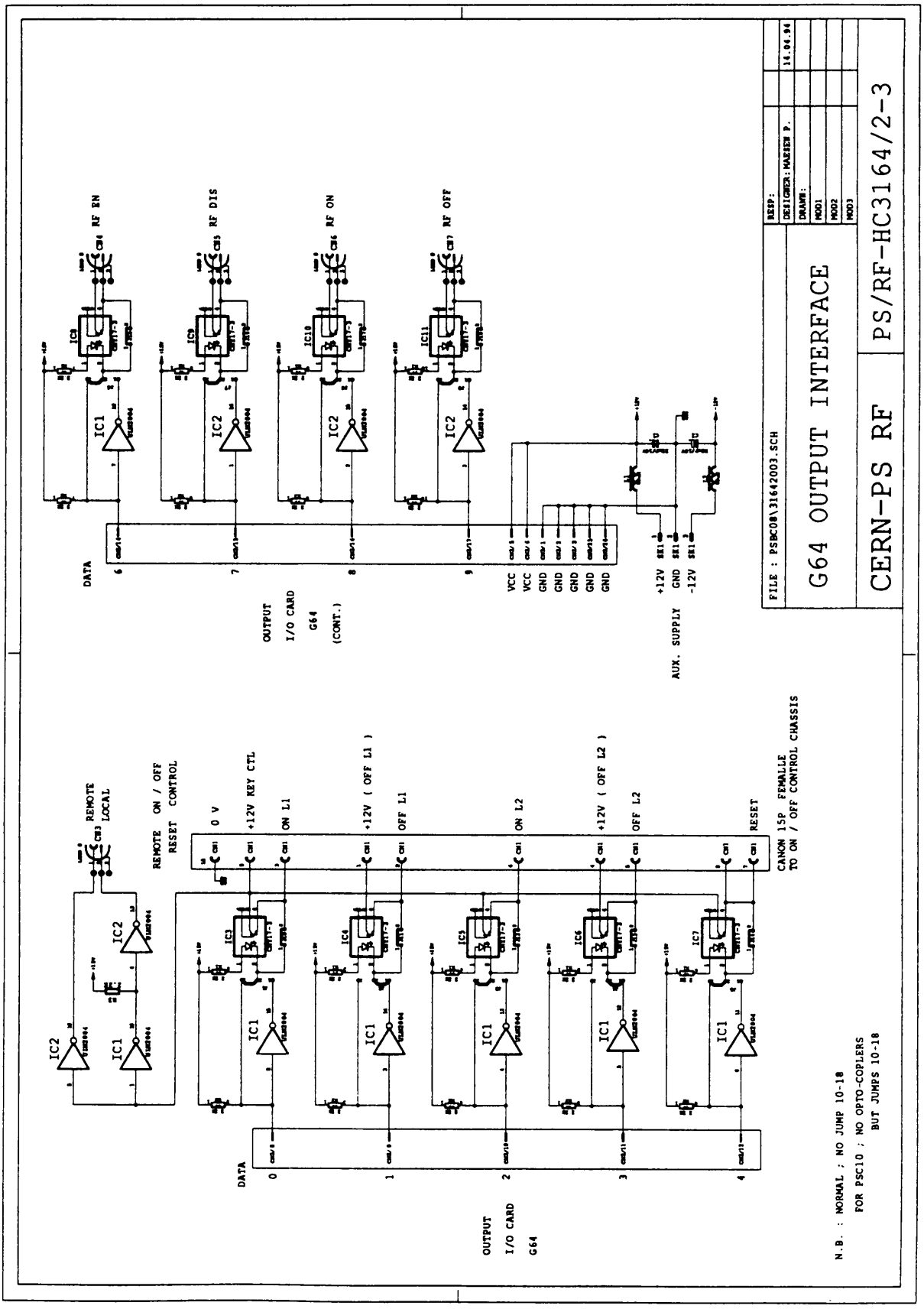


Appendix 10: Jumpers setting for the RTI module.

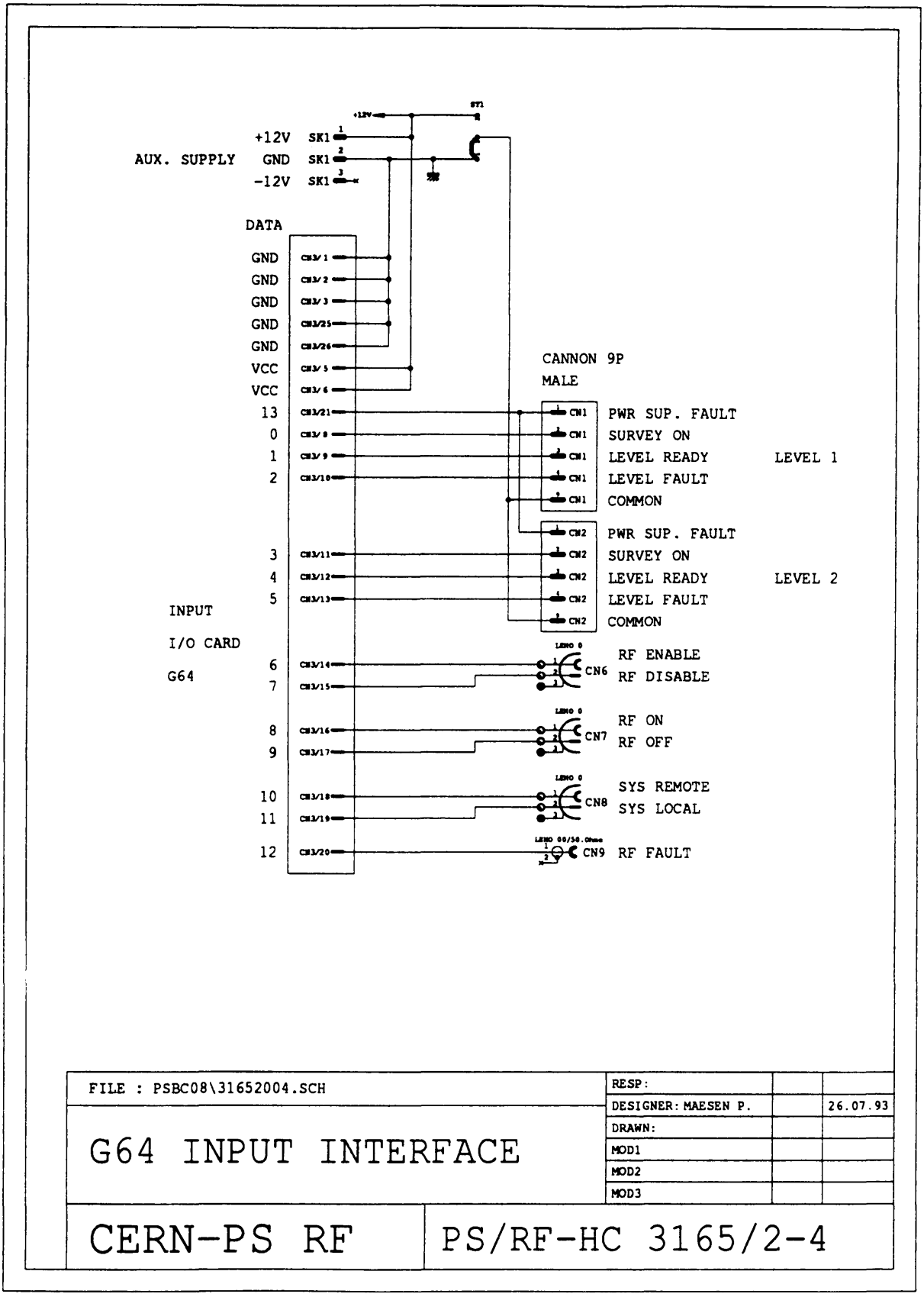
RTI address is set with jumper SW2. Other jumpers must be set as indicated here.:



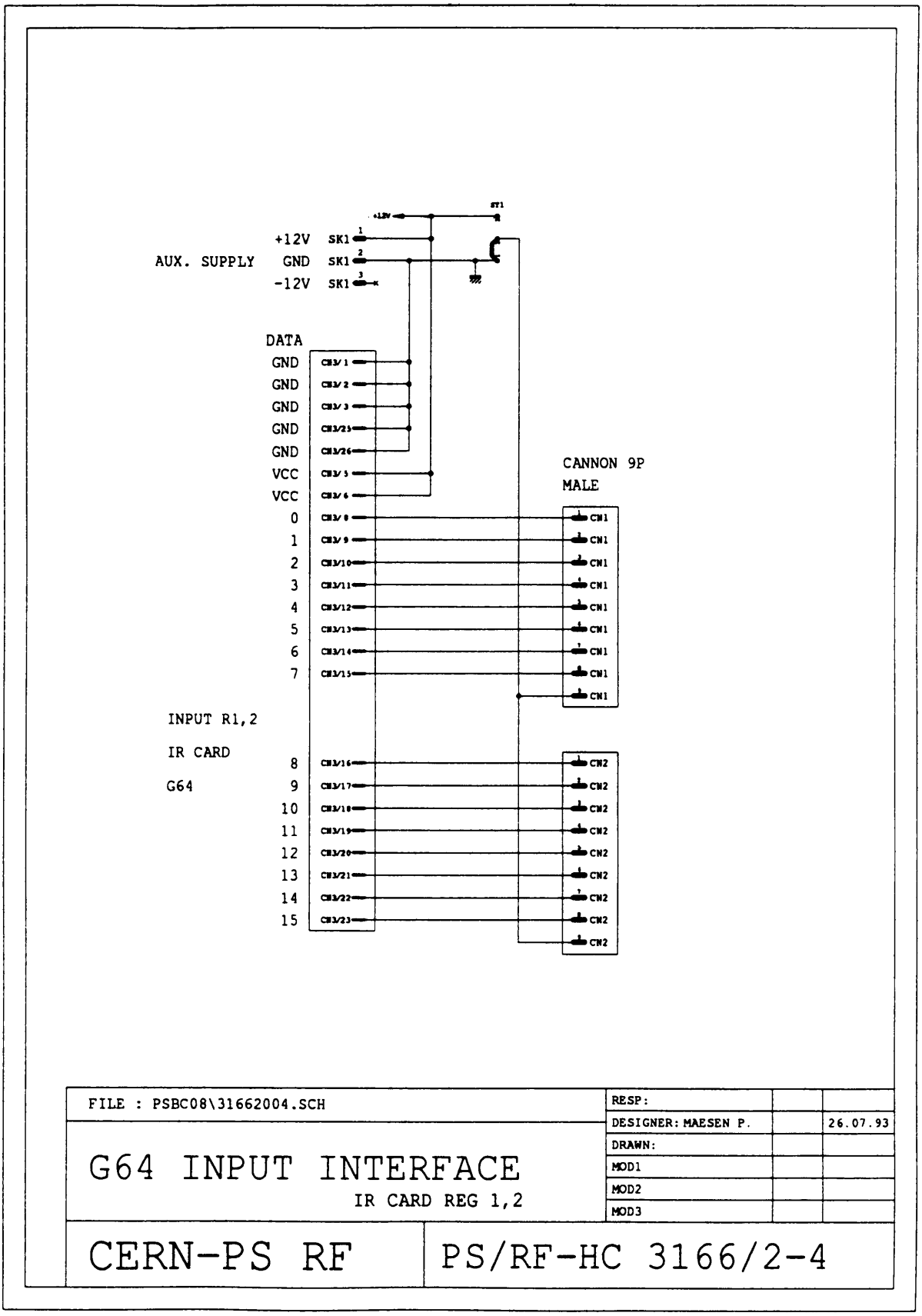
Appendix 11: G64 I/O output - Interlock interface.



Appendix 12: G64 I/O input - Interlock interface.



Appendix 13: G64 IR input - Interlock interface.



Appendix 14: Routines and module filename used in the G64 application program.

routine or function	file-name	description
	adc_ad.txt	contains QADC hardware addresses
	mil.inc	contains RTI hardware addresses
	p1.txt	main for Application Program
	pe1.cf	chain file that compiles and assembles
	pe3.cf	chain file that links and generates binary file
	pe1.ps	program stack + assembly routines
	pf_io.txt	contains I/O module hardware addresses
	pi.txt	initialises variables
	pmil.txt	MIL driver routines
	pmil2.txt	MIL driver routines
	pp.txt	control protocol routines
	pq.txt	routines for Qadc module
	pteph.txt	routines for I/O modules (except for QADC)
	px1.txt	extra routines
	px2.txt	extra routines
	parf.txt	global variables
acquis	pp.txt	general acquisition routine
amr_cv	pteph.txt	sends new amplitude reference
c_reset	pteph.txt	sends actuation RESET to amplifier
c_ofl1	pteph.txt	sends actuation OFF L1 to amplifier
c_ofl2	pteph.txt	sends actuation OFF L2 to amplifier
c_onl1	pteph.txt	sends actuation ON L1 to amplifier
c_onl2	pteph.txt	sends actuation ON L2 to amplifier
chk_st	px2.txt	checks equipment status (PSTAT, ASPEC,..)
control	pp.txt	checks message and send control values to eq.
cv_acq	px2.txt	re-arrange acq.values (AQN,AQN1,AQN2)
dectomin	pteph.txt	translates from degree (dec.) to degree,min,sec
del50	px2.txt	is a software delay
delay	pteph.txt	software delay
discv	pq.txt	disables conversion on QADC module
encv	pq.txt	enables conversion on QADC module
flt_rec	px2.txt	records fault status in memory
header_init	pmil.txt	initialises message header
imax	pi.txt	sets max values of variables
imin	pi.txt	sets min values of variables
init	pi.txt	initialises variables
in_sf	pi.txt	initialises the scaling factors
int1	pmil.txt	treats MIL interrupt
int2	pq.txt	treats interrupt from QADC module (not used)
lg_amsg	px1.txt	for test: displays acquis. message in detail
lg_cmsg	px1.txt	for test: displays control message in detail
lsb4	rteph.txt	4 LSB bits conversion
mil_main	pmil.txt	Initialises RTI module
mil_read	pmil.txt	Reads RTI Receive buffer
msg_rcpt	pmil2.txt	message reception
phs_cv	pteph.txt	sends new phase reference
r_aqnd	pq.txt	reads direct acquisition values
r_stat	pteph.txt	reads direct equipement status
readflgd	pq.txt	reads diagnostic bit in QADC module

Rlgint	pp.txt	Converts IEEE floating-point bytes to OmegaSoft long integer format
RReal	pmil2.txt	Converts IEEE floating-point bytes to OmegaSoft real format
rst_tio	pteph.txt	reset the unresetable fault time-out
s_act	px2.txt	sends actuation to amplifier
s_amsg	px1.txt	get acquis., and sends it to RTI buffer
s_ccvs	px2.txt	sends control values to equipment
s_aq04	px2.txt	sends fault acquisition message
s_aq05	px2.txt	sends specialist acquisition message
sconv	pq.txt	triggers softw. conversion on QADC module
send_acqmsg	pmil2.txt	sends ppm acquisition message
send_msg	pmil.txt	Writes RTI Transmit buffer
swap_header	pmil.txt	Swaps Quick packet header
Wlgint	pmil2.txt	Converts the OmegaSoft long integer to IEEE floating-point form
WReal	pmil2.txt	Converts the OmegaSoft real to IEEE floating-point form