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CERN - PS DIVISION

PS/ RF/ Note 95-05

AUTOMATIC DELAY COMPENSATION (PS/RF-LL 2059)

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Geneva, Switzerland
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1. INTRODUCTION

An "automatic delay compensation" is part of the "one turn delay feedback" system used in the CERN PS accelerator. It is represented as the one turn delay in Figure 1.

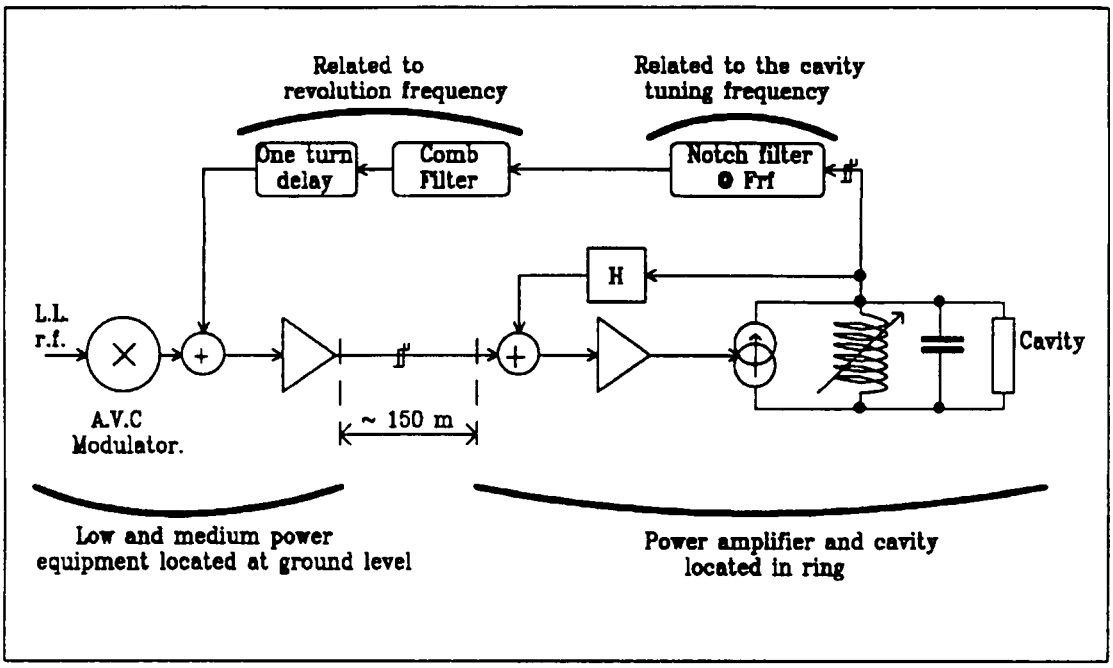


Figure 1. Overall block diagram of the PS "one turn delay feedback".

The aim of this circuit is to ensure that the total loop delay will remain equal to the variable revolution period T_{rev}, during the whole acceleration process.

Let "t_V" be the variable delay obtained in the "automatic delay compensation" and "t_0" the fixed delay in the rest of the loop.

We would like to have $T_{rev} = t_V + t_0$ at any time during the acceleration cycle.

2. DESCRIPTION

The principle of operation of an automatic delay compensation is shown schematically in Figure 2.

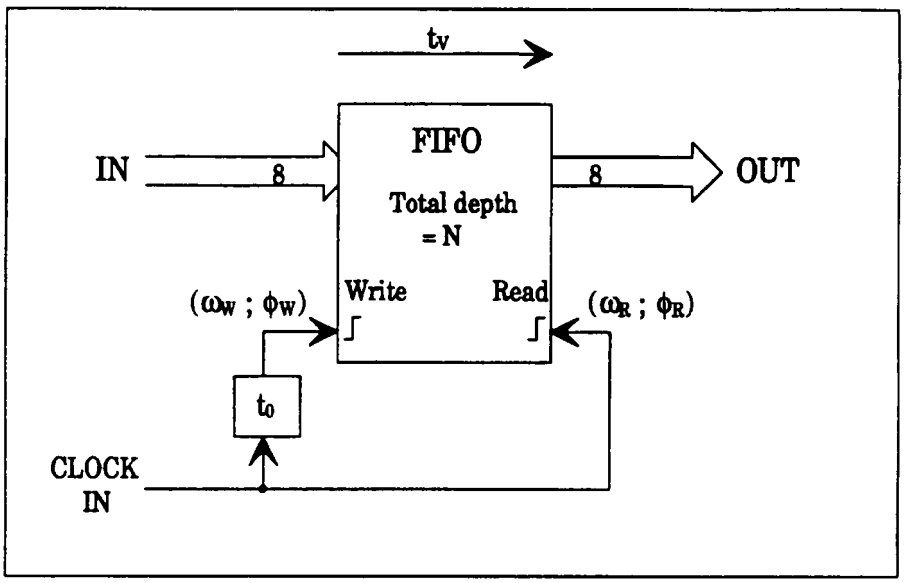


Figure 2. Simplified block diagram of an automatic delay compensation.

To simplify the later expressions, we shall assume the clock frequency variation during t_V or t_0 to be negligible.

This is to say:

$$\omega_W(t) = \omega_R(t) = \omega_{clk}(t).$$

This assumption is valid for the practical case encountered in the PS where:

$t_V < t_0 \leq 2\ \mu s$

$f_{clk} = 80.f_{rev}$

f_{rev} mean value $\approx$ 450 kHz

$f_{rev} / dt \leq 8$ Hz / μs

This means that the clock frequency variation is smaller than 354.10^{-5} % during t_0 in this application.

Considering these simplifications and using Figure 3 for a graphical interpretation, we can write the total delay experienced by a data passing through the FIFO at a given time:

$$t_V(t) = N_0.T_{clk}(t) - t_0 \qquad (1)$$

t_V: total delay through the FIFO.

T_{clk} : clock period

N_0 : total depth of the FIFO (in term of memory cells) measured when $T_{clk} > t_0$.

t_0 : delay between "read"and "write" clock

Equation (1) results from the typical behaviour of a FIFO, described in Figure 3.

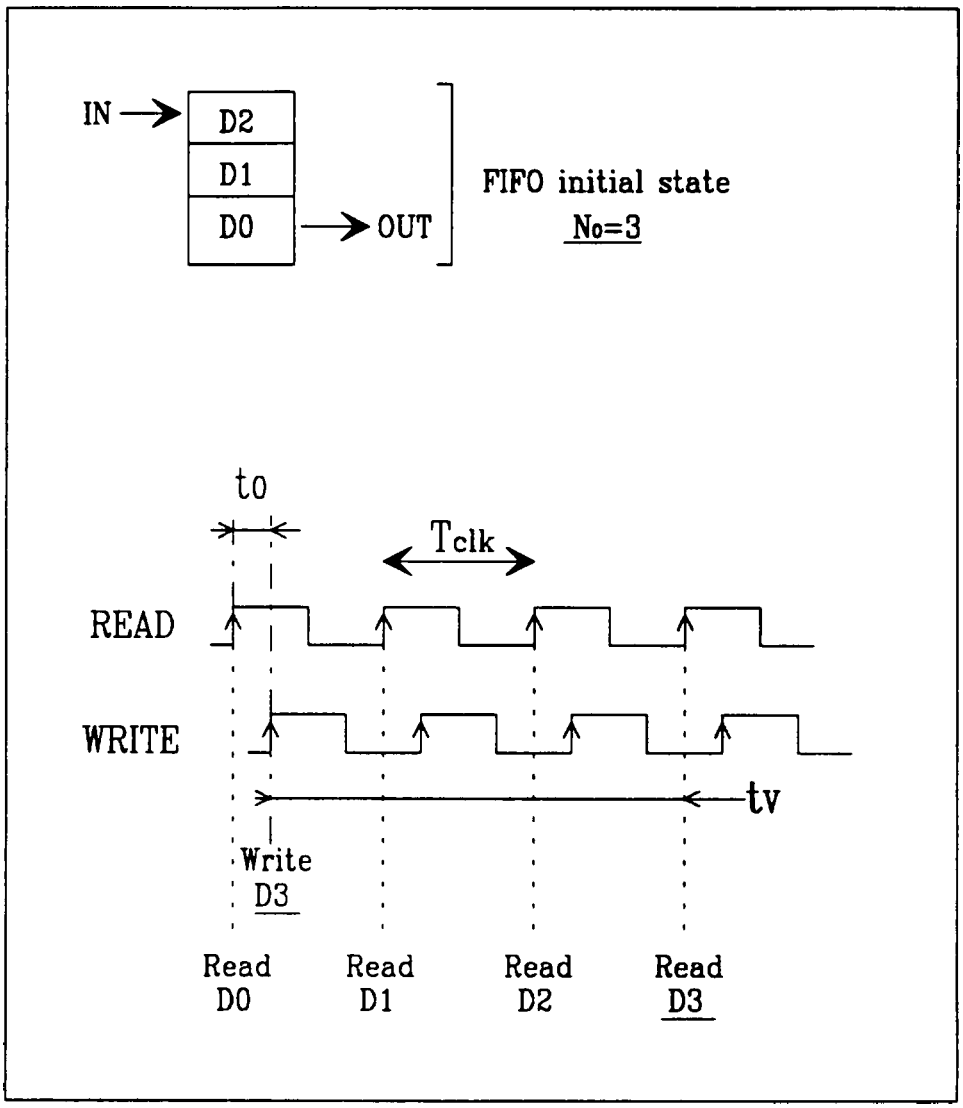


Figure 3. FIFO phase diagram for N = 3 and $t_0 < T_{clk}$.

The later diagram was drawn with $t_0 < T_{clk}$, but the same reasoning applies when T_{clk} shortens gradually to a value lower than t_0. In this case the FIFO depth "N" automaticaly shrinks to a value $N(t) = N_0 - k$, where "k" is the number of entire clock periods within t_0.

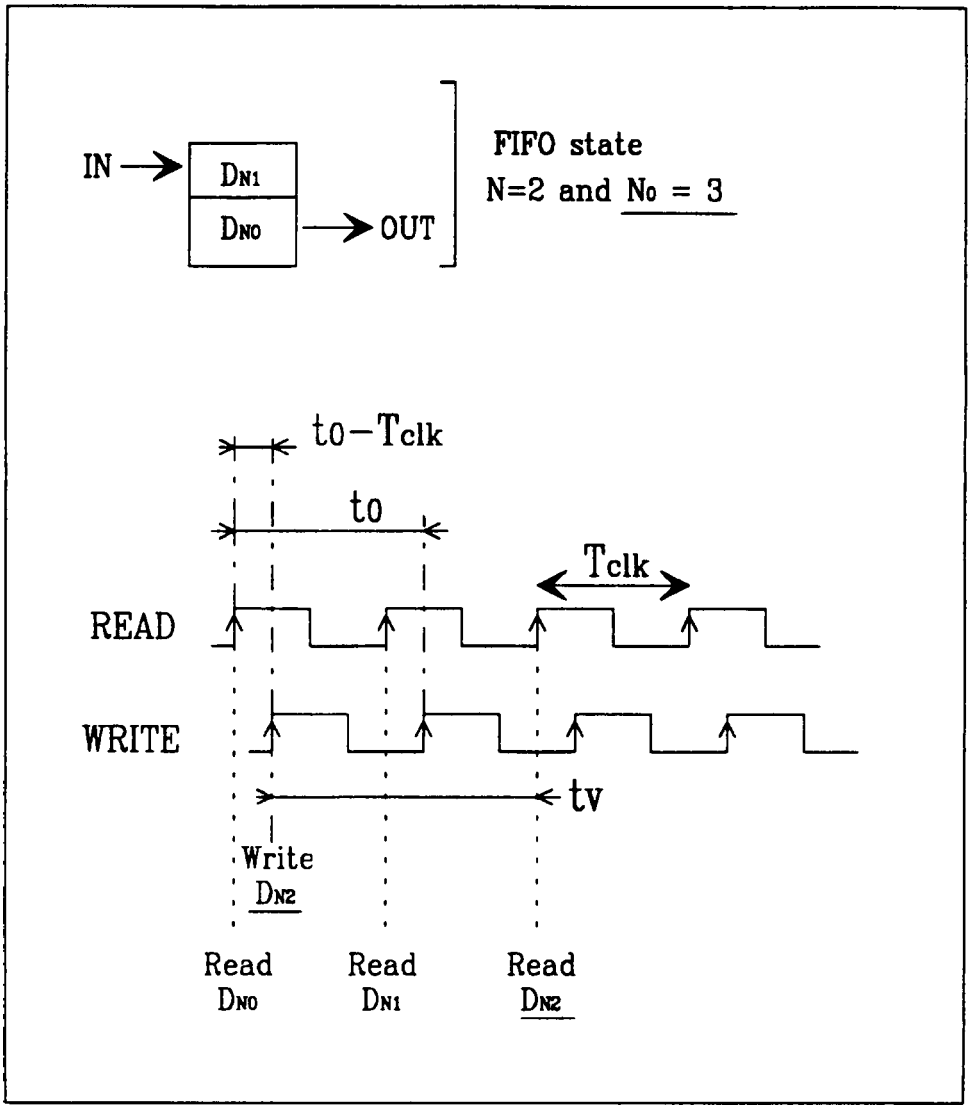


Figure 4. FIFO phase diagram obtained for $N_0 = 3$, after a clock frequency increase from ($T_{clk} > t_0$) to ($t_0 > T_{clk}$) (initial conditions as in Figure 3).

To be convinced that the FIFO depth decreases when the clock frequency increases (and vice-versa) we shall count the total amount of read and write clock periods at a given time, to check whether they differ.

If for example, after an accelerating cycle, there are more read cycles than write cycles, we can conclude that the FIFO depth has decreased in terms of memory cells.
Let's start at time t = 0, from $\omega_{clk} = \omega_0$, and compute the total phase shift until t = T, on both "read" and "write" clocks.

$$\Rightarrow (\phi_R - \phi_W)(T) = \int_0^T \omega_R(t)\cdot dt - \int_0^T \omega_W(t)\cdot dt + \phi_0$$

as for $t \le t_0$: $\underline{\omega_W(t) = \omega_R(t)} = \omega_0$

$$\Rightarrow (\phi_R - \phi_W)(T) = \int_0^T \omega_R(t)\cdot dt - \int_0^{t_0} \omega_0(t)\cdot dt - \int_{t_0}^T \omega_W(t)\cdot dt + \phi_0$$

as $\underline{\omega_W(t) = \omega_R(t - t_0)}$

$$\Rightarrow (\phi_R - \phi_W)(T) = \int_0^T \omega_R(t)\cdot dt - \int_0^{T-t_0} \omega_R(t)\cdot dt - \omega_0.t_0 + \phi_0$$

$$\Leftrightarrow (\phi_R - \phi_W)(T) = \int_{T-t_0}^T \omega_R(t)\cdot dt - \omega_0.t_0 + \phi_0$$

as $\omega_R = \omega_{clk}$ is considered as constant during t_0:

$$\boxed{\Rightarrow (\phi_R - \phi_W)(t) = \omega_{clk}(t).t_0 - \omega_0.t_0 + \phi_0} \qquad (2)$$

Phase difference between "read" and "write" clock of the FIFO, for a slowly increasing clock frequency

$\omega_0 = \omega_{clk}(0)$

$\phi_0 = (\phi_R - \phi_W)(0)$

So at time t, the difference between the number of read and write clock pulses is:

$$N(0) - N(t) = INT[(\phi_R - \phi_W)(t) / 2\pi]$$

$$\boxed{\Leftrightarrow N(0) - N(t) = INT[(f_{clk}(t).\ t_0) - (f_0.\ t_0) + (\phi_0 / 2\pi)]} \quad (3)$$

FIFO depth evolution in term of memory cells

INT(x): integer part of x

These equations show that the FIFO depth is evolving with the clock frequency.

The conclusion is that equation 1 is always valid and reflects the continuous evolution of the phase difference between read and write clocks.

The objective is to have:

$$t_V = T_{rev} - t_0 \quad (4)$$

(4) = (1) implies:

$$\boxed{T_{rev}(t) = N_0.T_{clk}(t)}$$

Expression relating the FIFO depth "N_0" (measured for $T_{clk} > t_0$) and the clock period "T_{clk}" with the revolution period "T_{rev}", before the acceleration process, so to have the proper automatic delay compensation.

Practical example (PS):

$T_{clk} = T_{rev} / 80 \quad \Rightarrow \quad N_0 = 80$
$t_0 = 1.73\ \mu s$

As in the PS we don't start from $f_{clk} = 0$, we have to preset the FIFO depth N to the value corresponding to the preset clock frequency.

Let's have $f_0 = 0$, $\phi_0 = 0$, $N(0) = 80$, $t_0 = 1.73\ \mu s$ and $fclk = (415.10^3.80)$ Hz in equation 3:

$$\Rightarrow N_{preset} = 80 - INT(57.436)$$

$$\boxed{\Leftrightarrow N_{preset} = 23}$$

Total amount of clock periods in the "one turn delay" loop for $f_{rev\ preset} = 415$ kHz and $t_0 = 1.73\ \mu s$

We also have to reevaluate the N_{preset} value of the FIFO itself, considering the delay, in clock periods, of the rest of the circuit (4.5 T_{clk}) and in in the "digital comb filter" (2.5 T_{clk})

$$\boxed{\Leftrightarrow N_{preset} = 16}$$

FIFO preset depth, in term of memory cells, computed for $f_{rev\ preset} = 415$ kHz and $t_0 = 1.73\ \mu s$

This value is obtained for SW1 and SW2 on 0000 position (maximun delay)

The next figure represents the actual hardware block diagram of an automatic delay compensation circuit.

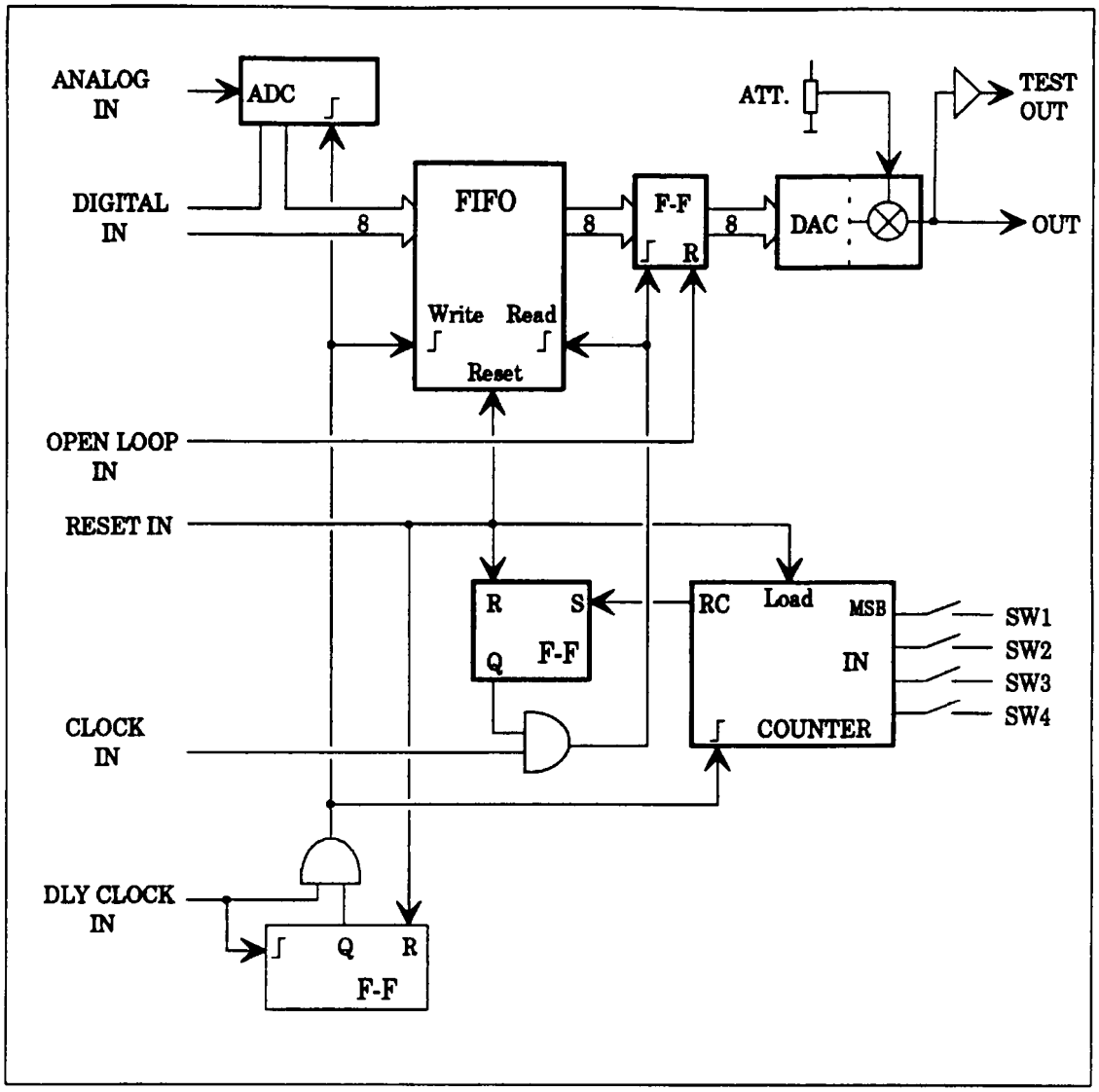


Figure 5. Block diagram of an automatic delay compensation.

3. HARDWARE SET-UP

To set up an automatic delay compensation requires a small screw-driver, a voltmeter, a network / spectrum analyser (1 kHz → 20 MHz), a sinewave generator (40 MHz) and an oscilloscope (bandwidth >120 MHz).

1. Make a connexion from pin 3 of IC5 to pin 2 IC11 and another from pin 6 and 7 of IC5 to pin 1 of IC11.

2. Make a connexion from pin 15 of IC19 to pin 7 IC12 and tie this last pin to -2V through a 100 Ω resistor.

3. Make a connexion from pin 6 of IC12 to pin 15 IC12 and tie this last pin to -2V through a 100 Ω resistor.

4. Cut the connexion between pin 15 of IC12 and pin 9 IC11 and then connect pin 3 IC12 to pin 9 IC11

5. Connect a 300 Ω resistor from J7 (connexion point on the PCB) to the 1 kΩ "Att."potentiometer on the front panel.

6. Make a visual test of the soldering (wiring side of the pcb).

7. This unit can be used with its either digital or analog input active, not both ! The selection is made by removing the unused input circuits (IC16 when digital, IC7-8 when analog)

8. Remove IC 7 and 8.

9. To set up the **ADC bias point**, measure the voltage on **pin 11 of IC16** and then set **P2** to have exactly half of this voltage on **pin 12 of IC12.**

10. Connect the hardware as in **Figure 6** and applie a reset pulse. Set the generator so to have a 10 dBm sinewave source signal. You should observe on both outputs the sample and hold (at the 40 MHz clock rate) version of the input. The out / in gain should be close to unity when the potentiometer **"Att."** is on zero and drop to 0.24 (-12 dB) when the value is 10.0.

11. Decrease the value of the modulation to -30 dB and ckeck the output structure with the spectrum analyser. Set **P1** (hysteresis control of the input comparators of the ADC) so as to obtain the lowest possible phase modulation sidebands.

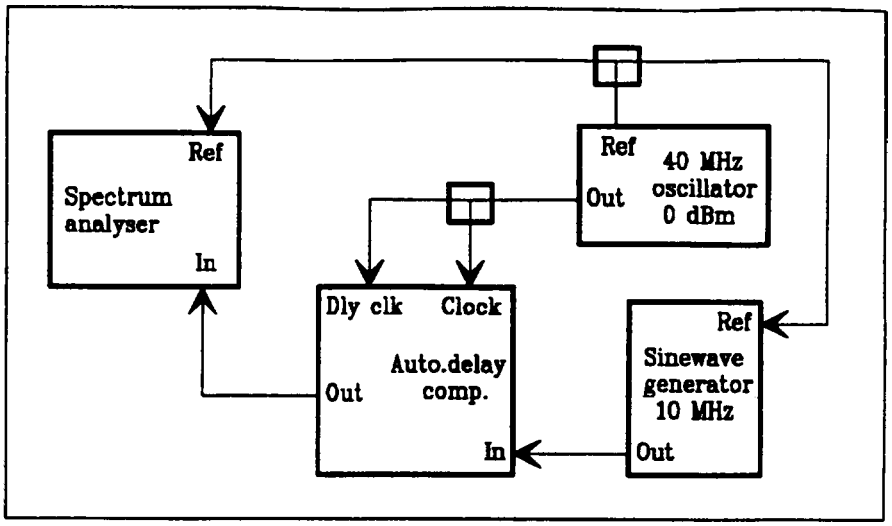


Figure 6. Test layout.

12. Set SW1 and SW2 to each of the values from "0001" to "1111" (with a reset applied after each setting) and ckeck that the input to output delay increases from 145 ns to 495 ns with 25 ns steps (clock period)

13. Remove IC16 and plug in IC7 and IC8.
    Check by connecting to ground the inputs Nr.1,3,5,7,9,11,13,15 of the digital input that pins 19,20,21,22,23,24,25,26 flip from ECL low to high level.

4. ELECTRICAL CHARACTERISTICS

Maximum input AC voltage: \ clock : 10 V_{p-p}
: \ analog : 2 V_{p-p}

Input impedance (clock and analog in): 50 Ω

Output impedance: 50 Ω in serial with 10 nF ⇔ 320 kHz cut-off frequency.

Maximum clock frequency: 70 MHz

Clock pulse width: > 5 ns

Analog input bandwidth (small signals): 60 kHz → 115 MHz

Analog output bandwidth: 320 kHz → 140 MHz

Test output bandwidth: 320 kHz → 30 MHz

Input voltage resolution: 7.8 mV (= 1 LSB)

Input-output transit time: $5.T_{clk}$ + 20 ns on 0001 position of SW1 and SW2 (minimum delay) + $1.T_{clk}$ for each binary increase + $0.5.T_{clk}$ for the harmonic analysis.
For SW1, SW2 = 0000 the total delay is $20.T_{clk}$ + 20 ns

Open loop and reset inputs: 2 V min, 50 V DC max

Out / in gain: 1 ≡ 0 dB (potentiometer "Att" at 0.0) to 0.24 ≡ -12 dB (pot. at 10.0)

5. ACKNOWLEDGMENTS

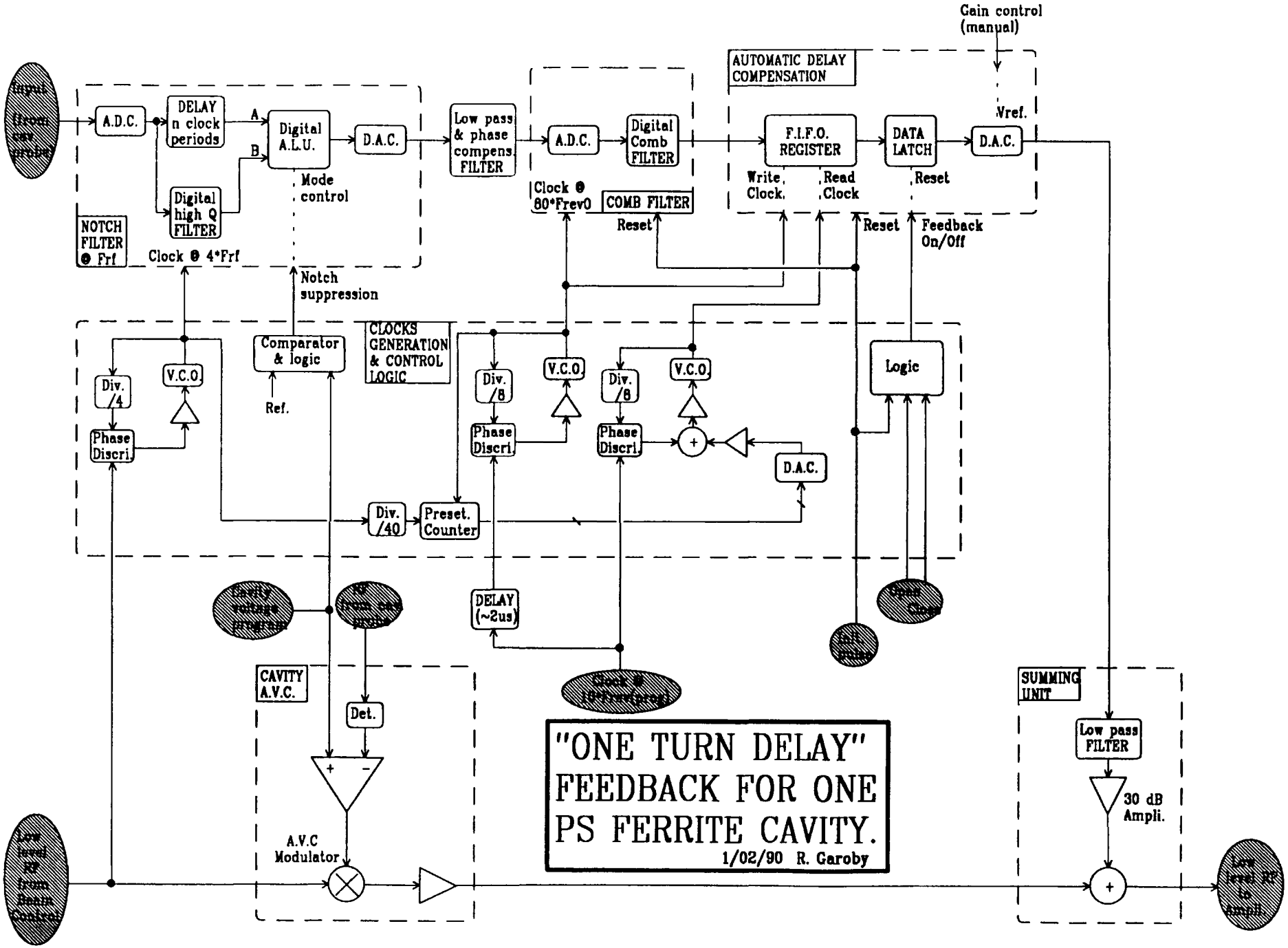
It is a pleasure to thank D. Boussard, J.L. Gonzalez and G. Lambert for their great help and their kindness in sharing with us their experience in all the domains involved in the "one turn delay feedback".

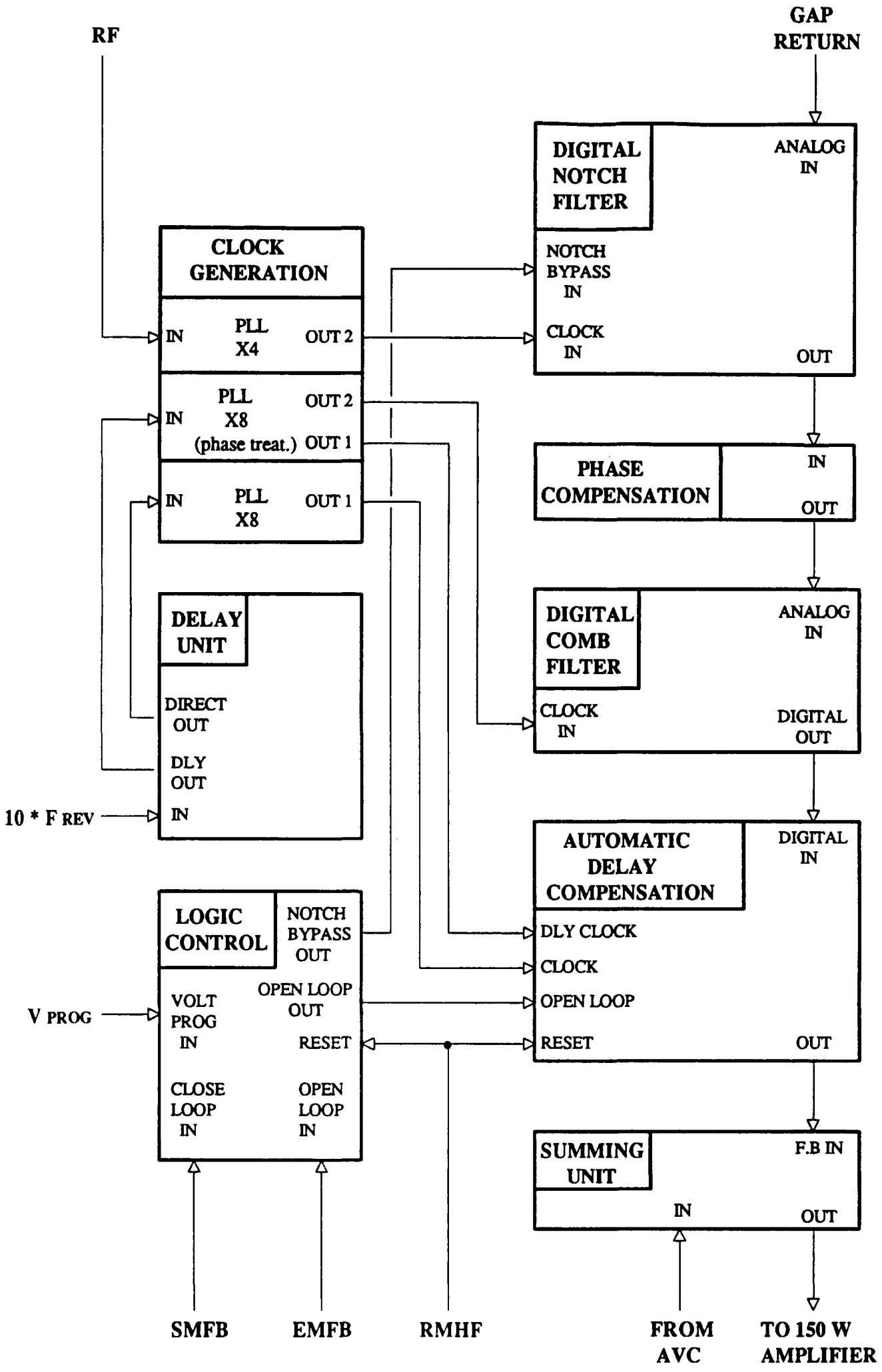
6. REFERENCE

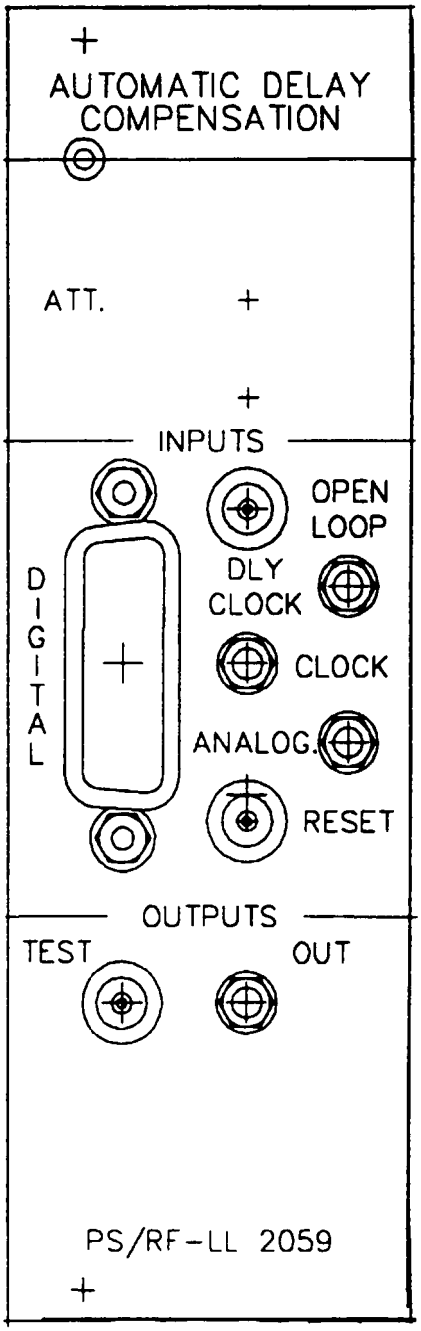
F. Blas, R. Garoby. Design and operational results of a "one-turn-delay feedback" for beam loading compensation of the cern PS ferrite cavities. CERN/PS 91-16 (RF).

Distribution:

PS/RF/LL section


Gain control (manual)
AUTOMATIC DELAY COMPENSATION
Vref.
Input from cav. probe
A.D.C.
DELAY n clock periods
A
B
Digital A.L.U.
D.A.C.
Mode control
Digital high Q FILTER
NOTCH FILTER @ Frf
Clock @ 4*Frf
Notch suppression
Low pass & phase compens. FILTER
A.D.C.
Digital Comb FILTER
Clock @ 80*Frev0
COMB FILTER
Reset
F.I.F.O. REGISTER
DATA LATCH
D.A.C.
Write Clock
Read Clock
Reset
Reset
Feedback On/Off
CLOCKS GENERATION & CONTROL LOGIC
Comparator & logic
Ref.
Div. /4
V.C.O
Phase Discri.
Div. /8
V.C.O
Phase Discri.
Div. /8
V.C.O
Phase Discri.
D.A.C.
Logic
Div. /40
Preset. Counter
Cavity voltage program
RF from cav. probe
DELAY (~2us)
Clock @ 10*Frev(prog)
Gate Origin
Gate pulse
CAVITY A.V.C.
Det.
A.V.C Modulator
SUMMING UNIT
Low pass FILTER
30 dB Ampli.
Low level RF from Beam Control
Low level RF to Ampli.
"ONE TURN DELAY" FEEDBACK FOR ONE PS FERRITE CAVITY.
1/02/90 R. Garoby


RF
GAP RETURN
DIGITAL NOTCH FILTER
ANALOG IN
NOTCH BYPASS IN
CLOCK IN
OUT
CLOCK GENERATION
IN
PLL X4
OUT 2
PLL X8
(phase treat.)
OUT 2
OUT 1
PLL X8
PHASE COMPENSATION
DELAY UNIT
DIRECT OUT
DLY OUT
10 * F REV
DIGITAL COMB FILTER
DIGITAL OUT
AUTOMATIC DELAY COMPENSATION
DIGITAL IN
DLY CLOCK
CLOCK
OPEN LOOP
RESET
LOGIC CONTROL
NOTCH BYPASS OUT
V PROG
VOLT PROG IN
OPEN LOOP OUT
CLOSE LOOP IN
OPEN LOOP IN
SUMMING UNIT
F.B IN
SMFB
EMFB
RMHF
FROM AVC
TO 150 W AMPLIFIER


AUTOMATIC DELAY
COMPENSATION
ATT.
INPUTS
DIGITAL
OPEN
LOOP
DLY
CLOCK
CLOCK
ANALOG.
RESET
OUTPUTS
TEST
OUT
PS/RF-LL 2059