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HIGH-SPEED, HIGH-PRECISION, BIPOLAR PROGRAMMABLE MAGNETS POWER SUPPLIES FOR FINE ΔQ AND $\int B\, d\ell$ TUNING IN THE FOUR RINGS OF THE CERN PROTON SYNCHROTRON BOOSTER (PSB)

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CONTENTS

SUMMARY

The operational characteristics of fourteen 10 kW bipolar programmable power supplies, built to feed two different sets of correction windings, are presented.

Having defined the basic technical options, the design criteria for the power assemblies as well as for the regulation, polarity inversion, and protection circuits are reported on.

The layout and the remote-control facilities of the supplies are briefly described.

1. INTRODUCTION

Fourteen (12+2 spare units) new auxiliary power supplies have been built for the QCF, QCD, and BDL windings of the PSB main magnets, within the framework of the "Multibatch filling" and "Antiproton Accumulator" projects[1-3].

Beyond the basic motivation of a faster pulse repetition frequency and of upgraded power ratings, the stringent performance specifications of these supplies were derived from the following requirements:

QCF,D supplies: to extend the operating range of the main Q tune supplies and to optimize the working point in the $Q_{H,V}$ plane during acceleration through individual fine programming of the Q values in the four PSB rings[4].

BDL supplies: to allow better equalization of the mean radial position between beams before ejection, or possibly individual adjustment of the position of the four beams for ejection of 2 × 5 bunches at different energies [with subsequent longitudinal recombination in the PS[5]].

Because of the load impedances and the required power ratings, the supplies of the two sets of windings are identical apart from the different coupling of the power components.

The technical solutions adopted and the decision to share development and production between CERN and industry has allowed more than 50% cost savings with respect to the most interesting offer of firms for an all-industry version.

2. THE CORRECTION WINDINGS

2.1 Electrical connections

The main magnet system of the PS Booster (Fig. 1) comprises 33 bending magnets (BHZ, reference unit included), 32 focusing lenses (QFO), and 16 defocusing lenses (QDE).

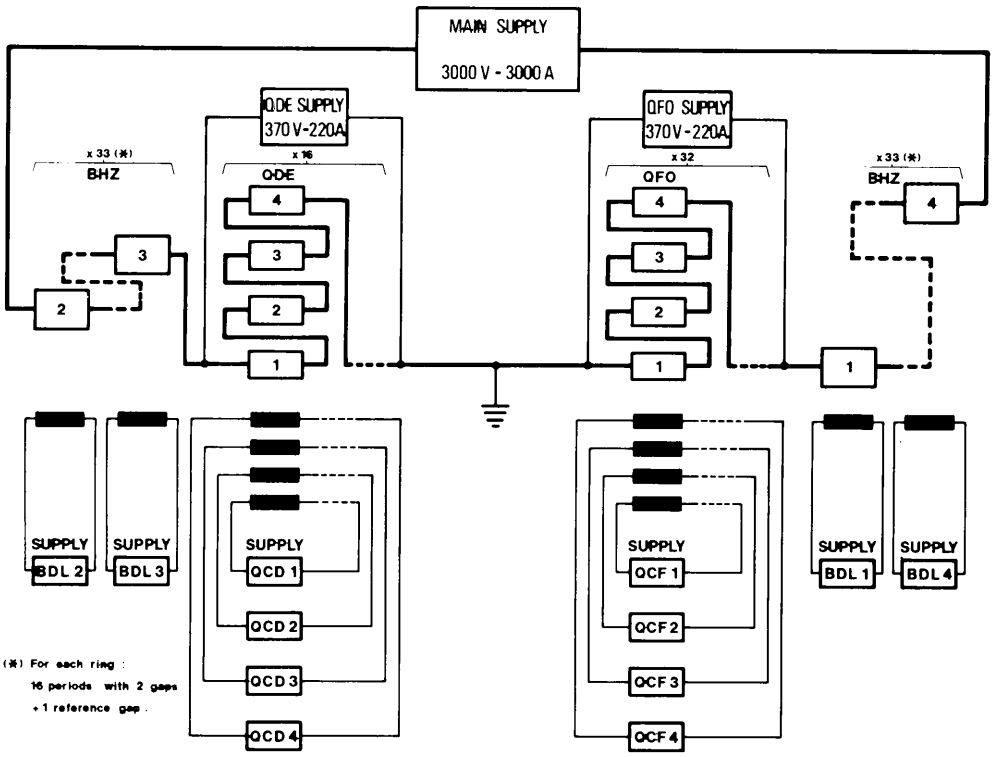


Fig. 1 Schematic layout of the main magnets windings (BHZ, QDE, QFO) of the PS Booster and of the auxiliary windings (BDL, QCF, QCD)

Four superimposed airgaps in each magnet accommodate the vacuum chambers of the Booster rings.

The main windings of the magnets are electrically series-connected (all four rings) and fed by a common power supply: tuning supplies are connected across the main defocusing and focusing circuits.

In addition, each gap of the bending and focusing magnets carries an auxiliary BDL, respectively QCF, QCD, correcting winding; these windings are again connected in series and form 12 circuits fed by separate power supplies.

Consequently the correction windings are magnetically coupled with the main ones and experience induced voltages of either polarity during each acceleration cycle.

The main current rises from 550 A to 2760 A within $\sim$ 300 ms and, after a 50 ms flat top, falls to its initial value within 150 ms with a $di/dt \leq 20$ kA/s; the voltage induced in the correction windings corresponds to the relation

$$U_i = \left(\frac{di}{dt}\right) \cdot \frac{L_p}{4} \cdot \frac{n_c}{n_p}$$

where $L_p/4$ is the inductance of the main circuit concerned, n_p and n_c are the numbers of turns of the main and correction windings.

2.2 Electrical parameters

The relevant electrical parameters concerning the main and correction windings are collected in Table 1 [6].

Table 1

Electrical parameters

	BDL	BHZ	QCF	QFO	QCD	QDE
- Number of separate windings in series	33		32		16	
- Magnet length of each magnet (m)	1.615		0.503		0.881	
- Specific magnetic induction or gradient (T/A, T/A•m)	0.358×10^{-4}	2.14×10^{-4}	0.695×10^{-3}	1.39×10^{-3}	0.695×10^{-3}	1.39×10^{-3}
- Number of turns	2	12	1	2	1	2
- Total inductance (mH)	6.8	164	0.98	8	0.83	6.62
- Total resistance (40 °C, cables included) (mΩ)	600	-	263	-	256	-
- Time constant L/R (ms)	11.33	-	3.72	-	3.24	-
- Maximum induced voltage (V)	130	-	20	-	17.5	-
- Maximum dv/dt of induced voltage (V/ms)	10	-	5	-	5	-
- Cross-section of cables (mm^2)	35	-	120	-	70	-
- Cable resistance (40 °C) (mΩ)	445	-	77	-	127	-

3. POWER SUPPLIES SPECIFICATIONS

The salient features of these programmable power supplies are:

- the current precision and stability;
- the permissible speed of current reference variations (QCF,D supplies);
- the capability to cope with large induced voltage of both polarities (BDL supplies in particular);
- the possibility of pulse-to-pulse polarity selection;
- compatibility with the standard interface, Hybrid Single Transceiver, of the NORD-CAMAC-based new computer system.

The technical specifications are collected in Table 2. The mode of operation of these power supplies is illustrated in Fig. 2.

Table 2

Power supplies specifications

	BDL	QCF,D
- a.c. input voltage	3 × 380 V ± 5%, 50 Hz	
- Peak (mean) output power (kW)	10 (8)	
- Peak (mean) output current (A)	50 (40)	100 (80)
- Peak (at I_{max}) output voltage (V)	200 (160)	100 (65)
- Maximum permissible di/dt for a ΔI of 20 A (A/ms)	1	20
- Current reproducibility and stability over 24 h (all causes of error included) (%)	0.1	
- Current precision for fast di/dt (%)	0.5	
- Digital current control range and resolution	2 to 100%, 12 bits	
- Minimum pulse repetition period with polarity inversion at I_{max} (s)	0.6	

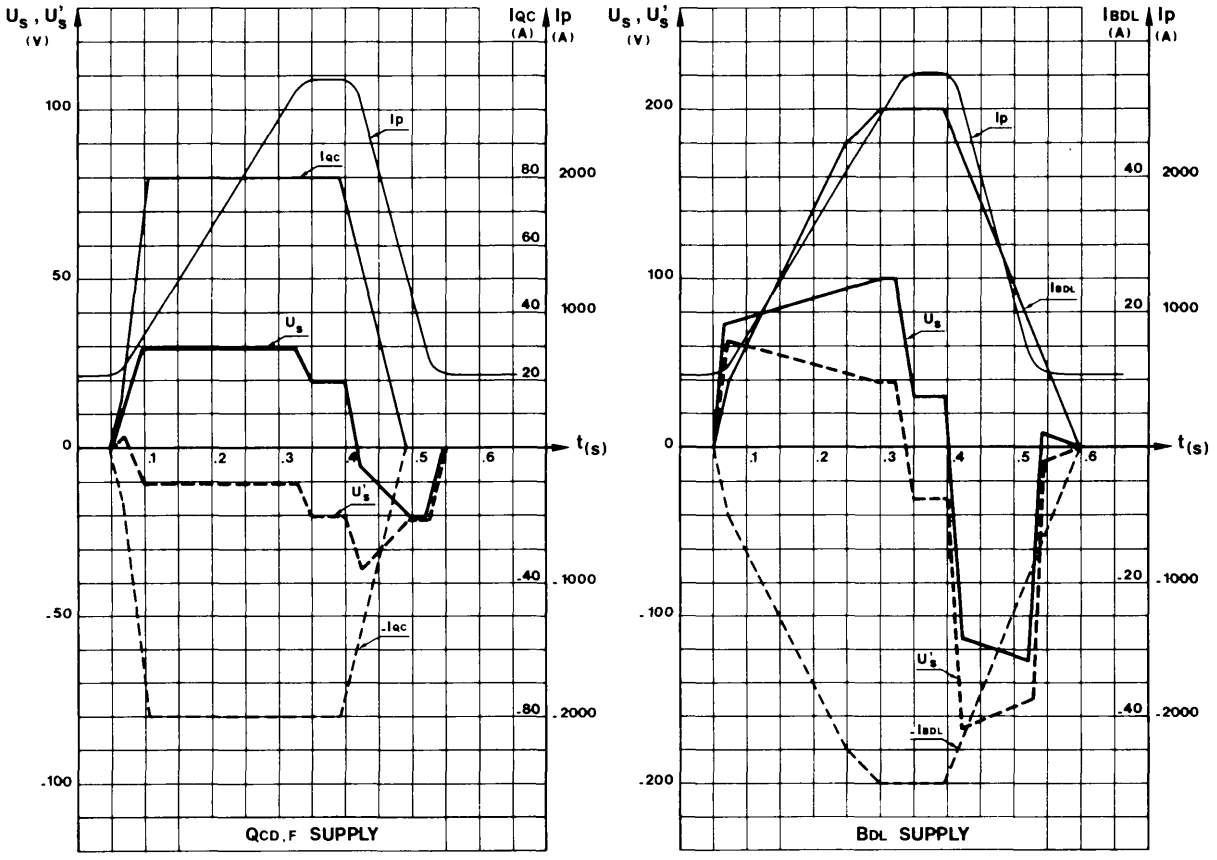


Fig. 2 Power supply output voltage U_s, U_s' for a given main winding current I_p and the shape of correction currents $\pm I_{QC}$ and $\pm I_{BDL}$

4. DESIGN CHARACTERISTICS

4.1 Power circuits

Owing to the fact that the output power of the BDL and QCF,D supplies is the same, and that the voltage/current parameters are complementary, the design can be considerably simplified by a series/parallel connection of identical power assemblies (Fig. 3).

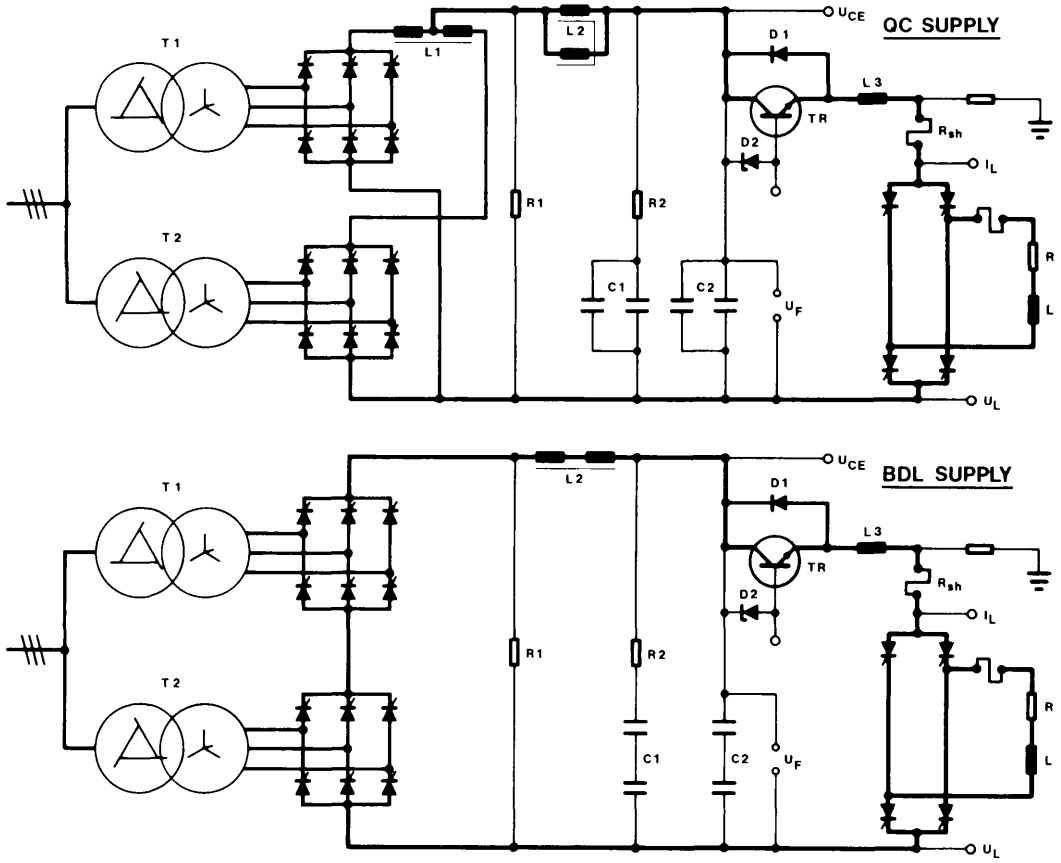


Fig. 3 Schematic layout of power assemblies

On the other hand, the required precision and fast changes of magnet current can be obtained with a classical series transistor regulators, adapted to the different supply output voltage, which contributes to safe operation of the thyristor polarity changer under no-current conditions.

Twelve-pulse thyristor rectifiers are employed to reduce the residual ripple, i.e. to allow a less powerful passive filter, and to counteract more promptly the load-induced voltage and the variations of collector voltage during pulsed operation.

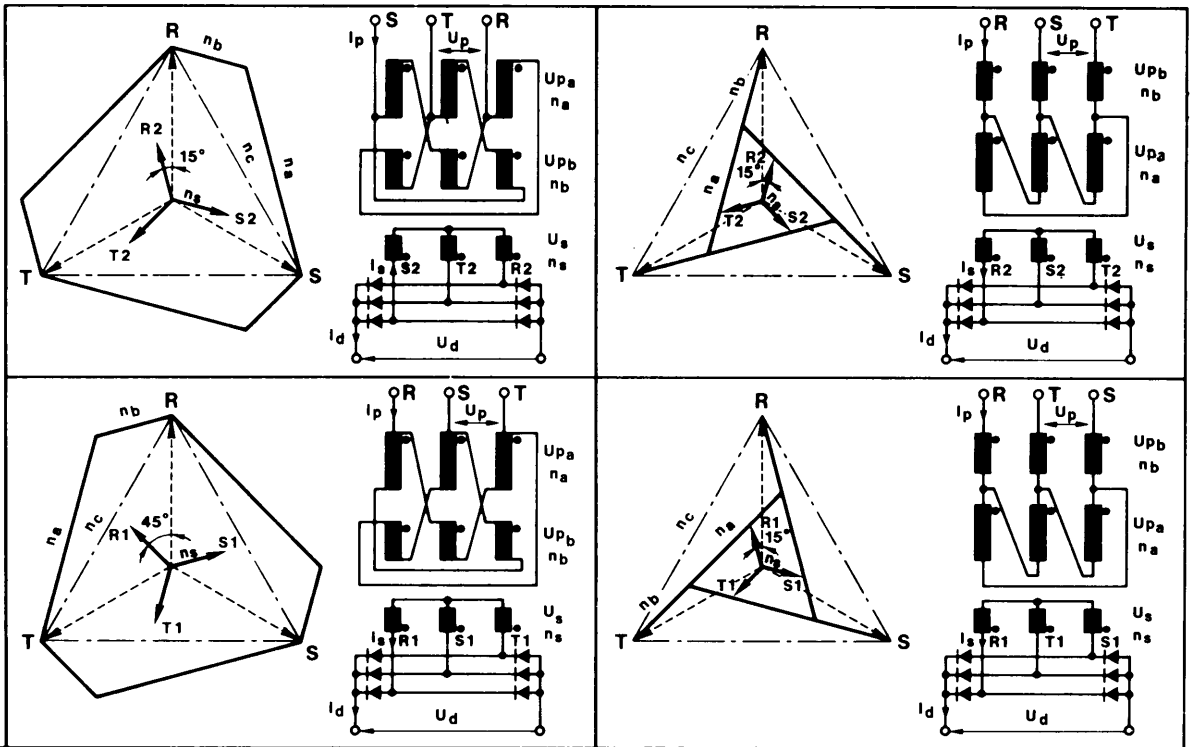
The passive LCR filter is a trade-off between the conflicting requirements of components compatible with the acceptable voltage drop $L \cdot (di/dt)$ and voltage

fluctuations $1/C \int i \cdot dt$, as well as with economical aspects, and of a corner frequency adapted to the rectifier bandwidth.

The filter components are series/parallel connected (the inductance has two separate windings on the same iron core) and an interphase reactor is used for the parallel operation of the rectifiers (QCF,D supplies).

4.1.1 Power transformers[7)]

The required 30° secondary phase voltage shift to obtain twelve-pulse rectifier operation is made on the primary of the transformers for higher angular precision. The extended-delta/star connection offers, with respect to the usual polygon/star version, the advantage of somewhat lower transformer ratings and of simpler layout (two phases are interchanged on identical transformers), as shown in Fig. 4.



n_a/n_b	2.732	1.732
$Up_a/Up{:}n_a/n_c$	0.816	0.518
$Up_b/Up{:}n_b/n_c$	0.299	0.299
Up/U_s	n_c/n_s	n_c/n_s
Up_a/U_s	n_a/n_s	n_a/n_s
Up_b/U_s	n_b/n_s	n_b/n_s
I_{pa}/I_s	n_s/n_c (=I_{pb}/I_s)	n_s/n_c
I_p/I_s	$\sqrt{3}.n_s/n_c$	$\sqrt{3}.n_s/n_c$(=I_{pb}/I_s)
I_s/I_d	0.816	0.816
U_s/U_d	0.427	0.427
P_p/P_d	1.17	1.08
P_s/P_d	1.05	1.05
P_m/P_d	1.11	1.065

Fig. 4 Characteristics of the polygon/star and extended-delta/star transformers

A grounded screen has been foreseen between primary and secondary windings, and all winding sections have been made separately accessible for testing.

Alternate current transformers (50 A/1 A) are mounted on two of the phases feeding the thyristor bridges.

4.1.2 Thyristor rectifier

The two six-pulse rectifiers are natural air cooled; their thyristors are fired by two main pulses at 60° interval and two interleaved auxiliary pulses, i.e. by a total of four pulses 30° apart.

4.1.3 Interphase reactor

An interphase reactor ensures acceptable current sharing and decoupling between parallel-connected rectifiers without the need of an active current balance.

This reactor has been designed according to the following relations, concerning voltage-time integral, magnetization characteristic, and inductance:

$$\int U_\sigma \, dt = \int NS \, dB_\sigma = \int L_\sigma \, di_\sigma = 95 \text{ V·ms} ,$$

$$\frac{\Delta i_\sigma}{\Delta B_\sigma} = \sqrt{\frac{S\delta}{L_\sigma \mu_0}} = \frac{SN}{L_\sigma} = 18 \text{ A/T} , \qquad \text{and} \qquad L_\sigma = \frac{N^2 S \mu_0}{\delta} = 4 \text{ mH} ,$$

where $S = 30$ cm^2 is the iron cross-section, $\delta \simeq 0.45$ mm the total air gap, and $N = 2 \times 12$ the number of turns. The most significative wave forms illustrating the operation of the rectifiers and interphase reactor of the QCF,D supplies are shown in Fig. 5.

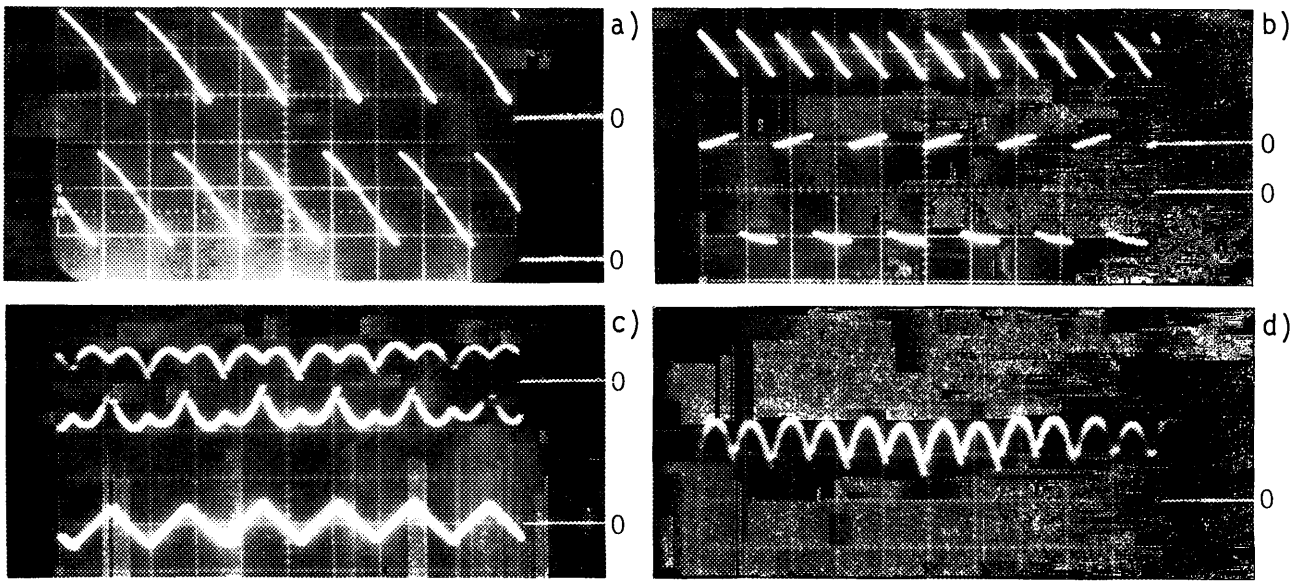


Fig. 5 Interphase reactor wave forms (QCF,D supplies):
a) Rectifier voltages U_1, U_2 ($\alpha \simeq 50°$);
b) Voltage at centre tap $[(U_1 + U_2)/2]$ and across the reactor ($U_\sigma = U_1 - U_2$);
c) Rectifier current i_1, i_2 (top) and magnetizing current $i_\sigma = i_1 - i_2$ (bottom);
d) Output current $i_1 + i_2$.
$I_L = 30$ A, $U_{CE} = 32$ V; scale: 2 ms/div., 50 V/div., 25 A/div.

4.1.4 Passive LCR filter[8)]

The LCR filter consists of an inductor with two separate windings and of MP capacitor (250 µF/unit) sections connected in series (BDL) or parallel (QCF,D supplies).

The corner frequency has been set as high as possible, taking into account the conflicting requirements of ripple attenuation and speed of response.

The voltage attenuation of the filter is given by the relation

$$\frac{U_o}{U_i} = \frac{1 + 2\xi\left(\frac{n}{n+1}\right)\tau_0 s}{\tau_0^2 s^2\left[1 + \frac{2n}{(n+1)^2}\xi\tau_0 s\right] + \frac{2n}{n+1}\tau_0 s + 1}$$

$$= \frac{(1 + \frac{s}{\omega_1})}{\left(1 + \frac{s}{\omega_2}\right)\left(1 + 2\chi\frac{s}{\omega_3} + \frac{s^2}{\omega_3^2}\right)},$$

with

$$\xi = \frac{R_2}{2} \cdot \sqrt{\frac{(C_1 + C_2)}{L_2}}\ ; \quad \tau_0 = \sqrt{L_2(C_1 + C_2)} = \frac{1}{\omega_0}\ ; \quad n = \frac{C_2}{C_1}\ .$$

The passive filter parameters are collected in Table 3.

Table 3

Parameters of LCR filter

	L_2 (mH)	R_2 (Ω)	C_1 (mF)	C_2 (mF)	ξ	$\omega_0/2\pi$ (Hz)	$\omega_1/2\pi$ (Hz)	$\omega_2/2\pi$ (Hz)	$\omega_3/2\pi$ (Hz)	χ
BDL	2	1.9	1.5	0.375	0.92	82.2	54.8	117.4	132.6	0.67
QCF,D	0.5	0.5	6	1.5	0.97	82.2	51.3	96.7	137	0.6

4.1.5 Transistor regulator

The current control loop acts through the series transistor regulator shown in Fig. 6.

Sixty NPN transistors in three groups are parallel-connected in the common emitter configuration. A resistor and a fuse are inserted in each emitter lead to improve current sharing and to isolate possible defective transistors; a zener diode and junction diodes protect the transistors against overvoltages.

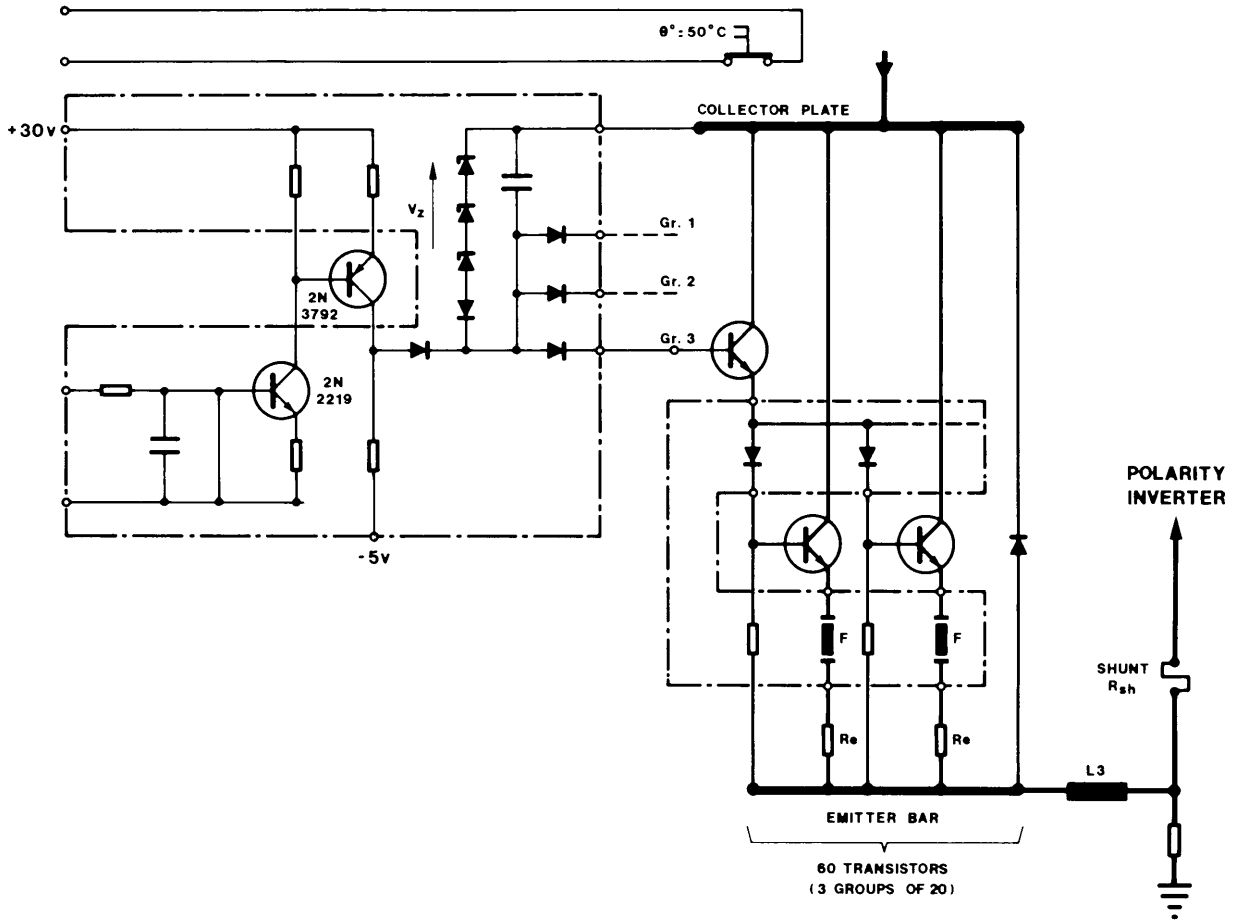


Fig. 6 Schematic circuit of series transistor regulator

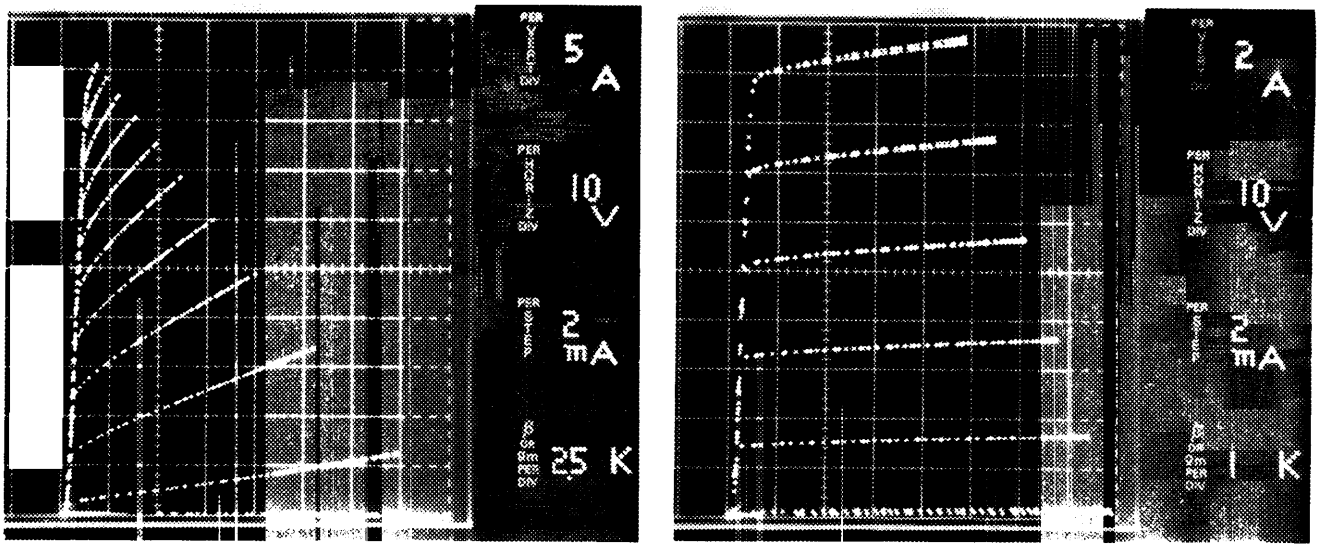
The power transistors are mounted on a water-cooled (Cd-coated) plate; the water circuits are designed for a $\Delta\theta_{max}$ of 5 °C per plate with ∿ 10 ℓ/min water flow. The temperature of the plate is monitored by a thermocontact acting at ∿ 50 °C.

Table 4 gives some further details about the transistor regulator. Typical families of curves measured for a group of 20 transistors are joined in Fig. 7.

Table 4

Transistor regulator components

	BDL	QCF,D
Type of NPN transistors	MJ423	2N3773
Number of transistors in parallel	3 × 20	3 × 20
Ratings (A; V; W)	10; 325; 125	16; 140; 150
Emitter resistance R_e (Ω)	0.56	0.33
Fuse rating (A)	2	4
Zener voltage V_Z (V)	100	70



a) 2M3773 transistors of QCF,D supplies b) MJ423 transistors of BDL supplies

Fig. 7 Typical family of U_{CE}, i_C curves for a group of 20 parallel-connected transistors

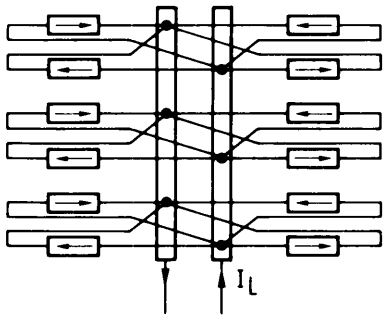
4.1.6 Emitter choke, shunt, polarity inverter

The capacitive currents due to thyristor commutations, the load-induced voltages, and the collector voltage ripple are external perturbations acting on the current control loop. To limit their effect, a 200 µH air-core inductor has been introduced in series to the emitter bar of the transistor regulator, and the supply has been earthed via a 10 Ω resistor (Fig. 6). As known[9], the effect of such an inductor is to strongly increase the output impedance of the transistors considered as a common-base stage: in our case,

$$Z_0 \simeq \frac{h_{ib} + X}{\Delta h + h_{ob} \cdot X} \simeq \frac{X}{h_{rb}} \simeq 10^3 \cdot X ,$$

with $X = \omega L \simeq 0.7\ \Omega$ at 600 Hz.

The current measuring shunt is built as a low-inductance parallel assembly of power resistors (Fig. 8), which have a temperature coefficient of $\leq$ 50 ppm/°C and are selected to obtain a precision error $\Delta R/R \leq 10^{-4}$ at 20 °C. These resistors are mounted on the same water-cooled Cu plate as the transistors.



SUPPLY	RESISTOR TYPE	VALUE (Ω)	QUANTITY	R_{sh} (mΩ)	1V/
BDL	RH 50 - 50 W	0,240	12	20	50 A
QC	RH 50 - 50 W	0,121	8	10	100 A
		0,119	4		

Fig. 8 Layout and characteristics of current measuring shunt

The polarity inverter consists of four natural-air-cooled thyristors (of the same type as for the BDL and QCF,D supplies); the polarity inversion occurs by forcing the load current to zero and commutating the firing pulses.

4.2 Regulation

Amongst the different solutions envisaged, two separate regulation systems have been implemented, as shown in Fig. 9:

- one, acting through the thyristor rectifiers, controls the working point of the power transistors independently of load current variations and induced voltage;
- the other, driving the transistor power amplifier, takes care of the precise current regulation according to the external reference function.

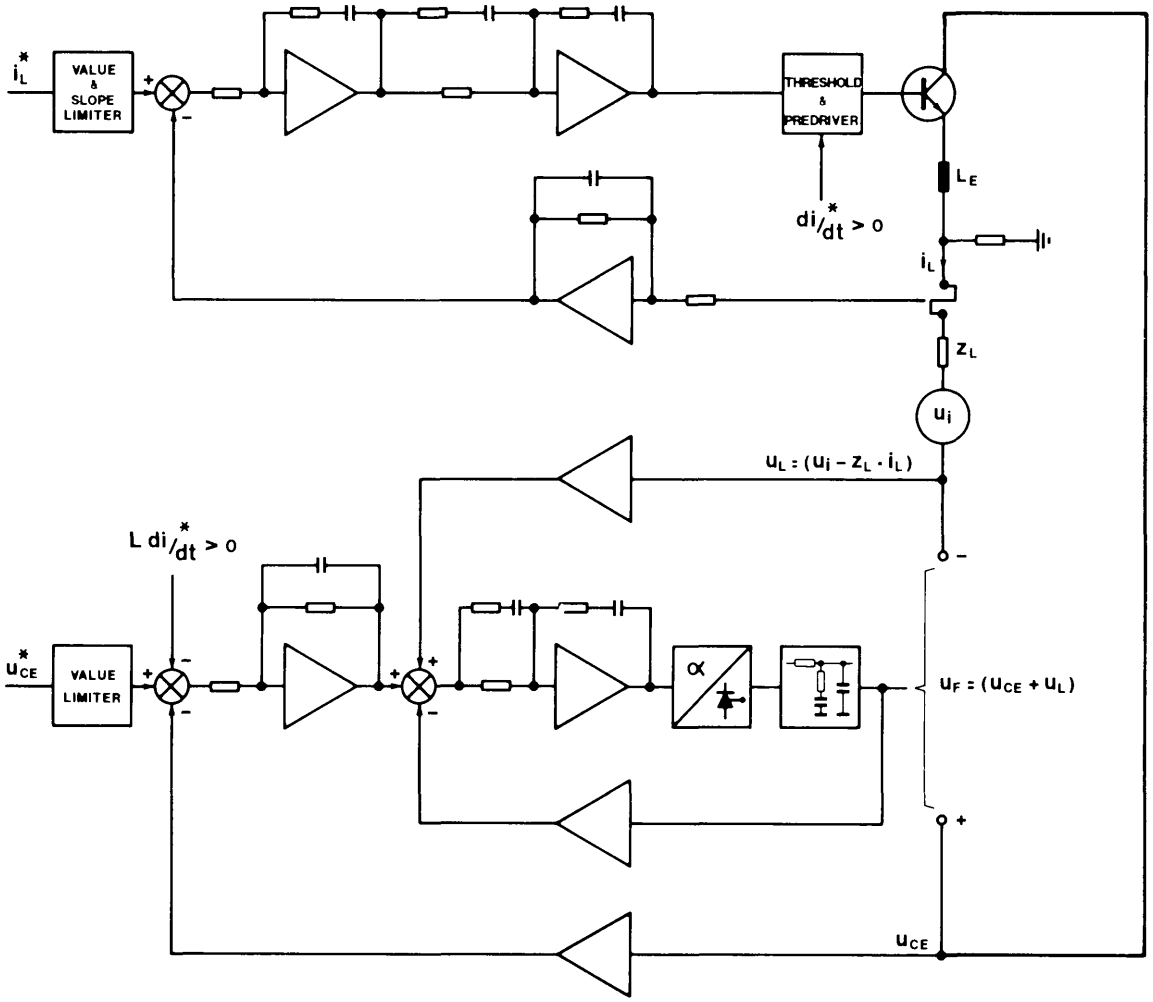


Fig. 9 Voltage and current regulation systems

4.2.1 Voltage control loops

The transistor voltage control is based on the following relations between the voltage U_F at the filter capacitor, the collector-emitter voltage U_{CE}, the

load voltage U_L, the induced voltage U_i, the load current i_L, and the load impedance Z_L:

$$U_F = U_{CE} + U_L ,$$

$$U_L = \pm U_i - Z_L i_L .$$

The problem is to keep the voltage U_{CE} inside a given working range and to achieve sufficient speed of control.

The transfer function of the passive filter is of the third order with a resulting corner frequency of $\sim$ 150 Hz and phase shift of up to -170° at $\sim$ 1 kHz. The 12-pulse rectifier can be assimilated to a sampler-clamper system with a mean sample frequency f_s = 600 Hz and a variable static gain depending on the firing angle α; an acceptable approximation up to the frequency $\sim f_s/4$ = 150 Hz is a transfer function of amplitude

$$G = K(\alpha) \left[\frac{\sin \pi(f/f_s)}{\pi(f/f_s)} \right]$$

and phase (rad)

$$\phi = -\pi(f/f_s) .$$

As shown in Fig. 9, a suitable correction is added to the passive filter and thyristor rectifier chain to obtain an internal U_F loop with the open-loop transfer function drawn in Fig. 10. The filter voltage reference U_F^* is derived by

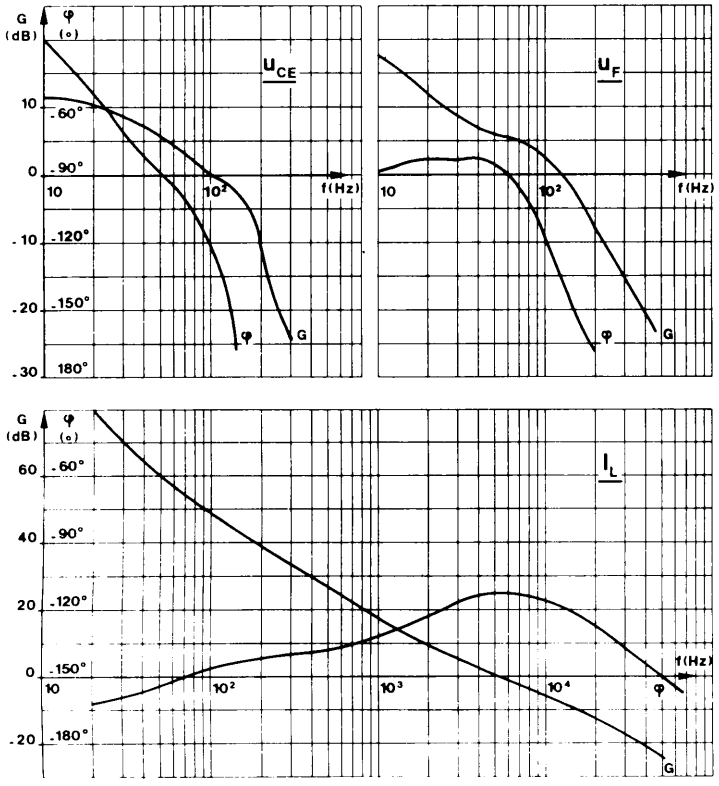


Fig. 10 Bode plots of open-loop transfer functions of the U_{CE}, U_F, and I_L regulation systems.

adding the total load voltage to the output of the U_{CE} controller, so as to compensate for the effects of load-current variations and induced voltages.

The external U_{CE} loop, corrected for fast positive current variations, has a bandwidth of $\sim$ 100 Hz and relatively low open-loop gain (Fig. 10), sufficient to limit the excursions of the transistor working point in all operational situations.

The gains of the internal U_F loop and superimposed U_{CE} loop have been experimentally matched to each other for best over-all performance.

4.2.2 Current control loop

The requirements of fast current variations (20 A/ms for the QCF,D supplies) and of low steady-state errors ($< 10^{-3}$) determine the closed-loop system bandwidth to be at least 3.5 kHz and the low-frequency open-loop gain to exceed 60 dB.

An open-loop transfer function of the type

$$G(s)H(s) = \frac{K(s\tau_a + 1)(s\tau_b + 1)(s\tau_c + 1)}{s^N(s\tau_1 + 1)(s\tau_2 + 1)(s\tau_3 + 1)} = \frac{\Theta_c(s)}{E(s)} ,$$

with N = 2 has been selected so as to eliminate steady-state errors for a ramp input as well.

The design procedure consisted first of measuring the open-loop transfer function $G_1(s)$ of the series transistor regulator and magnet load [including the predriver stage and the current measuring chain H(s)], which can be expressed as

$$G_1(s)H(s) = \frac{11}{\left(1 + \frac{s}{2\pi\ 16}\right)\left(1 + \frac{s}{2\pi\ 29000}\right)} ,$$

and of adding the required correcting functions

$$G_2(s) = \left[\frac{2\pi\ 49}{s}\left(1 + \frac{s}{2\pi\ 106}\right)\right]\left[\frac{2\pi\ 2680}{s} \cdot \frac{\left(1 + \frac{s}{2\pi\ 10}\right)\left(1 + \frac{s}{2\pi\ 1476}\right)}{\left(1 + \frac{s}{2\pi\ 292}\right)}\right]$$

The open-loop transfer function $[G_1(s) \cdot G_2(s) \cdot H(s)]$ is drawn in Fig. 10; the system is absolutely stable with a gain margin of > 30 dB and phase margin of 65°, if one assumes ideal operational amplifier characteristics.

In the case of a parabolic unit reference input corresponding to $\Theta_R(s) = 2/s^3$, the static error coefficient $\sqrt{K_a}$ is 500 Hz (extrapolation of the lower 40 dB/decade asymptote in Fig. 10).

The closed-loop transfer function has been studied both analytically and graphically (Bode and root-locus plots) to verify the transient response parameters.

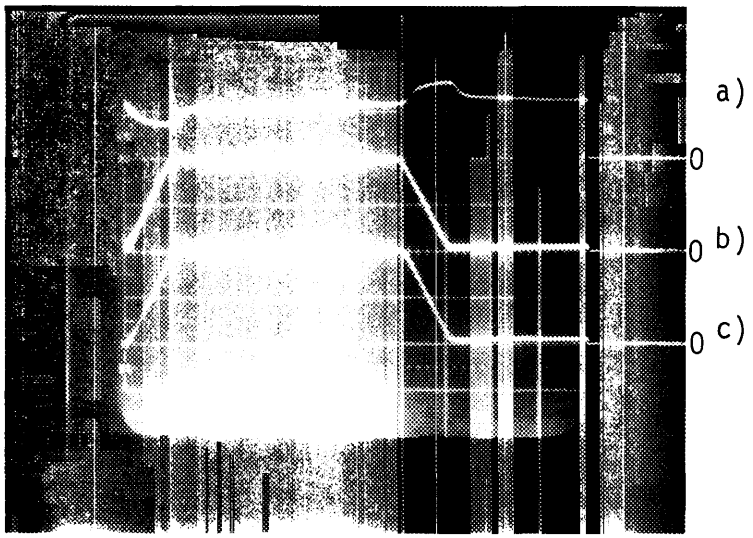


Fig. 11 a) Collector-emitter voltage U_{CE} of transistor regulator (50 V/div, 0.5 ms/div); b) Reference current (5 A/div); c) Load current (5 A/div).

Any delay of response of the current control loop in the case of abrupt changes in the reference slope, is eliminated by means of a di/dt modulated threshold at the input of the transistor regulator predriver. The performance of the current regulation is illustrated in Fig. 11.

4.3 Polarity inversion

This operation must occur in the absence of load-induced voltage; any inversion request is therefore enabled at the end of the main power supply cycle, and a time of ∿ 50 ms is allocated for it, according to Fig. 12, consisting of three intervals:

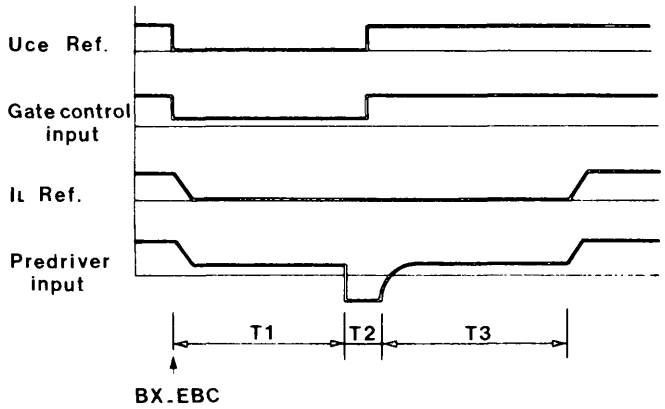


Fig. 12 Time sequence of polarity inversion

T_1: the U_{CE} and the load current references are set to zero;

T_2: in addition, the transistor regulator is blocked; the firing pulses to the rectifiers and to the inverter thyristors are suppressed and the voltage control-loop gain is reduced (integrator reset);

T_3: the gate pulses are switched onto the desired arms of the polarity inverter; the U_{CE} voltage recovers to its normal level and the blocking bias of the transistor regulator is gradually taken off.

To ensure reliable conduction of the inverter thyristors for any load current and induced voltage situation, a d.c. gate signal is used, which results from rectification of 180° phase-shifted pulses.

Only the thyristors of opposed inverter arms can receive gate current simultaneously.

4.4 Protections and interlocks

Besides the usual interlocks required for safe operation, one should mention the particular precautions taken to protect the transistor regulator: the U_{CE} voltage reference is limited in value, whilst the current reference is also limited in maximum slope. Overvoltage and/or overcurrent detection switches off the supply; the fuses in the transistor emitter links and the breakdown diode V_Z represent an additional protection at a higher level.

Because the transistors are mainly power limited, a circuit has been implemented to avoid overloads due to erroneous operation or equipment misbehaviour: the product of the measured voltage U_{CE} and load current i_L is compared with a signal proportional to the current reference; the U_{CE} reference is reduced as soon as the result of the comparison $\left[(i_L \cdot U_{CE}) - K \cdot i_{L_{Ref}}\right]$ becomes positive.

By so doing, one keeps the transistor working point within a permissible operating area limited by a constant-power hyperbola $(i_L \cdot U_{CE}) = K \cdot i_{L_{Ref}}$.

4.5 Control facilities

The remote current control and acquisition takes place via the CAMAC data transmission system and the standard power supply interface, i.e. the 12-bit Hybrid Single Transceiver (STH).

The current reference signal is derived from an analog computer-controlled function generator (AFG), and the shunt signal is remotely displayed by means of the newly implemented analog signals observation system (SOS).

Local control facilities of the current reference and polarity as well as visualization of the power supply state (ON, OFF, STAND-BY) and of the interlocks is provided.

The U_{CE} reference can only be adjusted locally on the supply front panel.

5. CONSTRUCTION

The QCF,D and BDL power supplies (power parts and electronics) have been manufactured by Clemessy (France) on the base of a CERN design.

The supply dimensions are those of a standard 19″ rack (Figs. 13a and b).

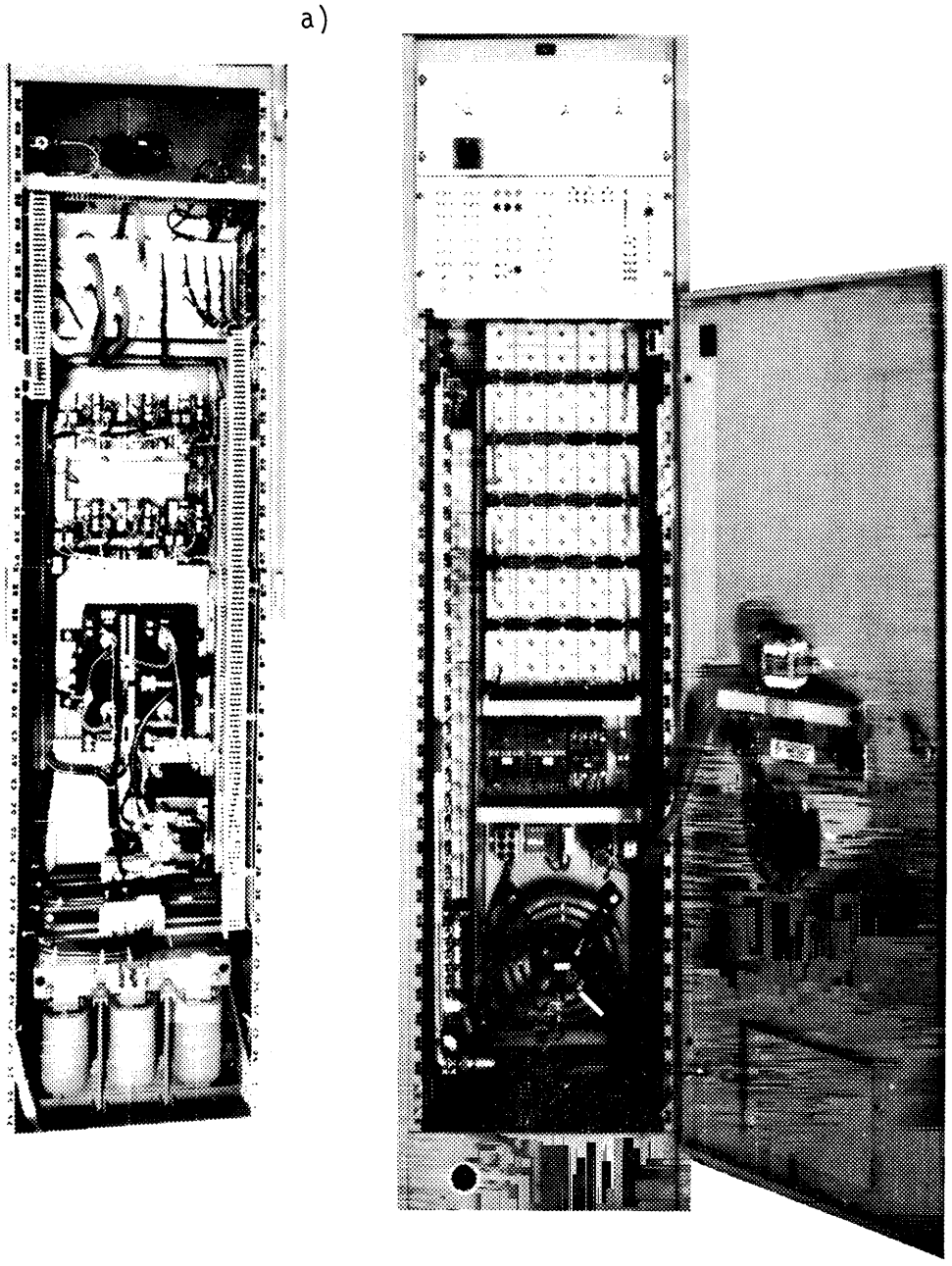


Fig. 13 Layout of BDL power supplies. a) Rear and b) front view.

The electronics occupies a 5H NIM crate and consists of seven plug-in units (Fig. 14):

- three-phase firing circuit (× 2);
- synchronization and unregulated 20 V supply;
- polarity inversion;
- auxiliary ±15 V and 30 V supplies;
- control and interlocks;
- current and voltage regulation.

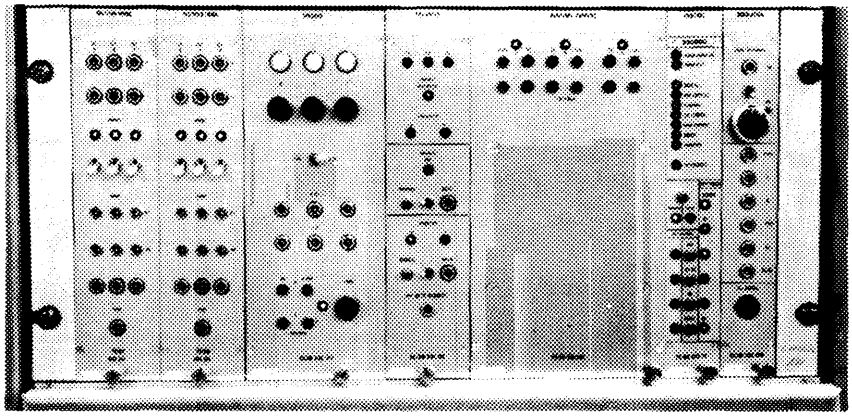


Fig. 14 Electronic crate

The voltage dividers for U_{CE}, U_L, and U_F (Fig. 3) which feed the regulation and the voltmeters on the upper part of the cabinet, the thyristors firing transformers, and pulse distributing networks are on separate printed circuits beside the power components.

Particular attention has been paid to certain operational aspects such as test facilities, safety, accessibility, separation of low-level and power signals, and earthing.

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Distribution: On request to Miss G. Maus, PS.

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