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DUAL CHANNEL FMC HIGH-VOLTAGE SUPPLY

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Abstract

The Beam Loss Monitoring (BLM) detectors and electronics are installed in the CERN accelerators to provide measurements of the beam loss and to protect from excessive losses. The majority of the BLM detector types require voltage biasing up to 2000 V_{DC} with a possibility to generate patterns to verify the connection chain from the detectors to the front-ends.

Currently, the power supply solution consists of Components Off-The-Shelf (COTS) large format power supplies with additional custom electronics and various interconnections to provide monitoring and remote control. For this reason, a market search has been done to identify a high reliability module suitable for dedicated BLM installations composed of a few detectors. The outcome of this market survey has justified the need to design a low-cost custom board, compatible with the CERN infrastructure and different detector types, as well as easily customizable to cover various installation architectures and needed voltage ranges.

The main characteristics of the developed board are: autonomy and full remote control; common hardware for different applications with a change of the DC\DC converter and a few components; smaller size than what is currently used as High-Voltage (HV) power supplies; multiple different high voltage or low voltage outputs for specific applications with the default design consisting of two positive high voltage outputs and one low voltage output; μV voltage sensing and mA current sensing capabilities; protection against overvoltage.

INTRODUCTION

The present article describes the design and test methodologies adopted to build and validate a dual channel high voltage supply in a FMC form factor. It will be used to bias BLM diamond detectors and mobile installations of ionization chambers and other beam instrumentation detectors in the CERN accelerators.

Next chapters highlight the effort put on the safety and operability aspects of the design related to the small form factor as well as the versatility and adaptability of the card for multiple use cases and applications.

DEVELOPMENT STRATEGY

Specifications

The first phase of the design focused on collecting specifications from all BLM systems at CERN, which are based mainly on ionization chambers with various dimensions and shapes, diamond detectors and silicon photomultipliers.

The outcome of the investigation is summarised in Table 1. A development baseline was defined to be a common platform for most of the BLM detectors with a board able to generate two high-voltage outputs and one low voltage output settable in a pre-defined range.

To minimize the development time, and to make the board compatible with several other platforms, the FPGA Mezzanine Card (FMC) form factor has been selected.

The CERN Beam Instrumentation Group has developed and already produced a large quantity of Intel Arria V based VME64x carrier for one High Pin Count (HPC) FPGA Mezzanine Card (FMC, VITA 57) called VFC-HD [1].

The additional requirements for FMC High-Voltage Supply were to keep the standard front panel width of 4HP, use SHV connector for high-voltage outputs and LEMO connectors for low voltage outputs. As an additional feature, it should be possible to plug adjacent boards into a VME crate without any risk of electrical discharges.

Table 1: Default Version Specifications

Version	Min Voltage [V]	Max Voltage [V]
V1	+175	+1734
V2	-175	-1734
V3	+5	+10

IMPLEMENTATION

Electronic Design

An XP Power AG Series DC/DC converter is the core component in the developed design. The AG Series is a broad line of ultra-miniature DC to HV DC converters that sets an industry standard in high-voltage miniaturization. Module are available in three categories of input voltages: 5 V, 12 V and 24 V. We have decided to use the 12 V series as default because it is the best compromise between the voltage and current level for the VME standard. Nevertheless, the FMC board is designed to be compatible with the 5 V series as well. The AG Series offers modules with positive or negative output voltages ranging from 100 V to 6000 V. The FMC High-Voltage Supply board is designed to work safely up to 2000 V. A possible extension up to 3000 V is still under evaluation.

Figure 1 shows a block diagram of the high-voltage interface. From the FMC connector, the mezzanine receives the +12 VDC power rail for the HV DC/DC converters and the +3.3 VDC power rails to the digital circuitry. A power enable digital signal is used to control, using Pulse Width Modulation (PWM), the +12 V_{DC} rail making it possible to adjust the main HV DC/DC accordingly, with the XP Power AG series that works at 12 V_{DC} or at 5 V_{DC}, while the voltage regulator is fine-

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tuned by a DAC and additional dedicated circuitry. The high-voltage output is monitored by a high-resolution ADC through a 1:1000 high-voltage divider. An auxiliary ADC measures the primary side of the HV DC/DC converter to indirectly monitor the power consumption at the output, and at the same time to allow a supervision algorithm to control power dissipation.

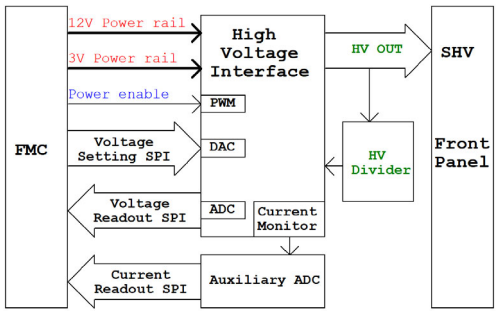

Figure 1: HV Supply basic block diagram.

Both high-voltage outputs available on the developed board have the same independent structure except for the auxiliary ADC which is shared by all output interfaces for the current consumption measurement. The low-voltage output has the same structure except for the HV divider (which is just a low voltage divider) and the ADC, since the auxiliary ADC, shared with the other output interfaces, is used for both output voltage read out and current measurement.

Figure 2 gives a global overview of the board structure: all connections through the FMC connector are on the left, while on the right side of the figure there is the front panel which carries two SHV connectors for the high-voltage outputs and also two LEMO connectors for the low voltage output. For the low-voltage outputs, we decided to bring out both the direct +12 V_{DC} (coming from the VME and controlled by a switch) and the adjustable output voltage.

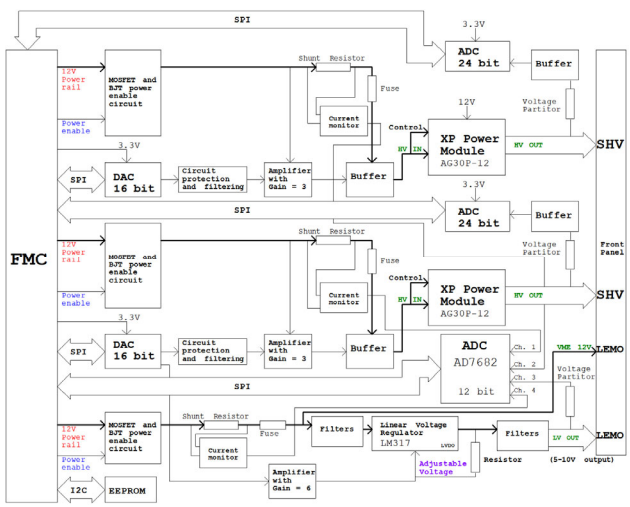

Figure 2: HV Supply detailed block diagram.

All interfaces share the same architecture, but they are independent from each other. Consequently, five independent SPI buses are routed to the FMC connector. An EEPROM is also present on the board and connected by I^2C as requested by the FMC standard specifications.

Figure 3 shows the circuitry used to control the HV DC/DC modules. The power enable circuit, controlled by the HV_ENABLE input, uses a BJT connected to a PMOS gate to safely control the 12 V power supply for the rest of the driver circuit. The PMOS source is connected to the 12 V power rail of the VME. This 12 V rail supplies the amplifiers and the BJT in the DAC amplifier circuit. Therefore, when the PMOS is off, the 12 V rail does not supply the amplifiers and BJT, and no HV signal is created. The circuit is simple but robust enough for our needs. When there is no power enable signal, the BJT does not conduct and the PMOS is off. When the power enable signal is on, the 3.3 V signal activates the BJT. This biases the PMOS gate allowing the PMOS to fully conduct and transmit the 12 V to the rest of the circuit. After the PMOS, there is a shunt resistor used to monitor the current consumption of the entire HV circuit (HV Driver, HV DC/DC Converter and HV Control Circuit). The current consumption is then measured as a voltage signal through a shunt connected to a current amplifier. This signal is digitized by an ADC and sent through SPI to the carrier board FPGA.

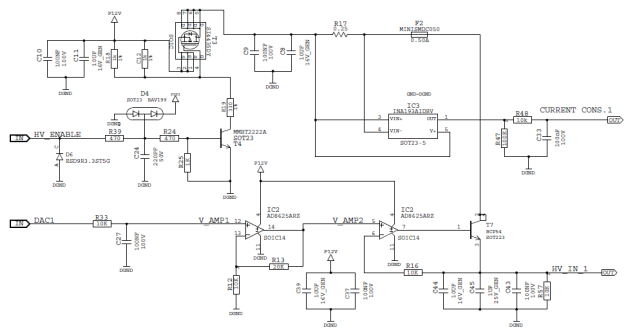

Figure 3: HV interface electrical drawing.

The HV_ ENABLE signal is a PWM with a duty cycle settable from 0 to 100%. For HV DC/DC converters that work with an input voltage of 5 V instead of 12 V, the power dissipation on the BJTs can be optimized by driving the power enable circuit with a 100 kHz PWM control signal @ 50% duty cycle.

In such a case, the output voltage of the enabling circuit becomes 6 V and the HV DC/DC output can be controlled by the DAC avoiding excessive power dissipation on the BJTs.

PCB Design

Functions on the PCB have been distributed as shown in Figure 4 and Figure 5. Most of the active and passive components are located on the top side of the board, while the bottom side is mostly dedicated to the high-voltage circuitry and power dissipation areas for active components. To increase the power dissipation performance, the PCB solder mask has been removed from the dissipation areas, in addition capped and filled vias

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have been selected. In such way we have maximized the dissipation area and its thermal exchange.

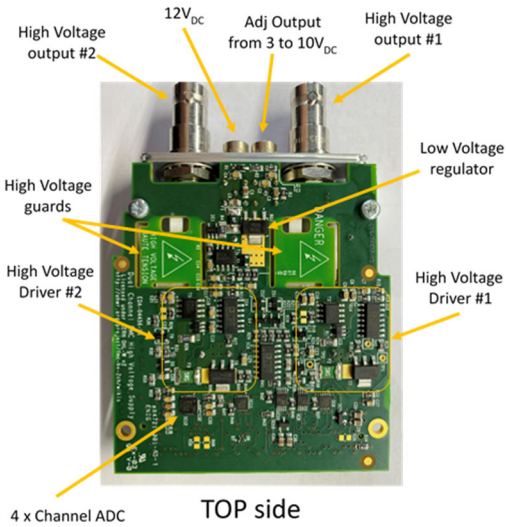

Figure 4: Board picture - top side.

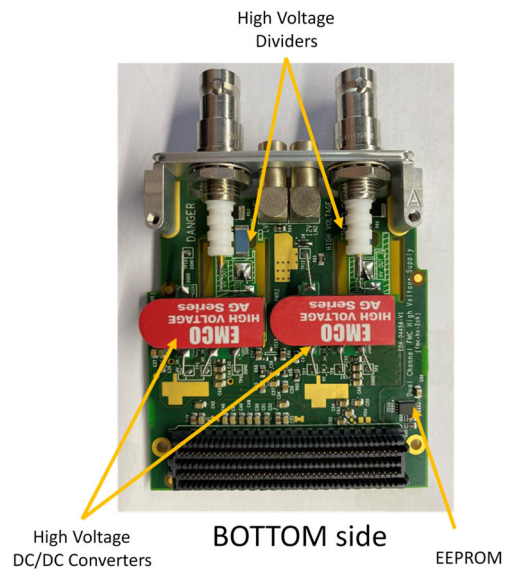

Figure 5: Board picture - bottom side.

The PCB design required particular attention due to the presence of high-voltage, which is a potential source of safety issues, electrical discharges, and current leakage. For these reasons, dedicated high-voltage guards have been created on the PCB by applying the following rules:

- A single wire connects the SHV connector to the HV DC/DC converter and the PCB pad for the HV divider.
- Except for the soldering pad of the HV wire (bottom side), all copper is removed in all PCB layers up to the top side in the HV high area.
- The minimum distance between HV copper and all other lines is greater than 5 mm in all directions.
- The PCB substrate has a Comparative Tracking Index (CTI) 0 for voltages greater than 600V.

Figure 6 highlights the layout implemented to build the high-voltage guards.

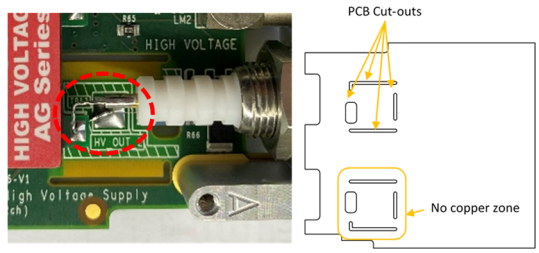

Figure 6: High-Voltage guards.

Detailed Documentation

The design is managed in Open Hardware Repository OHWR [2]. Detailed documents for the electronic design including the layout and the hardware design manual are available and public on the CERN EDMS archive [3].

Testing

Board testing was possible after its integration on the VFC-HD carrier, and thanks to the creation of a generic firmware (FW) interface module. The FW is based on a wishbone bus and available on the OHWR website.

In parallel to the FW creation, a script interface was written to allow both sending of commands through the VME bus and monitoring the HV power supply parameters. Such an interface allowed us to perform a full basic verification of the board and to successfully test it with the CERN ionization chamber and diamond BLM detectors. With a custom version of the board, it was possible to use it to directly drive a commercial Heinzinger NCE 3000 series high-voltage and high-power supply.

After the basic verifications, a successful safety check was performed by testing integration in a 19' chassis with adjacent boards. All power dissipation areas on the PCB were monitored with a FLIR E8 infrared camera. The HV power supply was installed without ventilation to create a non-nominal worst-case condition to check the limit of the design. In the worst case, the board hot spots were about 20 degrees Celsius above ambient temperature which accordingly to the calculation a reliable working condition.

Firmware

A low-level generic firmware was designed to validate the HV FMC prototype. As shown in Figure 7, the firmware implements control and status signals, 3 PWM modules, 5 SPI masters associated with a custom Finite State Machine (FSM) managing the ADC and DAC protocols and an I2C master with a standard Wishbone slave input interface.

This basic firmware was tested on a complete GHDL/GTKWave testbench instantiating a model of every component of the FMC. All the files are available on the OHWR.

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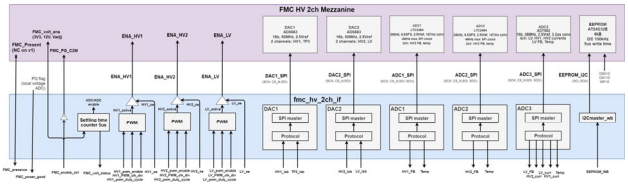

Figure 7: Low-level interface firmware architecture.

Control Algorithm

A control algorithm with two main functions is required inside the FPGA to operate the board efficiently. Firstly, it oversees the output voltage and steers it as close as possible to the set point. Secondly, it makes sure that the core module of the board that provides the high voltage is operated safely. These functionalities are necessary to operate the core module as its output voltage is set by not only the input voltage but also by the load attached to its secondary side. This load can have a resistive, capacitive, or inductive behaviour, thus making it difficult to operate without voltage feedback. In addition, the module needs to be protected against overvoltage and overcurrent.

Figure 8 shows the typical input-output characteristics of the DC-HVDC module for different loads as per the manufacturer's datasheet. The dashed line shows how much the output voltage can differ with a constant input voltage but under different loads. Without a load, the output voltage can damage the module as it crosses the safe operating limit (red line).

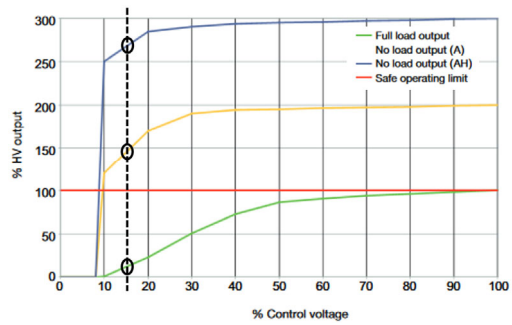

Figure 8: Module output voltage versus input voltage.

The load was modelled using Simulink to test different strategies for the feedback controller and select the optimal one. Figure 9 shows, as blue blocks, the feedback-based voltage and current controller selected for implementation. It is built around one integrator with a gain and a saturation to select the maximum voltage rate.

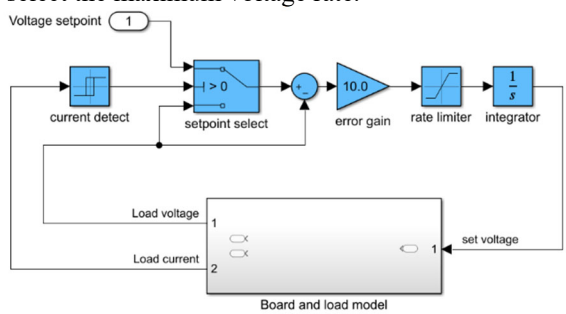

Figure 9: Voltage/current feedback controller principle.

The current limit detection controls a switch that lowers the set voltage until the current goes below the limit, making the module compatible with capacitive loads which will be charged with the highest possible current until they reach the desired voltage.

Figure 10 illustrates a simulation scenario where the set voltage (black line) is too high for the module with the load sinking too much current, therefore forcing the algorithm to limit the output voltage (red line).

The oscillation level is the set by the hysteresis selected in the current detection module.

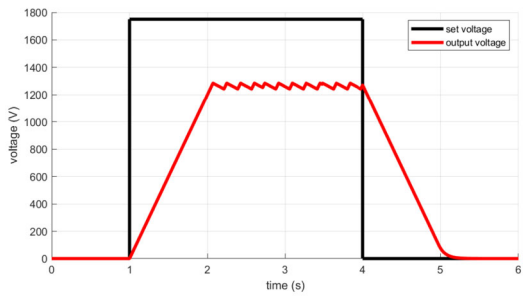

Figure 10: Simulated behaviour with a load drawing excessive current.

The selected algorithm is written in VHDL and simulated with traditional HDL tools. While Simulink models are generally 64 bits floating points number representation, the FPGA implementation uses lower precision to limit resources usage. The simulation with 32 bits fixed point numbers shows satisfactory precision and will be used for the final implementation.

The algorithm is still in development and an additional test campaign will be carried out as soon it is ready.

CONCLUSIONS

The first version of the dual channel FMC high voltage supply has been successfully validated, and all design details including the design manual, the low-level firmware and the control algorithm are public and available on the OHWR.

By following the design methodology described in this article, we have optimized the development time and maintained the flexibility by using a standard platform and selecting a core component which offers a large selection of output levels.

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[2] CERN, CERN Open Hardware License (CERN OHL), http://www.ohwr.org/projects/cernohl/wiki

[3] Dual Channel FMC High Voltage Supply CERN EDMS archive: https://edms.cern.ch/item/EDA-04456-V1-1/0