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TECHNICAL REPORT

The upgraded quench protection system for main quadrupoles in the LHC

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ABSTRACT: The protection of superconducting magnets is a very important issue and demanding challenge in the LHC and other superconducting accelerating facilities. The quench phenomenon can destroy components of the accelerator, and therefore this digital system was designed, implemented, tested, and installed near each superconducting magnet in the LHC tunnel. The quench detection principle relies on the extraction of resistive voltage by compensation of the inductive part of the voltage. This article presents briefly the architecture applied to the design and the validation of the FPGA-based quench detector for the main quadrupoles of the LHC. The article focusses on digital design with the use of FPGA by VHDL coding and on the verification by simulation. The design is a replacement for the old detection system.

KEYWORDS: Digital electronic circuits; Digital signal processing (DSP); Hardware and accelerator control systems; Acceleration cavities and superconducting magnets (high-temperature superconductor, radiation hardened magnets, normal-conducting, permanent magnet devices, wigglers and undulators)

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1 Introduction

The LHC (Large Hadron Collider) particle accelerator located at CERN (European Organisation for Nuclear Research) is the largest research instrument ever built. It comprises the largest superconducting system to produce a high magnetic field shaping the trajectory of the particles.

The need for a system of active magnet protection at the LHC originates from the nature of the superconducting cables used to build the magnets. The cables are not cryostable [1] and therefore a random and local temperature change can lead to a sudden transition to a normal conduction state. This phenomenon is named quench. The first distributed system of this kind was built more then forty years ago [2].

The LHC protection system comprises many subsystems. One of the sub-systems is the magnet quench protection system QPS (Quench Protection System) [3]. This system consists of the quench detection system QDS (Quench Detection System) and actuators which are activated once a quench is detected. Since the beginning of the LHC operation, the QDS has consisted of several kinds of detection devices. For various superconducting circuits, the detectors have utilised different technologies to perform the detection function. The base layer, still in operation, is based on classic

analogue technology using a measurement bridge and a comparator. For supervision, an 8-bit microcontroller with integrated analogue to digital converters (ADC (Analogue Digital Converter)) was used. Other devices, used in zones with no or little radiation were based on standalone ADC and digital signal processors [3]. During LS1 (Long Shutdown One) a number of new quench detectors built with FPGA (Field Programmable Gate Array) devices were introduced to the system to substitute older devices with modern technologies and improved immunity to SEE (Single Event Effect) [4].

The operation of the LHC is divided into periods of "physics runs" and "long shutdowns". During physics runs only little changes to the construction of the accelerator can be introduced. Therefore major upgrades and replacements are introduced in "long shutdown" periods. During LS2 (Long Shutdown Two), the device replacement campaign was launched for the main quadrupoles. The design was developed before LS2 and the development works included the design of analogue and digital hardware as well as the preparation of the VHDL (Very High Speed Integrated Circuit Hardware Description Language) code for the flash-based FPGA of Microchip®. The family of FPGA devices known as ProASIC3E are fabricated in 130 nm flash-based CMOS (Complementary Metal-Oxide-Semiconductor) technology with 7 metal layers [5]. The new device was designed, assembled, tested, and commissioned. This publication is dedicated to presenting this device in detail. A short overview of the system was already presented in conference [6].

2 Superconducting circuits of main quadrupoles in the LHC

In the LHC two beams circulate in two opposite directions: clockwise and counterclockwise. The two beams correspond to two beam pipes: external and internal with respect to the centre of the ring. The LHC consists of eight sectors. Each sector consists of a set of cells (average 25 cells per sector). One cell consists of two half-cells. Each half-cell consists of three dipoles MB (Main Bending) and one quadrupole MQ (Main Quadrupole). It means there are around 50 MQs and 150 MBs in the sector. Both types of magnets were constructed as twin aperture and thus contain coils for two beams. Therefore one can distinguish external and internal magnet apertures. The apertures are separated with 194 mm distance. The schematic view of one cell is presented in figure 1. In order to concentrate only on quadrupoles, the figure does not reflect the real geometric relationships. Actually, the length of one dipole MB is 16.5 m while the length of one quadrupole MQ is 5.3 m.

In the first half-cell, one beam running through the quadrupole is focused while the second is defocused. In the second half-cell, the configuration of the magnetic field is the opposite. All focusing parts of magnets MQ are connected serially (blue line) and powered by one power converter located at the end of the accelerator's sector with the current I_{mag} on the nominal level of 11.9 kA. Similarly, the defocusing parts of magnets MQ form a second circuit (red line). It means there are two superconducting circuits in each sector dedicated to the generation of the quadrupole fields in each half-cell.

One part of the MQ magnet consists of four coils connected in series which conduct a superconducting current as it is presented in figure 2 for the case of external aperture. The directions of the windings of the coils are marked by the direction of the round side of half-waves in the inductance symbol. The by-pass diode and protection resistor were also shown as passive quench protection elements. The middle point of the system of four coils is used as the lowest potential

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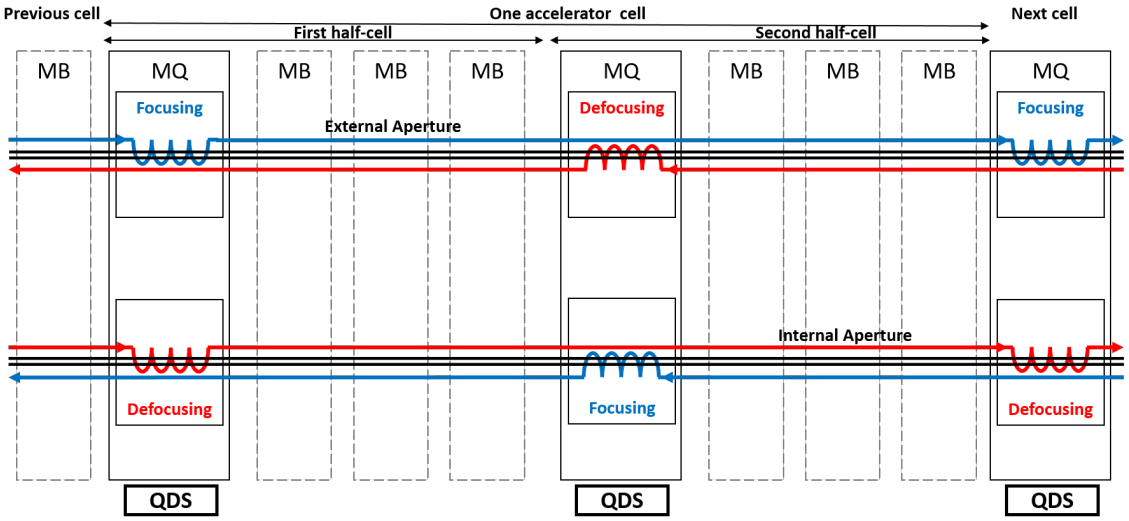

Figure 1. The general view of main quadrupole circuits presented over one cell of the accelerator's sector. Blue and red colours denote two superconducting circuits for focusing and defocusing coils.

of protection electronics. The digitised data is galvanically isolated before delivering to the digital core of the detector. The symbols $U_{1\mathrm{EXT}}$, $U_{2\mathrm{EXT}}$, and U_{QS0EXT} are used twice: on the left side of figure 2 as analogue voltages, and on the right side of figure 2 as digital values. Through the rest of this text, the symbols are used in the shortened form U_1, U_2, and U_{QS0} without denoting the aperture (EXT, INT).

For the voltage bridge in figure 2, the KVL (Kirchhoff's Voltage Law) was used for the upper and lower parts of the bridge:

$$U_1 + I_0 \cdot R_1 - U_{\mathrm{QS0}} = 0, \tag{2.1a}$$

$$-U_2 + U_{\mathrm{QS0}} + I_0 \cdot R_2 = 0. \tag{2.1b}$$

Subtracting these equations and assuming that $R_1 = R_2$, the diagonal voltage of the bridge is

$$U_{\mathrm{QS0}} = \frac{1}{2}(U_1 + U_2). \tag{2.2}$$

3 Quench protection unit for one quadrupole

The quench detection principle for LHC's Main Quadrupole magnets is based on the measurement of the resistive voltage drop over the magnet. In a superconducting state, this voltage would be zero. However, if the current I_{mag} is changing in the magnet with inductance L, an inductive voltage U_{ind} is present.

$$U_{\mathrm{ind}} = L\frac{di}{dt} \tag{3.1}$$

To differentiate between the inductive U_{ind} and the resistive U_{res} voltage, a measurement bridge is used as shown in figure 2. Comparing the voltages across two halves of the magnet with equal inductance compensates for the inductive voltage drop. Assuming that at the same time a quench

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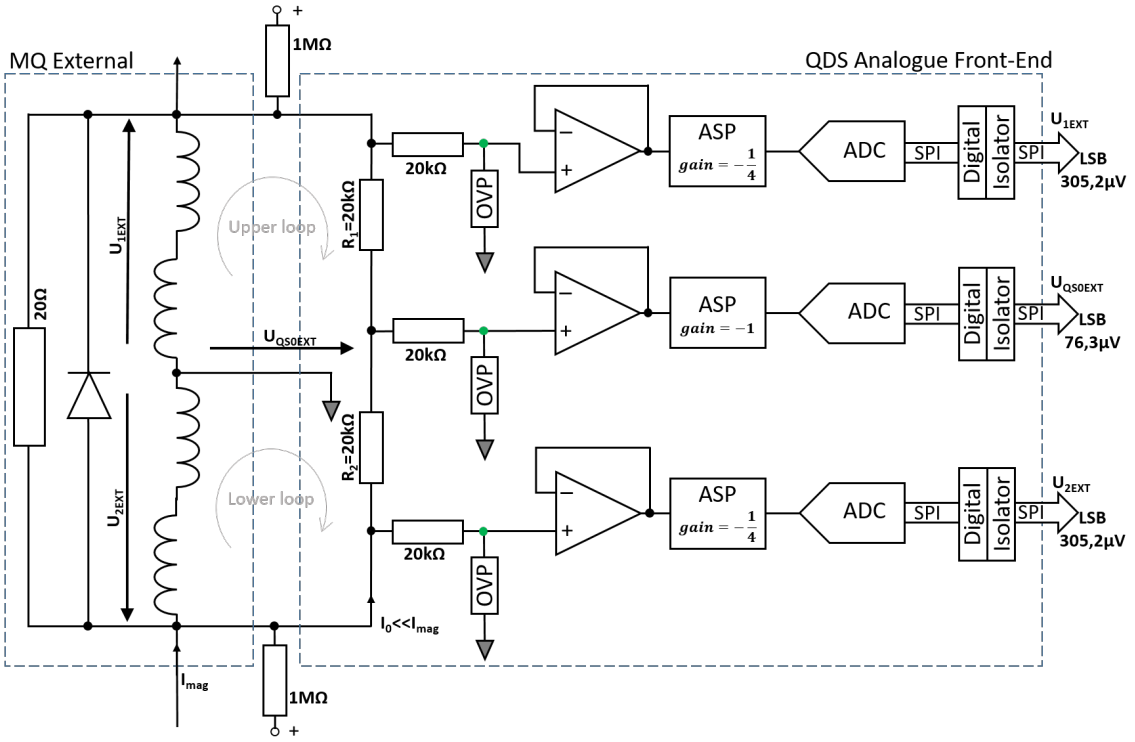

Figure 2. The connection of quadrupole magnet and analogue front-end of quench detector. On the right side, for each analogue channel, the resolution LSB of conversion to the digital signal, calculated with respect to input range is presented. The input points are marked with green.

appears only on one side of the magnet, this scheme is robust and reliable. For aperture-symmetric quenches, an additional detection system layer was installed in the past.

The voltages over the two halves of the magnet are named U_1 and U_2. The voltages U_1 and U_2 are measured in the opposite direction (figure 2), the sum of them gives zero or, in the case of the quench, is equal to the resistive part

$$U_{\text{res}} = U_1 + U_2. \tag{3.2}$$

The resistive part of the voltage is used to discriminate between the superconducting state and the quench event. When a quench is detected, a number of trigger signals are activated and sent to other parts of the protection unit and other subsystems of the accelerator. Two different actuators are activated by the quench detector in case of a quench.

The first is a local device which injects energy into the quenching magnet known as HDS (Heater Discharge Supply). To protect the magnet coils from overheating the quench heater power supply discharges a capacitor bank into the magnet's heater strips. The heaters are resistive tapes located directly on the surface of superconducting coils inside the magnet [7]. The tape heats the coil when HDS releases energy into it. In this way, the development of the quench phenomenon along the coil can be accelerated, hence distributing the energy loss to a larger area. Once the resistive voltage build-up exceeds around 6 V a cold by-pass diode is activated bypassing the decaying circuit current around the quenched magnet. This is a fundamental requirement to avoid damage to the coil.

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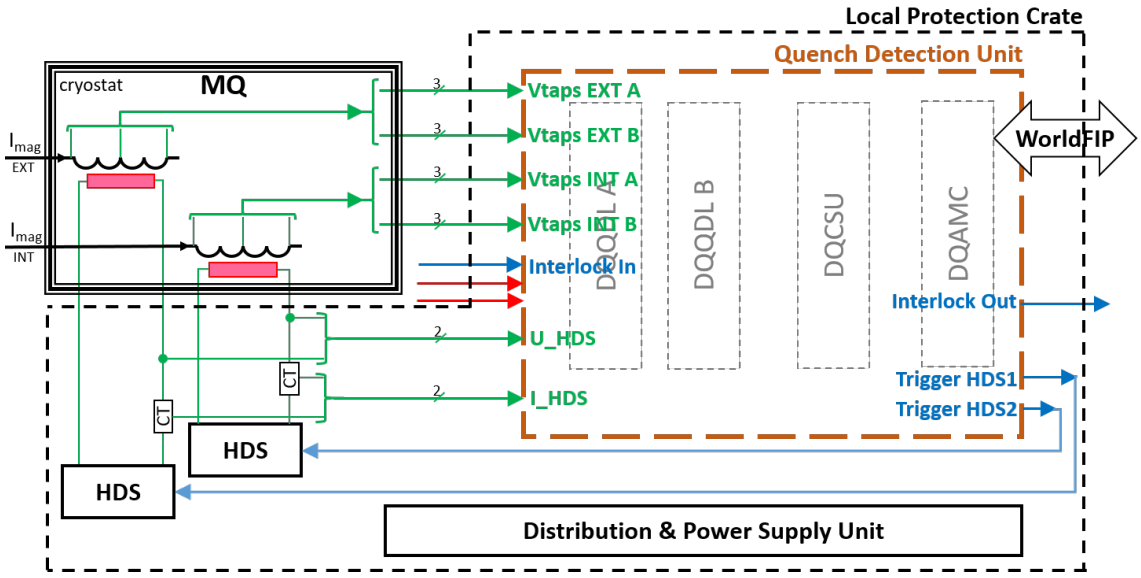

Figure 3. The signal flow block diagram of quench detection for main quadrupoles at the LHC. Green lines are analogue signals. Blue lines are trigger signals. Red lines are powering lines. Pink colour denotes quench heaters. The Brown dashed line denotes the quench detection unit. The Black dashed line denotes the local protection unit.

The second type of actuator is a relay rupturing a global current loop serving as a machine interlock. The interlock acts as a fast messaging system to initiate beam dump and power abort of the whole LHC accelerator [8].

The local protection unit designed to protect one LHC main quadrupole magnet consists of:

1. one quench detection unit,
2. two quench heater power supplies type DQHDS,
3. one distribution and power supply unit housing two power supplies on redundant AC feeders and two pulse CT (Current Transformer) to measure discharge current of DQHDS power supply.

The connections between the listed above elements and the protected magnet MQ are presented in figure 3. The lines in green indicate analogue signals. The pink rectangles represent quench heaters.

The quench detection unit consists of:

1. two redundant A and B quench detectors with accompanying interlock/trigger subsystems DQQDL,
2. one system controller performing local supervision of analogue signals and time synchronisation DQCSU,
3. one communication controller and field-bus controlled acquisition subsystem DQAMC.

The connections between the listed above components and their internal structures are presented in figure 4.

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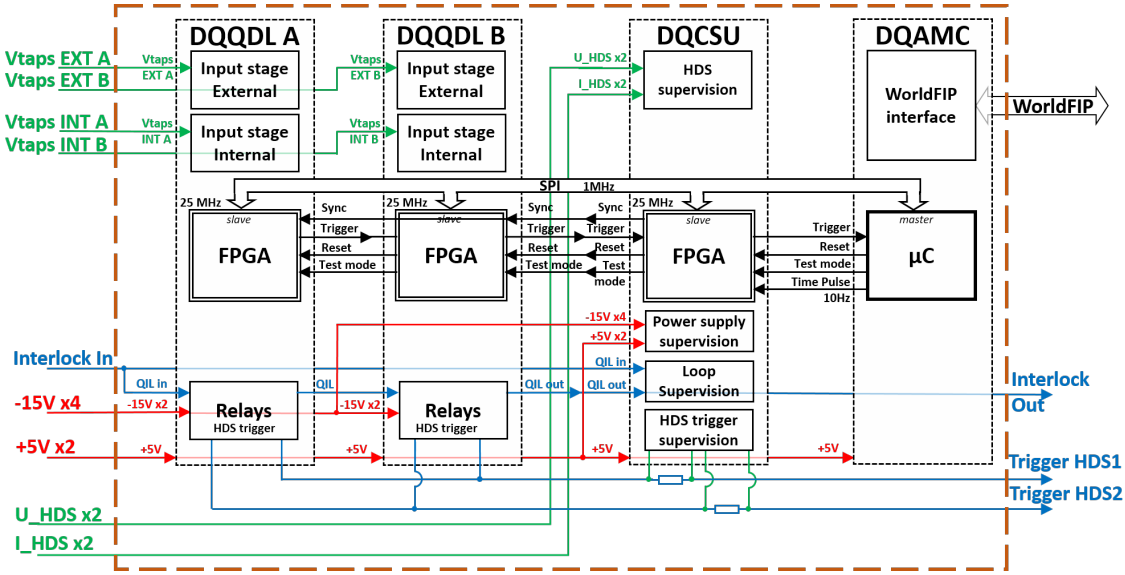

Figure 4. Detailed block diagram of the quench detection unit for LHC main quadrupoles. Colour code: green — analogue, blue — triggers, red — power, black — digital signals. Symbols **A** and **B** denote redundant boards of quench detector DQQDL and main analogue input signals. Twofold redundancy of signals is designated with '**x2**', while fourfold redundancy is marked with the symbol '**x4**'.

Both modules, DQQDL and DQCSU, are based on a flash-based FPGA which was chosen due to higher immunity to radiation especially in the sense of SEE. Further improvement of radiation tolerance was achieved by using a triplication of all flip-flops and memory blocks. A procedure of TMR (Triple Module Redundancy) was applied during the synthesis of the VHDL description [9]. In other words, the consumption of flip-flops is three times higher and several logic gates are added to vote between three output signals. Therefore, the choice of system clock frequency was dictated by a trade-off between speed and the FPGA's resource consumption. In order to fit two channels for two apertures with full TMR in one ProASIC3E FPGA with 1 500 000 system gates, a decision has been made to lower the system clock frequency to a value of 25 MHz.

The local protection crate is located in the LHC tunnel below a dipole magnet adjacent to the protected quadrupole. This location was chosen to reduce the exposure of the quench detection system to radiation. The redundant quench detectors are connected to the quadrupole magnet via redundant voltage taps. In case of a quench, the discharge of the DQHDS is monitored by the DQCSU. The communication with the accelerator control system is ensured by the DQAMC via a field bus. Since the DQAMC was recuperated from the previous installation, an interface board had to be developed to be able to adapt the small dimensions of the DQAMC board to the much bigger dimensions of the crate. The following sections describe the components of the quench protection unit in greater detail.

3.1 Quench detector DQQDL

The quench detector consists of two galvanically isolated analogue input stages and a common, FPGA based digital part.

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3.1.1 Analogue input stage

The detector input stages implement a measurement bridge that consists of the magnet coils and two resistors located on the PCB (Printed Circuit Board) of the input stage. The two voltages U_1 and U_2, as well as the bridge voltage U_{QS0}, are measured. Hence the front-end electronics consists of three independent channels as shown in figure 2. The input stages are galvanically separated from the rest of the protection electronics and referenced to the potential of the mid-point of the magnet coils. This potential is marked in figure 2 by a down-facing arrow symbol. Protection of the input stage against short voltage spikes is ensured by a transient voltage suppressor diode in combination with series resistors marked as OVP (OverVoltage Protection).

Given the analogue input range of −10 V to 10 V for U_1, U_2 channels and −2.5 V to 2.5 V for U_{QS0} channel, the ASP (Analogue Signal Processing) chain has to attenuate and level shift the input signals to match the input range of the ADC which is 0 V to 5 V (figure 2). Since three inverting amplifiers are used, the signal in front of the ADC is inverted with respect to the input. This is corrected in digital signal processing. To increase the resolution, a smaller input range of ±2.5 V was chosen for the U_{QS0} channel. Due to different attenuations (gain less than 1) in U_1, U_2 channels and in U_{QS0} channel, different resolutions LSB of digital signals exist in two kinds of processing chains.

The ADC of the SAR (Successive Approximation Register) type was chosen due to its radiation resistance. It can operate up to a sampling rate of 200 kSPS. The digital data is transmitted via an isolated SPI (Serial Peripheral Interface) interface to the detector's data processing element implemented in an FPGA.

3.1.2 FPGA firmware

All digital signal processing as well as the numerical operations of the quench detection algorithms are implemented in the quench detectors' main FPGA. The following sections describe the functions implemented in the FPGA firmware. The digital core inside the FPGA implements two identical detection algorithms: one for the external and one for the internal aperture of MQ (focusing and defocusing part of MQ). While some parts of the design are common such as communication, command decoding and data buffering, the quench detection works independently for each aperture. Figure 5 shows a block diagram of the FPGA firmware indicating this partition. The ADC interfaces which communicate with the ADCs via dedicated SPI buses, convert the serial data stream to a 16-bit two's complement signed integer. This unit is followed by a start-up unit which suppresses any data from the ADC until the analogue input stages are powered up and the ADC is working properly. The communication module controls the SPI connection to the communications controller type DQAMC. It decodes commands and buffers data from the signal-processing pipelines and configuration parameters. The memory of this module is implemented inside the FPGA using embedded SRAM (Static Random Access Memory) blocks to implement a triplicated memory with a depth of 64 B for each instance. This memory space is divided into a data region (20 B) which stores current samples from all measured channels and a configuration register region (44 B) which stores parameters. This memory is marked as `ctrl_reg` in figure 6 and 7.

Implementation of quench detection algorithm. The architecture of the quench detection algorithm is shown in figure 6. The three measured signals are conditioned by independent DSP chains.

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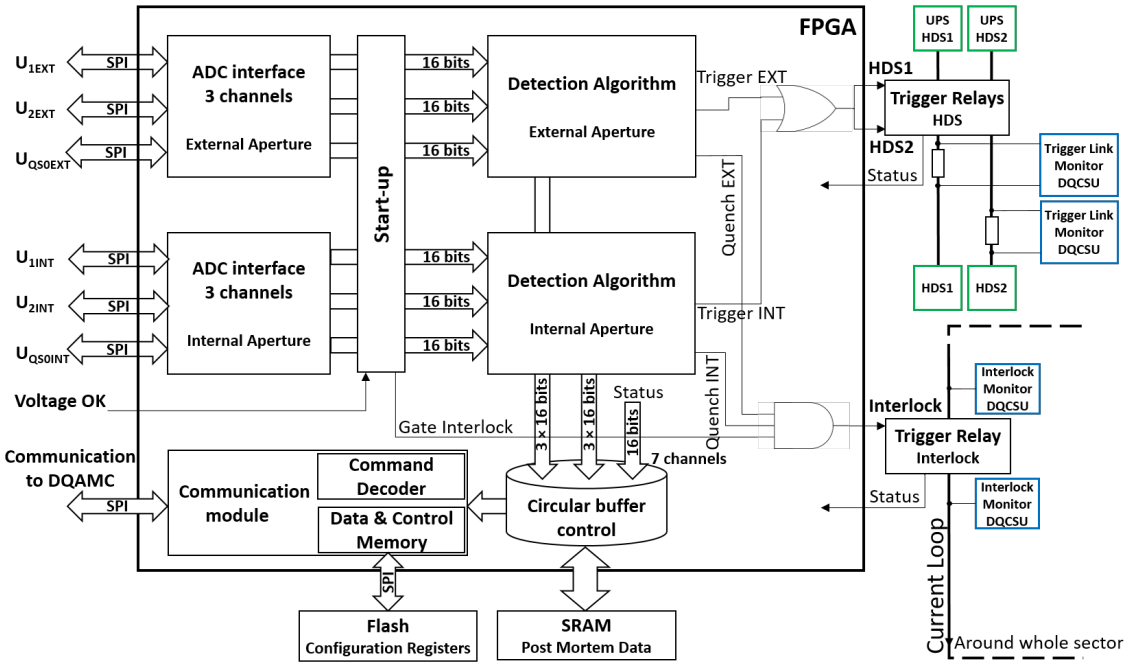

Figure 5. The simplified block diagram of digital hardware architecture implemented in FPGA together with some devices located on the DQQDL board. Redundancy is not included. Blocks in blue belong to another board named DQCSU. Blocks in green are separate units of quadrupole QDS.

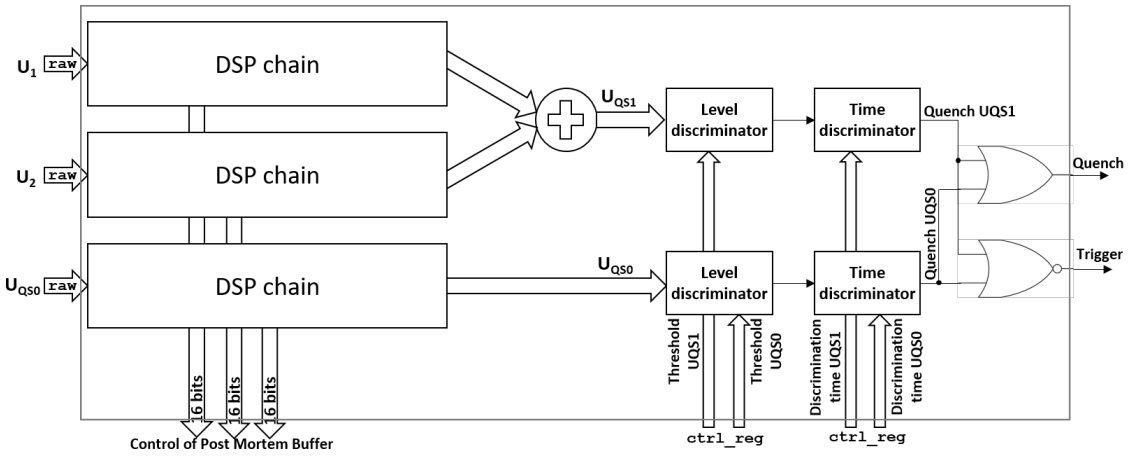

Figure 6. The simplified block diagram of VHDL code for detection algorithm of DQQDL board.

While coils' voltages U_1 and U_2 are added and their sum is compared to a threshold, the bridge voltage U_{QS0} is directly compared with a threshold. These two equivalent signals are used in a redundant way. Since the input range of the measured bridge signal is smaller its resolution is higher than the numerically computed signal. The outputs of the level discriminators are validated by time discriminators to avoid spurious triggering. Voltage level and time thresholds are configurable via the communication interface and are stored in flash memory outside the FPGA.

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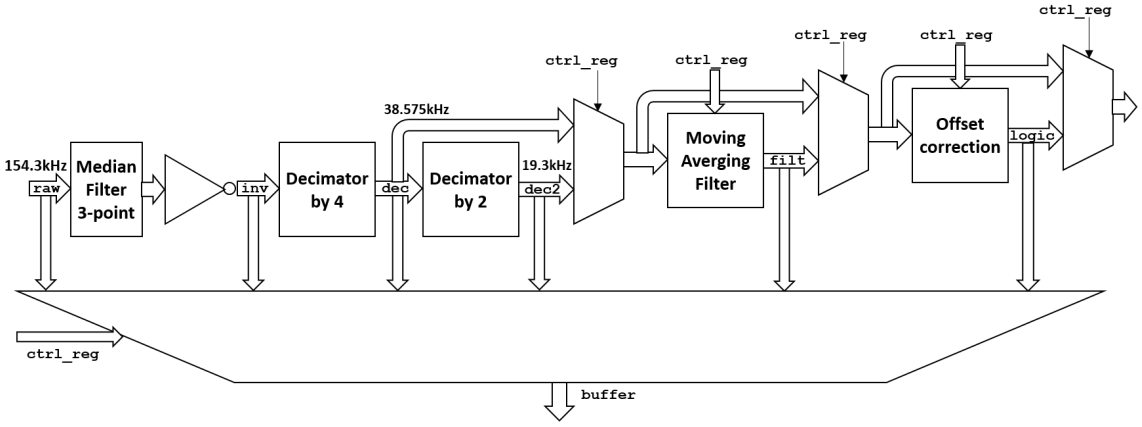

Figure 7. The simplified block diagram of VHDL code for DSP chain of DQQDL board.

Hardware interlocks and safety features. Each MQ is connected to two DQHDS as protection elements. Each of these is triggered by the quench detector via an independent trigger link controlled by a conventional relay for radiation tolerance purposes. As an additional level of redundancy each of these links is controlled by two parallel relays, hence each detector controls four heater trigger links which are coupled by diodes on the crate level. In case of a detected quench in any of the two circuits, all four links are activated. (Figure 5.) To avoid HDS triggers during the start-up phase of the detection board, the inputs to the signal pipelines feeding the quench detection algorithm modules are held at zero ($x0000$) until two conditions are fulfilled. First, the flag of powering of the analogue front-end modules has to indicate correct powering by activating signal `Voltage_OK`. Second, the flag indicating the correct ADC conversion has to be received from the ADC interface. When ADC is during conversion mode, the data line of the respective SPI link, should be in the low state. In case of a digital isolator is broken or its powering is missing this line would be constantly high. The start-up module generates an additional waiting time of $\approx$1.3 s. Then the input signals to the signal processing chains and to the quench logic are released. As long as the start-up module is active, the interlock loop is forced open, which blocks the powering of the magnet circuits. In this case, the status flags indicate the source of the open loop and allow a detailed diagnosis.

Digital signal processing. The data from the ADCs is processed before the quench detection logic is applied. The diagram in figure 7 shows the DSP chain. Some of the stages of this chain are separated from each other by two-to-one multiplexers. The multiplexer structure allows the use or omission of the output of a preceding stage. Selection signals for multiplexers are stored in configuration registers `ctrl_reg` and can be modified. As a first stage, the data is passed through a 3-point median filter which rejects single-sample errors which are typical for radiation-induced SEU (Single Event Upset). Due to the inverting nature of the analogue front-end, a digital inverter calculating the two's complement of data after the median filter is necessary. Next, the data which is sampled at 154.3 kHz, is decimated in two steps, first by a factor $n = 4$ and then by $n = 2$. The decimators sum-up n values and put the average of n points as the output value. The second decimator can be disabled via the control registers. Following the decimation stages, a moving averaging filter further limits the band of the signal. The length of this filter is also configurable

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via the control registers and its default value is set to 6.6 ms which efficiently rejects 150 Hz and multiples. The last stage is an offset correction stage which can be controlled by the control registers. A separate multiplexer allows selecting which data is recorded in the post-mortem buffer. There are six possibilities: raw data `raw`, inverted data `inv`, decimated by 4 `dec`, decimated by 8 `dec2`, filtered `filt`, and corrected `logic`.

Diagnostic buffers. As shown in figure 5 the quench detector is equipped with an SRAM as volatile memory. It is used to store the so-called post-mortem data which is used for the diagnosis of a quench event. It continuously stores seven streams of data in a circular buffer. In the case of an event, the circular buffer continues recording until half of its data is recorded before and a half after the event. A memory of capacity 1 Mword (2^{20} = 1 048 576) of 16-bits words is used. Given this size of memory, 74 898 samples before and after the trigger are recorded filling the entire available space. If the data is decimated by 4 (38.575 kHz), the time period covered by the buffer is 3.883 s. When the decimation factor is 8 (19.3 kHz), the time length of the buffer is 7.766 s. The buffer can be read in a decimated mode where the average of 16 samples is calculated during readout. In this mode, the rate of data in the buffer is 2.41 kHz and 1.205 kHz respectively.

Non-volatile data storage. To store the configuration parameters the detector board is equipped with flash memory as a non-volatile storage element. The flash memory contains 44 configuration 8-bit registers that hold critical parameters such as thresholds, offsets, filter length, ADC speed, discrimination times, selection signals for multiplexers, and many others.

3.2 System controller DQCSU

To ensure high reliability and availability of the QDS, critical parts of the system are monitored by the local supervision and timing synchronisation module DQCSU. The DQCSU implements the following functions:

1. quench heater discharge supervision,
2. quench heater trigger link current monitoring,
3. interlock loop monitoring,
4. remote power cycle of quench detectors and crate,
5. trigger and timing controller,
6. power supply monitoring.

To perform its functions, the system controller comprises fourteen ADCs to acquire measurement data from many different places in the system. Each path uses a dedicated DSP chain and delivers logging and PM (Post Mortem) data. The whole architecture of the digital algorithm implemented in the FPGA is presented in figure 8 and the summary of the signal channels is shown in table 1.

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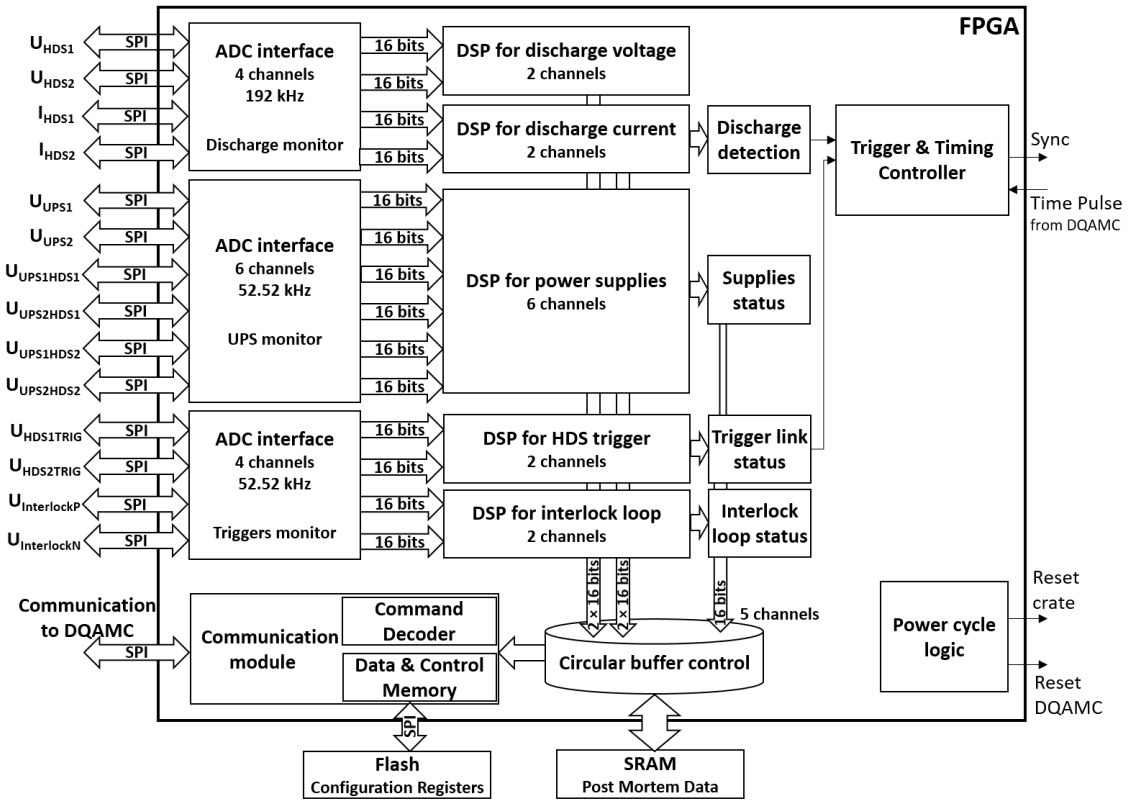

Figure 8. The simplified block diagram of digital hardware architecture implemented in FPGA together with some devices located on the DQCSU board.

Table 1. Overview about the analogue measurement channels of the DQCSU and their main characteristics. `median` stands for median filter, `mavg` stands for moving average filter, `dec` stands for decimation. A `flag` is saved in PM buffer indicating the violation of a pre-defined threshold.

Analogue channel name	Number of ADCs	Input range [V]	Sampling rate [kHz]	DSP chain architecture	PM buffer
`HDS voltage`	2	0 . . . 5 diff	192	none	yes
`HDS current`	2	0 . . . 2.4 (0 . . . 125A)	192	none	yes
`Supply 5V`	2	0 . . . 7.5	52.5	`mavg, dec`	flag
`HDS trig. supply`	4	0 . . . 20	52.5	`mavg, dec`	flag
`HDS trig. current`	2	0 . . . 7.5	52.5	`median, mavg, dec`	flag
`Loop monitor`	2	+/−78 V	52.5	`mavg, dec`	flag

HDS monitoring. The first data path group is denoted as discharge monitor in figure 8. It contains four channels of ADC working with a sampling rate 192 kHz (default value). This path monitors two HDSs by sampling the voltage (`HDS voltage`) of the capacitor and by sampling the current (`HDS current`) flowing through the quench heaters. The detailed recording of voltage and current during the discharge is essential to verify the proper functionality of the quench heater circuits.

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While a smooth dynamic resistance curve indicates normal heating effects of the quench heater, any discontinuities and spikes are indicators of damaged heater strips [10]. The analysis of the quench heater discharge is performed by software on the base of the PM file. The DQCSU acts therefore only as a data acquisition device. Experiments have shown that damaged heater strips tend to fail during the beginning of the discharge. Therefore, the buffer is recorded at four different data rates covering the beginning of the discharge with high time resolution while the end is recorded with lower speed. The total buffer length of 16384 points is divided into four blocks of 4096 points each recorded at the sampling rate shown in table 2.

Table 2. The four different blocks of the quench heater discharge buffer and respective data rates.

Buffer block	Time coverage [ms]	Sampling rate [kHz]
First	21.3	192
Second	42.6	96
Third	88.3	48
Fourth	170	24

Power supply supervision. Since the crate is powered by two redundant main power supplies, both signals need to be monitored to preserve redundancy. The signals of this group are denoted as UPS monitor in figure 8. The characteristics of the main 5 V monitoring channels are outlined in table 1 as channel denoted by `Supply 5V`. These voltages are compared to a threshold indicating the malfunction of the supply. The main supply voltages are transmitted in normal logging, but there is no PM buffer of the analogue values recorded. Instead, flags indicating the validity of the supply are saved in the PM buffer. This strategy was also chosen for the monitoring of the four HDS trigger voltages generated in the quench detection unit by four different DC-DC supplies (`HDS trig. supply`). All six input channels are connected to and digital signal processing pipeline comprising a moving average filter and a decimator. Following the pipeline, a comparator creates the respective power permission flags comparing the analogue reading to a threshold.

Monitoring of interlock loop and HDS trigger lines. The third signal group consists of an interlock loop and HDS triggering link monitors. It is denoted as a triggers monitor in figure 8. The interlock monitor samples voltages at the input and output of the interlock line in the quench detection units (`Loop monitor`). Since the interlock loop is shared by all 51 quench detection units of one LHC sector, the exact knowledge of the loop status at the input and output of each crate is essential for maintenance and interventions. The data sampled in these channels is processed the same way as the power supply monitors and compared against a threshold yielding an indicator flag. The last two channels monitor the current flowing through the trigger relay coil of the quench heater power supply (`HDS trig. current`). The voltage drop over a shunt resistor is monitored and allows precise diagnosis of the trigger link such as the number of quench heater supplies connected and the integrity of the cable connection. Since this signal is used to trigger the acquisition of PM data of the DQCSU, the DSP pipeline also contains a median filter to reject single-sample spikes induced by SEU. The median filter is followed by moving average and decimation filters.

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Trigger and timing controller. The precision of the absolute timestamp of the PM is essential for the analysis of quench events. Due to the fact that the quench detectors as well as the DQCSU are not time-aware, the crate controller has to translate the PM buffers from relative to absolute timing during the transmission of the data. To unload the microcontroller-based DQAMC from the time-critical function, the trigger and timing controller ensures the synchronous recording of the buffers by triggering the buffers of three devices at the same time. Furthermore, it measures the time interval with respect to the last known absolute time stamp stored in the DQAMC. A more detailed description of the timing synchronisation is given in the DQAMC section 3.3.

Remote power cycle option. Due to limited and difficult access to equipment in the tunnel during LHC operation, one of the important and very useful functions is the possibility to power cycle the whole local QDS system remotely. This feature is desired in the radiation environment in order to recover after a possible radiation-induced soft fault. Therefore the DQCSU contains a dedicated block to provide the support to remote power cycle the complete QDS and its network (field-bus) controller DQAMC.

3.3 Communications controller DQAMC

Equipment in the LHC tunnel communicates their data to the higher-level LHC controls software through a field-bus of WoldFIP™ type. The controller DQAMC was recuperated from the previous installation. The communication controller DQAMC consists of an 8-bit microcontroller and a specific WorldFIP™ interface chip. The microcontroller's SPI master interface communicates with the FPGAs on three other boards in the crate to gather data and to check or modify configuration parameters.

Timing and post-mortem transmission. The DQAMC controller sends a timing synchronisation pulse to the system controller DQCSU each time a WorldFIP™ interrupt has been received. This interrupt is linked to the global timing synchronisation of the LHC. This signal is denoted as Time Pulse and is visible in figure 8. The timing pulse is created during each field bus cycle, which is every 100 ms during normal operation. To achieve sub-millisecond timing synchronisation a counter is implemented inside the DQCSU which is stopped in case of a PM event. After reception of WorldFIP™ interrupt, the DQAMC resets this counter via a dedicated hardware line. In case of a PM trigger, this reset is disabled. Instead, the DQAMC reads the counter value and calculates the event time relative to its last received absolute timestamp. With this information, the PM data is transmitted using precise absolute time stamps although the quench detectors are not time-aware.

Due to the nature of the field bus as a shared medium and system limitations, the cycle time is limited to 100 ms hence the maximal data rate for one client is 960 bytes/s. Since the data structure during normal logging state and PM transmission does not change, one buffered sample is transmitted during each field bus cycle. Given the default length of the buffer of 149 790 points, the transmission would take more than 4 h. Therefore, the buffer is decimated during reading, which reduces the effective sample rate and hence the transmission speed by a factor of 16. Reading the decimated buffer with the length of 9 360 samples takes 15.6 min which is compatible with normal machine operation.

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3.4 Final VHDL code and its synthesis

The final codes for FPGA ProAsic3E for DQQDL and DQCSU have been synthesised using the tool Synplify® from Synopsys® and have been implemented using the designer tool available within Libero® SoC Design Suite (version 11.9 SP1) from Microchip®. The whole process from VHDL code to PDB (Programming DataBase) file was carried under control by a dedicated Powershell script. It was very convenient in order to maintain configuration throughout many repetitions of the implementation process during development. The finally achieved percentage of resource consumption within the device A3PE1500 is presented in table 3. Thanks to the reduction of the system clock frequency from the typical value of 40 MHz to the value of 25 MHz, one managed to fit the entire system with TMR into one FPGA. The challenge is especially visible in the case of system controller DQCSU with only a 4% margin of spare resources.

Table 3. The resource consumption for FPGA ProAsic3E A3PE1500.

FPGA Project	Resource consumption [%]
Quench detector DQQDL	78
System controller DQCSU	96

4 Verification and tests

To ensure the high dependability of the whole design, two independent verification methodologies were applied. The VHDL RTL (Register Transfer Level) source code was simulated both on the top level of both designs DQQDL and DQCSU, and on the level of individual design units across the design hierarchy. On the other hand, all hardware of the protection unit was tested using a dedicated automated test setup.

4.1 Verification of VHDL code

The presented projects were carefully verified by simulation. Simulation tasks were carried out using the simulator ModelSim® (Mentor Graphics®). Testbenches for the whole design were prepared according to figure 5 (without blue and green blocks) for DQQDL and to figure 8 for DQCSU. In both cases, the target of the verification was the complete RTL source code prepared for the purpose of synthesis and implementation in the FPGA. A behavioural VHDL unit was designed to model the functionality of the SPI slave interface inside the ADC in order to deliver input samples of measured voltages on magnets and other parts of the system. For flash and SRAM external to FPGA, validated models delivered by the manufacturers of these chips were used. On the other side of the processing chain, a behavioural model of the SPI master interface was necessary in order to mimic a receiver for logging data and PM data.

Below, two examples of simulated signal waveforms are presented. The first concerns quench detection by the DQQDL (figure 9). The second shows the generation of the precision quench time stamp by the DQCSU (figure 10).

Figure 9 presents the waveforms of the signals outside and inside the FPGA at the quench event. Digital 16-bits signals in an analogue format with vertical axis scales expressed in digital

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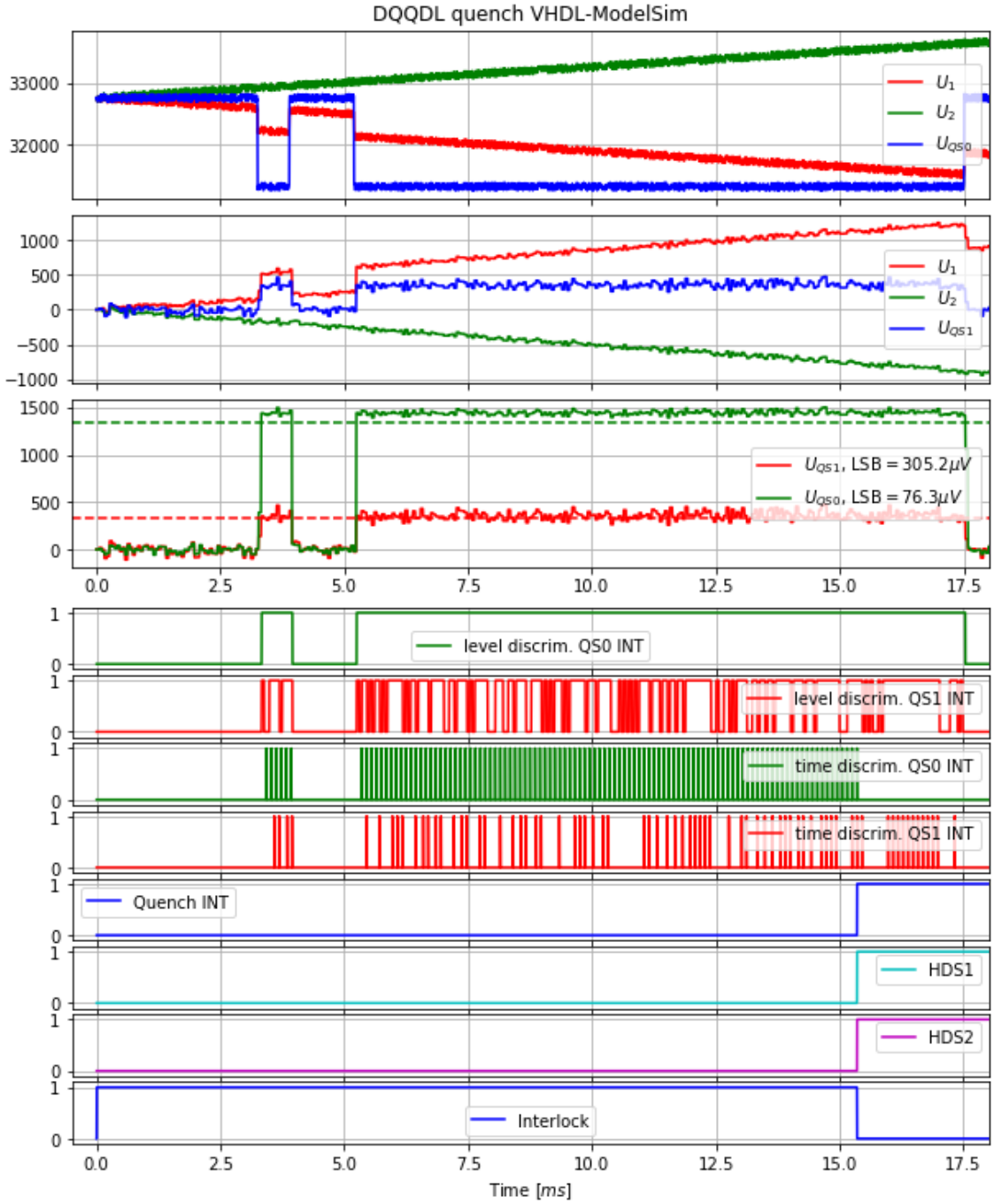

Figure 9. The simulated waveforms present the quench event in the internal aperture.

code values are shown in the upper three traces of the waveform plot. The next eight traces present 1-bit digital signals. In order to speed up the simulation, the start-up module was disabled for the simulation purpose only. In the DSP chain, the most time-consuming stages were also disabled, for example, the averaging filter.

The threshold values for level discriminators of QS0 and QS1 (analogue and digital measurement bridge) channels are adjustable independently and remotely. For the simulation, the same default values for thresholds were used. The threshold for QS0 and QS1 channels is 102.5 mV. However, in the third trace, there are two different dashed lines representing the threshold. Due to different LSB resolutions, this common threshold presented as a digital code splits into two different values. The threshold for QS0 (green) is four times bigger than for QS1 (red).

The default value of discrimination time is set to 1 ms and also can be remotely adjusted independently for the two channels.

The waveform at the top of figure 9 presents the input signals delivered by the ADCs. The voltage U_1 (red) ramps up and the voltage and U_2 (green) ramps down. The blue line represents the imbalance of the measurement bridge (figure 2). White noise was added to the signals, with an amplitude of 10 mV. In one of two coils (voltage U_1), an asymmetric excess voltage of 110 mV is added two times. First for a short period and then for a longer time. These signals were generated outside the simulator and were delivered to the input of the unit under test using a special behavioural module that mimics the SPI interface inside ADC.

The second trace shows the signals U_1 and U_2 after transformation by the DSP chain but the signal in the middle (blue) here is generated numerically by summation $U_{QS1} = U_1 + U_2$ (figure 7). Due to different gains in analogue front-end channels (figure 2), the digital values representing U_{QS1} are four times lower than for U_{QS0}. This is visible in the third trace of the waveforms.

The next two traces (fourth and fifth) show the outputs of the level discriminators. The discriminator for the QS0 channel was activated two times but the discriminator for the QS1 channel was activated many times. Many narrow pulses appear due to noise in the signal because, in this simulation, the filtering is disabled. The first pulse in the QS0 channel is too narrow to be validated by the time discriminator, but the wide pulse is longer than 1 ms discrimination time. The sixth and seventh traces show the activity of counting down in the counters inside the time discriminators. When the validation time elapsed, the counter in the QS0 channel reaches zero and the trigger signal is generated. This is shown in the remaining waveform traces in figure 9.

Figure 10 presents the waveforms concerning the functionality of the timing controller (figure 8). The most upper trace presents the content of a 32-bit counter in the analogue format with a vertical axis scale expressed in digital code values. The counter which is longer than the necessary number of bits ($\log_2(100\,\text{ms} \times 24\,\text{MHz}) < 22$) is useful for the case the Time Pulse arrives later than expected. In the worst case, when even 32-bits are not enough, a timeout flag is generated. The next three traces show 1-bit digital signals. A Time Pulse is generated by DQAMC every 100 ms as was already discussed in subsection 3.3. In the first digital trace, two pulses are visible. Between two consecutive pulses, the Time Counter counts up system clock pulses from the initial value zero and reaches a maximal value equal to 100 ms/41.666 ns = 2 400 039. The rising edge of the Quench INT signal is delivered from DQQDL boards. When a quench happens the counting-up is stopped and the current value is preserved in the register. During the PM acquisition, the value is transmitted in order to use it as a quench time-stamp with precision on the level of 100 ns and as

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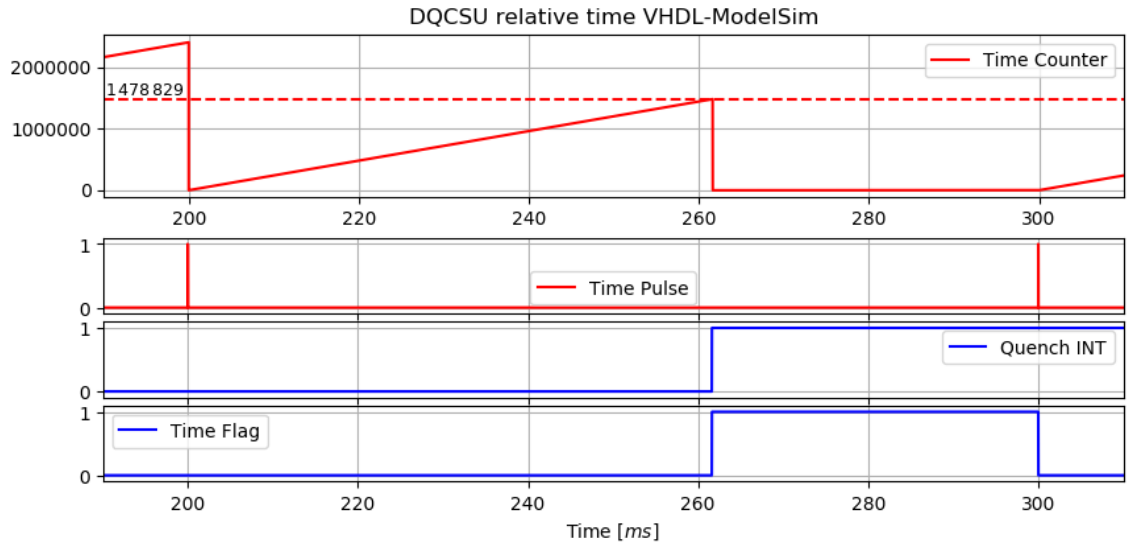

Figure 10. The generation of timestamp analysed by waveforms simulated.

an initial reference time for all samples in the post-mortem data set. The time-stamp of the Time Pulse is known to the network controller DQAMC. To improve the precision of time measurement, additionally, the value caught in the Time Counter must be transmitted. In the case presented in figure 10, this value is $1\,478\,829 \times 41\,667$ ps = 61 534 658.940 ns. This value is transmitted out to the DQAMC controller as four consecutive bytes during a standard read transaction of a 64-byte data and configuration block (logging). Up to the next Time Pulse, the counter holds zero, and the bit Time Flag remains activated.

4.2 Testing of radiation tolerance of the device

Since the local protection unit is installed below the LHC main dipole magnets, it is subject to radiation created by the accelerator operation. The location below the dipoles leads to a maximum dose rate of 10 Gy yr^{-1}. Hence the detector has been designed to withstand a dose of 200 Gy and to be immune to SEU. All electronic components susceptible to radiation have been tested either by the author's group or had been tested previously by other CERN groups. We chose a flash-based FPGA which stores its configuration in non-volatile memory cells which are immune to SEU. However, the registers and memories of the design are still susceptible to radiation. Design techniques such as TMR and triplication of memories have been used to increase the radiation tolerance of the design. To verify the system's tolerance to radiation, dedicated tests in the CHARM (CERN High energy AcceleRator Mixed field facility) facility at CERN have been performed. This facility, driven by the 24 GeV beam from PS (Proton Synchrotron) accelerator has been designed to create a radiation spectrum similar to that existing in the LHC tunnel during accelerator operation. The energy deposited by this radiation into the tested device is monitored and measured as an absorbed dose D in units Gy.

The radiation test for the entire device was carried out in CHARM [11] at position 10 in two campaigns, each consisting of two runs. In the following, a brief summary is presented. The behaviour of different detector functionalities was monitored for several days when the fully

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operational device was placed in the area where the mean dose rate was established at the level of 50 Gy/d. Each run lasted around 6 days. The time schedule and the doses are summarised in table 4. After the first campaign, several enhancements were introduced to the monitoring and measurement hardware and software. Between runs within the campaign, some interventions were carried out to restore the correct operation before continuing the irradiation. To verify the proper functionality of the detector, a very low-frequency sinusoidal wave was applied as a stimulus. Quench events were simulated by increasing the amplitude of the stimulus momentarily. The hardware interlocks of the detectors were also monitored. The acquired data from the detectors were transmitted via a field bus connection.

Table 4. The time schedule and the absorbed doses.

		Time [h]	Initial dose [Gy]	Final dose [Gy]	Dose rate [Gy d^{-1}]
Campaign 1	Run 1	115	0.0	218.0	44
	Run 2	133	218.0	450.0	44
Campaign 2	Run 3	116	0.0	156.5	32
	Run 4	118	156.5	353.7	40

4.2.1 Results

During each run, the continuous data acquisition via the field bus stopped after a dose of about 100 Gy. This was expected due to the known vulnerability of the WorldFIP ASIC (Application Specific Integrated Circuit) to radiation. Beyond that point, the function of the detectors was tested by simulating quench events via the input stimuli and subsequent verification of the loop opening and heater trigger line activation. The communication controller was changed after each run. We investigated the analogue signal integrity and found that a signal gain variation of less than 0.65% was observed for the duration of the whole test. The variation was less than 0.2% up to 100 Gy. The offset variation remained at a low of 10 mV for up to a dose of 100 Gy. Beyond 200 Gy, offset increased up to $\approx$ 0.5 mV/Gy. As a result, it was found that the DQCSU was functional up to an accumulated dose of 240 Gy 241 Gy. Both DQQDLs were functional up to 330 Gy in the first run. In the third run, one DQQDL failed at a dose of 140 Gy and in run 4 one DQQLD failed at a very low dose of 30 Gy. Investigations after the test traced this down to one digital isolator in run 3 and one operational amplifier in run 4. Since both components are used on both DQQDL and DQCSU and had been successfully tested in a separate campaign at PSI, we concluded that the failure of the two components was probably caused by damage during the manual assembly of the circuit boards. As mentioned in the previous chapters, the FPGA firmware was optimized to withstand SEU. During the test no SEU was detected inside the FPGA, hence the mitigation measures in the firmware are considered to be effective.

4.3 Production test procedure

In order to equip all LHC sectors with new local protection crates, 450 units had been produced. To test the produced circuit boards as well as the completed crate, three stages of tests had been performed. In the first stage, each circuit board was tested using a JTAG (Joint Test Action Group)

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compliant tester. After assembly of the chassis, the DQQDL and DQCSU board are programmed and the quench detection unit is tested. In this tester, the crate controller DQAMC is replaced by a USB to SPI interface of type NI USB 8451. This allows communication with the quench detectors and the crate controller in a much faster way than the crate controller thus reducing the test time by several orders of magnitude. Analogue and digital signals used as stimuli are generated by a NI PXI crate which also measures the interlock connections as a reaction of the system to the stimuli. The third tester verifies the functionality of the quench detection unit integrated into a local protection crate. This testbench also generates analogue and digital signals via a NI USB 6353 multi-function DAQ (Data AcQuisition) module. Different to the previous tester stages the quench detection unit is equipped with a DQAMC field bus coupler and thus communicates with the tester via WorldFIP™ and a standard LHC type gateway. This tester also tests the discharge of the two quench heater power supplies of the local protection crate into dummy resistors. The PM files of both quench detectors and crate controller are analysed by this tester.

Finally, the required 392 pieces for the tunnel plus spare pieces of the local protection crate were tested. Validated devices were installed in the tunnel and commissioned. During commissioning only one crate failed and was substituted with a different piece which underlines the effectiveness of the test strategy.

5 Complete view of the local detection system

Figure 11 shows the assembled crate of the new quench detection unit for the main quadrupoles. Four modules are inserted to create. Beginning from the left side, they are, respectively: two quench detectors DQQDL, one system controller DQCSU, and one communication controller DQAMC. To facilitate maintenance, the circuit boards are packaged in metal cassettes, which protect the electronics during transport and handling. The handles on the top and bottom of each cassette allow the toolless exchange of the modules. The indicator lights present on the front panel with respective explanations show the actual state of the unit, which further facilitates in-situ interventions.

6 Conclusion

The designs shown in this paper have been developed over several years. Immunity to soft errors was the main issue addressed during design and verification. The choice of technology, design methods, design rules, and architecture was made to achieve several goals: an increase in system dependability, enhancement of its diagnostic capabilities, enhanced maintainability, and increased flexibility in modification of the device settings.

In total, 392 pieces of the local protection unit were installed in the LHC tunnel. Hardware commissioning took place in the years 2021 and 2022. Since the main circuits of the LHC magnet system were trained to a new current equivalent of 6.8 TeV, many training quenches were observed. Table 5 lists the quench events on main quadrupole circuits that occurred during hardware commissioning.

In all the cases listed above, the function and data flow of the upgraded quench protection system for the main quadrupoles were correct and fully agreed with the specifications.

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Figure 11. The photo of a quench detection unit installed in the test facility.

Table 5. The summary of quadrupole quenches detected during hardware commissioning.

Number of quenches	Source of quench
63	Total quadrupole quenches during hardware commissioning
51	Training quenches
9	Test mode provoked quenches
3	Provoked by miscellaneous events

The physics run began in 2022 and 15 quench events took place during operation up to the end of September 2022. These were secondary quench events as a result of gaseous helium propagation from dipole magnet quenches through the cryogenic system. Again, the system properly detected all quenches and worked fully within specification. Furthermore, the system did not show any sensitivity to radiation from the accelerator operation. To conclude, the device described in this publication is operating smoothly and detected all quenches reliably, operated within specifications, and no faults were detected so far.

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Acronyms

ADC Analogue Digital Converter. 1, 7, 9–11, 14, 16

ASIC Application Specific Integrated Circuit. 18

ASP Analogue Signal Processing. 7

CERN European Organisation for Nuclear Research. 1, 17

CHARM CERN High energy AcceleRator Mixed field facility. 17

CMOS Complementary Metal-Oxide-Semiconductor. 1

CT Current Transformer. 4

DAQ Data AcQuisition. 19

DSP Digital Signal Processing. 7, 9, 10, 12, 16

FPGA Field Programmable Gate Array. 1, 6–8, 10, 11, 13, 14, 17, 18

HDS Heater Discharge Supply. 4, 9, 11, 12

JTAG Joint Test Action Group. 18

KVL Kirchhoff's Voltage Law. 3

LHC Large Hadron Collider. 1–6, 12, 13, 17–19

LS1 Long Shutdown One. 1

LS2 Long Shutdown Two. 1

LSB Least Significant Bit. 3, 7, 16

MB Main Bending. 2

MQ Main Quadrupole. 2–4, 7, 9

OVP OverVoltage Protection. 7

PCB Printed Circuit Board. 7

PDB Programming DataBase. 14

PM Post Mortem. 10–14, 16, 19

PS Proton Synchrotron. 17

QDS Quench Detection System. 1, 8, 10, 13

QPS Quench Protection System. 1

RTL Register Transfer Level. 14

SAR Successive Approximation Register. 7

SEE Single Event Effect. 1, 6

SEU Single Event Upset. 9, 12, 17, 18

SPI Serial Peripheral Interface. 7, 9, 13, 14, 16, 19

SRAM Static Random Access Memory. 7, 10, 14

TMR Triple Module Redundancy. 6, 14, 17

VHDL Very High Speed Integrated Circuit Hardware Description Language. 1, 6, 8, 9, 14

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