International Conference on Technology and Instrumentation in Particle Physics IOP Publishing
Journal of Physics: Conference Series **2374** (2022) 012129 doi:10.1088/1742-6596/2374/1/012129

Development of a hybrid single-photon imaging detector with embedded CMOS pixelated anode

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Abstract. The development of a single-photon detector based on a vacuum tube, transmission photocathode, microchannel plate and CMOS pixelated read-out anode is presented. This imager will be capable of detecting up to 1 billion photons per second over an area of 7 cm^2, with simultaneous measurement of position and time with resolutions of about 5 microns and few tens of picosecond, respectively. The detector has embedded pulse-processing electronics with data-driven architecture, based on the Timepix4 ASIC, producing up to 160 Gb/s data that will be handled by a high-throughput FPGA-based external electronics and data acquisition system. These performances will enable significant advances in particle physics, life sciences, quantum optics or other emerging fields where the detection of single photons with excellent timing and position resolutions are simultaneously required.

1. Introduction

This paper presents the design of an imager capable of detecting single-photons over a large surface (7 cm^2), with combined excellent position (5μm) and timing (few tens of picosecond) resolutions, high detection efficiency, high instantaneous rates (>1 Ghit/s), low dark count rate (10^2 Hz/cm^2) and with few hundred thousand front-end electronics channels working independently from each other.

2. Detector description

The working principle of the device is schematically shown in Fig. 1. A photon hitting the photocathode, deposited in the inner part of a transparent input window, ejects a photoelectron into a drift electric field, which transports the electron onto the microchannel plate (MCP). The MCP is a secondary electron multiplier which consists of an array of millions of thin parallel channels, each working as an independent electron multiplier, and electrodes on both surfaces for biasing [1]. The channel walls have a high secondary electron emission coefficient and thus, when photoelectrons enter the pores of a biased MCP, they are accelerated and hit the walls releasing secondary electrons. This causes an avalanche effect resulting in a cloud of electrons exiting from the rear surface. Finally, the released electron cloud is carried by another drift field onto the pixelated anode where it is sensed as a charge pulse by a pixelated anode, based on the Timepix4 application-specific integrated circuit (ASIC) developed in 65 nm CMOS technology [2].

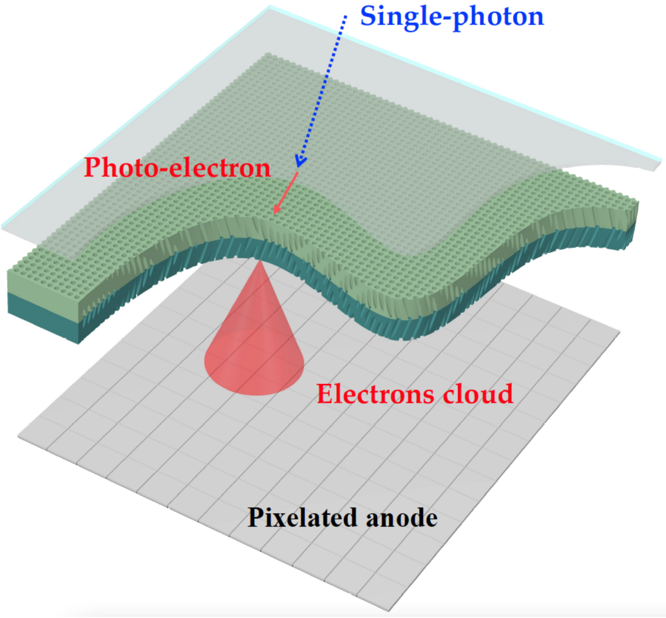

Figure 1. Detector schematic drawing.

The use of MCPs in combination with a photocathode embedded in a vacuum tube offers unique features for the detection of photons [3].

The vacuum tube section view is shown in Fig. 2: an input window with a drop-through is used to achieve a close gap between the photocathode and MCP. This proximity focusing allows better spatial resolution and magnetic field immunity.

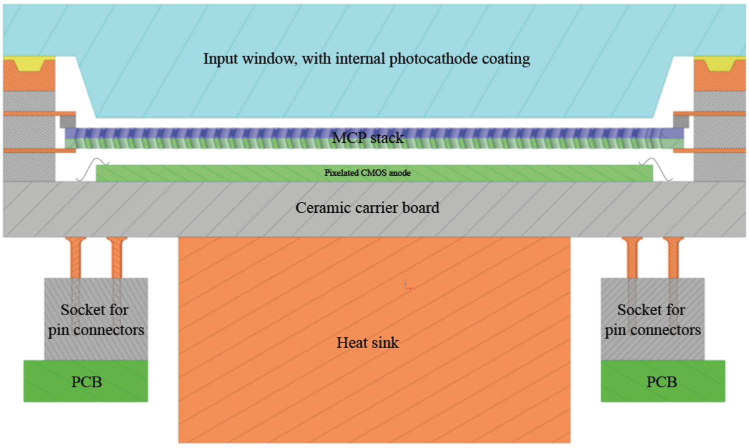

Figure 2. Section view of the detector, connected to the carrier PCB and heat sink.

Bialkali and multialkali are being considered for baseline photocathode material, which show large peak quantum efficiency in the blue region, low dark count rate ($\sim 10^2$ Hz/cm^2) and represent the best choice for timing performance.

A MCP with a Chevron configuration allows to easily reach the desired gain of $\sim 10^4$ and to reduce ion feedback. Coating the MCP pores with an atomic layer deposition (ALD) will also allow to operate these devices at very large integrated charge densities, exceeding 22 C/cm^2, which represents a lifetime increase by almost two orders of magnitude compared to a few years ago [4].

The detector anode is represented by the bare Timepix4 ASIC: the electron cloud signal amplified by the MCP will be sensed by the bump-bonding pads in each individual pixel. A single Timepix4 chip will be mounted on a ceramic carrier using die-attach and wire bonding connections. The use of a bare ASIC inside a vacuum tube has been already demonstrated [5, 6] and proved this approach to be solid. Vacuum and thermal compatibility of the materials used for assembly will be carefully verified. Getter strips are planned to be used inside the tube to improve vacuum quality.

The multilayer ceramic board provides vacuum feedthrough connections for the read-out chip input/output signals. The baseline interconnection solution is a Pin Grid Array (PGA) connection of the input/output signals on the back side, arranged around the perimeter to fit into a suitable socket on the "support" printed circuit board (PCB).

Simulations are being performed with Ansys HFSS to verify the integrity of some critical signals (for data transmission at 10 Gbps), in particular taking into account the wire-bonding connections, the signal routing though the ceramic PCB and the PGA connection.

When in operation, the Timepix4 ASIC will have a power dissipation of about 5 Watts inside the vacuum tube, which could raise the temperature enough to compromise operational stability and even the reliability of the tube vacuum sealing. Active cooling will be required to extract the heat generated by the ASIC out of the tube, and could be efficiently implemented by connecting a cooling system to the back of the heat sink.

3. Electronics and data acquisition

The Timepix4 ASIC has been developed by the Medipix4 Collaboration for use with hybrid pixel detectors in a wide range of applications and consists of an array of 512×448 pixels (0.23 M total pixels) with dimensions 55 μm × 55 μm for a total active area of 7 cm^2.

A simplified circuit schematics for a single pixel is shown in Fig. 3. The signal from the MCP is amplified and discriminated. The signal arrival time is time-stamped with a 195 ps LSB time-to-digital converter (TDC), corresponding to 56 ps r.m.s. resolution, and simultaneously the signal Time-over-Threshold (ToT) is measured with ∼1 ns resolution. The ToT information is crucial for reaching the desired timing and position resolutions, as it allows to correct for the time-walk effect and to apply a centroid algorithm, respectively. An optimised architecture has been designed for sparse read-out, where only pixels containing event information are read out, that can achieve a throughput of up 2.5 Ghits/s.

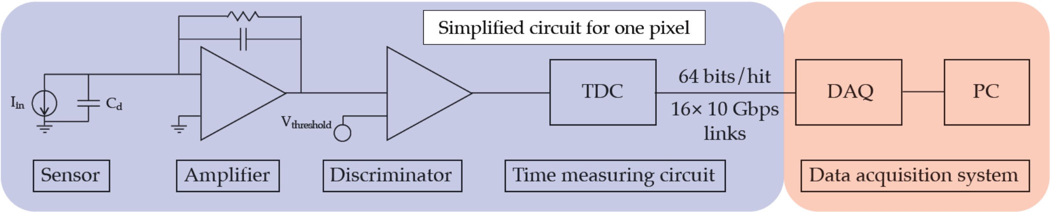

Figure 3. Simplified circuit schematics of the Timepix4 ASIC.

The ASIC features also a very low equivalent noise charge of about 70 electrons for a single pixel, which allows to set a conservative detection threshold of 500-700 e$^-$. With a typical signal of a few 10^4 electrons spread over a small number of pixels, the device will be fully efficient to the incoming electron cloud from the MCP and free of electronics noise. The only source of noise comes from the dark counts due to the photocathode ($\sim 10^2$ Hz/cm^2 for bialkali), which can be further reduced by cooling if needed. Dark count rate due to the MCP is negligible (<1 Hz/cm^2).

The architecture of the Timepix4 ASIC is data driven: only when a pixel is hit the data is transferred out of the tube, via 16 differential links configurable up to 5.12 Gbps. The maximum pixel hit rate allowed by the ASIC is about 2.5 Ghits/s: since each pixel produces 64 bits when hit, the maximum rate of data produced by the ASIC and sent to the external read-out electronics can be as high as 160 Gbps. This data rate can be tuned by controlling the flux of photons hitting the detector.

A support PCB equipped with a suitable socket for the insertion of the tube pins will be used. In order to increase the flexibility of the design, this PCB will have electro-optical transceivers which will link the ASIC to an FPGA-based (Field Programmable Gate Array) board for the exchange of configuration data and the collection of event data. The fiber optic links foreseen by this design will allow to remotely control and operate the "on-detector" electronics from an "off-detector" part of the read-out system which could be placed in accessible facilities, far from confined spaces or radiation environments in which the detector might be located for some applications.

The "off-detector" electronic cards will be based on state-of-the-art FPGAs. A carrier mezzanine board holding the detector socket will be connected to the main DAQ card through FPGA Mezzanine card (FMC) connectors. This connection will be used for the transmission of the ASIC power, slow control data and the 16 high-speed serial outputs. The use of FMC-to-FMC kapton cables will allow us to obtain systems with different geometries. Issues connected to signal attenuation due to the cable can be mitigated by placing repeaters on the critical signals. Similarly, power glitches will be avoided by placing step-down DC-DC converters on the carrier mezzanine.

On the main DAQ card FPGAs are used for detector configuration and monitoring. A Gigabit Ethernet connection will allow to receive commands from a remote server and to stream monitoring data. The 66b/64b encoded output data will be received at the full bandwidth of 16×10.24 Gbps and transmitted to a remote server using commercial optical transceivers. This card will also have the capability of receiving external signals used for multi-card synchronization. The last requirement is mandatory for the construction of large area systems based on multiple photodetectors.

For the practical applications of the detector we have foreseen two kinds of photon rate scenarios which have an impact on the required read-out architecture and DAQ resources: a high rate scenario, in which the photon rate will go up to the maximum possible rate of 2.5 Ghits/s, and a medium-low rate scenario, in which the photon rate will be lower than the maximum by a couple of orders of magnitude. In the high rate scenario the peak data transfer rate can reach 160 Gbps; the raw data will be sent directly to a PC for storage using a dedicated PCIe receiver card implementing either a custom protocol or 100GbE for optical data decoding. In the medium-low rate scenario, the FPGAs will also be able to perform data pre-processing (e.g. time ordering, clustering, correction algorithms, etc.) on the input data which will allow to reduce even more the data bandwidth to the PC and to provide the end-user with refined information (e.g. pixel cluster information, etc.) at the "online" level.

4. Conclusions

A detector for visible single photons, based on a bare Timepix4 CMOS ASIC embedded in a vacuum tube with a MCP is under development for the detection of very high photon rates with simultaneous measurement of time and position. The optimised geometry and the use of a pixelated anode developed in 65 nm CMOS technology will allow to fully exploit the excellent timing and position resolution performance of a MCP.

The performance of the presented single-photon imaging technology go much beyond the state-of-the-art and will open new research paths in different fields of science like high-energy physics, life sciences and other emerging fields [7] .

Acknowledgments

This project has received funding from the European Research Council (ERC) under the European Union's Horizon 2020 research and innovation programme (Grant agreement No. 819627).

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