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The serial and LVDS signal repeaters for the ATLAS New Small Wheel sTGC trigger

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The ATLAS New Small Wheel uses highly routable twin-ax ribbon cables for board-to-board connections on the wheel. Due to signal attenuation and dispersion, serial and LVDS repeaters were necessary to be placed along the connections from the NSW sTGC Pad Front-end boards to the Pad Trigger, from the Pad Trigger to the strips Front-end boards and from there to the Router boards. In this note we provide the justification for using the Repeater boards, the design and the performance of the pre-production boards for the 4.8 Gb/s Serial and the 640 Mb/s LVDS Repeaters during their tests at the NSW Vertical Slice Lab and the on-wedge tests. The commissioning and integration of the Repeater boards is given in Section 5.

Contents

1 Introduction

The NSW [1] ATLAS sub-detector readout and trigger system is composed of electronic units residing on the detector (Front-End, data aggregator and trigger boards) and the off-detector electronics, which include the NSW Trigger Processor and the readout units. The schematic of the NSW electronics and data flow is shown in Figure 1 with the sTGC related part on the top of the graph. The Front-end cards (pFEB and sFEB [2]) have interconnections to the Pad Trigger and Router [3] that are housed in the Rim-crate at a distance up to 6.25 m. The Rim-crates are located on the outer edge of the Wheels.

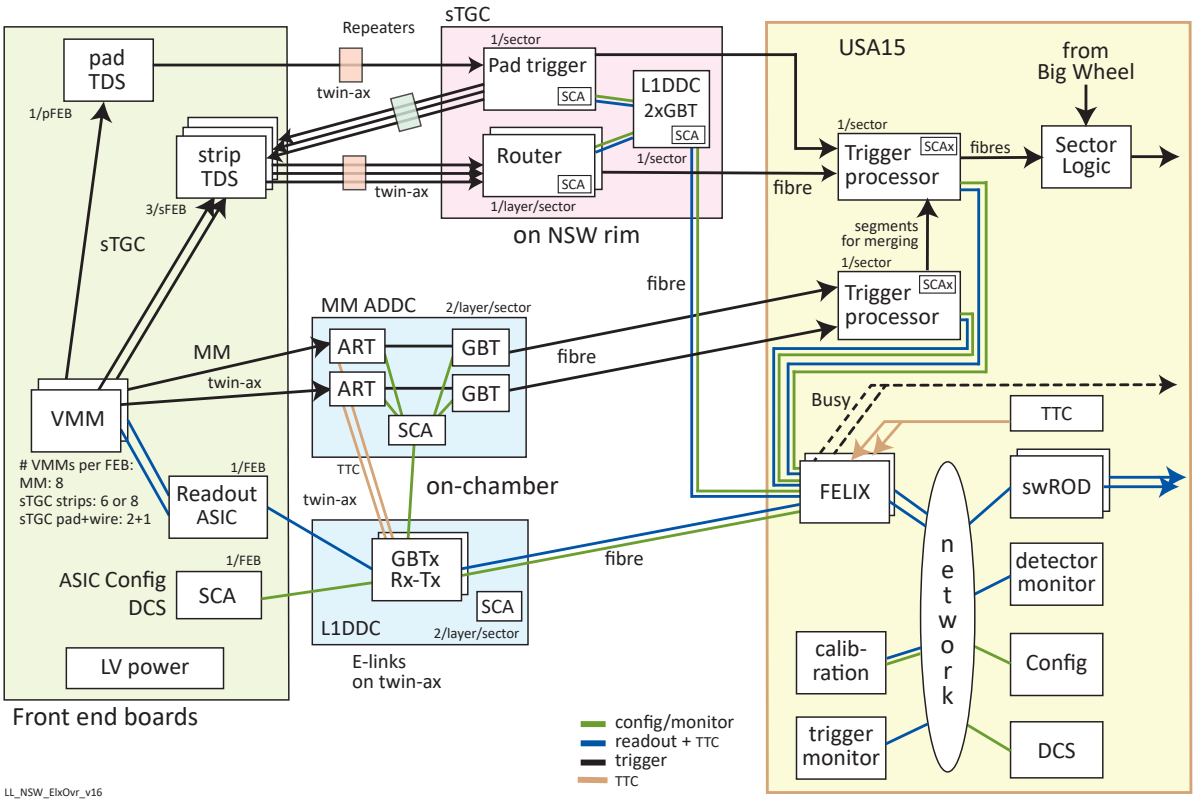

Figure 1: NSW electronics and data flow schematic. The Repeaters are shown as three boxes on the sTGC twin-ax connections.

The connections between the pFEB, the sFEB and the Pad Trigger and Router are done using the 3M SL8800 Series MiniSAS cables (four twin-ax pairs in a ribbon, two ribbons per connector) [4, 5]. The cross-section of each ribbon is shown in Figure 2. The Pad-TDS [6] to Pad Trigger and the strip-TDS to Router links operate at a speed of 4.8 Gb/s; the Pad Trigger to strip-TDS at 640 Mb/s, based on LVDS signals. The MiniSAS twin-ax ribbon cable attenuation at 10 GHz is 4.9 dB/m for the silver-plated cable (Ag on 30 AWG Cu). Table 1 shows the attenuation of the tin-plated and the silver-plated cables for frequencies 0.5 to 20 GHz.

Silver-plated twin-ax cables were finally preferred because they have reduced attenuation at higher frequencies and lower prices. A large number of tin-plated cables were already in stock and they are used in the connection from Pad Trigger to sFEB (640 Mb/s). As is shown later in this report, the long distance between the Front-end cards to the Rim crate requires the use of repeaters to guarantee low error rate operation.

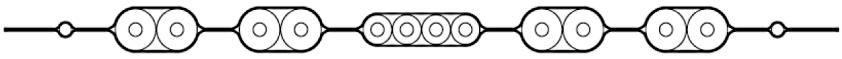

Figure 2: Cross-section of the MiniSAS twin-ax ribbon cable showing four pairs, four single-ended "side-band"conductors, the shield and two shielding drains. The cable dimensions are 15.6×0.9 mm.

Table 1: Twin-ax cables attenuation for tin and silver-plated twin-ax cables.

Frequency (GHz)	**0.5**	**1.0**	**2.0**	**5.0**	**10.0**	**15.0**	**20.0**
Tin-plating (dB/m)	-0.90	-1.4	-2.2	-4.0	-7.5	-10.9	-14.6
Silver-plating (dB/m)	-0.85	-1.2	-1.7	-3.2	-4.9	-6.8	-8.8

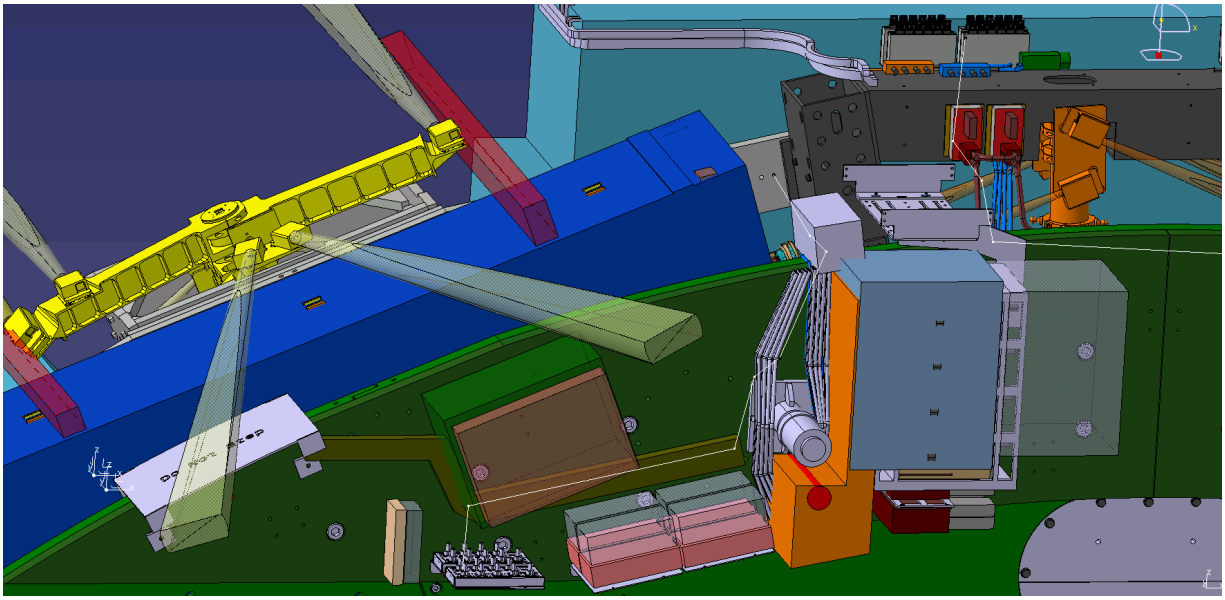

Figure 3: The Rim-crate location in the outer part of the wheel (Light blue box in the right side).

2 Serial Repeater boards SRL1R – pFEB to Pad Trigger and sFEB to Router

Serial repeaters single MiniSAS connectors boards (SRL1R) are used for the 4.8 Gb/s connections pFEB to Pad Trigger and sFEB to Router. The design is based on the Low power quad-channel repeater chip of Texas Instruments, DS100BR410, with 10.3125 Gb/s equalizer and de-emphasis driver [7]. The repeater input and output signals are AC-coupled. The TDS ASIC on the sFEB and pFEB has a driver with a $\pm$ 500 mV swing. The Router and Pad Trigger FPGA inputs are conditioned with the same DS100BR410 receiver chip. A 3D drawing of the Serial Repeater is shown in Figure 4: two MiniSAS connectors with the cables plugged on either side, two Nano-Fit [8] power supply connectors and the configuration jumper connector in the middle. The configuration jumpers provide the possibility to select among eight different discrete equalizer boost values from 2.7 to 28.9 dB. The Nano-Fit (Molex) is a 2-pin connector available only in a through-hole version. Shorts to the copper shield are prevented by cutting the pins short and soldering them in the holes. The connector's two plastic pins that insert into the PCB prevent straining the soldered pins. Placing power connectors on both ends of the board allows routing the 2.5 V power

cable from the L1DDC boards [9] without bending, irrespective of their relative position. It also enables connecting a second repeater in parallel. The repeater chips are placed on the backside of the PCB to allow contact with the copper pad of the shielding for passive cooling.

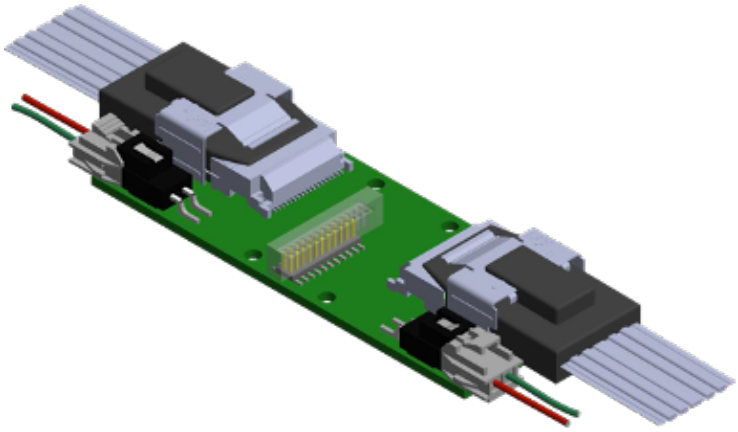

Figure 4: 3D rendering of the SRL1R Repeater card

Power: The L1DDC board supplies 2.5 V via a shielded twisted pair. The shielding of the power cable is connected to the cage of the L1DDC. According to the repeater chip data sheet [7], its typical power consumption for four channels is 220 mW. The SRL1R board consumption for the three used channels is estimated to be 213 mW.

Shielding and grounding: SRL1R is enclosed in a shielding cage, which provides continuity of the input and output cable shields. Cable shield, cable drain and side-bands are connected together and to the enclosing shielding box. The Shield of the power cable is connected to the cage of L1DDC and it is not connected at the Repeater side. The shielding cage is a copper box consisting of two parts as shown in Figures 5 and 6. A thermal pad is placed between the repeater chip and the copper box lower surface. The rest of the surface is isolated with a Kapton foil.

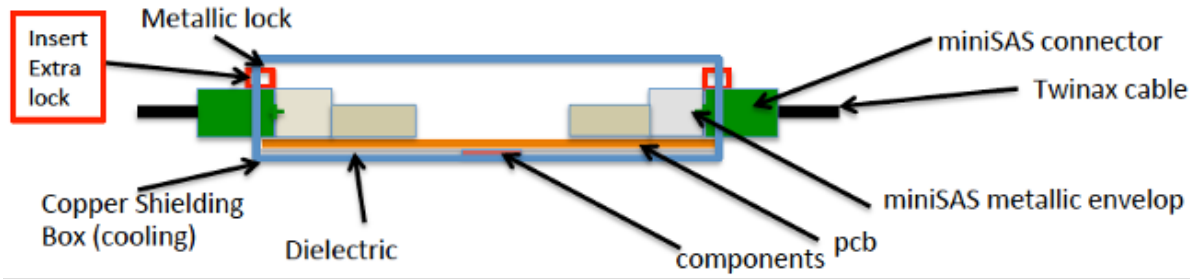

Figure 5: Schematic of the shielding box

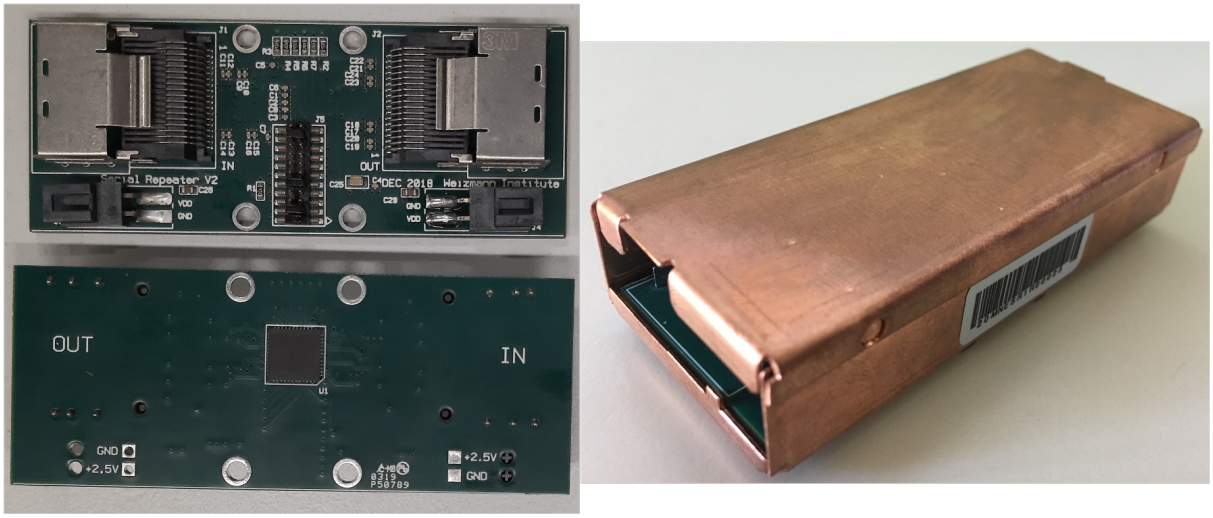

Figure 6: Photos of the final SRL1R card (left) and the copper shielding box (right)

2.1 Location and cables

A MiniSAS to 4 × SATA Breakout cable connects four pFEBs via the SATA connector, thus three SRL1R are needed per wedge for the Large sectors (see Figure 7) and only two per wedge for the Small sectors because the outer pFEBs are close enough to the Rim-crate.

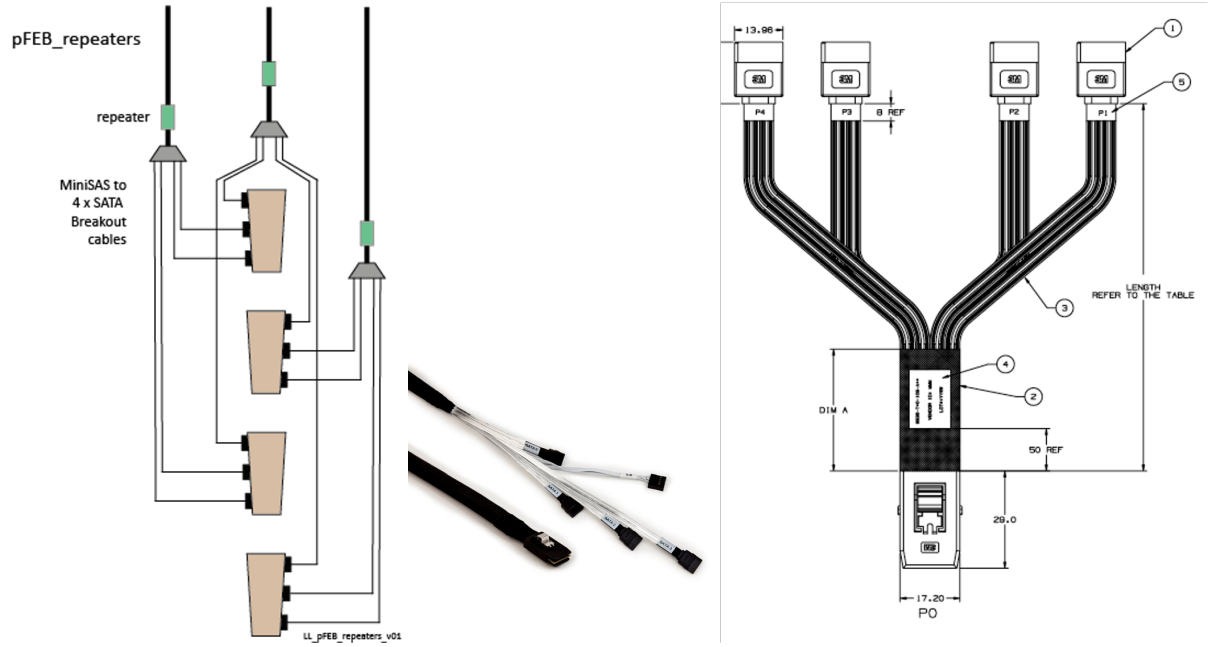

Figure 7: pFEB connection via MiniSAS to 4 × SATA Breakout cable to a SRL1R and subsequently to the Pad Trigger (left) and photo (middle) and schematic of the cable (right).

Every sFEB connects via a twin-ax cable to a SRL1R and subsequently via another twin-ax to the Router in the Rim-crate. Every wedge requires 15 SRL1Rs for the Large Sector while for the Small Sectors only 12 per wedge. Figure 8 shows the location of the serial repeaters on the wedges.

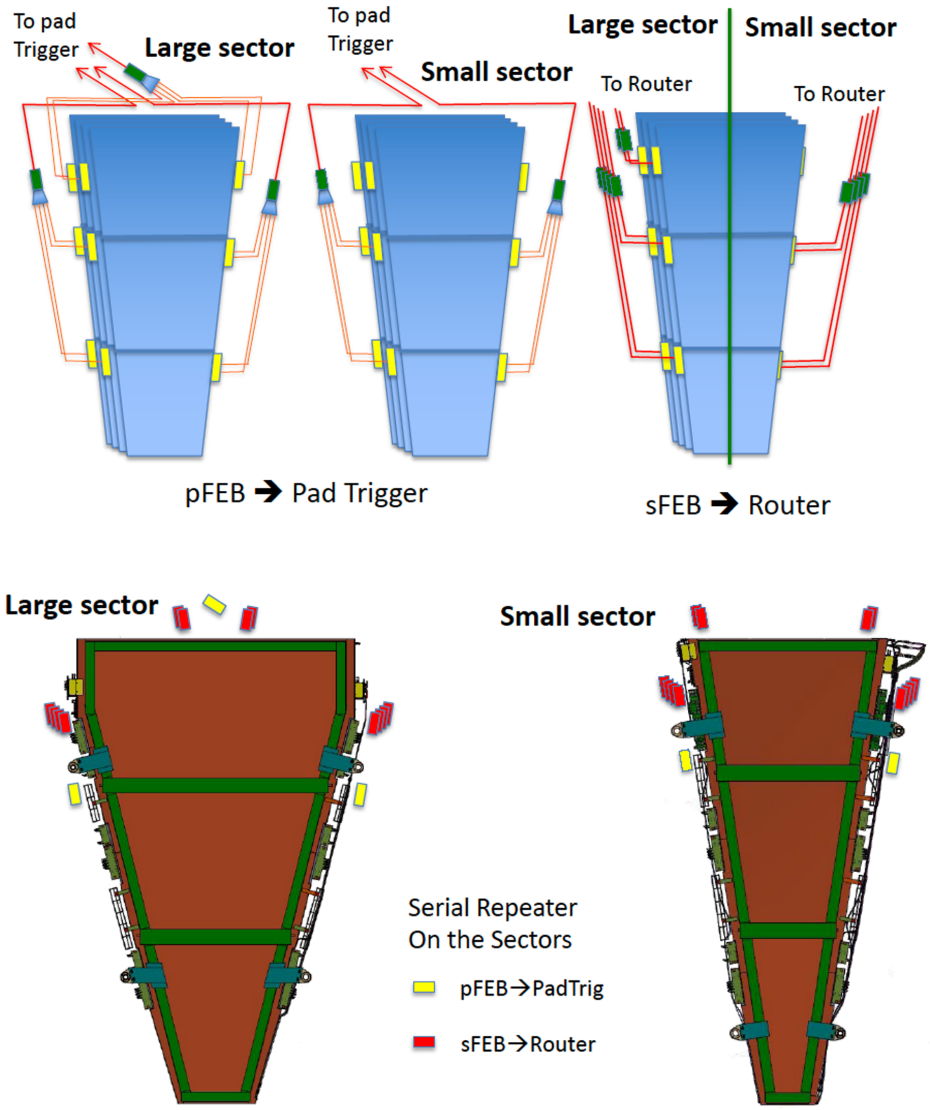

Figure 8: Location of the SRL1Rs for the pFEB and the sFEB links, on the Large and the Small sectors.

Most of the 768 SRL1R's are located near the L1DDC at the edges of the wedge. A small number of SRL1R's may be powered by the LVD6R Repeater modules sitting on top of the spokes behind the Large Sectors.

Serial Repeaters heat dissipation per sector: The power consumption of the serial repeaters on the Large sectors is estimated to be 3.2 W (15 x 213 mW/Repeater), while for the Small sectors the consumption is estimated to be 2.6 W (12 x 213 mW/Repeater).

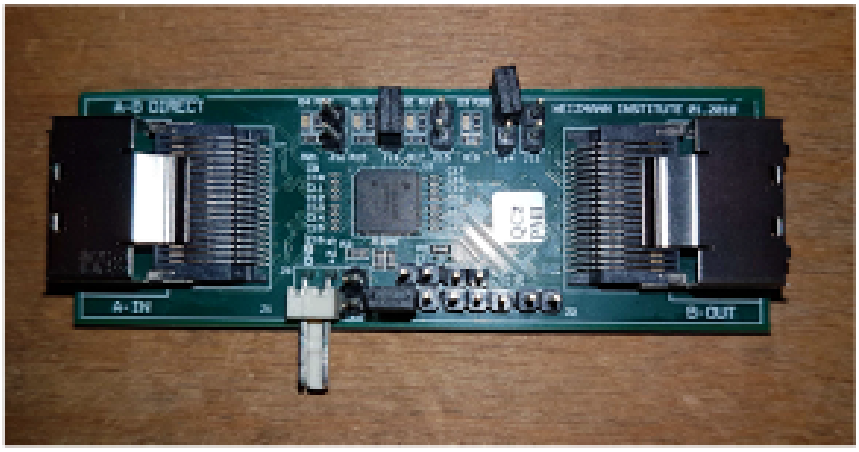

Figure 9: Photo of the first version of the serial Repeater SRL1R-V0

2.2 SRL1R-V0 production and tests

A first production of SRL1R-V0 confirmed the necessity of their use. A photo of this type is shown in Figure 9. The difference between the SRL1R-V1 as described in the previous sections are: 1) All components are on the upper PCB side, 2) There is one 2-pin power connector vertical to the repeater, 3) There is no provision for a shielding cage.

The SRL1R-V0 were tested in test benches at the University of Michigan and also at the NSW Vertical Slice Lab (VS). Extensive tests were performed using different twin-ax cables (tin-plated and silver-plated of various lengths and different lots); eye-diagrams in various configurations were taken using a dedicated clock and IBERT tests were done to certify their low error rate. The tests showed a variation of the performance for different lots (transmission errors for one lot, but not for a second one) and also were sensitive to jitter variations. The conclusion is that for a low error rate operation, Serial Repeaters are necessary for cable lengths above 4 m, offering at the same time a good margin. The eye-diagram for data transfer at 4.8 Gb/s is shown in Figure 10 for the path from sFEB to Router using: a 3 m tin-plated twin-ax), followed by an SRL1R and a 3 m tin-plated twin-ax. Silver-plated twin-ax cables were not available at the time of this test, while the tin-plated twin-ax used, present 50% worse attenuation at these frequencies.

IBERT tests ran for several hours at the VS setup presenting a behavior with negligible bit error ratio at the level of less than 10^{-13}.

2.3 SRL1R-V1 pre-production

In Section 2 the second version of the SRL1R is described, which was modified to comply with the integration electrical and mechanical requirements in the sTGC Trigger and readout chain. We have taken into account proper grounding, defined the power supply sources, take care of the heat dissipation, provide shielding and also take care of the twin-ax cables lengths. For proper timing, cable differences are quantized to one clock (320 MHz) or 62.5 cm.

Thirty SRL1Rs have been produced (see Figure 6) which were tested in the same test bench in the Vertical Slice Lab (sFEB to Router and pFEB to Pad Trigger) as the first version of the Repeaters. Twenty-nine SRL1R passed all the tests without error and one presented a problem with one link that gave continuous

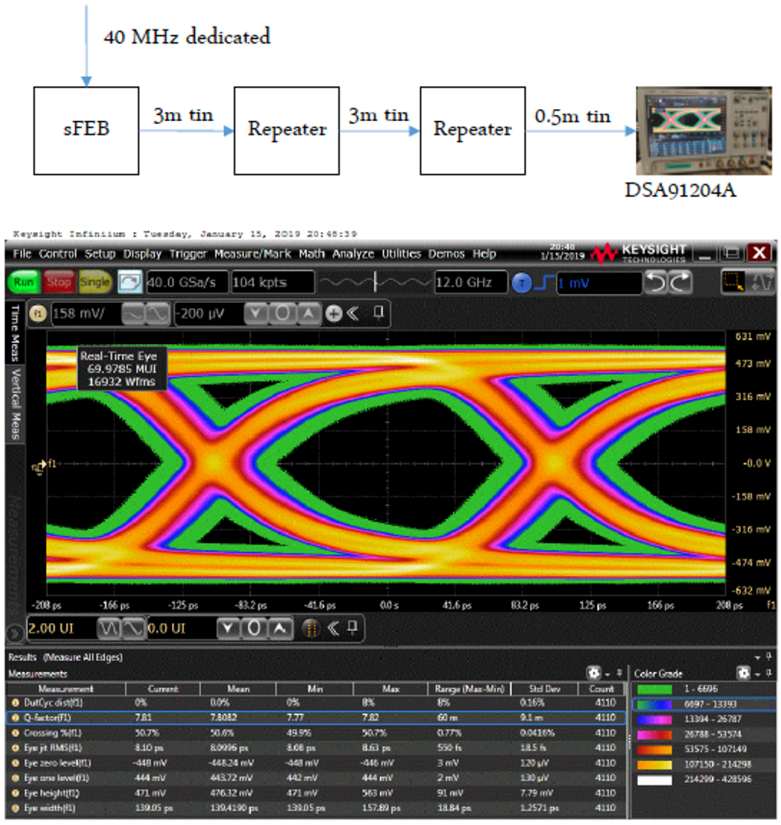

Figure 10: Eye-diagram for the sFEB to Router data transfer using SRL1R-V0.

errors. Optical inspection of the bad SRL1R did not show any visible problem that could explain the observed behavior. The temperature on the repeater chip during operation reached 34 °C in the open air. Some tests were performed in which the Front-end cards were placed on the wedge but the cabling was not in the final layout. Those tests ran for longer periods with negligible error rate up to 10^{-14}. A more complete 14-hour test consisting of a Pad Trigger connected via a LVD1R to an sFEB and subsequently to a Xilinx KC705 evaluation board for error-checking at 4.8 Gb/s was completed with zero errors.

2.4 On wedge tests of the SRL1R

Before the final production of the 768 (+ spares) SRL1R boards, the repeaters were tested in realistic conditions and also their temperature was monitored during operation. SRL1Rs are cooled passively with a copper pad in contact with the repeater chip. The tests have been performed on Wedge Module 0 with the Faraday cage included.

The SRL1Rs were powered from the L1DDCs and PRBS31 tests were performed in order to certify the integrity of the data transfer. This was certified to a level of BER of less than 10^{-14}. Even though the SRL1R power consumption is low (213 mW per board), their temperature was monitored in operation using a dedicated system with eight probes. The probes were placed on the backside of the SRL1Rs in contact with the copper pad. The temperature was monitored over a period of about 11 hours (about 40000 s). The temperature did not show any excess and varied from 22 to 25.5 °C following a daily variation.

Temperatures were registered under the following conditions: 1) SRL1R in open air (VS), temperature on chip: 34 °C, 2) SRL1R with copper pad, open air (probe on copper pad): 30 °C and 3) SRL1R with shielding, in the cable bundle, wrapped with plastic bag (probe on copper pad): 22 to 28 °C.

An evaluation of the heat dissipation and the temperature profile (isothermal curves) was done, using copper as passive cooler and a box surrounding SRL1R. The maximum temperature reached at a steady state was 28 °C, while the measured temperatures with the probes were between 26 to 28 °C. Figure 11 shows the temperature distribution around the repeater chip, as it was calculated with the COMSOL FEM analysis program.

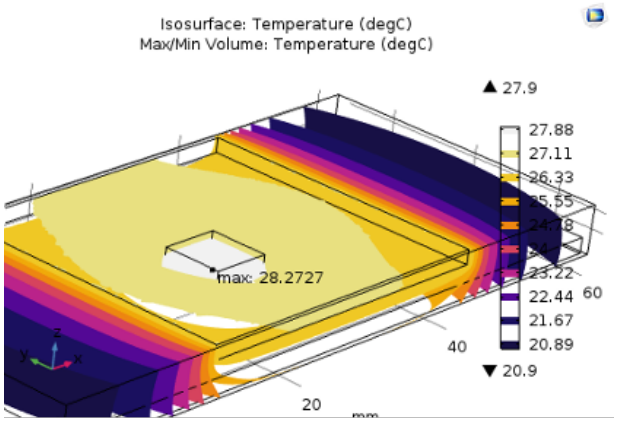

Figure 11: Temperature profile near the serial repeater chip as simulated by COMSOL [10]

3 LVDS Repeaters boards LVD1R – Pad Trigger to sFEB

The LVDS repeaters were initially designed to have single input-output twinax connections. Their consumption is about 1 W thus requiring active cooling. The second version of the LVD1R (Figure 13) is described in this paragraph. LVD1R is based on the Micrel 3.2 Gb/s Precision single channel LVDS buffer, SY58605U [11], with less than 300 ps delay and less than 135 ps part-to-part skew. The repeater input and output signals are DC-coupled. The Pad Trigger output runs a 640 Mb/s 7-bit DDR bus with 320 MHz clock from the Pad Trigger. sTDS receiver on the sFEB is for the four band-ID lines SLVS (from GBTx, IBM 130 nm) minimum swing 100 mV, while for the clock, frame and BCID lines is LVDS 1-to-4 fan-outs minimum swing 200 mV. A more convenient design was a six-tuple of LVD1R repeaters that groups six single LVDS repeaters in one - the LVD6R - which was easier to accommodate for cooling.

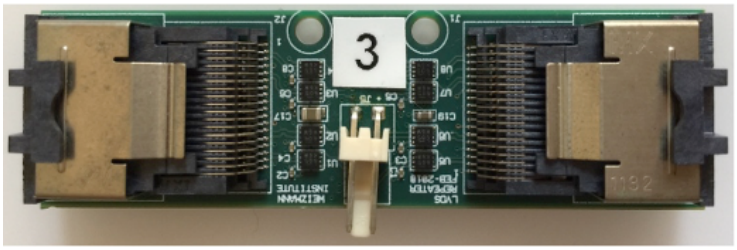

Figure 12: Photo of the LVD1R_V0 Repeater card.

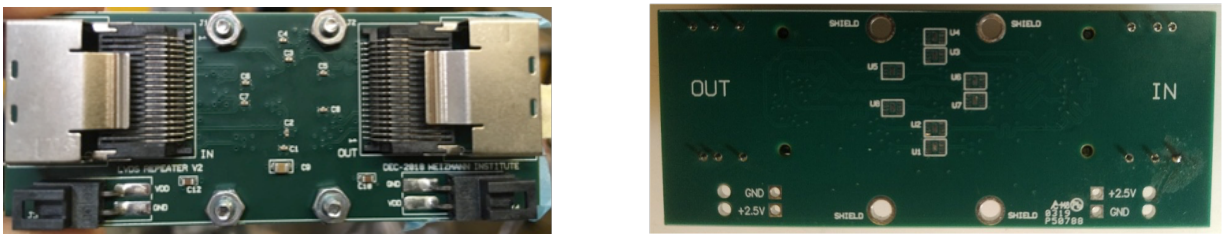

Figure 13: LVD1R_V1 Repeater photos, front face on the left and rear face on the right

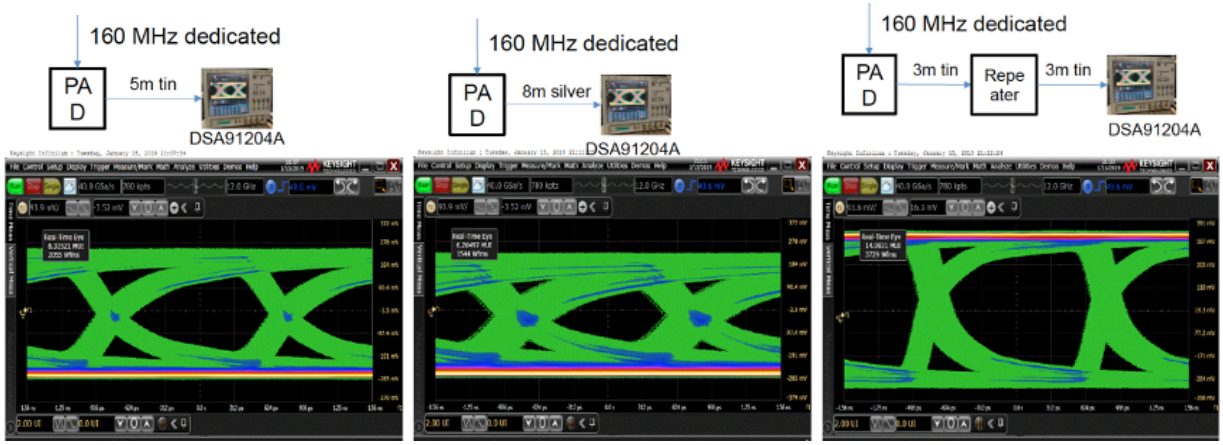

Figure 14: Eye diagrams for 5 m tin-plated twin-ax and 8 m silver-plated twin-ax and 3 m tin + LVD1R + 3 m tin.

3.1 LVD1R-V0 production and tests

Similarly to the serial Repeaters, LVD1R were produced in order to confirm the necessity of their use. As already mentioned, due to the wrong routing of the signals, only individual channel tests were possible to perform. Figure 12 shows a picture of the LVD1R-V0 Repeater. Extensive tests similar to the ones reported above for the SRL1R_V0 were performed which showed the necessity to use LVD1R Repeaters. The eye-diagram of the 8 m silver-plated twin-ax was bad with unstable link, while the link with the 5 m tin-plated twin-ax was of good quality (see Figure 14). The use of the LVD1R clearly improves the eye-diagram significantly. (Silver-plating was not expected to improve the low-frequency LVDS links.)

The case of a realistic length of 6.25 m was not possible to perform because we did not possess this cable length at that time. From the comparison of the eye-diagrams as well as the IBERT tests, we concluded that the use of LVDS Repeaters would be the safest choice.

3.2 LVD1R_V1 production and tests

Twelve LVD1R_V1 cards were produced together with the 30 SRL1R. The new LVD1Rs were fully tested as the routing of the signals was corrected and found that all 12 cards function properly. Extensive tests for 14 hours were performed with the Front-end cards plugged on the wedge. The temperature on the repeater chips during operation rose to 45 °C in the open air. The LVD1R have been tested on wedge (see above tests for the SRL1Rs) for their functionality, despite having initially grounding problems. All LVD1R

cards were tested and found to function properly in short and long overnight tests with BER $< 10^{-14}$. For this test, a copper pad was placed on the back of the LVD1R for thermal protection, because of their high consumption (≈ 1 W per board). The temperature of the LVD1R in the open air with the copper pad didn't exceed 40 °C. The LVD1R is not used in the final system but instead 6-tuple boards with six LVD1Rs, the LVD6R, are used instead with proper cooling. This is the subject of the following paragraphs on the LVD6R boards.

4 The LVD6R boards – Pad Trigger to sFEB connection in final layout

As already reported above, the LVD6R boards are used for the Pad Trigger to sFEB connection at 640 Mb/s. Since the consumption of the LVD6R board is close to 6 W per board, proper cooling is required. Four LVD6R boards per sector are needed. LVD6R boards are placed only on the spokes behind the Large Sectors as there is no space near the Small Sectors, thus on every spoke there are four boards serving the Large Sector and four the nearby Small sectors (two from the left side and two from the right side). This is shown in the schematic of Figure 15.

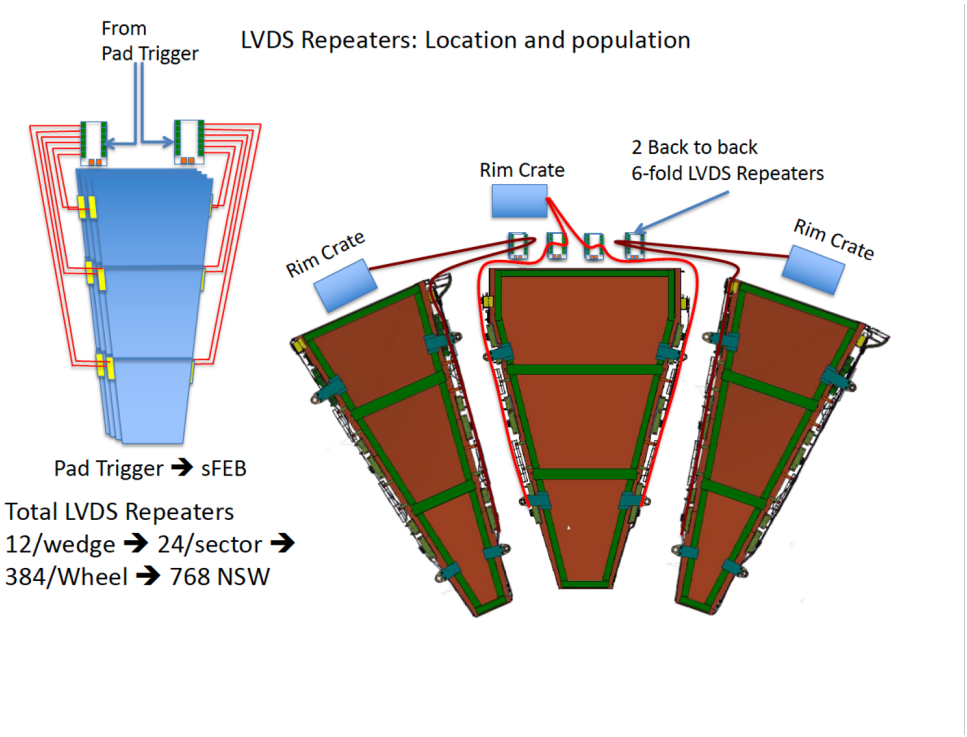

Figure 15: Schematic diagram of the placement of the LVD6R on the spokes behind the Large Sectors.

4.1 The LVD6R_V0 board

The design of each cable of the LVD6R is the same as the LVD1R design except that the 2.5 V power is provided by one FEASTMP_CLP module ([12], [13]) for all six. (Figure 16). The FEAST module is placed in the middle of the board in order: 1) To have them aligned in the back-to-back placement of the

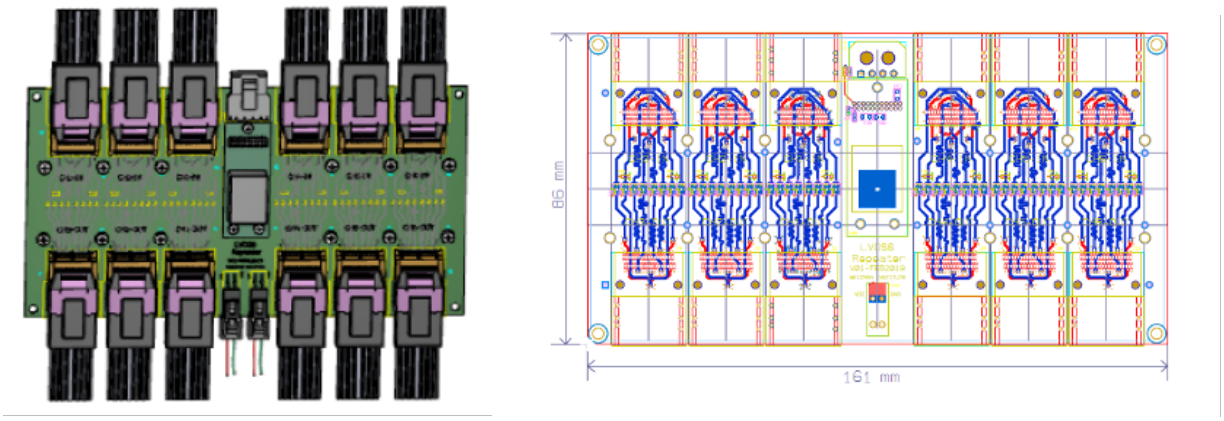

Figure 16: The LVD6R board 3D-schematic (left) and electronic design (right)

LVD6R doublets (see Figure 17) and avoid possible interference with the repeater channels of the opposite board and 2) To have all the input twin-ax cables on one side and all the output cables on the opposite side. Both LVD6R are fixed with brass screws on the cooling bar, so the repeater chips and the FEAST are in thermal contact with the cooling bar through thermal pads. The shielding box is supported, through the four holes in the corners of the PCBs, using threaded rods with spacers in between the boards for rigidity. All the materials used are not ferromagnetic as the LVD6Rs are placed inside the ATLAS magnetic field.

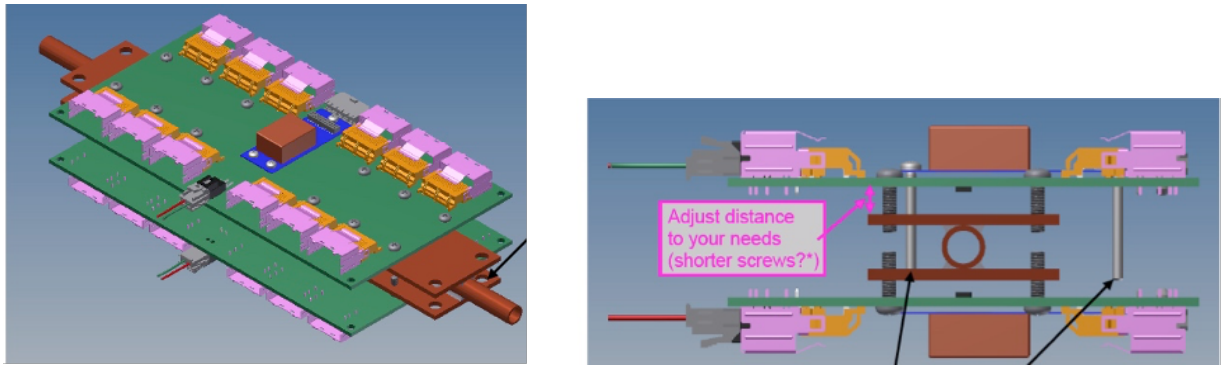

Figure 17: CAD drawings of the doublet LVD6R connected to the cooling copper bar. The tube in the middle for the cooling water circulation is visible.

The LVD6R is powered via the Molex connector to one ICS [14] channel. Two Nano-Fit connectors can provide power to nearby SRL1R Repeaters that may not be possible to power from the L1DDCs. The grounding follows the same principles as for the LVD1R with the exception that the shielding box is connected only to one ("LVD1R") Repeater channel on the LVD6R. The LVD6R performance is the same as the LVD1R Repeaters.

For the pre-production, three LVD6R boards were assembled and another two were ready before the end of June 2019, thus enough LVD6R to complete one sector. Two essential tests, described below, were performed with the LVD6R: proper functionality (particularly with the use of the FEASTMP_CLP module) and adequate cooling.

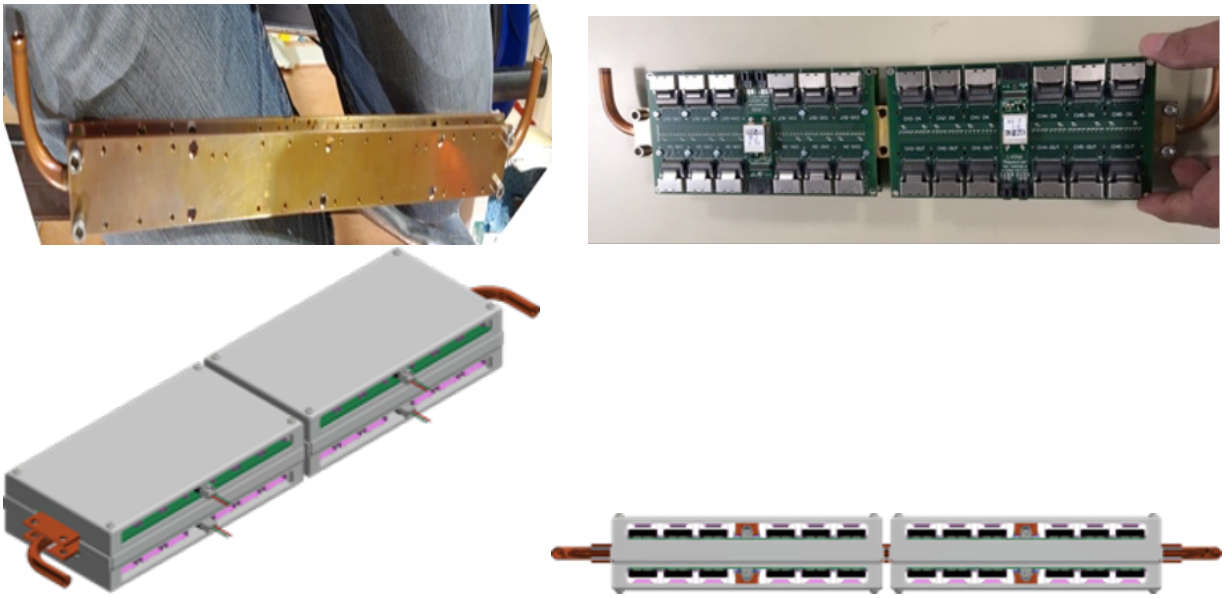

Figure 18: Photographs of the doublet LVD6R connected to the cooling copper bar. The tube in the middle for the cooling water circulation is visible.

4.2 The LVD6R functionality tests

Three LVD6R were assembled and have been tested successfully. For every LVD6R card, every one of the six LVDS channels was tested in the Vertical Slice Lab with the same setup as described in Sections 3.1 and 3.2. Every channel was tested in a short test with BER $< 10^{-11}$ and selected channels at random were tested for long periods with BER $< 10^{-13}$. The data transmission was not possible to test with simultaneous operation due to lack of sufficient number of Front-end cards.

4.3 LVD6R mechanical support and cooling

The LVD6R boards are mechanically supported on the spokes behind the large sectors. Figure 18 shows the cooling bar, LVD6Rs fixed on the cooling bar, two schematic views of the whole system consisting of: the cooling bar, the four LVD6R boards with the shielding box and a schematic of the whole system supported on the spoke. The cooling pipes are also shown. All issues of mechanical support, replacement operation and cooling have been clarified and defined. The LVD6Rs have been tested concerning the heat dissipation and the temperature profiles under intense operation. Data were being transmitted through all six LVDS channels without checking for their integrity, as this was the subject of the previous paragraphs. A monitoring system has been used with seven temperature probes: one for each of the six LVDS channels and one for the FEASTMP [12]. The probes were placed on top of the repeater chips, covered by a 1mm thick thermal gap pad (Bergquist Gap Pad 5000S35 [15]). The "sandwich" was then clamped to the cooling bar with screws (see Figure 19). Placing the probes on top of the repeater chips may affect the heat dissipation because the LVDS buffers are very small, but still the result is on the safe side.

When operating the LVD6R in the open air, the temperature reaches 45 °C. Connecting the LVD6R to the cooling bar, the temperature of the LVDS drops to about 37 to 38 °C and that of the FEAST to about 40 °C. Connecting the bar to the chiller without water circulation yet another drop is seen to 32 °C on the LVDS

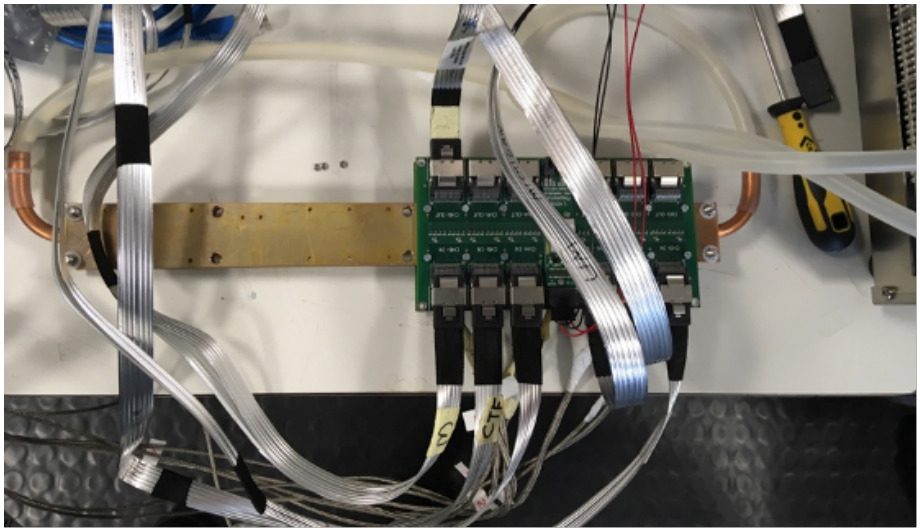

Figure 19: Photograph of the setup for the LVD6R temperature monitoring. Two LVD6R are fixed on the cooling bar that is connected with pipes to the chiller. Six twin-ax cables (input) are connected and seven thermal probes.

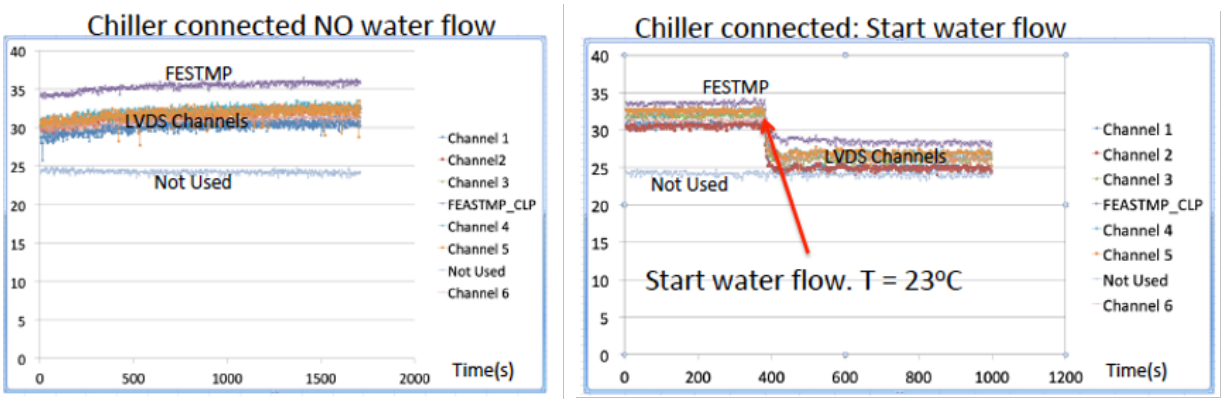

Figure 20: FEAST and LVDS buffers temperature under operation without water flow (left) and with water flow (right). The step on the temperature drop is visible when water starts flowing.

and 36 °C on the FEASTMP. Operating the chiller with water temperature at 23 °C (as it will be in normal NSW operation), the temperature of the LVDS drops to about 26 °CC and that of the FEAST (opposite side of the PCB) to around 28 °C. Figure 20 shows the evolution in time of the temperature with the chiller connected, without and with water flow.

The temperature of the LVD6R was simulated with the FEM program Comsol and the data fit very well with the simulation. Figure 21 shows the temperature distribution around the LVDS buffer chips.

Concluding, the LVD6R are fully validated concerning their functionality and the data integrity during data transfer. The cooling of the board and the FEAST are very effective and much below their operation limits.

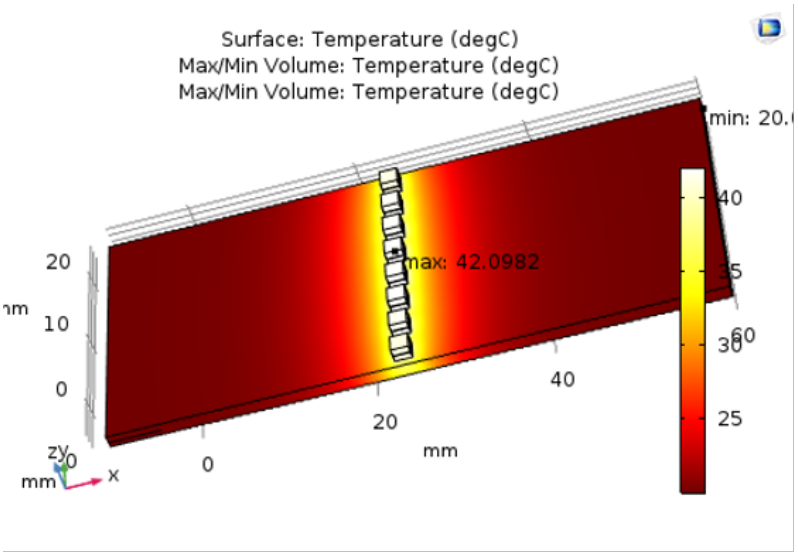

Figure 21: Comsol evaluation of the LVDS repeater chips under operation. Maximum temperature is estimated to be 42 °C, while the measured one is 45 °C.

5 Commissioning and integration

Full production of the 880 SRL1R Repeaters boards and their copper shielding was completed by November 2019. In January 2020 the final SRL1R Repeaters were assembled in their shielding/cooling boxes. A detailed study was performed to conclude on the boost of the repeaters and the value of 12 dB was a common optimal choice for all different cable lengths combinations. The assembly included the following steps: 1) Placing the gap pads, 2) Placing of the protective Kapton, 3) Assemble box, 4) Place the jumpers for the boost selection, 5) Kaptonize box externally, 6) Create and attach the labels according to the database and 7) Insert in the database. All SRL1R Repeaters were tested on a test-bed that was developed especially for that purpose in a loop-back configuration. The Xilinx VC707 evaluation board [16] was used together with a mezzanine card for the loop-back test. All 880 SRL1R boards were tested with only four failures, thus with a yield greater than 99%. Figure 22 shows the assembly (left), the testing (middle) and the use at the VS lab of the SRL1R Repeaters.

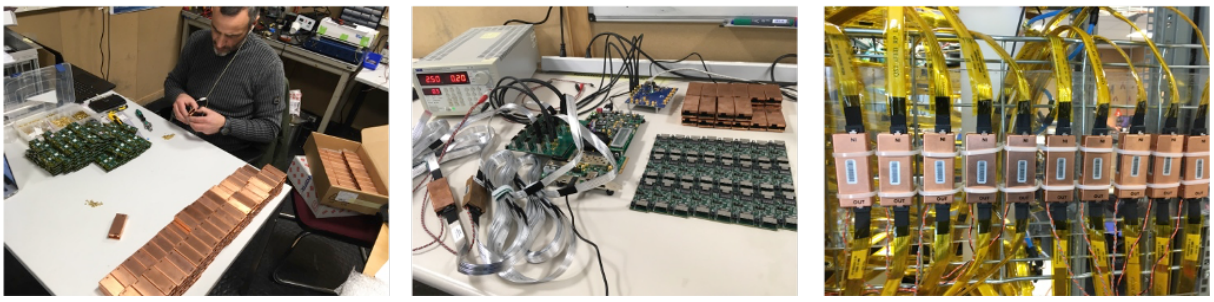

Figure 22: Assembly (right), testing on the Xilinx VC707 test bench (middle) and use in the Vertical Slice setup of the SRL1R Repeaters

The SRL1Rs boards were integrated on the sectors in Building 180, before assembling it with the Micromegas sectors in Building 191. The grounding of the Repeaters was according to the ATLAS

rules [17]. Thus the twin-ax grounding formed a continuation with the shielding and was isolated from the return of the power supply. Even though the Small sectors integration went smoothly, in the Large sectors, a serious problem of noise appeared. The correction was to connect together the SRL1Rs board power return line and the board shielding.

All 144 LVD6R boards were assembled on their cooling bar and enclosed in their shielding by October 2020. All LVD6R boards were tested in loop-back testing and none was found to present a problem. 128 LVD6R boards in blocks of four, enclosed in their shielding were placed around the wheels on the spokes of the large sectors, i.e. (two wheels) x (16 LVD6R cooling bars) x (four LVD6R boards). Figure 23 shows Wheel A and the placement of the LVD6R cooling bars on the spokes of the large sectors.

All spare SRL1R and LVD6R Repeater boards are kept in the controlled temperature and humidity storage box at the Vertical Slice Lab. The SRL1Rs are already assembled in their shielding boxes ready to be used. The LVD6R boards are not mounted on cooling bars as a replacement of a broken board would be done individually on an existing cooling bar.

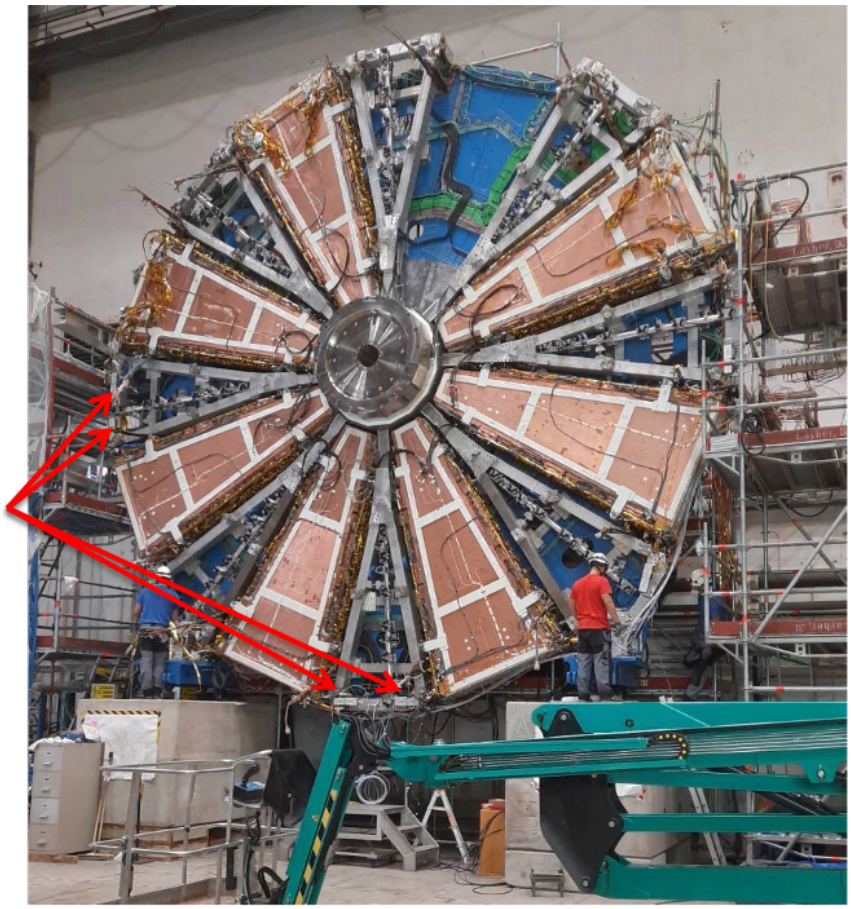

Figure 23: Placement of the LVD6R cooling bars on Wheel A, as shown by the red arrows.

6 Conclusions

Serial and LVDS Repeaters are needed to restore the sTGC trigger signals in their connections from the FE boards to the Pad Trigger and the Router and also between the Pad Trigger and the sFEBs. Those signals are attenuated as they propagate long distances up to 6.25 m. A detailed study was performed to identify the channels that required restoration of the signals and serial (SRL1Rs) and LVDS (LVD6Rs) Repeaters were designed and build for the connections 1) pFEB–Pad Trigger, sFEB–Router and 2) Pad Trigger–sFEB respectively. 768 SRL1Rs and 128 LVD6R Repeaters are needed for both Wheels. Detailed studies showed their proper operation. At the time of writing this note, about one year after the Repeater's integration on the Wheels, no problems have been reported.

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