Hardware Design and Testing of the Generic Rear Transition Module (GRM) for the Global Trigger Subsystem of ATLAS Phase-II Upgrade

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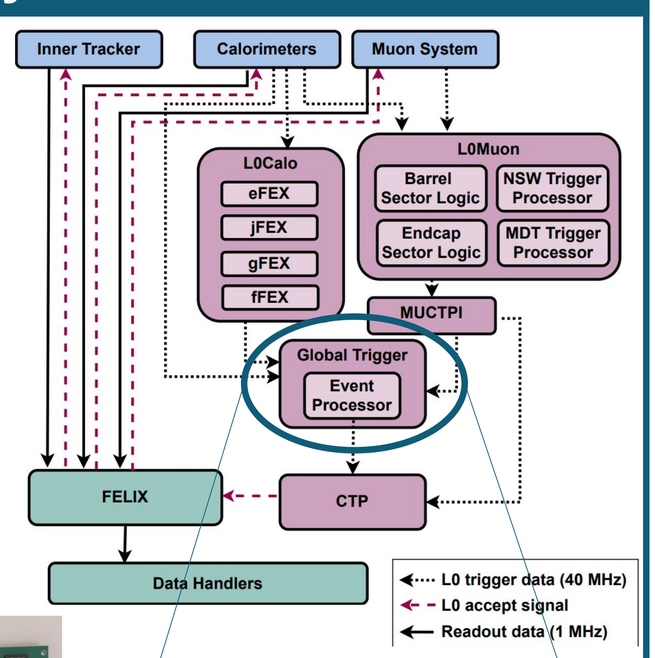
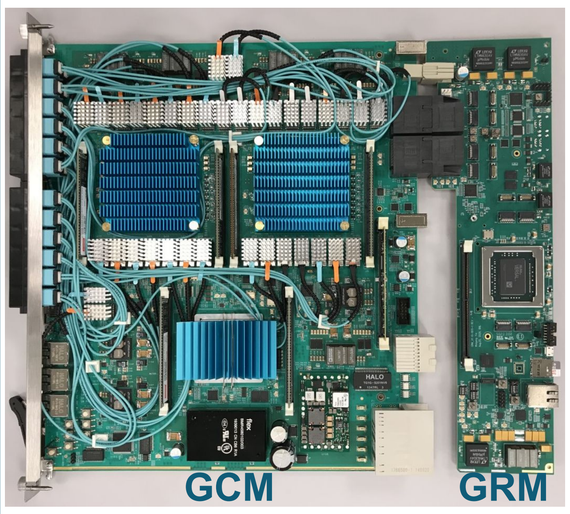
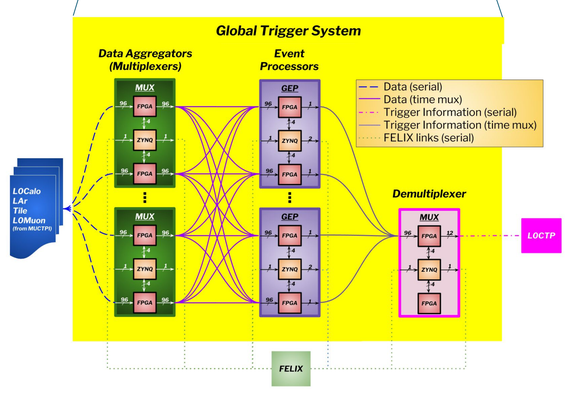
Global Trigger Subsystem

The Run-4 (high-luminosity LHC) single-level, 10 μs-latency trigger of the ATLAS experiment will feature the new **Global Trigger subsystem**, performing offline-like algorithms on full-granularity calorimeter data. Time-multiplexers (MUX) concentrate full bunch-crossing events onto single Global Event Processors (GEPs). Several MUX and GEP firmware nodes run on **identical hardware**, an ATCA front board called 'Global Common Module' (GCM). A matching rear transition module (RTM), called '**Generic RTM**' (**GRM**), was designed to mitigate the risks of the complex design and power management.

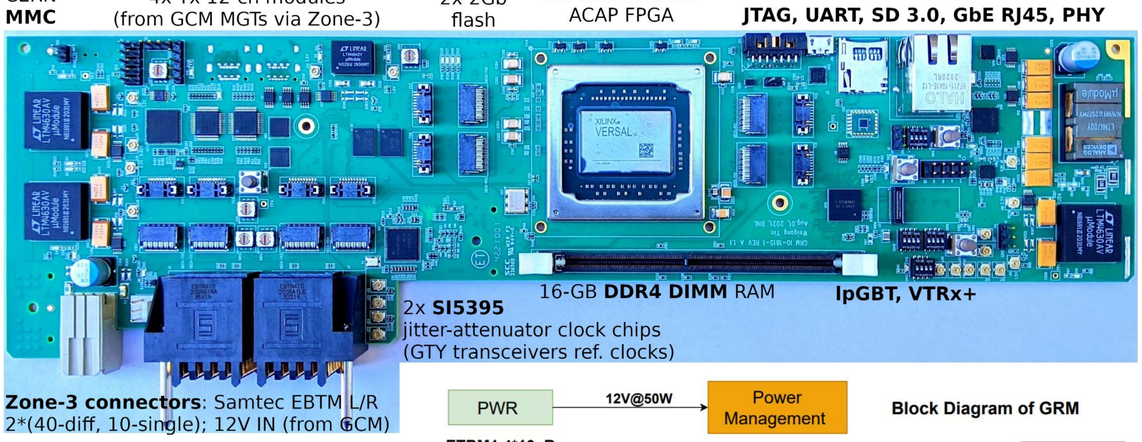






GRM Hardware

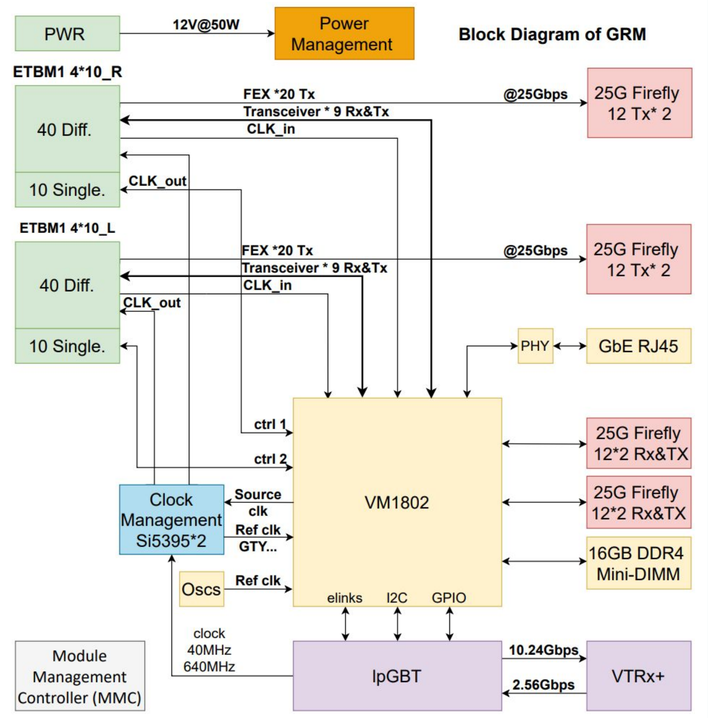
2x **ADM1066** power mgmt. sequencing and monitoring
Samtec **ECUO FireFly** 25-Gb/s 2x TxRx 12-ch pairs (6 GTY quads)
5x **LTM4xxx** dual-rail DC/DC regulators
CERN **MMC**
Samtec **ECUO FireFly** 25-Gb/s 4x Tx 12-ch modules (from GCM MGTs via Zone-3)
QSPI 2x 2Gb flash
Versal Prime Xilinx VM1802 ACAP FPGA
JTAG, UART, SD 3.0, GbE RJ45, PHY



GRM's photo and block diagram show the board's main features.

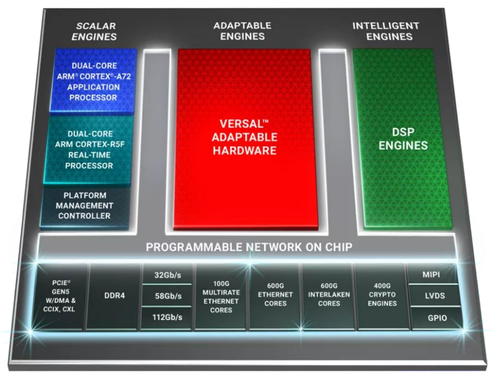
124x **25.8-Gb/s MGT** links:
- 24x TxRx VM1802 GTY with 2x 12-ch FireFly pairs (for communication with FELIX);
- 18x TxRx (VM1802 comms to GCM FPGAs, via Zone3);
- 40x Tx links from GCM (via Zone3) to 4 FireFly modules (expanding GCM readout).

Radiation-hard ASICs **lpGBT** and VTRx+ enable emulation of Phase-II detector front-ends, allowing early integration tests.



GRM Versal bring-up

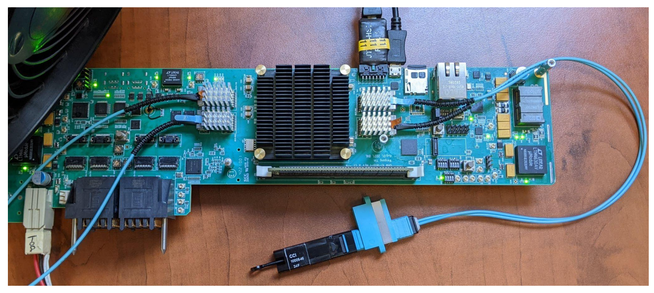
GRM's innovative Xilinx **Versal Prime** SoC for heterogeneous computing (ACAP FPGA) was configured with Control, Interfaces, Processing System (CIPS), Network-On-Chip (NOC) and DDRMC IPs. All CIPS interfaces, such as DDR4 memory, GbE and UART were tested successfully. The OS was cross-compiled via PetaLinux 2021.2, and Python scripts were developed to configure and monitor the power and thermal performances from the several I2C devices.

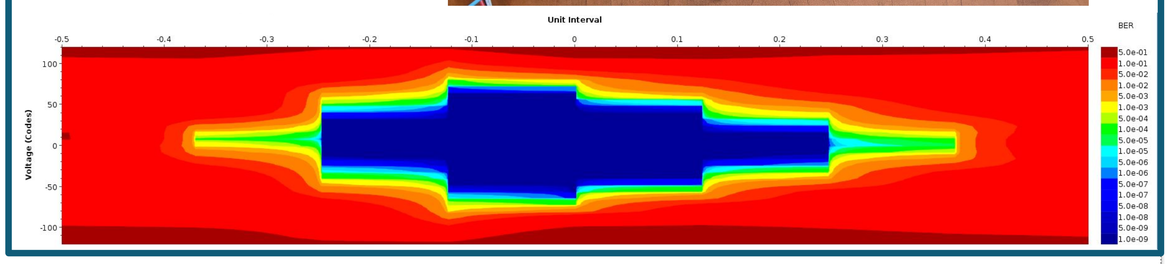


GRM Transceiver testing

Versal **GTY** MGTs and Samtec ECUO **FireFly** 14-Gb/s and 25-Gb/s optical modules were tested in PRBS loopback with Xilinx **IBERT**. All links run **error-free** achieving BER < 10^{-13}.

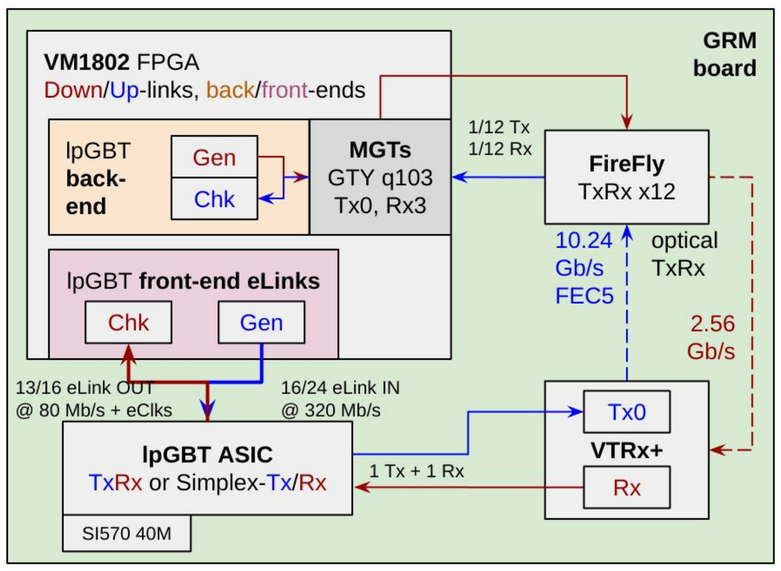
Link	Open area	
Quad -MGT	12.8 Gb/s	25.8 Gb/s
106-0	6848	4865
205-0	7360	5184
206-0	8000	6080
Avg.	7900	5380





GRM lpGBT testing with VM1802

lpGBT functionality and its interfacing to the **VM1802** FPGA were also exercised on GRM. The lpGBT ASIC is firstly configured via I2C by the OS. Custom logic is used to generate, send, receive and check data on **uplink** & **downlink**. Data loopbacks run via electrical eLinks (with LVDS & CLPS standards) and via optics, through VTRx+ and FireFly pair (asymmetric 10.24 & 2.56 Gb/s), as the block diagram shows.



Conclusions and Outlook

ATLAS Global Trigger is a new firmware-focused trigger subsystem running on common hardware platform. The GRM board design, fabrication and testing have been completed successfully. All its hardware functionality has been validated. A first-time demonstration of **Versal** and **lpGBT** interfacing was achieved, and as both devices will play crucial roles in ATLAS TDAQ for a long time, this experience on GRM will also be valuable to several other projects (e.g. GCMv3 revision and FELIX FLX18* Phase-II hardware).

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