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THE DUAL QUADRATURE DIRECT DIGITAL SYNTHESIZER TECHNICAL MANUAL

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Abstract

The dual Quadrature Direct Digital Synthesizer is a new developed module which, in combination with a GFAS, can be used to generate two independent pairs of quadrature sine waves. The frequency of the generated sine waves is determined be the function programmed in the GFAS. The Dual Quadrature D.D.S. is a general purpose module, but it was initially designed for the P.S. Booster longitudinal Mode Analyzer System to act as a synchrotron frequency programmer.

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25 February 1999

Table of contents:

Introduction. 3.

1. The hardware description. 4.

1.1. The digital logic. 5.
1.1.1. The three workings modes of the module. 5.
1.1.2. The serial to parallel converter. 6.
1.1.3. The multiplexers. 6.
1.1.4. The ALTERA program. 8.

1.2. The D.D.S. integrated circuit. 11.

1.3. The DAC and filtering output circuit. 15.

2. The characteristics. 16.

3. The calibration procedure. 17.

4. The D.Q.D.D.S. as synchrotron frequency programmer. 19.

Acknowledgement. 20.

References. 20.

Annexes:

1. Schematics of the Dual Quadruature Direct Digital Synthesizer module.
2. The ALTERA AHDL program listing with comments.
3. The Q2334 D.D.S. data sheet.
4. The AD9713BBN D.A.C. data sheet.
5. The Dual Quadrature Direct Digital Synthesizer module front panel.
6. The PCB component view.

Introduction.

The Dual Quadrature Direct Digital Synthesizer (DQDDS) is a new developed NIM module which, in combination with a GFAS, can be used to generated two independent pairs of quadrature sine waves. The frequency of the generated sine waves is determined by the programmed function of the GFAS.

The module can generate the two independent pairs of quadrature sine waves with a frequency range which goes from DC to 1MHz with a resolution up to 1Hz.

The 1st chapter will give a detailed description of the module and its operation by explaining the different parts of the block diagram

Chapter 2 will summarize the characteristics of the module.

The module needs to be calibrated before using it in any system. This calibration is rather simple and a procedure is given in the 3rd chapter of this note.

Initially the DQDDS was designed for the P.S. Booster longitudinal Mode Analyzer System to act as a synchrotron frequency programmer. The 4th and last chapter will briefly describe how to use the DQDDS is such a system.

1. The hardware description.

The Dual Quadrature Direct Digital Synthesizer (DQDDS) generates two independent pairs of sinusoidal signals in quadrature. This means that the relative phase between the two outputs differs 90° of which the output "OUT*" is lagging in respect to the output "OUT". The block diagram is illustrated in figure 1.1, in which we can see that the module is made of two identical channels. In the following paragraphs, only one channel will be discussed.

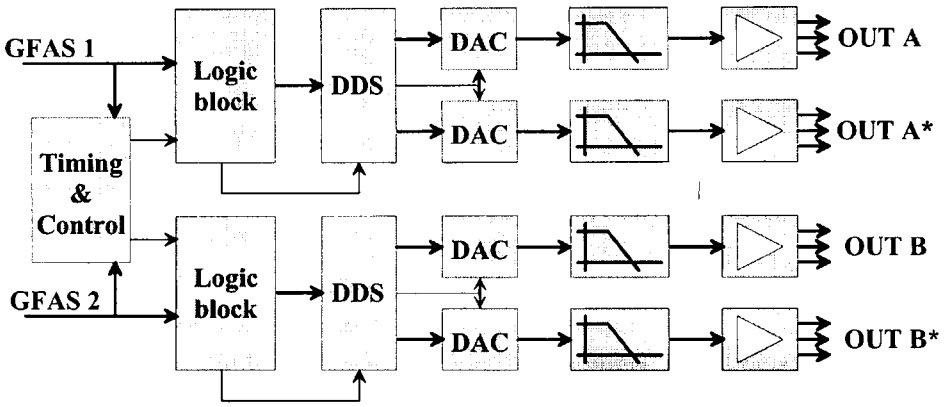

Figure 1.1: The dual quadrature direct digital synthesizer block diagram.

A GFAS sends every 20us during approximately 4us its 16-bit data in a serial format to its destination, which in this case is the DQDDS. This data is converted into parallel as soon as it enters the serial/parallel converter, which is part of the "logic block". The obtained parallel data is then stored in a buffer until the complete frequency word is sent. Immediately after the data is released from the buffers it is send to the D.D.S. chip in 4 times 8 bytes.
Once the D.D.S. received a clock signal indicating that the frequency word is completely present in the D.D.S. input buffers it starts generating a pair of quadrature sine waves with a frequency corresponding to the frequency word that was sent by the GFAS. The D.D.S. will then generated a series of 12-bit words, representing the amplitude of the sine wave to be generated. A digital to analog converter (DAC) will produce the actual sine wave as a staircase. The filters will smooth the signal and suppress the unwanted digital noise and clock signals. Output buffers will provide 3 outputs of the same signal.

1.2. The digital logic.

In the block diagram of figure 1.1 we see two identical blocks called "logic block". This logic block is a collection of different digital functions integrated in one electrical programmable logic device from the producer "ALTERA" Figure 1.2 shows the schematic contents of the programmable device.

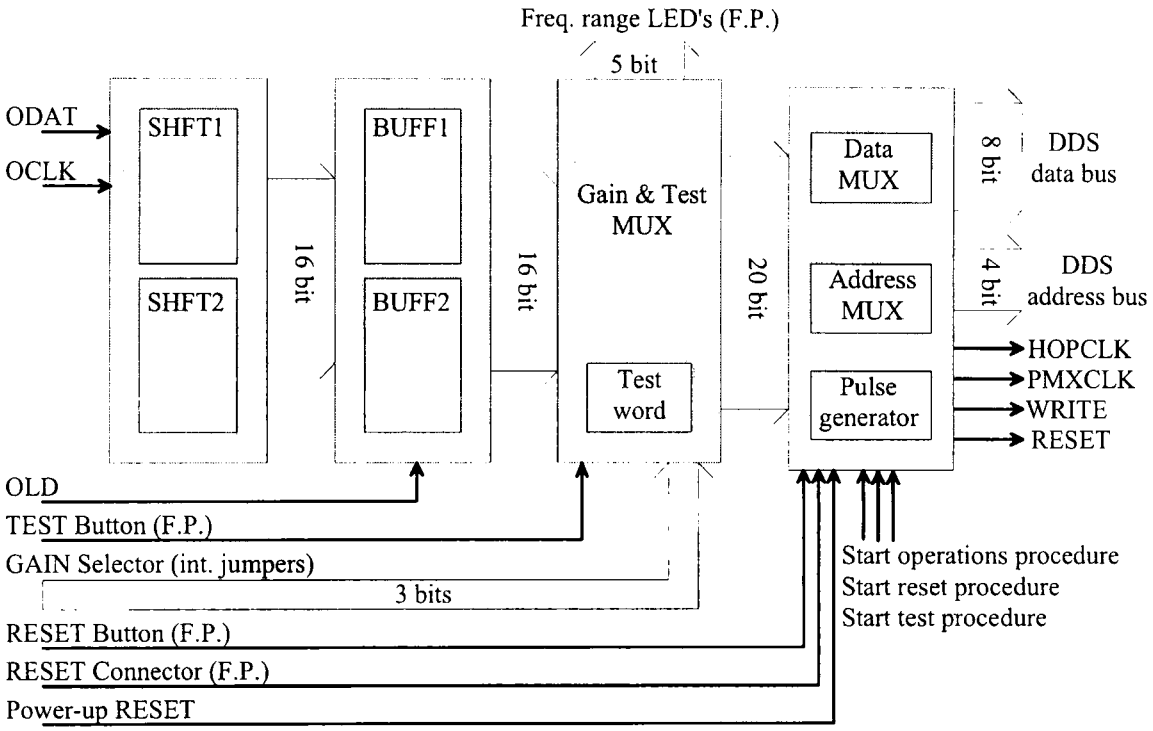

Figure 1.2: The schematic contents of the logic block.

1.1.1. The three working modes of the module.

The module can work in three different modes depending on the external conditions:

1. Operation mode
2. Test mode
3. Reset mode

Operation mode:
In the operation mode the 16-bit data coming from the GFAS is used to generate the output frequency. The operational mode is automatically active when the reset and test mode are inactive.

Test mode:
The test mode, activated by the button on the front panel, gives the user the possibility to send a pre-programmed 16-bit freqeuncy word to the D.D.S. This will ease the search in case of a problem.

Reset mode:
The reset mode is necessary in order to be able to (re-)intitialize the D.D.S. and to reset the contents of the registers. This mode is activated at power-up, by pushing the front panel reset button or pulsing the reset input.

1.1.2. The serial to parallel converter.

The serial data coming from the GFAS is converted into parallel data. This serial to parallel converter is nearly the same as the one used on the GFA's DAC cards and is partly integrated in the logic block.
The serial data is formatted in the following way:

- Each bit has a time frame of 250 ns.
- A logic '1' is high during ¾ of a bit time frame (~190 ns).
- A logic '0' is high during ¼ of a bit time frame (~65 ns).
- The serial data consists of 16-bits and has thus a time length of 4us.
- Each 20us a new 16-bit word is sent.

When one samples the original serial data in a on the rising edge of the delayed serial data, one can demodulate the serial data and convert it into parallel data by means of shift registers. In reality the serial data enters via an opto-coupler which transmits the data to a PAL and an active delay circuit. The output of the PAL provides two important signals:

- The original serial data (ODAT)
- The delayed serial data (OCLK), which acts as clock for demodulation.

These two signals enter the serial in and parallel out shift registers, which are programmed in the logic block. When the complete 16-bit word is stored in the shift registers, according the principle described above, a clock signal (OLD) latches the data into the buffers. At the same moment the data is available for further treatment by the logic block.

1.1.3. The multiplexers.

The logic block contains 4 types of multiplexers:

- The gain multiplexer
- The test multiplexer
- The data multiplexer
- The address multiplexer

The gain & test multiplexer:

This multiplexer provides the link between the serial to parallel converter and the data multiplexer. The D.D.S. chip can accept 32-bit wide frequency words. The serial frequency word send by the GFAS is only 16-bit wide. This offers the possibility to shift the 16-bit word within the 32-bit wide D.D.S. region. This way one can change the output frequency range and thus the frequency gain.

The gain & test multiplexer provides:

- Gain selection (set by 3 onboard jumpers).
- Data multiplexing between:
  - Operational mode data (16-bit data word from the serial input).
  - Test mode data (16-bit internally pre-programmed frequency word).
- Visualization of the chosen gain on the front panel by means of LED's.

The multiplexer is constructed so that the 16-bit word can be shifted within a range of a 20-bit word. This provides 5 different gain settings and thus frequency ranges. The gain multiplexer is controlled by 3 jumpers: GC2, GC1 and GC0. Table 1 shows the properties going with the different jumper settings.

MSB		LSB					
GC2	GC1	GC0	Start frequency	End frequency	Frequency step	Gain	LED on
0	0	0	0 Hz.	65kHz.	1 Hz.	1	L1
0	0	1	0 Hz.	131kHz.	2 Hz.	2	L2
0	1	0	0 Hz.	262kHz.	4 Hz.	4	L3
0	1	1	0 Hz.	524kHz.	8 Hz.	8	L4
1	0	0	0 Hz.	1048kHz.	16 Hz.	16	L5
1	0	1	0 Hz.	65kHz.	1 Hz.	1	None
1	1	0	0 Hz.	65kHz.	1 Hz.	1	None
1	1	1	0 Hz.	65kHz.	1 Hz.	1	None

Table 1: The jumpers setting and properties of the gain multiplexer.

Table 2 shows the distrubution of the 16-bit frequency word within the 20-bit range as a function of the gain jumper settings.

MSB		LSB	Multiplexer output bits																			
GC2	GC1	GC0	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Gain
0	0	0	0	0	0	0	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	1
0	0	1	0	0	0	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	2
0	1	0	0	0	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	4
0	1	1	0	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	8
1	0	0	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	16
1	0	1	0	0	0	0	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	1
1	1	0	0	0	0	0	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	1
1	1	1	0	0	0	0	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	1

Table 2: The frequency word position as a function of the gain jumper settings.

Table 3 finally shows the position of the 16-bit frequency word within the complete 32-bit range of the D.D.S. chip. All the leading bits (b0, b1,b2....) are logically '0'

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DDS data word
0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0	Gain multiplexer data output
0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0	Gain = 1
0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0	Gain = 2
0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0	Gain = 4
0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0	Gain = 8
0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0	Gain = 16

Table 3: The frequency word position as a function of the gain jumper settings.

The data & address multiplexer:

The data and address multiplexer are constructed in the ALTERA chip by means of a state machine. It makes sure that the complete 32-bit frequency word is sent in 4 times to the different addresses. It also generates the clock pulses in order to confirm the data and to start the generation of the sine waves by D.D.S.

The way the data is written to the different addresses (registers) is discussed in the next paragraph, that deals about the program in the ALTERA chip.

1.1.4. The ALTERA program.

The ALTERA is an electrically programmable logic device. The language used for programming the chip is the Altera Hardware Description Language (AHDL).

The entire program, with useful comments, can be found in Annex 2.

As mentioned previously the module can work in three different modes. Depending on the choice of these modes the programmed state machine will execute different commands.

In figure 1.3 we see the most important steps and corresponding actions of the state machine in the operation and test mode.

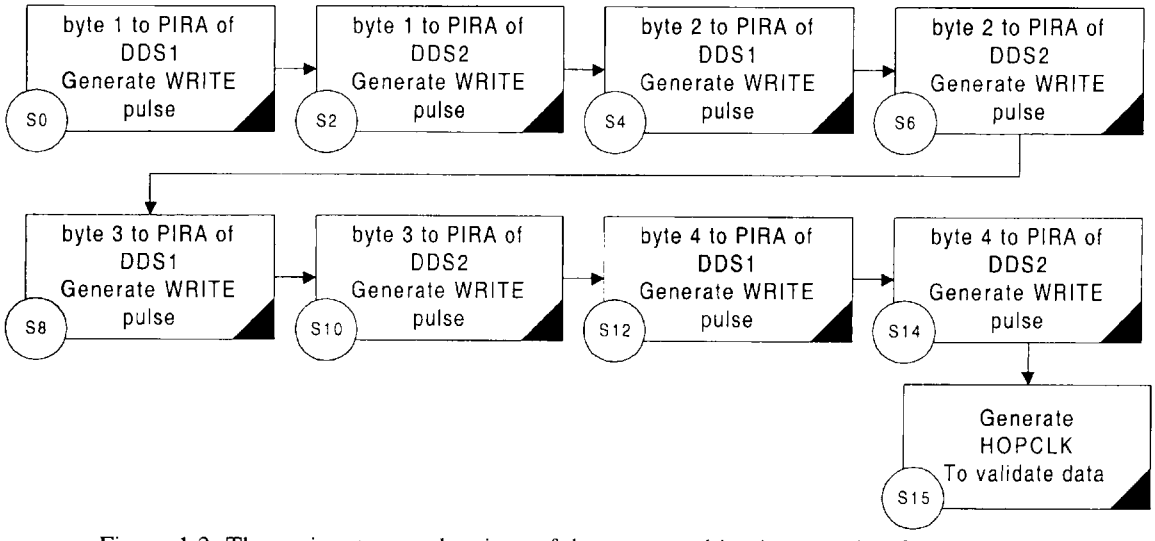

Figure 1.3: The major steps and actions of the state machine in operational or test mode.

As already mentioned the 32-bit frequency word is written in 4 times to the 1st Phase Increment Register (PIRA) of the dual D.D.S. chip. Once the complete frequency word is received by the two channels of a single D.D.S. chip the so called HOPCLK is asserted in order to validate the data. The D.D.S. will now start generating the sine waves with a frequency corresponding to the programmed frequency word. The exact address coding is given in paragraph 1.2. and annex 3.

Figure 1.4 shows the major steps and actions of the state machine when it is operating in the reset mode.

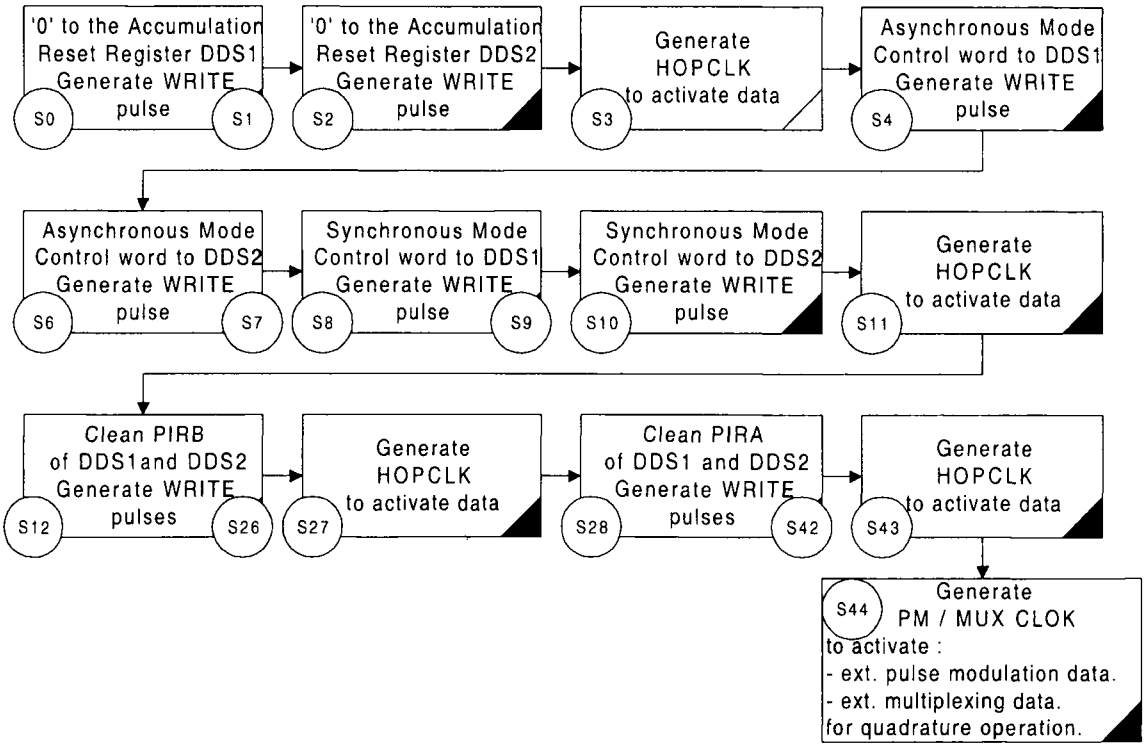

Figure 1.4: The major steps and actions of the state machine in the reset mode.

In the reset mode all registers are cleaned and data necessary for quadrature operation are loaded. Here again I like to refer to paragraph 1.2 and annex 3. for the exact address coding and to annex 2 for the entire and commented program.
These state machines are started by the incoming data. Figure 1.5 shows a timing diagram in which one can see how the state machines, in the EPLD, are controlled.
The ODAT input is where the data from the GFAS enters the module. This is thus a bit stream. A monostable multivibrator generates a kind of inhibit signal (OLD) that makes it possible to convert the serial data into parallel data and to store it in a buffer. When all the data has been received, the OLD goes high. The up going flank of the OLD signal enables the output of the buffers so that the parallel data is available for the multiplexers. It also starts other monostable multivibrators, for each operational mode one, that are combined to one signal, by means of an OR relationship, in the EPLD, called START COUNT. This

signal generates the VALID COUNT signal that is synchronous with the ELPD 4MHz clock. During the high time of the VALID COUNT signal the state machine is running. When the state machine has finished its cycle, it automatically resets the VALID COUNT signal to '0'. At the same time the state machine is forced to its initial position where it is ready to perform another sequence for the next frequency word, 20us later.

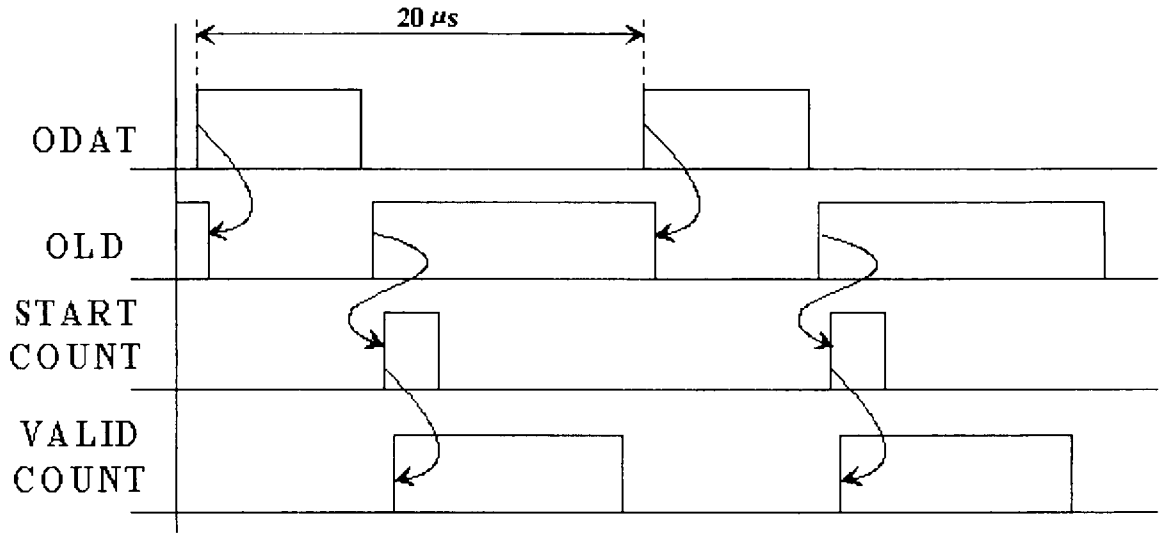

Figure 1.5: The Timing diagram of the data transfer sequence.

1.2. The D.D.S. integrated circuit.

This paragraph will deal with the way the D.D.S. chip is programmed in order to generate quadrature signals. A copy of the original data sheet can be found in annex 3. Figure 1.6 shows the a diagram of the internal structure of the Q2334 D.D.S. chip.

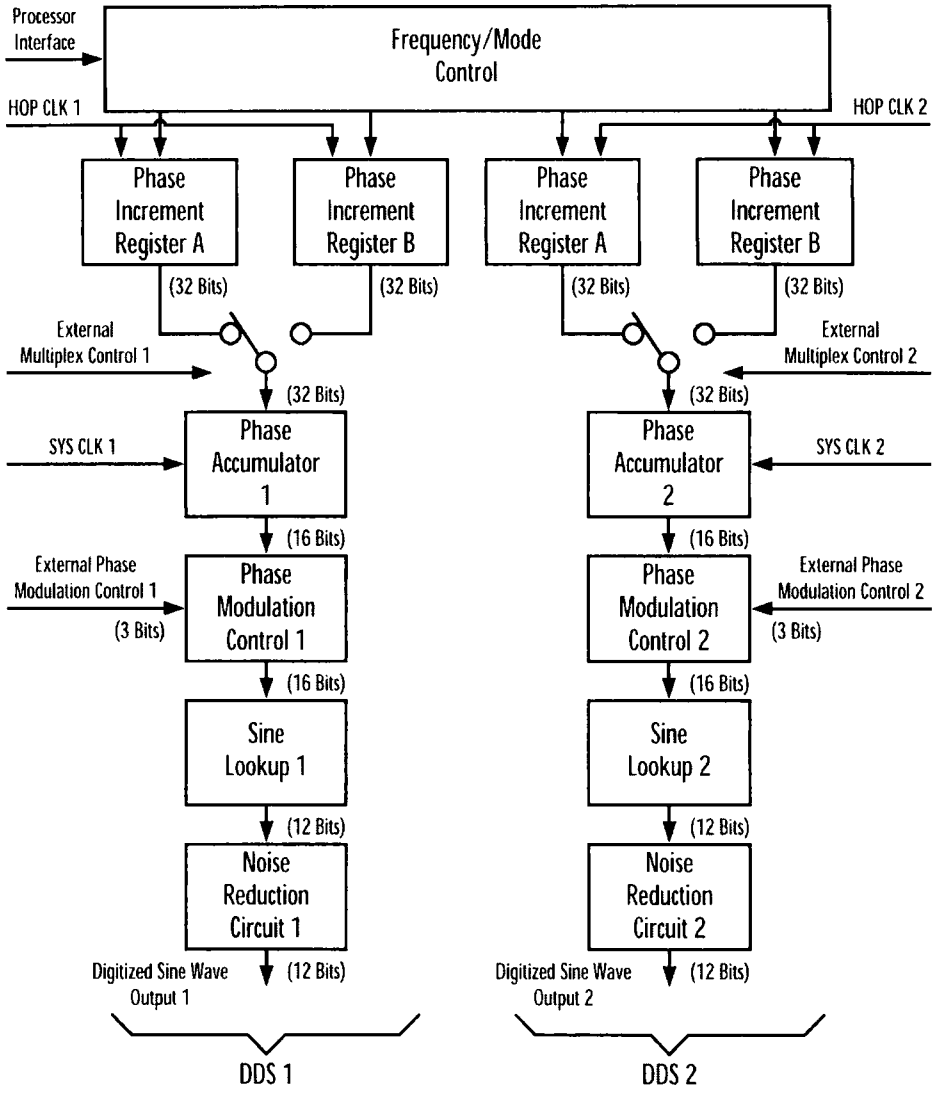

Figure 1.6: the internal structure of the Q2334 quadrature direct digital synthesizer

The 32-bit frequency word is entered via the 8-bit processor interface. When the complete word is sent to the two D.D.S. channels a HOPCLK signal clocks the data from the frequency/mode control block into the Phase Increment Register PIR, in our case PIRA. The PIRB can be used to perform internal phase modulation and is set to '0' in our case. The switch of the external multiplex control is set as drawn in the picture. This means that the phase accumulator uses the data from PIRA.

The SYSCLK, which in our case is the same for both channels, now adds each time the information in the PIRA to the value present in the phase accumulator.
The value is send to the sine lookup table, which will output a 12-bit value for the sine wave amplitude.

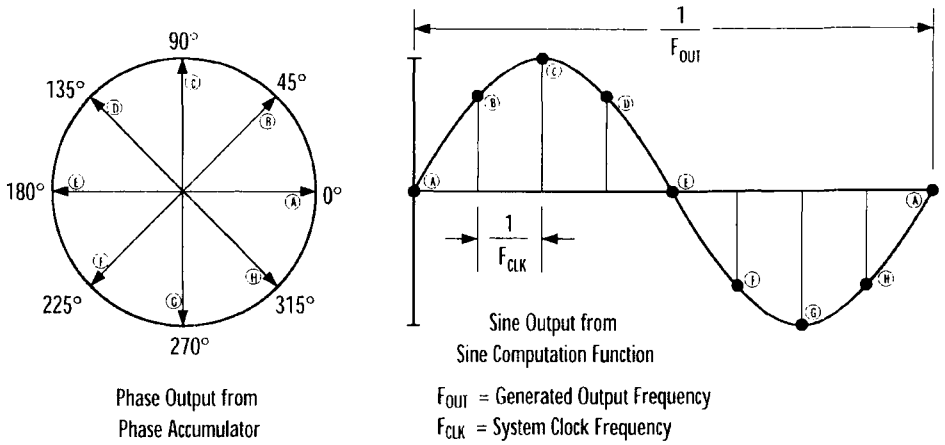

Figure 1.7: A sample sine wave generation.

The generated frequency can then be calculated with the next formula:

$$F_G = \frac{F_S \cdot \Delta\Phi}{2^N}$$

Where:

- F_G = the generated frequency
- F_S = the system clock frequency
- N = the number of bits (32)
- $\Delta\Phi$ = the phase increment value programmed in the PIR.

The phase modulation control block gives the possibility to add a phase shift to one channel in respect to the other. This is done by 3 so-called external phase modulation offset bits. The phase offset as a function of the bit settings is given in table 4. In our case the 2nd D.D.S. is lagging 90° in respect to the 1st channel.
This is done by making the PM ext. bit 2 of the 1st D.D.S. channel '1', which gives a absolute phase offset of 90°. When we make all PM ext. bits of the the 2nd D.D.S. channel '0', which gives an absolute phase offset of 0°, then we have a relative phase offset of 90°. This data is activated after assertion of the PM clock signal, which is done during the reset procedure.

PM EXT BIT2	PM EXT BIT1	PM EXT BIT0	Abs. Phase offset
0	0	0	0°
0	0	1	45°
0	1	0	90°
0	1	1	135°
1	0	0	180°
1	0	1	225°
1	1	0	270°
1	1	1	315°

Table 4: The external phase modulation offset settings of one D.D.S. channel.

For proper operation of the D.D.S. chip we also need to configure the two mode control registers illustrated in figure 1.8 and figure 1.9.

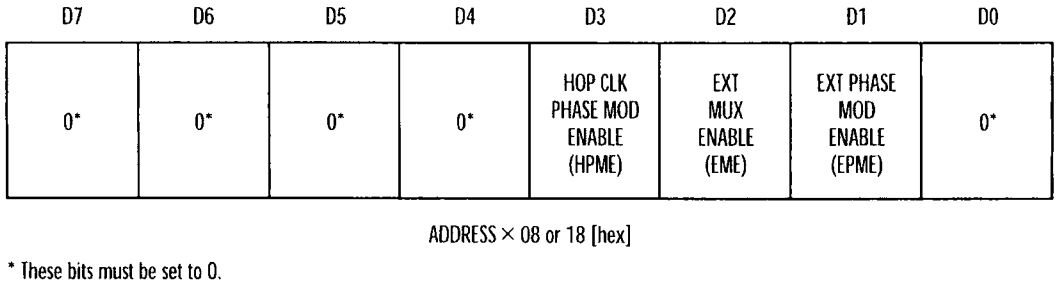

Figure 1.8: The configuration of the synchronous mode control (SMC) register.

The SMC word is pre-programmed in the ALTERA device and is: '00000010'

- Bit D7, D6, D5, D4, D0 must be set to '0'
- HPME : Hop Clock Phase Modulation Enable.
  1 : When internal phase modulation is wanted. PIRB is added to the phase accumulator once each time the HOP CLK signal is asserted
  0 : When internal phase modulation is unwanted.
- EME : External Multiplexer Enable.
  1 : The external multiplexer determines whether PIRA or PIRB will be used for the phase accumulation process.
  0 : The external multiplexer control is disabled, the signal on the EXT MUX inputs is ignored and the PIRA register will be used for the accumulation process.
- EPME : External Phase Modulation Enable.
  1: The PM EXT BITS are read and the corresponding phase offset is latched into the DDS each time the PM CLK is asserted.
  0 : When external phase modulation is unwanted. The PM EXT BITS are ignored.

The EPME bit of the SMC register is set to '1' in order to be able to apply external phase modulation for quadrature operation. In this mode the three PM EXT BITS per DDS are read and the corresponding phase offset is latched into the DDS each time the PM CLK is asserted. In order to operate in quadrature mode the phase difference between the two DDS functions must be 90° of which OUT* is lagging.

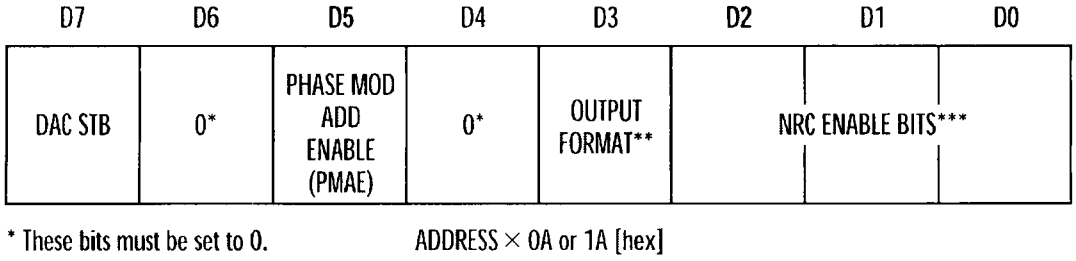

Figure 1.9: The configuration of the asynchronous mode control (AMC) register.

The AMC word is also pre-programmed in the ALTERA device and is: '00001110'

- Bit D6, D4 must be set to '0'
- DAC STB : DAC Strobe (delayed version of the system clock).
  1 : DAC Strobe inverted in relation to the system clock.
  0 : DAC Strobe not inverted in relation to the system clock.
- PMAE : Phase Modulation Add Eneable.
  Only used when PMAE bit of the SMC register is '1'. This means that the PMAE bit is not used in our case.
- OUTPUT FORMAT.
  1 : The output format is OFFSET BINARY
  0 : The output format is TWO's COMPLEMENT
- NRC ENABLE BITS.
  When the on chip noise reduction circuit is used, the umber of significant bits to be used from the DAC outputs must be programmed into the NRC ENABLE BITS. In our case 12 bit DAC's are used and therefore D2, D1, D0 = 110b or 5h.

The SMC and AMC registers are both initialized when the reset procedure is executed by the state machine.

In paragraph 1.1.4 we have seen the flow charts of the state machines, programmed in the EPLD. During the execution of the state machine, part of the frequency word are written in the different registers. Table 5 gives the exact address coding of the microprocessor interface of the DDS circuit.

DDS1 REGISTER ADDRESS (HEX)	DDS2 REGISTER ADDRESS (HEX)	FUNCTION
00	10	PIRA Bits 0-7 (LSB)
01	11	PIRA Bits 8-15
02	12	PIRA Bits 16-23
03	13	PIRA Bits 24-31 (MSB)
04	14	PIRB Bits 0-7 (LSB)
05	15	PIRB Bits 8-15
06	16	PIRB Bits 6-23
07	17	PIRB Bits 24-31 (MSB)
08	18	SMC
09	19	Reserved (not used)
0A	1A	AMC
0B	1B	Reserved (not used)
0C	1C	ARR
0D	1D	Reserved (not used)
0E	1E	AHC
0F	1F	Reserved (not used)

Table 5: D.D.S. Microprocessor interface address map

1.3. The D.A.C. and filtering output circuit.

As previously mentioned the DDS sends the amplitude information by means of 12-bits to the DAC inputs. The information is transmitted as TTL level signals.
The conversion of the 12-bits information from the D.D.S. into a real amplitude of a sine wave at a given phase is done by the D.A.C. The data sheet of the D.A.C. is given in annex 4.
The D.A.C. has a symmetric current output, which is converted to a voltage output by operational amplifiers. More details on this circuit can be found in chapter 3, where we can find the schematics and the calibration procedure of the circuit.
A standard 'Micro Circuits' filter with a cut-off frequency of 5MHz smoothes the signal and filters out the clock signal.
The output of the filter is then buffered by 3 operational amplifiers, providing 3 outputs of each channel in quadrature, on the front panel.

2. The characteristics.

Inputs :

Serial input A and B : TTL level serial data
Reset input : Open collector level reset signal.
When input is "1" the module will be reinitialized and the output frequency will be forced to 0 Hz.

Outputs :

Channel A OUT : 3 connectors (type : Lemo)
Channel A OUT* : 3 connectors (type : Lemo)
Channel B OUT : 3 connectors (type : Lemo)
Channel B OUT* : 3 connectors (type : Lemo)

The frequency range and resolution are set by jumpers as mentioned in paragraph 1.1.3.

Frequency range : DC – 1.048 MHz.
Frequency resolution : 1 Hz – 4 Hz
Frequency refresh rate : The GFAS send each 20us a new frequency word.
Voltage range : 0.1 V peak to 4 V peak.
Output impedance : 50 ohm
Relative "OUT-OUT*"
Phase error : < 0.1°

3. The calibration procedure.

The main part of the module is digital and does not need calibration. However there are two parts that need to be calibrated. The first part is the power supply for the analog components on the board, while the second part consists of adjusting the output amplitude and baseline of the circuit behind each DAC.

The power supplies

There are two power supplies on the boards a digital and analog one. The digital power supply is fixed at +5V and –5V. The analog power supply also needs to provide +5V and –5V but needs to be adjusted with certain accuracy.

- Adjust the +5V:
  Connect a voltmeter to the +5V power supply on the printed circuit board (i.e. pin 2 of RG1).
  Adjust the output voltage by means of potentiometer P9 on exactly +5V.
- Adjust the -5V:
  Connect a voltmeter to the -5V power supply on the printed circuit board (i.e. pin 3 of RG2).
  Adjust the output voltage by means of potentiometer P10 on exactly -5V.

The output circuits

The schematic of an output circuit is given in figure 1.10. The board contains four of these circuits and the calibration procedure is identical for all four of them with the only difference being the names of the components.

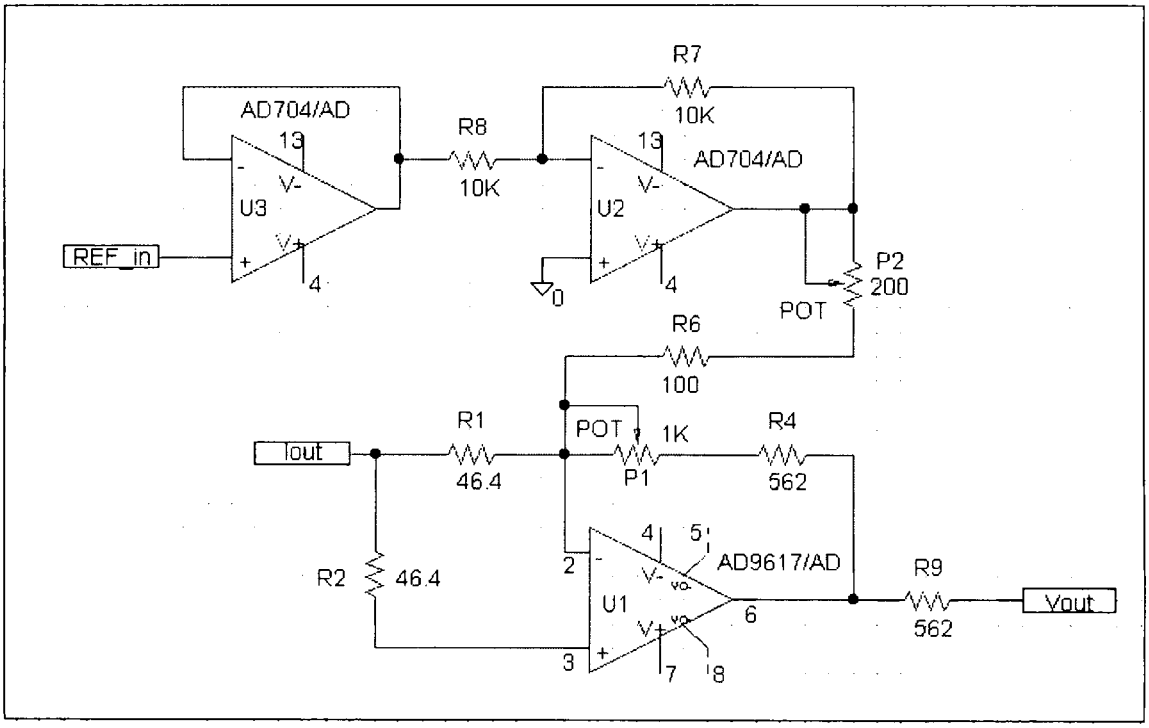

Figure 1.10: The DAC output circuit schematics.

The DAC has a current output that enters the schematic by means of the box called "Iout". This incoming current is converted into a voltage by means of two resistors, R1 and R2. The operational amplifier U1 amplifies the sum of, the input signal "Iout" and the output of U2.
Potentiometer P1 is used to adjust the amplitude of the output signal on "Vout".

The DAC provides a reference output signal on one of its pins. This reference signal is fed into the operational amplifiers U3 and U2, which act as buffers. The output of U2 is fed into U1 scaled by P2 and R6.
This part of the circuit is responsible for the baseline of the output voltage. By adjusting P2 one can change the base line.
This means that there are two adjustments per output channel to be made.

- Adjust the amplitude of the output signal:
  Make sure that the jumpers behind the operational amplifiers are placed in such a way that the signal on the front panel outputs is filtered.
  Switch the power supply on and perform a reset by pushing the front panel reset button.
  Force the output to oscillate with the internally pre-programmed frequency by means of pushing the front panel "Force Output Frequency" button.
  Connect an oscilloscope to output "OUT" of channel A on the front panel.
  Adjust, by means of turning potentiometer P1, the amplitude of the sine wave signal to the desired value, which is normally 2V peak when the output is not terminated, and 1V peak when the output is terminated by 50 ohm.
- Adjust the baseline of the output signal:
  After having adjusted the amplitude of the output signal one can adjust the baseline (not before!).
  The signal is still present on the outputs, if not repeat the first part of the previous procedure.
  Connect the oscilloscope again to the output "OUT" of channel A. Make sure that the input of the oscilloscope is set to "DC". Adjust now, by means of turning potentiometer P2, the baseline of the signal. In other words, make the output signal oscillate around the zero.

Repeat this procedure for the outputs "OUT*" of channel A , "OUT" and "OUT*" of channel B.

This completes the calibration of the module, it should now be ready for use.

4. The D.Q.D.D.S. as synchrotron frequency programmer.

Initially this module was designed to be used as a so-called "Synchrotron Frequency Programmer" for the P.S. Booster longitudinal mode analyzer system.
The module is build as a multi purpose module, but can easily be used as a synchrotron frequency programmer. Here I will briefly describe how the module can be used in the mode analyzer system.
In the notes of reference [1] and [2] is described how the mode analyzer system works, and which part of the old system is being replaced by the new D.Q.D.D.S.
The quadrature pair output of the D.Q.D.D.S. is fed into the FS and FS* inputs of the mode analyzer module [3]. The module is now used to generate a calculated synchrotron frequency, which changes constantly throughout the acceleration cycle.
The synchrotron frequency function is generated by a GFAS, which serial output is connected to the serial input of the D.Q.D.D.S.
An application that runs on a workstation acquires the cavity voltages, the phase difference between the cavities and the magnetic field from the machine, with a time resolution of 1 ms. Subsequently it will calculate for each millisecond the synchrotron frequency which will be stored in the GFA table.
As soon as the next accelerating cycle, concerned, is executed the GFA will generate a serial bit stream of synchrotron frequency values which is send to the D.Q.D.D.S. module.
As previously mentioned the module will now generate this synchrotron frequency as a quadrature pair that is used by the mode analyzer system.

Acknowledgements.

I like to thank:

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- W. Heinze of the C.O. group who provided me some information about the serial to parallel interface, used in the GFAS DAC module.
- N. Lopez who made the schematic and the printed circuit board drawings.

References.

1. Electronics for the Longitudinal Active Damping System for the CERN P.S. Booster.
   B. Kriegbaum and F. Pedersen
   CERN / PS / BR / 77-9
2. A new Synchrotron Frequency Programmer for the CERN P.S. Booster.
   R. R. Steerenberg
   PS / OP / NOTE 95-52
3. Mode Analyzer
   F. Pedersen
   PS / BR / NOTE 77-13

Annex 1.

Schematics of the Dual Quadruature Direct Digital Synthesizer module.

The complete schematic is an A1 size drawing and is therefore not included in all notes.

A copy can be obtained at the author.

Annex 2.

The ALTERA AHDL program listing with comments.

```
TITLE       "Serial GFA to parallel DDS interface version 1.8";


% Description of RESET procedure :
  1. The phase increment registers are cleaned by writing data to the two ARR
     registers of both DDS1 and DDS2. A HOPCLK is generated in order to
     activate the reset of these ARR registers.
  2. The AMC registers of both DDS1 and DDS2 are filled with the asynchronous
     mode control word, which is described in detail in the Q2334 dual direct
     digital synthesizer data sheet of Qualcomm on page 13.
  3. The SMC registers of Both DDS1 and DDS2 are filled with the synchronous
     mode control word, which is described in detail in the Q2334 dual direct
     digital synthesizer data sheet of Qualcomm on page 12.
  4. A HOPCLK is generated in order to activate the AMC and SMC data, so that
     the DDS knows how it has to operate.
  5. The PIR B registers of both DDS1 and DDS2 are filled with 0000h.
     A HOPCLK is generated in order to validate the data in the PIR B
     registers. This is done in order to avoid unwanted internal phase
     modulation by means of the stored data in the PIR B registers.
  6. The PIR A resisters of both DDS1 and DDS2 are filled with 0000h.
     A HOPCLK is generated in order to validate the data in the PIR A register.
     This way the output frequency after reset will be 0Hz for both outputs.
  7. A PMXCLK is generated in order to fix a 90 degree phase shift between the
     two outputs, of which "OUT" (DDS1) is lagging 90 degrees in respect to
     "OUT*" (DDS2). This gives a clock puls on PMCLOCK and MUXCLOCK of the DDS
     chip simultanously and enables quadrature outputs.
%

% Description of the OPERATION procedure :
  1. The PIR A registers of both DDS1 and DDS2 are filled with the data coming
     from the gain selector (databus GD) and with zeros for the other bits.
  2. A HOPCLK is generated in order to activate the data in PIR A.
%

% Modifications made since earlier versions :
  1. The test word is internally defined and not changeble from the outside as
     before. The test input jumpers/pins can not be used anymore!!!
%

% Additional information :

%


CONSTANT GAIN1    = B"000";              % 0 -   65 KHz. %
CONSTANT GAIN2    = B"001";              % 0 -  131 KHz. %
CONSTANT GAIN3    = B"010";              % 0 -  262 KHz. %
CONSTANT GAIN4    = B"011";              % 0 -  524 KHz. %
CONSTANT GAIN5    = B"100";              % 0 - 1048 KHz. %
CONSTANT SMCWORD  = B"00000010";         % for details see Q2334 data sheet %
CONSTANT AMCWORD  = B"00001110";         % for details see Q2334 data sheet %
CONSTANT TSTWORD  = B"1111111111111111"; % max. frequency for selected gain %


FUNCTION JKFF   (j, k, clk, clrn, prn)
  RETURNS       (q);
FUNCTION 74164 (clk, clrn, a, b)
  RETURNS       (qa, qb, qc, qd, qe, qf, qg, qh);
FUNCTION 74273 (clrn, clk, d[8..1])
  RETURNS       (q[8..1]);

SUBDESIGN gfas2dds
  (
  ODAT                    : INPUT;  % Data from ser/par GAL pin 17 %
  OCLK                    : INPUT;  % CLOCK from ser/par GAL PIN 16 %
  OLD                     : INPUT;  % pos. edge for Load Data in BUFF1/2 %
  GC[2..0]                : INPUT;  % 3 bit Gain Control set by jumpers %
  RESET_BUTTON            : INPUT;  % Reset button on module front panel %
  RESET_CONNECTOR : INPUT;  % Reset connector on the module front panel %
  POWERUP                 : INPUT;  % Reset after power up %
  TEST_BUTTON             : INPUT;  % Test button on module front panel %
  CLOCK                   : INPUT;  % DIGITAL CLOCK 4 MHZ. %
  STRT_OP_PROC            : INPUT;  % Startpuls for OPERATION procedure %
  STRT_RST_PROC           : INPUT;  % Startpuls for RESET procedure %
  STRT_TST_PROC           : INPUT;  % Startpuls for TEST procedure %
  RESET_OUT               : OUTPUT; % Reset output for strtrstproc logic %
  LED[5..1]               : OUTPUT; % 5 bit LED range/gain indication %
  DDDS[7..0]              : OUTPUT; % 8 bit Databus for DDS %
  ADDS[4..0]              : OUTPUT; % 5 bit Addressbus for DDS %
  HOPCLK          : OUTPUT; % HOPCLK in order to activate DDS data %
  PMXCLK          : OUTPUT; % PM & MUX clock for reset procedure %
  WRITE                   : OUTPUT; % WRITE puls for latching data into DDS %
  )


VARIABLE
  SHFT1, SHFT2    : 74164; % shift reg. for serial data from GFAS%
  BUFF1, BUFF2    : 74273; % buffer for storing parallel data from SHFT1/2%
  COUNTFF         : JKFF;           % Counter for bit machine %
  FD[15..0]       : NODE;           % Databus from BUFF's to GAIN_MUX%
  GD[19..0]       : NODE;           % Databus behind gain mux%
  START_COUNT     : NODE;           % Combination for start counter condition %
  VALID_COUNT     : NODE;           % "1" when bit machine counter is enabled %
  END_COUNT       : NODE;           % Condition for stop bit machine counter %
  RESET           : NODE;           % "1" when module is in RESET mode %
  TEST            : NODE;           % "1" when module is in TEST mode %
```

```
OPERATION       : NODE;          % "1" when module is in OPERATION mode %
WR              : NODE;          % Internal WRITE puls %

COUNT : MACHINE OF BITS (BIT_F,BIT_E,BIT_D,BIT_C,BIT_B,BIT_A)
        WITH STATES
          (                 %        RESET          :    OPERATIONAL     %
          S0  = B"000000", % 00h => 0Ch ARR DDS1   : byte1 PIRA DDS1    %
          S1  = B"000001",
          S2  = B"000010", % 00h => 1Ch ARR DDS2   : byte1 PIRA DDS2    %
          S3  = B"000011", % HOPCLK ARR active     :                     %
          S4  = B"000100", % AMC => 0Ah AMC DDS1   : byte2 PIRA DDS1    %
          S5  = B"000101",
          S6  = B"000110", % AMC => 1Ah AMC DDS2   : byte2 PIRA DDS2    %
          S7  = B"000111",
          S8  = B"001000", % SMC => 08h SMC DDS1   : byte3 PIRA DDS1    %
          S9  = B"001001",
          S10 = B"001010", % SMC => 18h SMC DDS2   : byte3 PIRA DDS2    %
          S11 = B"001011", % HOPCLK AMC/SMC active :                     %
          S12 = B"001100", % byte1 PIRB DDS1       : byte4 PIRA DSS1    %
          S13 = B"001101",
          S14 = B"001110", % byte1 PIRB DDS2       : byte4 PIRA DDS2    %
          S15 = B"001111", %                       : HOPCLK data active %
          S16 = B"010000", % byte2 PIRB DDS1       :                     %
          S17 = B"010001",
          S18 = B"010010", % byte2 PIRB DDS2       :                     %
          S19 = B"010011",
          S20 = B"010100", % byte3 PIRB DDS1       :                     %
          S21 = B"010101",
          S22 = B"010110", % byte3 PIRB DDS2       :                     %
          S23 = B"010111",
          S24 = B"011000", % byte4 PIRB DDS1       :                     %
          S25 = B"011001",
          S26 = B"011010", % byte4 PIRB DDS2       :                     %
          S27 = B"011011", % HOPCLK data valid     :                     %
          S28 = B"011100", % byte1 PIRA DDS1       :                     %
          S29 = B"011101",
          S30 = B"011110", % byte1 PIRA DDS2       :                     %
          S31 = B"011111",
          S32 = B"100000", % byte2 PIRA DDS1       :                     %
          S33 = B"100001",
          S34 = B"100010", % byte2 PIRA DDS2       :                     %
          S35 = B"100011",
          S36 = B"100100", % byte3 PIRA DDS1       :                     %
          S37 = B"100101",
          S38 = B"100110", % byte3 PIRA DDS2       :                     %
          S39 = B"100111",
          S40 = B"101000", % byte4 PIRA DDS1       :                     %
          S41 = B"101001",
          S42 = B"101010", % byte4 PIRA DDS2       :                     %
          S43 = B"101011", % HOPCLK data active    :                     %
          S44 = B"101100"  % PMXCLK quadrature     :                     %
          );


BEGIN

  %*************************************************************************
  *              Declaration of the possible functional modes              *
  *************************************************************************%
  RESET     = POWERUP # RESET_BUTTON # RESET_CONNECTOR;      % Reset mode      %
  TEST      = TEST_BUTTON & !RESET;                  % Test mode       %
  OPERATION = !RESET & !TEST;                                % Operation mode  %


  %*************************************************************************
  *                  Connections on SHFT1 and SHFT2                        *
  *************************************************************************%
  SHFT1.a = ODAT;
  SHFT2.a = SHFT1.qh;
  SHFT1.(b, clrn) = VCC;
  SHFT2.(b, clrn) = VCC;
  SHFT1.clk = OCLK;
  SHFT2.clk = OCLK;


  %*************************************************************************
  *                  Connections on BUFF1 and BUFF2                        *
  *************************************************************************%
  BUFF1.d[8..1] = SHFT1.(qh, qg, qf, qe, qd, qc, qb, qa);
  BUFF2.d[8..1] = SHFT2.(qh, qg, qf, qe, qd, qc, qb, qa);
  BUFF1.clk  = OLD;
  BUFF2.clk  = OLD;
  BUFF1.clrn = VCC;
  BUFF2.clrn = VCC;


  %*************************************************************************
  *      Databus connections between BUFF1/2, TSTWORD and GAIN MUX         *
  *************************************************************************%
  IF TEST
    THEN FD[15..0] = TSTWORD;                % fill MSByte with test word %
      ELSE FD[15..8] = BUFF2.(q[8..1]);              % MSByte of GFA data %
           FD[7..0]  = BUFF1.(q[8..1]);              % LSByte of GFA data %
  END IF;
```

```
%************************************************************************
*                      GAIN_SELECTOR logic description                  *
************************************************************************%
CASE GC[2..0] IS
   WHEN GAIN1 =>               % 0 -   65 KHz. %
       GD[15..0]  = FD[15..0];
       GD[19..16] = GND;
       LED[5..2]  = GND;
       LED1       = VCC;  % Range (2^8 - 2^23) LED on module front %
   WHEN GAIN2  =>              % 0 -  131 KHz. %
       GD[0]      = GND;
       GD[16..1]  = FD[15..0];
       GD[19..17] = GND;
       LED[5..3]  = GND;
       LED2       = VCC;  % Range (2^9 - 2^24) LED on module front %
       LED1       = GND;
   WHEN GAIN3  =>              % 0 -  262 KHz. %
       GD[1..0]   = GND;
       GD[17..2]  = FD[15..0];
       GD[19..18] = GND;
       LED[5..4]  = GND;
       LED3       = VCC;  % Range (2^10 - 2^25) LED on module front %
       LED[2..1]  = GND;
   WHEN GAIN4  =>              % 0 -  524 KHz. %
       GD[2..0]   = GND;
       GD[18..3]  = FD[15..0];
       GD[19]     = GND;
       LED5       = GND;
       LED4       = VCC;  % Range (2^11 - 2^26) LED on module front %
       LED[3..1]  = GND;
   WHEN GAIN5  =>              % 0 - 1048 KHz. %
       GD[3..0]   = GND;
       GD[19..4]  = FD[15..0];
       LED5       = VCC;  % Range (2^12 - 2^27) LED on module front %
       LED[4..1]  = GND;
END CASE;


%************************************************************************
*      Address, write puls, clock generation and data distribution.     *
************************************************************************%
START_COUNT = (STRT_RST_PROC # STRT_TST_PROC # STRT_OP_PROC);

COUNTFF.prn  = VCC;
COUNTFF.clrn = VCC;
COUNTFF.clk  = CLOCK;
COUNTFF.j    = START_COUNT;
COUNTFF.k    = END_COUNT;
```

```
VALID_COUNT  = COUNTFF.q;                % "1" when counting is enabled %

COUNT.clk = CLOCK;
COUNT.reset = POWERUP;

CASE (COUNT) IS

  WHEN S0 => % 000000 %
      IF (RESET & VALID_COUNT)
      % 00h => 0Ch : 00h => ARR of DDS1 ==> Reset accumulation of DDS1 %
        THEN ADDS[4..0] = (GND,VCC,VCC,GND,GND);
             DDDS[7..0] = GND;
             !WR        = GND;
             COUNT      = S1;
        ELSIF ((TEST # OPERATION) & VALID_COUNT)
        % 00h => 00h : byte1 => PIRA DDS1 %
          THEN ADDS[4..0] = GND;
               DDDS[7..0] = GND;
               !WR        = GND;
               COUNT      = S1;
           ELSE !WR   = VCC;
                COUNT = S0;
      END IF;

  WHEN S1 => % 000001 %
      IF (RESET & VALID_COUNT)
        THEN ADDS[4..0] = (GND,VCC,VCC,GND,GND);
             DDDS[7..0] = GND;
             !WR        = VCC;
             COUNT      = S2;
        ELSIF ((TEST # OPERATION) & VALID_COUNT)
          THEN ADDS[4..0] = GND;
               DDDS[7..0] = GND;
               !WR        = VCC;
               COUNT      = S2;
           ELSE !WR   = VCC;
                COUNT = S0;
      END IF;

  WHEN S2 => % 000010 %
      IF (RESET & VALID_COUNT)
      % 00h => 1Ch : 00h => ARR of DDS2 ==> Reset accumulation of DDS2 %
        THEN ADDS[4..0] = (VCC,VCC,VCC,GND,GND);
             DDDS[7..0] = GND;
             !WR        = GND;
             COUNT      = S3;
        ELSIF ((TEST # OPERATION) & VALID_COUNT)
        % 00h => 10h : byte1 => PIRA DDS2 %
```

```
        THEN ADDS[4..0] = (VCC,GND,GND,GND,GND);
             DDDS[7..0] = GND;
             !WR        = GND;
             COUNT      = S3;
         ELSE !WR   = VCC;
              COUNT = S0;
    END IF;

WHEN S3 => % 000011 %
    IF (RESET & VALID_COUNT)
    % Generate HOPCLK ==> Activate reset of ARR in both DDS1 and DDS2 %
      THEN ADDS[4..0] = (VCC,VCC,VCC,GND,GND);
           DDDS[7..0] = GND;
           !WR        = VCC;
           HOPCLK     = !CLOCK;
           COUNT      = S4;
       ELSIF ((TEST # OPERATION) & VALID_COUNT)
         THEN ADDS[4..0] = (VCC,GND,GND,GND,GND);
              !WR        = VCC;
              COUNT      = S4;
          ELSE !WR   = VCC;
               COUNT = S0;
    END IF;

WHEN S4 => % 000100 %
    IF (RESET & VALID_COUNT)
    % AMC => 0Ah : AMC WORD => DDS1 %
      THEN ADDS[4..0] = (GND,VCC,GND,VCC,GND);
           DDDS[7..0] = AMCWORD;
           !WR        = GND;
           COUNT      = S5;
       ELSIF ((TEST # OPERATION) & VALID_COUNT)
       % GD[7..0] => 01h : byte2 => PIRA DDS1 %
         THEN ADDS[4..0] = (GND,GND,GND,GND,VCC);
              DDDS[7..0] = GD[7..0];
              !WR        = GND;
              COUNT      = S5;
          ELSE !WR   = VCC;
               COUNT = S0;
    END IF;

WHEN S5 => % 000101 %
    IF (RESET & VALID_COUNT)
      THEN ADDS[4..0] = (GND,VCC,GND,VCC,GND);
           DDDS[7..0] = AMCWORD;
           !WR        = VCC;
           COUNT      = S6;
       ELSIF ((TEST # OPERATION) & VALID_COUNT)
```

```
        THEN ADDS[4..0] = (GND,GND,GND,GND,VCC);
             DDDS[7..0] = GD[7..0];
             !WR        = VCC;
             COUNT      = S6;
         ELSE !WR   = VCC;
              COUNT = S0;
    END IF;

WHEN S6 => % 000110 %
    IF (RESET & VALID_COUNT)
    % AMC => 1Ah : AMC WORD => DDS 2 %
      THEN ADDS[4..0] = (VCC,VCC,GND,VCC,GND);
           DDDS[7..0] = AMCWORD;
           !WR        = GND;
           COUNT      = S7;
       ELSIF ((TEST # OPERATION) & VALID_COUNT)
       % GD[7..0] => 11h : byte2 => PIRA DDS2 %
         THEN ADDS[4..0] = (VCC,GND,GND,GND,VCC);
              DDDS[7..0] = GD[7..0];
              !WR        = GND;
              COUNT      = S7;
          ELSE !WR   = VCC;
               COUNT = S0;
    END IF;

WHEN S7 => % 000111 %
    IF (RESET & VALID_COUNT)
      THEN ADDS[4..0] = (VCC,VCC,GND,VCC,GND);
           DDDS[7..0] = AMCWORD;
           !WR        = VCC;
           COUNT      = S8;
       ELSIF ((TEST # OPERATION) & VALID_COUNT)
         THEN ADDS[4..0] = (VCC,GND,GND,GND,VCC);
              DDDS[7..0] = GD[7..0];
              !WR        = VCC;
              COUNT      = S8;
          ELSE !WR   = VCC;
               COUNT = S0;
    END IF;

WHEN S8 => % 001000 %
    IF (RESET & VALID_COUNT)
    % SMC => 08h : SMC WORD => DDS1 %
      THEN ADDS[4..0] = (GND,VCC,GND,GND,GND);
           DDDS[7..0] = SMCWORD;
           !WR        = GND;
           COUNT      = S9;
       ELSIF ((TEST # OPERATION) & VALID_COUNT)
```

```
        % GD[15..8] => 02h : byte3 => PIRA DDS1 %
          THEN ADDS[4..0] = (GND,GND,GND,VCC,GND);
               DDDS[7..0] = GD[15..8];
               !WR        = GND;
               COUNT      = S9;
           ELSE !WR   = VCC;
                COUNT = S0;
    END IF;

WHEN S9 => % 001001 %
    IF (RESET & VALID_COUNT)
      THEN ADDS[4..0] = (GND,VCC,GND,GND,GND);
           DDDS[7..0] = SMCWORD;
           !WR        = VCC;
           COUNT      = S10;
        ELSIF ((TEST # OPERATION) & VALID_COUNT)
          THEN !WR        = VCC;
               ADDS[4..0] = (GND,GND,GND,VCC,GND);
               DDDS[7..0] = GD[15..8];
               COUNT      = S10;
           ELSE !WR   = VCC;
                COUNT = S0;
    END IF;

WHEN S10 => % 001010 %
    IF (RESET & VALID_COUNT)
    % SMC => 18h : SMC WORD => DDS2 %
      THEN ADDS[4..0] = (VCC,VCC,GND,GND,GND);
           DDDS[7..0] = SMCWORD;
           !WR        = GND;
           COUNT      = S11;
        ELSIF ((TEST # OPERATION) & VALID_COUNT)
        % GD[15..8] => 12h : byte3 => PIRA DDS2 %
          THEN ADDS[4..0] = (VCC,GND,GND,VCC,GND);
               DDDS[7..0] = GD[15..8];
               !WR        = GND;
               COUNT      = S11;
           ELSE !WR   = VCC;
                COUNT = S0;
    END IF;

WHEN S11 => % 001011 %
    IF (RESET & VALID_COUNT)
    % Generate HOPCLK ==> Activate AMC and SMC words in both DDS1 and DDS2 %
      THEN ADDS[4..0] = (VCC,VCC,GND,GND,GND);
           DDDS[7..0] = SMCWORD;
           !WR        = VCC;
           HOPCLK     = !CLOCK;
           COUNT      = S12;
        ELSIF ((TEST # OPERATION) & VALID_COUNT)
          THEN ADDS[4..0] = (VCC,GND,GND,VCC,GND);
               DDDS[7..0] = GD[15..8];
               !WR        = VCC;
               COUNT      = S12;
           ELSE !WR   = VCC;
                COUNT = S0;
    END IF;

WHEN S12 => % 001100 %
    IF (RESET & VALID_COUNT)
    % 00h => 04h : 00h => byte1 PIRB DDS1 %
      THEN ADDS[4..0] = (GND,GND,VCC,GND,GND);
           DDDS[7..0] = GND;
           !WR        = GND;
           COUNT      = S13;
        ELSIF ((TEST # OPERATION) & VALID_COUNT)
        % GD[19..16] => 03h : byte4 => PIRA DDS1 %
          THEN ADDS[4..0] = (GND,GND,GND,VCC,VCC);
               DDDS[7..4] = GND;
               DDDS[3..0] = GD[19..16];
               !WR        = GND;
               COUNT      = S13;
           ELSE !WR   = VCC;
                COUNT = S0;
    END IF;

WHEN S13 => % 001101 %
    IF (RESET & VALID_COUNT)
      THEN ADDS[4..0] = (GND,GND,VCC,GND,GND);
           DDDS[7..0] = GND;
           !WR        = VCC;
           COUNT      = S14;
        ELSIF ((TEST # OPERATION) & VALID_COUNT)
          THEN ADDS[4..0] = (GND,GND,GND,VCC,VCC);
               DDDS[7..4] = GND;
               DDDS[3..0] = GD[19..16];
               !WR        = VCC;
               COUNT      = S14;
           ELSE !WR   = VCC;
                COUNT = S0;
    END IF;

WHEN S14 => % 001110 %
    IF (RESET & VALID_COUNT)
    % 00h => 14h : 00h => byte1 PIRB DDS2 %
      THEN ADDS[4..0] = (VCC,GND,VCC,GND,GND);
```

```
            DDDS[7..0] = GND;
            !WR        = GND;
            COUNT      = S15;
        ELSIF ((TEST # OPERATION) & VALID_COUNT)
        % GD[19..16] => 13h : byte4 PIRA DDS2 %
          THEN ADDS[4..0] = (VCC,GND,GND,VCC,VCC);
               DDDS[7..4] = GND;
               DDDS[3..0] = GD[19..16];
               !WR        = GND;
               COUNT      = S15;
             ELSE !WR   = VCC;
                  COUNT = S0;
    END IF;

WHEN S15 => % 001111 %
    IF (RESET & VALID_COUNT)
      THEN ADDS[4..0] = (VCC,GND,VCC,GND,GND);
           DDDS[7..0] = GND;
           !WR        = VCC;
           COUNT      = S16;
      ELSIF ((TEST # OPERATION) & VALID_COUNT)
        THEN ADDS[4..0] = (VCC,GND,GND,VCC,VCC);
             DDDS[7..4] = GND;
             DDDS[3..0] = GD[19..16];
             !WR        = VCC;
             HOPCLK     = !CLOCK;
             COUNT      = S0;
             END_COUNT  = VCC;
           ELSE !WR   = VCC;
                COUNT = S0;
    END IF;

WHEN S16 => % 010000 %
    IF (RESET & VALID_COUNT)
    % 00h => 05h : byte2 PIRB DDS1 %
      THEN ADDS[4..0] = (GND,GND,VCC,GND,VCC);
           DDDS[7..0] = GND;
           !WR        = GND;
           COUNT      = S17;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S17 => % 010001 %
    IF (RESET & VALID_COUNT)
      THEN ADDS[4..0] = (GND,GND,VCC,GND,VCC);
           DDDS[7..0] = GND;
           !WR        = VCC;
```

```
           COUNT      = S18;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S18 => % 010010 %
    IF (RESET & VALID_COUNT)
    % 00h => 15h : byte2 PIRB DDS2 %
      THEN ADDS[4..0] = (VCC,GND,VCC,GND,VCC);
           DDDS[7..0] = GND;
           !WR        = GND;
           COUNT      = S19;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S19 => % 010011 %
    IF (RESET & VALID_COUNT)
      THEN ADDS[4..0] = (VCC,GND,VCC,GND,VCC);
           DDDS[7..0] = GND;
           !WR        = VCC;
           COUNT      = S20;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S20 => % 010100 %
    IF (RESET & VALID_COUNT)
    % 00h => 06h : byte3 PIRB DDS1 %
      THEN ADDS[4..0] = (GND,GND,VCC,VCC,GND);
           DDDS[7..0] = GND;
           !WR        = GND;
           COUNT      = S21;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S21 => % 010101 %
    IF (RESET & VALID_COUNT)
      THEN ADDS[4..0] = (GND,GND,VCC,VCC,GND);
           DDDS[7..0] = GND;
           !WR        = VCC;
           COUNT      = S22;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S22 => % 010110 %
```

```
    IF (RESET & VALID_COUNT)
    % 00h => 16h : byte3 PIRB DDS2 %
      THEN ADDS[4..0] = (VCC,GND,VCC,VCC,GND);
           DDDS[7..0] = GND;
           !WR        = GND;
           COUNT      = S23;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S23 => % 010111 %
    IF (RESET & VALID_COUNT)
      THEN ADDS[4..0] = (VCC,GND,VCC,VCC,GND);
           DDDS[7..0] = GND;
           !WR        = VCC;
           COUNT      = S24;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S24 => % 011000 %
    IF (RESET & VALID_COUNT)
    % 00h => 07h : byte4 PIRB DDS1 %
      THEN ADDS[4..0] = (GND,GND,VCC,VCC,VCC);
           DDDS[7..0] = GND;
           !WR        = GND;
           COUNT      = S25;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S25 => % 011001 %
    IF (RESET & VALID_COUNT)
      THEN ADDS[4..0] = (GND,GND,VCC,VCC,VCC);
           DDDS[7..0] = GND;
           !WR        = VCC;
           COUNT      = S26;
       ELSE !WR   = VCC;
            COUNT = S0;
    END IF;

WHEN S26 => % 011010 %
    IF (RESET & VALID_COUNT)
    % 00h => 17h : byte4 PIRB DDS2 %
      THEN ADDS[4..0] = (VCC,GND,VCC,VCC,VCC);
           DDDS[7..0] = GND;
           !WR        = GND;
           COUNT      = S27;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S27 => % 011011 %
    IF (RESET & VALID_COUNT)
      THEN ADDS[4..0] = (VCC,GND,VCC,VCC,GND);
           DDDS[7..0] = GND;
           !WR        = VCC;
           HOPCLK     = !CLOCK;
           COUNT      = S28;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S28 => % 011100 %
    IF (RESET & VALID_COUNT)
    % 00h => 00h : byte1 PIRA DDS1 %
      THEN ADDS[4..0] = GND;
           DDDS[7..0] = GND;
           !WR        = GND;
           COUNT      = S29;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S29 => % 011101 %
    IF (RESET & VALID_COUNT)
      THEN ADDS[4..0] = GND;
           DDDS[7..0] = GND;
           !WR        = VCC;
           COUNT      = S30;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S30 => % 011110 %
    IF (RESET & VALID_COUNT)
    % 00h => 10h : byte1 PIRA DDS2 %
      THEN ADDS[4..0] = (VCC,GND,GND,GND,GND);
           DDDS[7..0] = GND;
           !WR        = GND;
           COUNT      = S31;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S31 => % 0111111 %
```

```
    IF (RESET & VALID_COUNT)
      THEN ADDS[4..0] = (VCC,GND,GND,GND,GND);
           DDDS[7..0] = GND;
           !WR        = VCC;
           COUNT      = S32;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S32 => % 100000 %
    IF (RESET & VALID_COUNT)
    % 00h => 01h : byte2 PIRA DDS1 %
      THEN ADDS[4..0] = (GND,GND,GND,GND,VCC);
           DDDS[7..0] = GND;
           !WR        = GND;
           COUNT      = S33;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S33 => % 100001 %
    IF (RESET & VALID_COUNT)
      THEN ADDS[4..0] = (GND,GND,GND,GND,VCC);
           DDDS[7..0] = GND;
           !WR        = VCC;
           COUNT      = S34;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S34 => % 100010 %
    IF (RESET & VALID_COUNT)
    % 00h = 11h : byte2 PIRA DDS2 %
      THEN ADDS[4..0] = (VCC,GND,GND,GND,VCC);
           DDDS[7..0] = GND;
           !WR        = GND;
           COUNT      = S35;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S35 => % 100011 %
    IF (RESET & VALID_COUNT)
      THEN ADDS[4..0] = (VCC,GND,GND,GND,VCC);
           DDDS[7..0] = GND;
           !WR        = VCC;
           COUNT      = S36;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S36 => % 100100 %
    IF (RESET & VALID_COUNT)
    % 00h => 02h : byte3 PIRA DDS1 %
      THEN ADDS[4..0] = (GND,GND,GND,VCC,GND);
           DDDS[7..0] = GND;
           !WR        = GND;
           COUNT      = S37;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S37 => % 100101 %
    IF (RESET & VALID_COUNT)
      THEN ADDS[4..0] = (GND,GND,GND,VCC,GND);
           DDDS[7..0] = GND;
           !WR        = VCC;
           COUNT      = S38;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S38 => % 100110 %
    IF (RESET & VALID_COUNT)
    % 00h => 12h : byte3 PIRA DDS2 %
      THEN ADDS[4..0] = (VCC,GND,GND,VCC,GND);
           DDDS[7..0] = GND;
           !WR        = GND;
           COUNT      = S39;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S39 => % 100111 %
    IF (RESET & VALID_COUNT)
      THEN ADDS[4..0] = (VCC,GND,GND,VCC,GND);
           DDDS[7..0] = GND;
           !WR        = VCC;
           COUNT      = S40;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S40 => % 101000 %
    IF (RESET & VALID_COUNT)
    % 00h => 13h : byte4 PIRA DDS1 %
```

```
      THEN ADDS[4..0] = (GND,GND,GND,VCC,VCC);
           DDDS[7..0] = GND;
           !WR        = GND;
           COUNT      = S41;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S41 => % 101001 %
    IF (RESET & VALID_COUNT)
      THEN ADDS[4..0] = (GND,GND,GND,VCC,VCC);
           DDDS[7..0] = GND;
           !WR        = VCC;
           COUNT      = S42;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S42 => % 101010 %
    IF (RESET & VALID_COUNT)
    % 00h => 13h : byte4 PIRA DDS2 %
      THEN ADDS[4..0] = (VCC,GND,GND,VCC,VCC);
           DDDS[7..0] = GND;
           !WR        = GND;
           COUNT      = S43;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S43 => % 101011 %
    IF (RESET & VALID_COUNT)
      THEN ADDS[4..0] = (VCC,GND,GND,VCC,VCC);
           DDDS[7..0] = GND;
           !WR        = VCC;
           HOPCLK     = !CLOCK;
           COUNT      = S44;
        ELSE !WR   = VCC;
             COUNT = S0;
    END IF;

WHEN S44 => % 101100 %
    IF (RESET & VALID_COUNT)
    % Generate PMXCLOCK in order to make quadrature outputs %
      THEN ADDS[4..0] = GND;
           DDDS[7..0] = GND;
           !WR        = VCC;
           PMXCLK     = !CLOCK;
           END_COUNT  = VCC;
                COUNT      = S0;
             ELSE !WR   = VCC;
                  COUNT = S0;
        END IF;

  END CASE;

  %*************************************************************************
  *              Connection of internal nodes to output pins              *
  *************************************************************************%
  RESET_OUT = RESET;
  WRITE = !WR;                    % Connect WR node to WRITE output pin %

END;
```

Q2334

DUAL DIRECT DIGITAL SYNTHESIZER

FEATURES

- Two Complete Direct Digital Synthesizer Functions On-chip
- Processor Interface for Control of Phase and Frequency
- Patented Algorithmic Sine Lookup Function
- Patented Noise Reduction Circuit
- Synchronous PSK and FSK Modulation Inputs
- Phase Resolution: 0.00000008° Using Processor-controlled Phase Adjustment
- Double Buffered Registers Allow Synchronous, Phase Coherent Frequency Change
- Simple External Multiplex Control for Binary Frequency Shift Keying (BFSK) Modulation
- Low Power: 667 mW Maximum at 50 MHz Clock Frequency per DDS
- Evaluation Board Available: Q0310

APPLICATIONS

- Spread Spectrum Modulators
- Quadrature Oscillators
- Programmable Frequency Synthesizers
- Satellite Receivers
- Cellular Base Stations
- Magnetic Resonance Imaging (MRI)
- VXI-based ATE
- SONAR/RADAR
- Paging Systems
- High Performance Test Equipment
- Digital Radios and Modems
- HF Transceivers
- Local Oscillator Generation for VSAT, DBS, and GPS Applications

CONTENTS

INTRODUCTION 4-3

GENERAL DESCRIPTION 4-3

INTERNAL ARCHITECTURE 4-4
- Processor Interface 4-4
- Phase Increment Registers (PIRs) 4-4
- Mode Control Registers 4-4
  - Synchronous Mode Control (SMC) Register 4-4
  - Asynchronous Mode Control (AMC) Register 4-5
  - Accumulator Reset Register (ARR) 4-7
  - Asynchronous Hop Clock (AHC) 4-7
- Phase Increment Multiplexer Control 4-7
- Phase Accumulator 4-8
- Phase Modulation Control 4-8
- Sine Lookup Function 4-8
- Noise Reduction Circuit (NRC) 4-8

INPUT/OUTPUT SIGNALS 4-9
- Signals Common for Both DDSs 4-9
- Signals Independent for each DDS 4-10

MODES OF OPERATION 4-12
- Basic Synthesizer Mode 4-12
- Phase Modulation Mode 4-12
  - Internal Phase Modulation 4-12
  - External Phase Modulation 4-13
- Binary Frequency Shift Keying (BFSK) Modulation Mode 4-13
- Minimum Shift Keying (MSK) Modulation Mode 4-13
- Frequency Hopping Mode 4-14

PIPELINE DELAY 4-14

TECHNICAL SPECIFICATIONS 4-15
- Absolute Maximum Ratings 4-15
- DC Electrical Characteristics 4-15
- Timing Specifications 4-16

PLCC PACKAGING 4-19

Q0310 DDS EVALUATION BOARD 4-20
- DDS System Diagram 4-20

RECOMMENDED SOCKETS 4-20

PATENT REFERENCES 4-21

INTRODUCTION

QUALCOMM's Q2334 Dual Direct Digital Synthesizer (DDS) generates high resolution digitized sine wave signals using phase accumulation techniques combined with a patented on-chip sine lookup and Noise Reduction Circuit (NRC). The Q2334 contains two independent DDS functions controlled from a single microprocessor interface. This interface controls both the phase and the frequency of the generated sine waves as well as the device's operating mode. Synchronous inputs are also provided to allow for phase and frequency modulation.

The Q2334 provides greater than 76 dB rejection of phase truncation spurs and 72 dB amplitude quantization signal-to-noise ratio. This synthesizer is ideally suited for applications requiring high resolution sine wave generation, fast phase and frequency switching, and excellent phase and frequency stability.

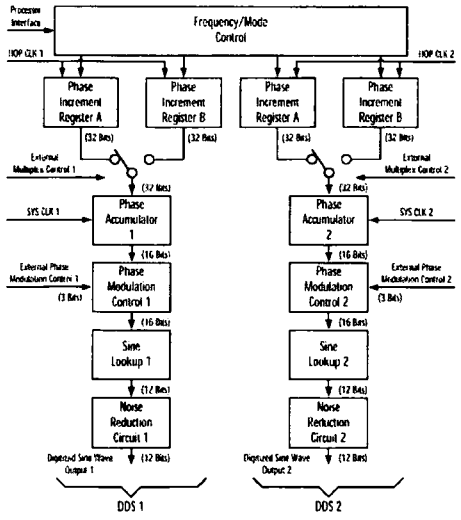
The two independent on-chip DDS functions provide an efficient technique for implementation of full-duplex systems, quadrature oscillators, and spread spectrum systems.

GENERAL DESCRIPTION

The Q2334 consists of two independent DDS functions, each controlled by a common microprocessor interface, as illustrated in Figure 1. Each DDS contains the following:

- Two Phase Increment Registers (PIR) A and B
- External Multiplex (Phase Increment Register) Control
- 32-Bit Wide Phase Accumulator
- 3-Bit External Phase Modulation Control
- Patented Sine Lookup Algorithm (see *Patent Reference 1*)
- Patented Noise Reduction Circuit (NRC) (see *Patent Reference 2*)

Figure 1. Q2334 Dual DDS Block Diagram



INTERNAL ARCHITECTURE

PROCESSOR INTERFACE

The processor interface controls the phase and frequency of the Q2334 DDS and is compatible with commonly used 8-bit microprocessors. This interface includes address decoding, chip selection, and write controls to load all on-chip control and phase increment registers. Table 1 provides the register address map for the device. Each register is write-only and is decoded from the five-bit input address bus.

Table 1. Q2334 Microprocessor Interface Register Address Map

DDS1 REGISTER ADDRESS (HEX)	DDS2 REGISTER ADDRESS (HEX)	FUNCTION
00	10	PIRA Bits 0-7 (LSB)
01	11	PIRA Bits 8-15
02	12	PIRA Bits 16-23
03	13	PIRA Bits 24-31 (MSB)
04	14	PIRB Bits 0-7 (LSB)
05	15	PIRB Bits 8-15
06	16	PIRB Bits 6-23
07	17	PIRB Bits 24-31 (MSB)
08	18	SMC
09	19	Reserved (not used)
0A	1A	AMC
0B	1B	Reserved (not used)
0C	1C	ARR
0D	1D	Reserved (not used)
0E	1E	AHC
0F	1F	Reserved (not used)

PHASE INCREMENT REGISTERS (PIRs)

Two independent 32-bit phase increment registers (A and B) are provided for each DDS function in the Q2334. Each phase increment register is 32-bits wide. Phase Increment Register A (PIRA) of each DDS provides the phase increment for the most basic single-frequency operation. Phase Increment Register B (PIRB) provides the phase increment for a range of functions useful in various modes of operation of the DDS. The 32-bit value for each register is loaded using four 8-bit write operations. Each PIR is double-buffered and the phase increment used by the phase accumulator is unaffected by this new stored value until a hop clock signal is asserted.

MODE CONTROL REGISTERS

The specific mode of the DDS operation is controlled by the Synchronous Mode Control (SMC) register and the Asynchronous Mode Control (AMC) register. The SMC is used for operations that may change throughout the operation of the DDS. The AMC should be setup once during initialization.

SYNCHRONOUS MODE CONTROL (SMC) REGISTER

The SMC register and the two PIRs are double buffered. That is, these registers can be loaded at any time using the processor interface, but the values become active only when the signal HOP CLK is asserted. This makes possible the advanced synchronous phase and frequency change features of the Q2334 which are especially important when using the device in modulation or phase-locked loop applications.

The Asynchronous Hop Clock (AHC) can also be used to activate the double-buffered settings. Refer to the *Asynchronous Hop Clock* section for more information.

Figure 2 provides the bit definition for this SMC register. Bit 0 (LSB), 4, 5, 6, and 7 are reserved and should be set to logic "0". The remaining bits of the SMC register are the Hop Clock Phase Modulation Enable (HPME), External Multiplexer Enable (EME), and the External Phase Modulation Enable (EPME). Each of these bits is described below.

HOP CLOCK PHASE MODULATION ENABLE (HPME)

The HPME bit is used when operating in the Internal Phase Modulation Mode. When the HPME bit is set to logic "1", the phase increment value stored in PIRB is added to the phase accumulator once each time the HOP CLK signal is asserted. If the Phase Modulation Add Enable (PMAE) bit is set to logic "0", all 32 bits of PIRB are used for the one time. However, if the PMAE bit is set to "1", the 8 MSB of PIRB are added to the 8 MSB of PIRA to form the 8 MSB to be accumulated with the 24 LSB of PIRA.

When the HPME bit is set to a logic "1", the HOP CLK signal is internally extended to two SYS CLK

Figure 2. Q2334 Synchronous Mode Control (SMC) Register

D7	D6	D5	D4	D3	D2	D1	D0
0*	0*	0*	0*	HOP CLK PHASE MOD ENABLE (HPME)	EXT MUX ENABLE (EME)	EXT PHASE MOD ENABLE (EPME)	0*

ADDRESS × 08 or 18 [hex]

* These bits must be set to 0.

cycles. The two SYS CLK cycles make it possible for the phase accumulator to add the contents from PIRB once, and then switch the process immediately back to PIRA. To disable the Internal Phase Modulation Mode, as is the case when you want to reconfigure operation to the Basic Oscillator Mode for example, the HPME bit is reset to "0". The HOP CLK is required to initiate this change and during the HPME's transition from "1" to "0", the HOP CLK is no longer internally extended to two SYS CLK cycles and therefore the accumulation process will still accumulate the contents from PIRB. In order to switch the accumulation process back to PIRA, re-load PIRA with the intended frequency value, then assert another HOP CLK. Asserting a successive HOP CLK without re-loading PIRA will not switch the accumulation process from PIRB to PIRA. If desired, the contents of PIRB can be loaded with the same contents intended for PIRA concurrently with the HPME bit being disabled to "0". If this is done, then when the HPME transitions, the output will look as though only PIRA is being accumulated, although the user will want to make sure to re-load PIRA with the desired value and assert another HOP CLK so the accumulation process ends up on PIRA.

EXTERNAL MULTIPLEXER ENABLE (EME)

The EME bit enables the External Multiplex Control. When this bit is set to logic "1", the EXT MUX signal determines whether the value stored in PIRA or PIRB will be used for the phase accumulation process. The selection on the EXT MUX signal is synchronously activated on the rising edge of the MUX CLK signal when the EME is set to logic "1". If the EME bit is set to logic "0", then the External Multiplex Control is disabled and the signal on EXT MUX is ignored. In this case, the contents of PIRA will be used for the accumulation process.

EXTERNAL PHASE MODULATION ENABLE (EPME)

The EPME enables the External Phase Modulation function. When this bit is set to "1", the PM EXT BITS are read and the corresponding phase offset is latched into the Q2334 each time the PM CLK is asserted. If External Phase Modulation is not used, set the EPME bit to "0". (Refer to the *External Phase Modulation* section.)

ASYNCHRONOUS MODE CONTROL (AMC) REGISTER

The AMC register has an active value once the information has been written to it. This register does not require a HOP CLK signal to become active. The AMC register of each DDS function includes control bits which should only be configured during initialization of the Q2334. The AMC commands should be activated before any other commands are asserted to the DDS in order for all commands to be received and processed properly. These control bits, as shown in Figure 3, include the DAC strobe or DAC strobe invert (DAC STB, DAC STB/), Phase Modulation Add Enable (PMAE), Output Format, and NRC Enable. Each of these is described below. Bits 4 and 6 of the AMC register are reserved and should be set to "0".

DAC STROBE, DAC STROBE INVERT (DACSTB, DACSTB/)

The DAC Strobe is a delayed version of the system clock which is provided along with the DAC BIT outputs in order to facilitate strobing this digitized sine value into a sample and hold DAC or other register. A non-inverted or inverted DAC Strobe is provided so that DAC devices with different triggering requirements can be easily accommodated. The DAC Output Timing specifications must be synchronized with respect to the falling edge of SYS CLK and are therefore only guaranteed in relation to the falling edge of SYS CLK. Trying to use the DACSTB timing associated with the rising edge of SYS CLK could potentially violate DAC setup time and result in strobing erroneous DAC BIT data.

When the AMC's D7 register is set to a "0", the DAC Strobe is non-inverted in relation to the system clock. This allows the falling edge of DACSTB to be used in compliance with SYS CLK. When the D7 register is set to a "1", the sense of the DAC Strobe is inverted in relation to the system clock. This allows the rising edge of DACSTB to be used in compliance with SYS CLK.

PHASE MODULATION ADD ENABLE (PMAE)

The PMAE bit is not used unless the HPME bit is set to "1". The PMAE bit controls the way in which the value stored in PIRB is used for the one-time accumulation by the phase accumulator. When the PMAE bit is set to logic "1" and PIRB is active for accumulation, the 8 MSB of PIRB are added to the 8 MSB of PIRA to form the 8 MSB to be accumulated. The 24 LSB of PIRA are used as the 24 LSB of the phase accumulator input value. This technique is useful for systems utilizing the Internal Phase Modulation Mode of operation. By storing the synthesizer frequency in the PIRA and modifying only the most significant byte of the PIRB, a 256-state phase modulator is implemented. This feature saves computation time in the processor controlling the DDS operation when a phase modulation system with 256-state (i.e., 360°/256 = 1.41 degrees) phase resolution is adequate. Using only the 8 MSB of PIRB to control the phase modulation allows the user to establish a byte wide Direct Memory Access (DMA) control from the processor to the DDS function phase modulation register (i.e., PIRB), thus simplifying the processor

Figure 3. Q2334 Asynchronous Mode Control (AMC) Register

D7	D6	D5	D4	D3	D2	D1	D0
DAC STB	0*	PHASE MOD ADD ENABLE (PMAE)	0*	OUTPUT FORMAT**	NRC ENABLE BITS***		

* These bits must be set to 0.

ADDRESS × 0A or 1A [hex]

**Output Format	D3
Two's Complement	0
Offset Binary	1

***DAC SIZE (# OF BITS)	D2	D1	D0
6	0	0	0
7	0	0	1
8	0	1	0
9	0	1	1
10	1	0	0
11	1	0	1
12	1	1	0
DISABLE NRC	1	1	1

overhead required to control the DDS function in rapidly switching phase modulation systems. When the PMAE bit is set to logic "0", all 32-bits of PIRB will be accumulated in the phase accumulator when PIRB is active allowing a phase resolution of $360°/2^{32}$, i.e, 84 nano degrees.

OUTPUT FORMAT

The Output Format bit determines the binary coding of the DAC output bits of each DDS function. When this bit is set to logic "1", the DAC output is encoded in offset binary format. When this bit is set to logic "0", the DAC output bits are encoded in two's complement format. Table 2 shows the effect of the setting of the Output Format bit.

Table 2. Q2334 DAC Output Formats

VALUE	OUTPUT FORMAT = 1 (OFFSET BINARY) MSB LSB	OUTPUT FORMAT = 0 (TWO's COMPLEMENT) MSB LSB
MAX Value	111111111111	011111111111
...	111111111110	011111111110
...	...	...
...	...	...
Half MAX + 1	100000000000	000000000000
Half MAX – 1	011111111111	111111111111
...	...	...
...	...	...
...	000000000001	100000000001
MIN Value	000000000000	100000000000

NRC ENABLE

When using the on-chip Noise Reduction Circuit (NRC) function, the number of significant bits to be used from the DAC outputs must be programmed into NRC Enable bits. The DAC bit-width is encoded in three bits as shown in Figure 3. When using a DAC with fewer than 12-bits resolution, the most significant DAC output bits are valid. The NRC function is disabled when the NRC Enable bits are set to 111 (binary). The function of the NRC circuit is described in the *Noise Reduction Circuit*section.

ACCUMULATOR RESET REGISTER (ARR)

Each DDS function on the Q2334 includes an Accumulator Reset Register (ARR). By writing any value to the ARR, the accumulator reset function is armed. The next time the HOP CLK is asserted, the phase accumulator is reset to zero.

ASYNCHRONOUS HOP CLOCK (AHC)

Each DDS function includes an Asynchronous Hop Clock (AHC) register. When any value is written to this register, the previously stored values in the double-buffered PIRA, PIRB, and SMC registers are activated. This allows processor control of activation of these settings in an identical fashion as with the assertion of the HOP CLK signal. Note that the HOP CLK signal must be "Low" when the AHC register is accessed in order to activate the new register values. Also note that the timing for the AHC is exactly the same as the HOP CLK signal. Activation of the stored settings occurs within four SYS CLK periods after writing to the AHC register.

The AMC register has an active value once the information has been written to it. This register does not require a HOP CLK signal to become active.

PHASE INCREMENT MULTIPLEXER CONTROL

The phase increment multiplexer function selects which PIR (A or B) is used for the accumulation process. This multiplexing function provides a simple Binary Frequency Shift Keying (BFSK) interface to the DDS.

The signal EXT MUX controls the selection of the value stored in either PIRA or PIRB. For EXT MUX = 0, PIRA is selected; for EXT MUX = 1, PIRB is selected. The signal MUX CLK enables the selection made by the EXT MUX signal. The selection made by the EXT MUX signal is activated synchronously once during the low-to-high transition on the MUX CLK signal.

The MUX CLK signal is internally synchronized to the SYS CLK signal of the DDS. (Refer to the *Asynchronous Input* information contained in Figure 11 and Table 10.) The selection of the EXT MUX control may occur as frequently as once every four periods of SYS CLK. (Refer to the *External Control Timing* information contained in Figure 10 and Table 9.)

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PHASE ACCUMULATOR

Two 32-bit wide phase accumulators are included in the Q2334, one for each DDS function. These accumulators compute and store the sum of the previously computed phase value and the phase increment value from either PIRA or PIRB once during each period of SYS CLK.

PHASE MODULATION CONTROL

Using the external phase modulation inputs, PM EXT BIT0-2, the output of the phase accumulator can be offset by phase increments of 45 degrees (from 0 degrees to 315 degrees) without affecting the operation of the phase accumulator. Table 3 shows the phase offset for the possible settings of the 3-bit external phase modulation inputs. These inputs are latched into the DDS function when the signal PM CLK is asserted. Changes in the external phase modulation are synchronized internally to the DDS function. This provides a simple 8-Phase Shift Keying (8PSK) interface to the DDS.

Refer to the *Modes of Operation* section for more detailed information on phase modulation.

SINE LOOKUP FUNCTION

The Q2334 DDS implements a patented technique to generate a sine wave lookup (see *Patent Reference 1*). This algorithm takes the 16 MSB from the phase accumulator to generate a 12 bit sine wave value. Using this high precision lookup function, the phase truncation noise of the sine wave output is kept below 76 dB. This technique differs considerably from the traditional method of using a ROM lookup function.

Table 3. Q2334 External Phase Modulation Offset Settings

PM EXT BIT 2	1	0	ABSOLUTE PHASE OFFSET (degrees)
0	0	0	0
0	0	1	45
0	1	0	90
0	1	1	135
1	0	0	180
1	0	1	225
1	1	0	270
1	1	1	315

This advanced look-up technique provides highly accurate and precise sine wave generation.

NOISE REDUCTION CIRCUIT (NRC)

Noise due to amplitude quantization is often assumed to be random and uniformly distributed. However, because a sine wave function is periodic, this is not always the case. At certain output frequencies, amplitude quantization errors become highly correlated, thereby causing spurs.

Spurs associated with round-off errors of the quantized sine wave outputs can be significantly reduced by enabling the on-chip Noise Reduction Circuit (NRC). This patented circuit distributes the noise energy evenly across the frequency band, thus reducing the amplitudes of peak spurious components (see *Patent Reference 2*).

It is important to properly set the NRC Enable bits, because the operation of the NRC is scaled to the LSB. If an incorrectly sized DAC is specified, performance will be reduced.

If the Q2334 is used to generate narrowband outputs and a low noise floor is required, the signal should be bandpass filtered and the NRC disabled. As stated above, when the NRC is enabled it distributes the noise evenly across the frequency band and raises the noise floor. When the NRC is disabled, the noise floor is slightly lower and the quantization errors show up as discrete spurious. However, since the signal is bandpass filtered, the broadband spurious will be negligible.

The output of the NRC (a 12-bit wide digitized sine wave) is normally connected to an external DAC function. This output value can be encoded in offset binary or two's complement format (see Figure 3).

Figures 4 and 5 show typical spectra of the analog converted outputs from the Q2334 with the NRC enabled and disabled. These spectra were measured with the DDS operating with a 10-bit DAC. The synthesized frequency in each of these figures is 10.8 MHz from a 30 MHz system clock frequency. The measurement frequency spans from 0 to 15 MHz, the resolution bandwidth is 30 kHz, the video bandwidth is 3 kHz, and the scale is 10 dB per vertical division.

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Figure 6 shows the typical performance of the Q2334 DDS when operating with a 10-bit DAC with NRC disabled and no LPF. This figure shows a 5 MHz output generated from a 20 MHz system clock frequency and the image at 15 MHz. This 15 MHz spur results from the negative image folded around the 30 MHz clock frequency. This image would normally be filtered by a LPF at the output of the DAC.

Figure 4. Q2334 Typical Spectrum with NRC Enabled (10-bit DAC)

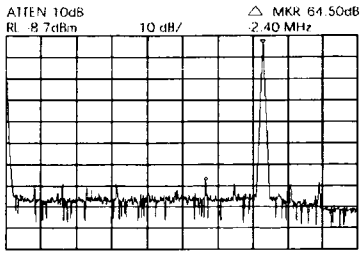


Figure 5. Q2334 Typical Spectrum with NRC Disabled (10-bit DAC)

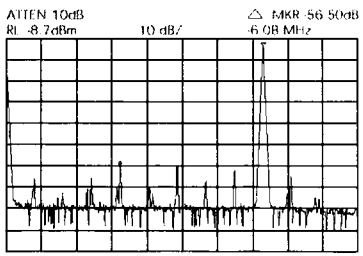
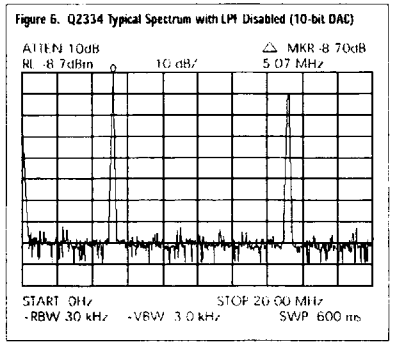


Figure 6. Q2334 Typical Spectrum with LPF Disabled (10-bit DAC)



INPUT/OUTPUT SIGNALS

Figure 7 provides the pin configuration of the Q2334 DDS package and Table 4 provides a summary of the input/output signal pin assignments.

SIGNALS COMMON FOR BOTH DDSs

The following signals are used in common for both DDS functions on the Q2334.

DATA0...DATA7

INPUTS (6, 7, 8, 9, 43, 42, 41, 40)

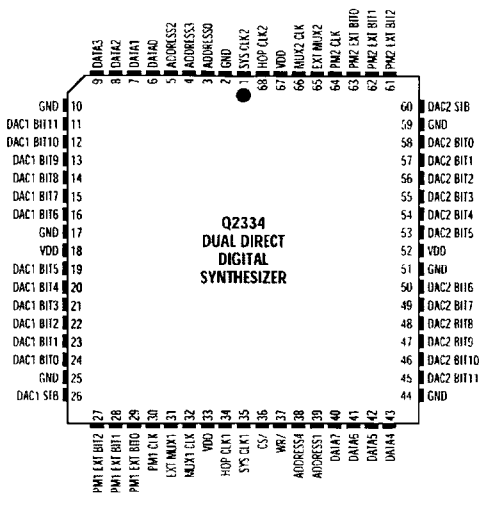
8-bit data bus for writing values to the on-chip processor interface registers. This bus is used for write operations only. DATA0 is the LSB.

ADDRESS0...ADDRESS4

INPUTS (3, 39, 5, 4, 38)

5-bit address bus to select the internal processor interface registers. Addresses must be held fixed during the active period of the WR/ signal. ADDRESS0 is the LSB.

Figure 7. Q2334 Package Pin Configuration



CS/

INPUT (36)

Chip Select. Must be held "Low" during processor write accesses to the Q2334. Can be held "Low" all the time.

WR/

INPUT (37)

When "Low" while CS/ is "Low", writes the value of the data bus to the register determined by the address bus.

V_{DD}

INPUT (18, 33, 52, 67)

Provides power to all Q2334 circuitry.

GND

INPUT (2,10,17, 25, 44, 51, 59)

Provides electrical ground reference for signal and power inputs.

SIGNALS INDEPENDENT FOR EACH DDS

The following signals pertain to a specific DDS function (1 or 2) on the Q2334.

SYS CLK1, SYS CLK2

INPUT (35, 1)

Provides the fundamental clock frequency of the synthesized sine waveform. Internal operations of the phase accumulator, external phase modulation, and phase increment registers are synchronized to this clock signal.

HOP CLK1, HOP CLK2

INPUT (34, 68)

The HOP CLK signal controls the activation of the selection of the double buffered registers. HOP CLK must be active "High" for at least one SYS CLK period and can be asserted once every ten SYS CLK periods.

Table 4. Q2334 Input/Output Signals

PIN #	NAME	I/O TYPE	DESCRIPTION	PIN #	NAME	I/O TYPE	DESCRIPTION
1	SYS CLK2	INPUT	System Clock to DDS #2	35	SYS CLK1	INPUT	System Clock to DDS#1
2	GND	INPUT	Ground Connection	36	CS/	INPUT	Chip Select - Low during Processor Writes
3	ADDRESS0	INPUT	Processor Interface Address Bus-bit 0 (LSB)	37	WR/	INPUT	Writes the Value of Data Bus into Register - Active Low
4	ADDRESS3	INPUT	Processor Interface Address Bus-bit 3				
5	ADDRESS2	INPUT	Processor Interface Address Bus-bit 2	38	ADDRESS4	INPUT	Processor Interface Address Bus-bit 4 (MSB)
6	DATA0	INPUT	Processor Interface Data Bus-bit 0 (LSB)	39	ADDRESS1	INPUT	Processor Interface Address Bus-bit 1
7	DATA1	INPUT	Processor Interface Data Bus-bit 1	40	DATA7	INPUT	Processor Interface Data Bus-bit 7 (MSB)
8	DATA2	INPUT	Processor Interface Data Bus-bit 2	41	DATA6	INPUT	Processor Interface Data Bus-bit 6
9	DATA3	INPUT	Processor Interface Data Bus-bit 3	42	DATA5	INPUT	Processor Interface Data Bus-bit 5
10	GND	INPUT	Ground Connection	43	DATA4	INPUT	Processor Interface Data Bus-bit 4
11	DAC1 BIT11	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 11 (MSB)	44	GND	INPUT	Ground Connection
				45	DAC2 BIT11	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 11 (MSB)
12	DAC1 BIT10	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 10	46	DAC2 BIT10	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 10
13	DAC1 BIT9	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 9	47	DAC2 BIT9	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 9
14	DAC1 BIT8	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 8	48	DAC2 BIT8	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 8
15	DAC1 BIT7	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 7	49	DAC2 BIT7	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 7
16	DAC1 BIT6	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 6	50	DAC2 BIT6	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 6
17	GND	INPUT	Ground Connection	51	GND	INPUT	Ground Connection
18	V_{DD}	INPUT	+5V Power Supply Connection	52	V_{DD}	INPUT	+5V Power Supply Connection
19	DAC1 BIT5	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 5	53	DAC2 BIT5	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 5
20	DAC1 BIT4	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 4	54	DAC2 BIT4	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 4
21	DAC1 BIT3	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 3	55	DAC2 BIT3	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 3
22	DAC1 BIT2	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 2	56	DAC2 BIT2	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 2
23	DAC1 BIT1	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 1	57	DAC2 BIT1	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 1
24	DAC1 BIT0	OUTPUT	DDS#1 Digitized Sine Wave Output-bit 0 (LSB)	58	DAC2 BIT0	OUTPUT	DDS#2 Digitized Sine Wave Output-bit 0 (LSB)
25	GND	INPUT	Ground Connection	59	GND	INPUT	Ground Connection
26	DAC1 STB	OUTPUT	DDS#1 Synchronous Strobe to Facilitate Clocking the DAC BITs into a DAC	60	DAC2 STB	OUTPUT	DDS#2 Synchronous Strobe to Facilitate Clocking the DAC BITs into a DAC
27	PM1 EXT BIT2	INPUT	DDS#1 Controls the External PM Value-bit 2	61	PM2 EXT BIT2	INPUT	DDS#2 Controls the External PM Value-bit 2
28	PM1 EXT BIT1	INPUT	DDS#1 Controls the External PM Value-bit 1	62	PM2 EXT BIT1	INPUT	DDS#2 Controls the External PM Value-bit 1
29	PM1 EXT BIT0	INPUT	DDS#1 Controls the External PM Value-bit 0	63	PM2 EXT BIT0	INPUT	DDS#2 Controls the External PM Value-bit 0
30	PM1 CLK	INPUT	DDS#1 Enables the Values in PM EXT BITs	64	PM2 CLK	INPUT	DDS#2 Enables the Values in PM EXT BITs
31	EXT MUX1	INPUT	DDS#1 Controls which PIR is Being Accumulated	65	EXT MUX2	INPUT	DDS#2 Controls which PIR is Being Accumulated
32	MUX1 CLK	INPUT	DDS#1 Enables the Value on EXT MUX1	66	MUX2 CLK	INPUT	DDS#2 Enables the Value on EXT MUX2
33	V_{DD}	INPUT	+5V Power Supply Connection	67	V_{DD}	INPUT	+5V Power Supply Connection
34	HOP CLK1	INPUT	Hop Clock to DDS#1	68	HOP CLK2	INPUT	Hop Clock to DDS#2

EXT MUX1, EXT MUX2

INPUT (31, 65)

When latched into the DDS with the signal MUX1 CLK (or MUX2 CLK) this signal determines which PIR (A or B) will be used for the incremental phase accumulator input value. When the EXT MUX signal is set to "1", the value stored in PIRB will be used by the phase accumulator. When the EXT MUX signal is set to "0", the value stored in PIRA will be used.

MUX1 CLK, MUX2 CLK

INPUT (32, 66)

The rising edge of this signal latches and enables the value on the EXT MUX inputs. This signal must be held "High" for a minimum of three SYS CLK periods. Activation of the EXT MUX inputs is synchronized internally to SYS CLK.

PM1 EXT BIT0...PM1 EXT BIT2,
PM2 EXT BIT0...PM2 EXT BIT2

INPUTS (29, 28, 27, 63, 62, 61)

External phase modulation inputs which control 45 degree phase offsets in the phase accumulated values in accordance with the settings provided in Table 3. PM EXT BITs are active when the signal PM CLK is asserted and are synchronized internally to the DDS function to SYS CLK.

PM1 CLK, PM2 CLK

INPUT (30, 64)

The rising edge of this signal latches and enables the value on the PM EXT BIT inputs. This signal must be held "High" for a minimum of three SYS CLK periods. The PM EXT BIT inputs are synchronized internally to SYS CLK.

DAC1 BIT0...DAC1 BIT11, DAC2 BIT0...DAC2 BIT11

OUTPUTS (24, 23, 22, 21, 20, 19, 16, 15, 14, 13, 12, 11, 58, 57, 56, 55, 54, 53, 50, 49, 48, 47, 46, 45)

Digitized sine wave outputs encoded in offset binary or two's complement format, depending on settings in the AMC Registers. One sample is generated during each period of SYS CLK. DAC BIT 0 is the LSB.

DAC1 STB, DAC2 STB

OUTPUT (26, 60)

Provides a synchronous strobe to facilitate clocking of the DAC BIT outputs into an external register or sampled DAC. One DAC STB is generated during each period of SYS CLK. Essentially, the DAC STB (or DAC STB/) is a delayed version of SYS CLK.

MODES OF OPERATION

Each DDS can be independently set to perform a wide range of expanded functions of the basic operation, as described in the following paragraphs

BASIC SYNTHESIZER MODE

In its most Basic Operational Mode, each DDS on the Q2334 can provide a fixed frequency digitized sine wave output. The frequency of this sine output is determined by the frequency of the clock input and the value stored in the PIRs. (See formula (1) in the *Phase Increment Value* section of the *General DDS* section.)

To set the Q2334 up in a Single Frequency Output Mode, the SMC should be set to "00" (hex). The AMC should be set according to the size of the DAC selected and the desired output format. The PMAE bit should also be set to "0". (Refer to the *Simple Oscillator Mode Example* section.)

PHASE MODULATION MODE

The Q2334 provides two means to implement phase modulation of a basic frequency output, referred to as Internal Phase Modulation and External Phase Modulation.

Internal Phase Modulation provides extremely fine resolution up to 0.00000008° of the phase adjustment (2^{32} - state phase resolution), while External Phase Modulation is designed for 45° increment phase shifts.

INTERNAL PHASE MODULATION

Internal Phase Modulation operates as a differential phase adjustment technique and requires use of the processor interface. The Internal Phase Modulation Mode is activated by loading PIRA with the correct phase increment for the basic frequency without phase modulation. PIRB is then loaded with the phase increment value equal to the phase increment value stored in PIRA plus the value of the desired phase offset. The phase accumulator uses PIRA for most phase accumulations.

Setting the HPME bit in the SMC register to logic "1" arms the DDS to use the 32-bit value in PIRB for one phase accumulation cycle when the signal HOP CLK is asserted. Since the phase increment value in PIRB is only used once for each HOP CLK assertion, the net effect is to cause a phase change to the generated sine wave.

When the PMAE bit is set to logic "1", the 8 MSB of PIRB are added to the 8 MSB of PIRA to form the 8 MSB to be accumulated with the 24 LSB of PIRA. This 32-bit value is used for one-time accumulation. If PMAE is "0", all 32 units of PIRB will be used for the accumulation

The one-time phase shift occurs every time the HOP CLK signal is asserted. The phase shift can occur as often as the HOP CLK signal can be asserted. (Refer to *Processor Interface Timing* shown in Figure 8 and Table 7).

If it is desired to change the phase offset value, PIRB must be reloaded before the HOP CLK cycle with the new phase offset for the next HOP CLK period. The HPME bit will remain set to "1" until reset by the processor. (Refer to the *Hop Clock Phase Modulation Enable* section.)

EXTERNAL PHASE MODULATION

External Phase Modulation operates as an absolute phase adjustment technique and utilizes special synchronous inputs separate from the processor interface. When using the External Phase Modulation Mode, the phase increment value for the unmodulated input is written into PIRA. PIRB is not used in the External Phase Modulation Mode.

The External Phase Modulation Enable (EPME) bit in the SMC register is set to logic "1" to enable the External Phase Modulation Mode. When the EPME bit is set to "1", the phase offset determined by the PM EXT BITs are latched into the DDS function each time the signal PM CLK is asserted. This PM EXT BIT setting causes a phase offset in 45° increments as indicated in Table 3. This mode of operation allows very simple control of the DDS as a binary, quartenary, or 8-ary phase shift keyed (8PSK) modulator.

BINARY FREQUENCY SHIFT KEYING (BFSK) MODULATION MODE

Two PIRs are provided for each DDS function allowing for Binary Frequency Shift Keyed (BFSK) modulation without any additional hardware. The Q2334 provides signals allowing this switch to occur synchronously.

BFSK Modulation is achieved by setting the phase increment value in PIRA to generate the first frequency and the value in the PIRB to generate the second frequency. The EME bit is then set to logic "1" to enable the external multiplexer controls.

If the EXT MUX signal is set to logic "1" when the MUX CLK signal is asserted, the phase accumulator will choose the phase increment value from PIRB. If the EXT MUX signal is set to logic "0" when the MUX CLK is asserted, the phase accumulator will choose the phase increment value from PIRA. Changing the value of the EXT MUX input causes the alternation between the frequency controlled by PIRA and the frequency controlled by PIRB.

After the BFSK Mode is set up and the PIRA and PIRB contents are active, the EXT MUX signal can be changed as fast as the MUX CLK can be asserted. (See *External Control Timing* shown in Figure 10 and Table 9). The MUX CLK timing is the only restriction on how fast the accumulation can be switched from PIRA to PIRB.

MINIMUM SHIFT KEYING (MSK) MODULATION MODE

The Minimum Shift Keying (MSK) Modulation Mode is a subset of the BFSK Mode described above. The operation is the same, but the two frequencies are selected at a known mathematically determined rate. The MSK Modulation Mode is linear MSK and can be generated by setting the frequency shift rate equal to the separation between the two frequencies. This is where MSK got its name, since it is the minimum spacing between the two frequencies that can be accomplished while still recovering the signal with a given shift rate. If the frequency spacing is closer than the frequency shift rate, the information cannot be recovered. If the spacing is too far apart, the information can be retrieved using FSK demodulation techniques, although MSK will not be generated from the resultant spectra. To produce the two MSK frequencies, the values in PIRA and PIRB correspond to incrementing and decrementing phase values (respectively) that must change through ±90 degrees for each symbol time of the frequency shift rate. This is obtained by loading PIRA and PIRB with frequency values such that the mid-point value between them is separated by ± FSK rate/2. This must occur without any phase discontinuities but since the DDS changes frequencies in a phase continuous fashion, this is not a problem. The overall result due to the slow phase transitions between the frequencies is a reduction in the high-frequency spectral content, thus attenuating the sidelobes. The spectrum is said to be more efficient since more power is contained in the main lobe and less in the sidelobes. The EME bit of the SMC register is set to logic "1", as in the BFSK Mode, and the EXT MUX and MUX CLK signals control the shift between the values of PIRA and PIRB.

FREQUENCY HOPPING MODE

Simple frequency hopping can be enabled by writing a new phase increment value of the desired frequency in PIRA. Since PIRA is a double buffered register, this value will be activated at the next assertion of the HOP CLK signal.

Assuming each frequency to be generated requires all 32 bits to be changed, then four 8-bit writes to PIRA would be needed. (See *Processor Interface Timing* shown in Figure 8 and Table 7.) After PIRA has been loaded, the assertion of the HOP CLK will activate these settings and the resulting frequency will be output from the Q2334 within 31 clock cycles. The frequency value can be changed as fast as the new phase increment value can be written to PIRA and a HOP CLK signal asserted. (Also see Figure 8 and Table 7.) Once all 32 bits have been activated, the contents will remain until the register is written again. Subsets within the register may also be written. This allows for the changing of an existing register value using a single 8-bit write as opposed to four 8-bit writes.

PIPELINE DELAY

The output of the Q2334 DDS will reflect the change in status activated by the HOP CLK within 30 to 31 SYS CLK periods. When the EXT MUX signal is enabled, the associated PIR will affect the output in 29 to 30 SYS CLK periods after the MUX CLK has been asserted. If External Phase Modulation is implemented, the phase shift will occur 28 to 29 SYS CLK periods after the rising of the PM CLK.

The one SYS CLK ambiguity occurs because the MUX CLK, PM CLK, and HOP CLK signals are allowed to be asynchronous in relation to the SYS CLK. To keep the internal operation of the Q2334 synchronous, the signals are input to synchronizing circuitry which resolves the signal to within one clock period.

TECHNICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 5 shows the absolute maximum ratings of the Q2334. Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data book is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Q2334 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTE
Storage Temperature	T_S	-55	+85	°C	–
Operating Temperature	T_A	0	+70	°C	–
Junction Temperature	T_J	–	+150	°C	1
Voltage on any Input Pin	–	-0.3	V_{DD} + 0.3	V	–
Voltage on VDD & any Output Pin	–	-0.3	+7.0	V	–
DC Input Current	I_{IH}	-10	+10	µA	–

Note:

1. For thermal management consideration, the Junction to Case Thermal Resistance, θ_{JC} is 10.7°C/W typical, and the Junction to Ambient Thermal Resistance, θ_{JA} is 33°C/W typical.

DC ELECTRICAL CHARACTERISTICS

Table 6 shows the DC electrical characteristics for the Q2334.

Table 6. Q2334 DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	4.75	5.25	V	–
High-level Input Voltage	V_{IH}	2.0	V_{DD} + 0.3	V	–
Low-level Input Voltage	V_{IL}	-0.3	0.8	V	–
Input Leakage Current	I_L	–	1.0	µA	–
High-level Output Voltage	V_{OH}	2.4	–	V	1
Low-level Output Voltage	V_{OL}	–	0.4	V	2
Power Dissipation @ Maximum SYS CLK	P_D	–	0.67 @50 MHz	W	3,4

Notes:

1. I_{OH} = - 1.6 mA.
2. I_{OL} = 1.6 mA.
3. Power rating is per DDS. If both DDS1 and DDS2 are operating at same conditions, the power will be doubled.
4. For other clock frequencies,
   Power ≤ (13.33 mW/MHz) • (Clock Frequency);
   Current ≤ (2.66 mA/MHz) • (Clock Frequency).

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TIMING SPECIFICATIONS

Figures 8 through 11 and Tables 7 through 10 show the timing specifications of the Q2334.

Figure 8. Q2334 Processor Interface Timing Diagram

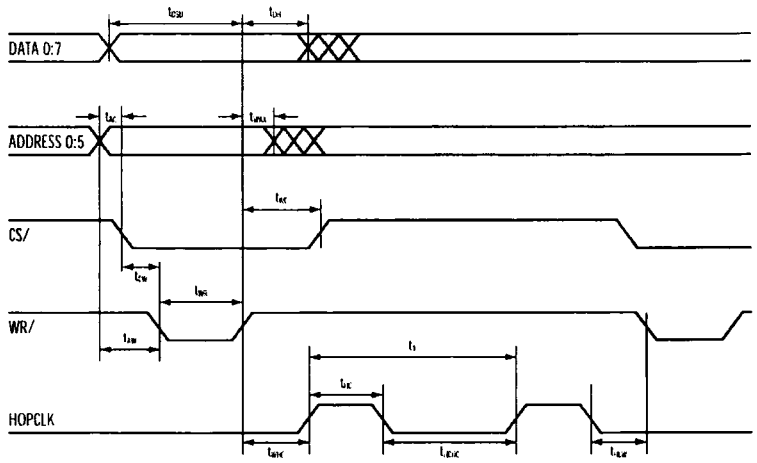

Table 7. Q2334 Processor Interface Timing Parameters

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Data Setup to WR/ Rising	t_{DSU}	10	–	ns	–
Data Hold After WR/ Rising	t_{DH}	5	–	ns	–
Address Valid to CS/ Falling	t_{AC}	0	–	ns	–
Address Hold After WR/ Rising	t_{AWR}	5	–	ns	–
CS/ Setup to WR/ Falling	t_{CW}	0	–	ns	–
CS/ Hold After WR/ Rising	t_{WC}	0	–	ns	–
WR/ Rising to HOP CLK Rising	t_{WHC}	10	–	ns	1
HOP CLK Pulse Width	t_{HC}	t_{CYC}	–	ns	2
HOP CLK Falling Edge to HOP CLK Rising Edge	t_{HCHC}	4 • t_{CYC}	–	ns	2
HOP CLK Falling Edge to WR/	t_{HCW}	10 • t_{CYC}	–	ns	1,2
Address Valid to WR/ Falling	t_{AW}	15	–	ns	–
WR/ Period	t_{WR}	40	–	ns	–
Time Between HOP CLK	t_3	10 • t_{CYC}	–	ns	2

Notes:

1. When CS/ is active "Low".
2. t_{CYC} is the system clock period.

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Fax: (619) 658-1556

Figure 9. Q2334 DAC Output Timing Diagram

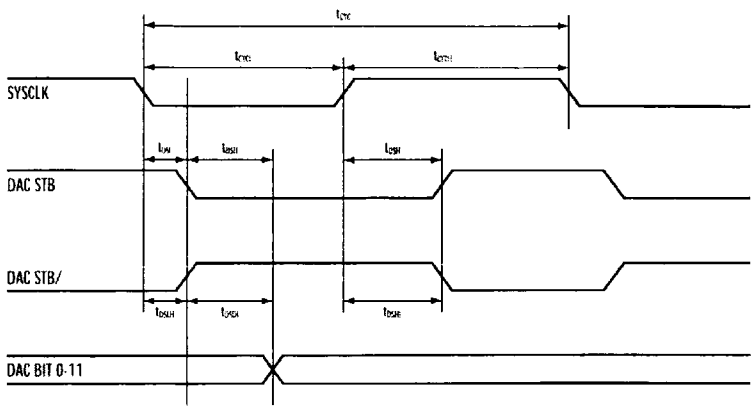

Table 8. Q2334 DAC Output Timing Parameters

		20 MHz Max Clock		30 MHz Max Clock		40 MHz Max Clock		50 MHz Max Clock			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
SYS CLK Cycle Period	t_{CYC}	50	1000	33	1000	25	1000	20	1000	ns	1, 2, 3
SYS CLK Low Period	t_{CYCL}	22	478	15	485	11.25	488.75	8.5	491.5	ns	–
SYS CLK High Period	t_{CYCH}	22	478	15	485	11.25	488.75	8.5	491.5	ns	–
SYS CLK Low to DAC STB Low	t_{DSL}	–	10	–	10	–	10	–	10	ns	4
SYS CLK Low to DAC STB/ High	t_{DSLH}	–	10	–	10	–	10	–	10	ns	4
SYS CLK High to DAC STB High	t_{DSH}	–	10	–	10	–	10	–	10	ns	4
SYS CLK High to DAC STB/ Low	t_{DSHL}	–	10	–	10	–	10	–	10	ns	4
DAC STB Low to DAC BIT Output	t_{DSD}	4	20	4	17	4	17.5	4	14	ns	4
DAC STB/ High to DAC BIT Output	t_{DSDI}	4	20	4	17	4	17.5	4	14	ns	4

Notes:

1. The Q2334C-50N will operate up to 30 MHz maximum clock with $-55 \le T \le 125°C$ and $4.5 \le V_{DD} \le 5.5$ V.
2. The Q2334C-50N will operate up to 40 MHz maximum clock with $-40 \le T \le 85°C$ and $4.5 \le V_{DD} \le 5.5$ V.
3. The Q2334 contains dynamic logic. Minimum SYS CLK frequency is 1.0 MHz.
4. Assumes a 25pF capacitive loading.

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Figure 10. Q2334 External Control Timing Diagram

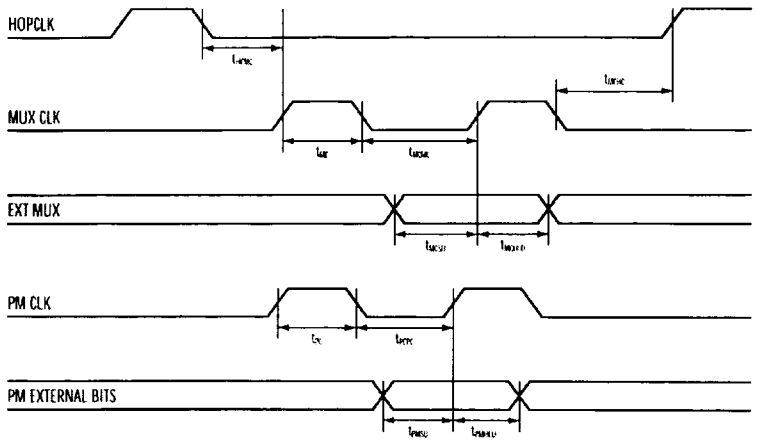

Table 9. Q2334 External Control Timing Parameters

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
HOP CLK Falling to MUX CLK Rising	t_{HCMC}	t_{CYC}	–	ns	1
MUX CLK High Period	t_{MC}	3 * t_{CYC}	–	ns	1
MUX CLK Low Period	t_{MCMC}	t_{CYC}	–	ns	1
MUX CLK Falling to HOP CLK Rising	t_{MCHC}	10 * t_{CYC}	–	ns	1
EXT MUX Setup to MUX CLK	t_{MCSU}	10	15	ns	–
EXT MUX Hold After MUX CLK	t_{MCHLD}	10	15	ns	–
PM CLK High Period	t_{PC}	3 * t_{CYC}	–	ns	1
PM CLK Low Period	t_{PCPC}	t_{CYC}	–	ns	1
PM Data Setup to PM CLK	t_{PMSU}	10	15	ns	–
PM Data Hold After PM CLK	t_{PMHLD}	10	15	ns	–

Notes:

1. t_{CYC} is the system clock period.

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PLCC PACKAGING

The Q2334C-50N is packaged in the 68-pin plastic leaded chip carrier (PLCC) shown in Figure 11. The dimensions are given in inches and (mm).

Figure 11. Q2334 68-pin PLCC Package Diagram

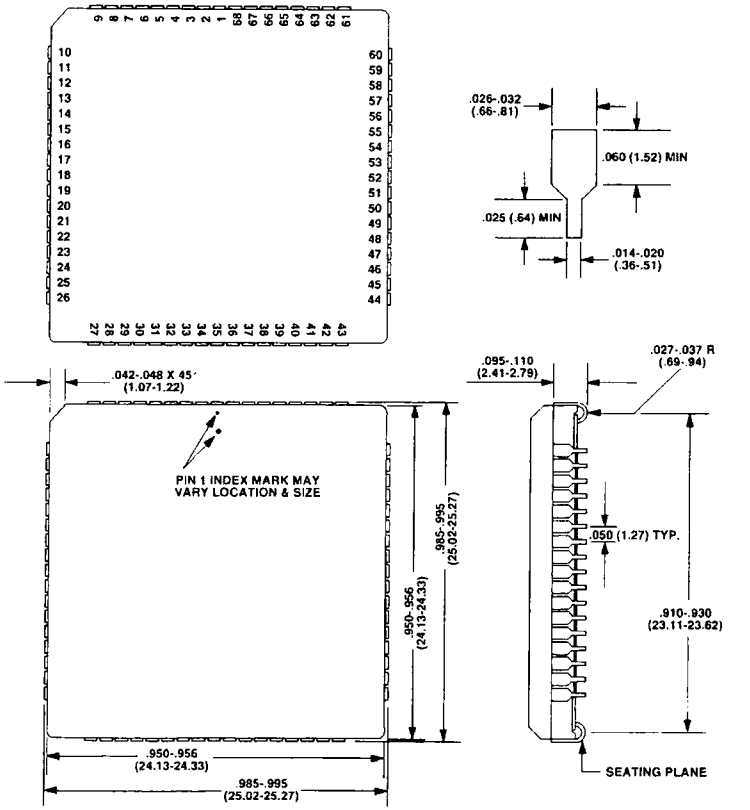
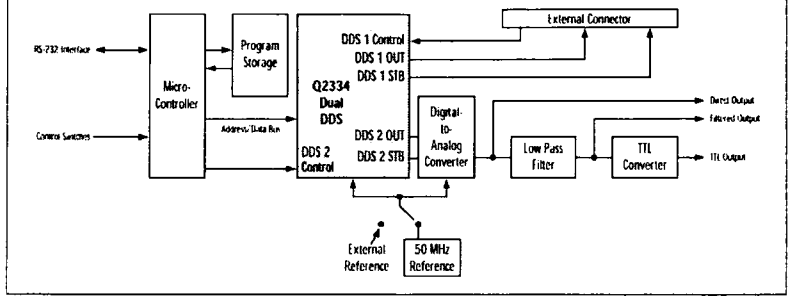


Figure 12. Q0310 Block Diagram



Q0310 DDS EVALUATION BOARD

The Q0310 is an evaluation board for the Q2331 DDS. The Q0310 is a complete DDS System that includes a Q2334C-50N, pre-programmed microcontroller, 10 bit DAC, and low pass filter all designed onto an 8" x 4" x 1.5" printed circuit card that is fully assembled and tested. An 8031 microcontroller controls the DDS using a monitor program contained in the on-board EPROM. This program interacts through the switches on the board for stand-alone operation or through the RS-232 port for remote operation. A block diagram of this particular configuration is shown in Figure 12. The menu-driven monitor program can exercise all of the following modes of operation:

- Basic Oscillator
- Frequency Sweep (Fast or Slow)
- Frequency Hop
- 8-PSK Modulator
- 256-PSK Modulator
- MSK Modulator

A Q0310 User's Guide with complete documentation including schematics, parts list, and microcontroller code (available in floppy disk) is included.

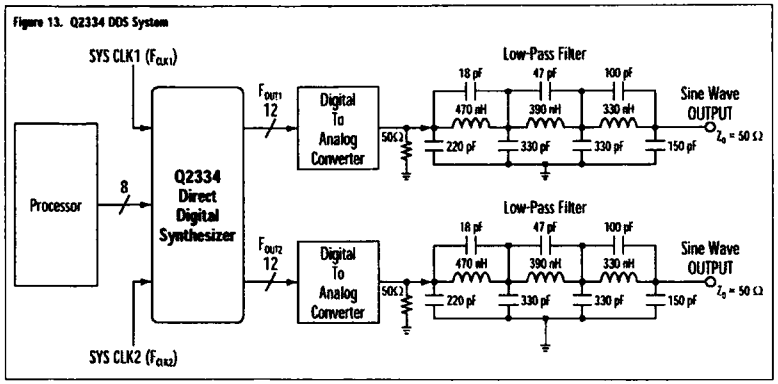
DDS SYSTEM DIAGRAM

Figure 13 provides a basic diagram of a Q2334 DDS system. Note the LPF used is a seven pole elliptical filter designed for operation with a 50 MHz clocked DDS, which rolls off at approximately 20 MHz. This is the filter topology used in the Q0310 DDS Evaluation Board. Each system has different specifications, and the design of the LPF should take the system requirements into account.

RECOMMENDED SOCKETS

Methode Electronics 213-052-602 Low Profile Surface Mount 68-pin carrier socket, AMP 821574-1 thru-hole 68-pin carrier socket.

Figure 13. Q2334 DDS System



PATENT REFERENCES

1.) U.S. Patent No. 4,905,177 - "High Resolution Phase to Sine Amplitude Conversion," QUALCOMM, Feb. 27, 1990.

2.) U.S. Patent No. 4,901,265 - "Pseudorandom Dither for Frequency Synthesis Noise," QUALCOMM, Feb. 13, 1990.

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ANALOG DEVICES

12-Bit, 100 MSPS D/A Converters

AD9712B/AD9713B

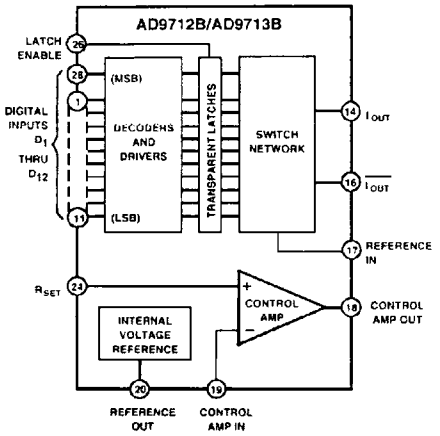
FEATURES
100 MSPS Update Rate
ECL/TTL Compatibility
SFDR @ 1 MHz: 70 dBc
Low Glitch Impulse: 28 pV-s
Fast Settling: 27 ns
Low Power: 725 mW
1/2 LSB DNL (B Grade)
40 MHz Multiplying Bandwidth

APPLICATIONS
ATE
Signal Reconstruction
Arbitrary Waveform Generators
Digital Synthesizers
Signal Generators

GENERAL DESCRIPTION

The AD9712B and AD9713B D/A converters are replacements for the AD9712 and AD9713 units which offer improved ac and dc performance. Like their predecessors, they are 12-bit, high speed digital-to-analog converters fabricated in an advanced oxide isolated bipolar process. The AD9712B is an ECL-compatible device featuring update rates of 100 MSPS minimum; the TTL-compatible AD9713B will update at 80 MSPS minimum.

FUNCTIONAL BLOCK DIAGRAM



Designed for direct digital synthesis, waveform reconstruction, and high resolution imaging applications, both devices feature low glitch impulse of 28 pV-s and fast settling times of 27 ns. Both units are characterized for dynamic performance and have excellent harmonic suppression.

The AD9712B and AD9713B are available in 28-pin plastic DIPs and PLCCs, with an operating temperature range of –25°C to +85°C. Both are also available for extended temperature ranges of –55°C to +125°C in cerdips and 28-pin LCC packages.

REV. B

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AD9712B/AD9713B–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

($-V_S$ = –5.2 V; $+V_S$ = +5 V (AD9713B only); Reference Voltage = –1.2 V; R_{SET} = 7.5 kΩ; V_{OUT} = 0 V (virtual ground); unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9712B/AD9713B AN/AP Min	AN/AP Typ	AN/AP Max	AD9712B/AD9713B BN/BP Min	BN/BP Typ	BN/BP Max	AD9712B/AD9713B SE/SQ Min	SE/SQ Typ	SE/SQ Max	AD9712B/AD9713B TE/TQ Min	TE/TQ Typ	TE/TQ Max	Units
RESOLUTION				12			12			12			12		Bits
DC ACCURACY															
Differential Nonlinearity	+25°C	I		±1.25	±1.0		±0.75	±0.5		±1.5	±1.0		±1.0	±0.5	LSB
	Full	VI		±2.0			±1.5			±2.0			±1.5		LSB
Integral Nonlinearity	+25°C	I		±1.5	±1.0		±1.0	±0.75		±1.75	±1.5		±1.25	±1.0	LSB
("Best Fit" Straight Line)	Full	VI		±2.0			±1.75			±2.0			±1.75		LSB

Parameter (Conditions)	Temp	Test Level	AD9712B All Grades Min	AD9712B All Grades Typ	AD9712B All Grades Max	AD9713B All Grades Min	AD9713B All Grades Typ	AD9713B All Grades Max	Units
INITIAL OFFSET ERROR									
Zero-Scale Offset Error	+25°C	I		0.5	2.5		0.5	2.5	µA
	Full	VI			5.0			5.0	µA
Full-Scale Gain Error[1]	+25°C	I		1.0	5		1.0	5	%
	Full	VI			8			8	%
Offset Drift Coefficient	+25°C	V		0.01			0.01		µA/°C
REFERENCE/CONTROL AMP									
Internal Reference Voltage	+25°C	I	1.14	1.18	1.22	1.14	1.18	1.22	V
	Full	VI	1.12		1.24	1.12		1.24	V
Internal Reference Voltage Drift	Full	V		50			50		ppm/°C
External Reference Output Current	Full	IV	50		+500	50		+500	µA
Amplifier Input Impedance	+25°C	V		50			50		kΩ
Amplifier Bandwidth	+25°C	V		300			300		kHz
REFERENCE INPUT[2]									
Reference Input Impedance	+25°C	V		3			3		kΩ
Reference Multiplying Bandwidth[3]	+25°C	V		10			40		MHz
DYNAMIC PERFORMANCE									
Full-Scale Output Current[4]	+25°C	V		20.48			20.48		mA
Output Compliance Range	+25°C	IV	1.2		+2	1.2		+2	V
Output Resistance	+25°C	IV	2.0	2.5	3.0	2.0	2.5	3.0	kΩ
Output Capacitance	+25°C	V		15			15		pF
Output Update Rate[5]	+25°C	IV	100	110		80	100		MSPS
Output Settling Time (t_{ST})[6]	+25°C	V		27			27		ns
Output Propagation Delay (t_{PD})[7]	+25°C	V		6			7		ns
Glitch Impulse[8]	+25°C	V		28			28		pV-s
Output Rise Time[9]	+25°C	V		2			2		ns
Output Fall Time[9]	+25°C	V		2			2		ns
DIGITAL INPUTS									
Logic "1" Voltage	Full	VI	1.0	0.8		2.0			V
Logic "0" Voltage	Full	VI		1.7	1.5			0.8	V
Logic "1" Current	Full	VI			20			20	µA
Logic "0" Current	Full	VI			10			600	µA
Input Capacitance	+25°C	V		3			3		pF
Input Setup Time (t_S)[10]	+25°C	IV	0.5	–0.3		0.5	–0.3		ns
	Full	IV	0.8			0.8			ns
Input Hold Time (t_H)[11]	+25°C	IV	1.8	1.2		1.8	1.2		ns
	Full	IV	2.0			2.0			ns
Latch Pulse Width (t_{LPW}) (LOW)	+25°C	IV	2.5	1.7		2.5	1.7		ns
(Transparent)	Full		2.8			2.8			ns
AC LINEARITY[12]									
Spurious-Free Dynamic Range (SFDR)									
1.23 MHz; 10 MSPS; 2 MHz Span	+25°C	V		75			70		dB
5.055 MHz; 20 MSPS; 2 MHz Span	+25°C	V		72			72		dB
10.1 MHz; 50 MSPS; 2 MHz Span	+25°C	V		68			68		dB
16 MHz; 10 MSPS; 10 MHz Span	+25°C	V		68			68		dB

Parameter (Conditions)	Temp	Test Level	AD9712B All Grades Min	AD9712B All Grades Typ	AD9712B All Grades Max	AD9713B All Grades Min	AD9713B All Grades Typ	AD9713B All Grades Max	Units
POWER SUPPLY[5]									
Positive Supply Current (+5.0 V)	+25°C	I					6	12	mA
	Full	VI						14	mA
Negative Supply Current (–5.2 V)[14]	+25°C	I		140	178		145	184	mA
	Full	VI			183			188	mA
Nominal Power Dissipation	+25°C	V		728			784		mW
Power Supply Rejection Radio (PSRR)[15]	+25°C	I		30	100		30	100	μA/V

NOTES

[1]Measured as error in ratio of full-scale current to current through R_{SET} (160 μA nominal); ratio is nominally 128.

[2]Full-scale variations among devices are higher when driving REFERENCE INPUT directly.

[3]Frequency at which the gain is flat ±0.5 dB; R_L = 50 Ω, 50% modulation at midscale.

[4]Based on I_{FS} = 128 (V_{REF}/R_{SET}) when using internal amplifier.

[5]Data registered into DAC accurately at this rate; does not imply settling to 12 bit accuracy.

[6]Measured as voltage settling at midscale transition to ±0.024%, R_L = 50 Ω.

[7]Measured as the time between the 50% point of the falling edge of LATCH ENABLE and the point where the output signal has left a 1 LSB error band around its previous value.

[8]Peak glitch impulse is measured as the largest area under a single positive or negative transient.

[9]Measured with R_L = 50 Ω and DAC operating in latched mode.

[10]Data must remain stable for specified time prior to falling edge of LATCH ENABLE signal.

[11]Data must remain stable for specified time after rising edge of LATCH ENABLE signal.

[12]SFDR is defined as the difference in signal energy between the fundamental and worst case spurious frequencies in the output spectrum window, which is centered at the fundamental frequency and covers the indicated span.

[13]Supply voltages should remain stable within ±5% for normal operation.

[14]108 mA typ on Digital $-V_S$, 37 mA typ on Analog $-V_S$.

[15]Measured at ±5% of $+V_S$ (AD9713B only) and $-V_S$ (AD9712B or AD9713B) using external reference.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) (AD9713B Only) ..... +6 V
Negative Supply Voltage ($-V_S$) ..... 7 V
Analog-to-Digital Ground Voltage Differential ..... 0.5 V
Digital Input Voltages (D_1–D_{12}, LATCH ENABLE)
AD9712B ..... 0 V to $-V_S$
AD9713B ..... –0.5 V to $+V_S$
Internal Reference Output Current ..... 500 μA
Control Amplifier Input Voltage Range ..... 0 V to –4 V
Control Amplifier Output Current ..... ±2.5 mA
Reference Input Voltage Range (V_{REF}) ..... 0 V to $-V_S$
Analog Output Current ..... 30 mA
Operating Temperature Range
AD9712B/AD9713BAN/AP/BN/BP .....–25°C to +85°C
AD9712B/AD9713BSE/SQ/TE/TQ .....–55°C to +125°C
Maximum Junction Temperature[2]
AD9712B/AD9713BAN/AP/BN/BP ..... +150°C
AD9712B/AD9713BSE/SQ/TE/TQ ..... +175°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Storage Temperature Range .....–65°C to +150°C

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances with parts soldered in place: 28-pin plastic DIP: θ_{JA} = 37°C/W, θ_{JC} = 10°C/W; 28-pin PLCC: θ_{JA} = 44°C/W, θ_{JC} = 14°C/W; Cerdip θ_{JA} = 32°C/W, θ_{JC} = 10°C/W; LCC: θ_{JA} = 41°C/W, θ_{JC} = 13 C/W. No air flow.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9712BAN	–25°C to +85°C	28-Pin PDIP	N-28
AD9712BBN	–25°C to +85°C	28-Pin PDIP	N-28
AD9712BAP	–25°C to +85°C	28-Pin PLCC	P-28A
AD9712BBP	–25°C to +85°C	28-Pin PLCC	P-28A
AD9712BSQ/883B	–55°C to +125°C	28-Pin Cerdip	Q-28
AD9712BSE/883B	–55°C to +125°C	28-Pin LCC	E-28A
AD9712BTQ/883B	–55°C to +125°C	28-Pin Cerdip	Q-28
AD9712BTE/883B	–55°C to +125°C	28-Pin LCC	E-28A
AD9713BAN	–25°C to +85°C	28-Pin PDIP	N-28
AD9713BBN	–25°C to +85°C	28-Pin PDIP	N-28
AD9713BAP	–25°C to +85°C	28-Pin PLCC	P-28A
AD9713BBP	–25°C to +85°C	28-Pin PLCC	P-28A
AD9713BSQ/883B	–55°C to +125°C	28-Pin Cerdip	Q-28
AD9713BSE/883B	–55°C to +125°C	28-Pin LCC	E-28A
AD9713BTQ/883B	–55°C to +125°C	28-Pin Cerdip	Q-28
AD9713BTE/883B	–55°C to +125°C	28-Pin LCC	E-28A

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

PIN DESCRIPTIONS

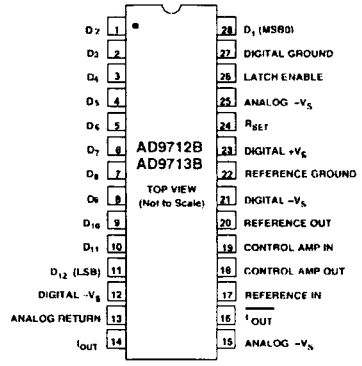
Pin #	Name	Function
1-10	D_2–D_{11}	Ten bits of twelve-bit digital input word.
11	D_{12} (LSB)	Least Significant Bit (LSB) of digital input word.
12	DIGITAL $-V_S$	One of two negative digital supply pins; nominally –5.2 V.
13	ANALOG RETURN	Analog ground return. This point and the reference side of the DAC load resistors should be connected to the same potential (nominally ground).
14	I_{OUT}	Analog current output, full-scale output occurs with digital inputs at all "1."
15	ANALOG $-V_S$	One of two negative analog supply pins; nominally –5.2 V.
16	$\overline{I_{OUT}}$	Complementary analog current output; zero scale output occurs with digital inputs at all "1."
17	REFERENCE IN	Normally connected to CONTROL AMP OUT (Pin 18). Direct line to DAC current source network. Voltage changes at this point have a direct effect on the full-scale output value of unit. Full-scale current output = 128 (Reference voltage/R_{SET}) when using internal amplifier.
18	CONTROL AMP OUT	Normally connected to REFERENCE INPUT (Pin 17). Output of internal control amplifier, which provides a temperature-compensated drive level to the current switch network.
19	CONTROL AMP IN	Normally connected to REFERENCE OUT (Pin 20) if not connected to external reference.
20	REFERENCE OUT	Normally connected to CONTROL AMP IN (Pin 19). Internal voltage reference, nominally 1.18 V.
21	DIGITAL $-V_S$	One of two negative digital supply pins; nominally –5.2 V.
22	REFERENCE GROUND	Ground return for the internal voltage reference and amplifier.
23	DIGITAL $+V_S$	Positive digital supply pin, used only on the AD9713B; nominally +5 V. No connection to this pin on AD9712B.
24	R_{SET}	Connection for external resistance reference. Full-scale current out = 128 (Reference voltage/R_{SET}) when using internal amplifier. Nominally 7.5 kΩ.
25	ANALOG $-V_S$	One of two negative analog supply pins; nominally –5.2 V.
26	LATCH ENABLE	Transparent latch control line. Register is transparent when LATCH ENABLE is LOW.
27	DIGITAL GROUND	Digital ground return.
28	D_1 (MSB)	Most Significant Bit (MSB) of digital input word.

Input Coding vs. Current Output

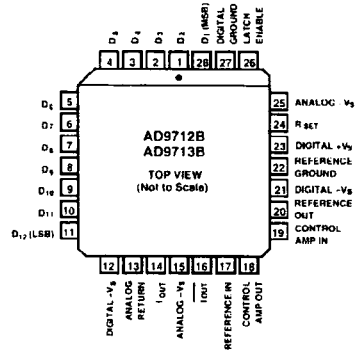
Input Code D_1–D_{12}	I_{OUT} (mA)	$\overline{I_{OUT}}$ (mA)
111111111111	–20.475	0
000000000000	0	20.475

PIN CONFIGURATIONS

DIP

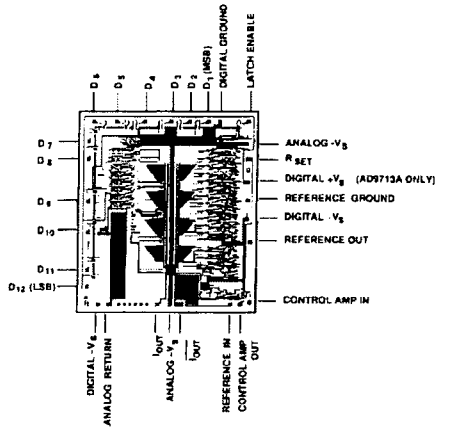


PLCC/LCC



DIE LAYOUT AND METALIZATION INFORMATION

Die Dimensions	220 × 196 × 15 (±2) mils
Pad Dimensions	4 × 4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Nitride



THEORY AND APPLICATIONS

The AD9712B and AD9713B high speed digital-to-analog converters utilize Most Significant Bit (MSB) decoding and segmentation techniques to reduce glitch impulse and maintain 12-bit linearity without trimming.

As shown in the functional block diagram, the design is based on four main subsections: the Decoder/Driver circuits, the Transparent Latches, the Switch Network, and the Control Amplifier. An internal bandgap reference is also included to allow operation with a minimum of external components.

Digital Inputs/Timing

The AD9712B employs single-ended ECL-compatible inputs for data inputs D_1–D_{12} and LATCH ENABLE. The internal ECL midpoint reference is designed to match 10K ECL device thresholds. On the AD9713B, a TTL translator is added at each input; with this exception, the AD9712B and AD9713B are identical.

In the Decoder/Driver section, the four MSBs (D_1–D_4) are decoded to 15 "thermometer code" lines. An equalizing delay is included for the eight Least Significant Bits (LSBs) and LATCH ENABLE. This delay minimizes data skew, and data setup and hold times at the latch inputs; this is important when operating the latches in the transparent mode. Without the delay, skew caused by the decoding circuits would degrade glitch impulse.

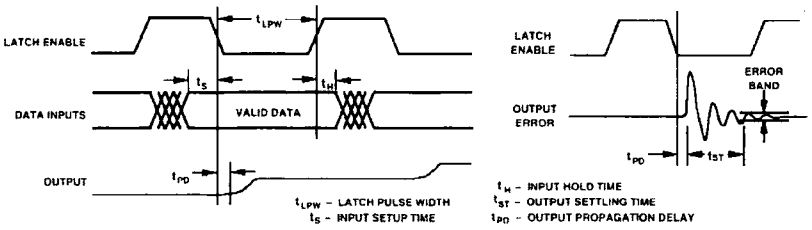
The latches operate in their transparent mode when LATCH ENABLE (Pin 26) is at logic level "0." The latches should be used to synchronize data to the current switches by applying a narrow LATCH ENABLE pulse with proper data setup and hold times as shown in the Timing Diagram. An external latch at each data input, clocked out of phase with the Latch Enable, operates the AD9712B/AD9713B in a master slave (edge-triggered) mode. This is the optimum way to operate the DAC because data is always stable at the DAC input. An external latch eases timing constraints when using the converter.

Although the AD9712B/AD9713B chip is designed to provide isolation from digital inputs to the outputs, some coupling of digital transitions is inevitable, especially with TTL or CMOS inputs applied to the AD9713B. Digital feedthrough can be reduced by forming a low-pass filter using a (200 Ω) series resistor in series with the capacitance of each digital input; this rolls off the slew rate of the digital inputs.

References

As shown in the functional block diagram, the internal bandgap reference, control amplifier, and reference input are pinned out for maximum user flexibility when setting the reference.

When using the internal reference, REFERENCE OUT (Pin 20) should be connected to CONTROL AMP IN (Pin 19). CONTROL AMP OUT (Pin 18) should be connected to REFERENCE IN (Pin 17) through a 20 Ω resistor. A 0.1 μF ceramic capacitor from Pin 17 to $-V_S$ (Pin 15) improves settling by decoupling switching noise from the current sink base line. A reference current cell provides feedback to the control amp by sinking current through R_{SET} (Pin 24).



Timing Diagram

Full-scale output current is determined by CONTROL AMP IN and R_{SET}, according to the equation:

$$I_{OUT}\,(FS) = (CONTROL\ AMP\ IN/R_{SET}) \times 128$$

The internal reference is nominally −1.18 V with a tolerance of ±3.5% and typical drift over temperature of 50 ppm/°C. If greater accuracy or better temperature stability is required, an external reference can be utilized. The AD589 reference shown in Figure 1 features ±10 ppm/°C drift over temperatures from 0°C to +70°C.

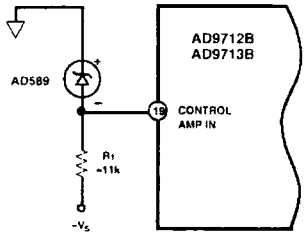


Figure 1. Use of AD589 as External Reference

Two modes of multiplying operation are possible with the AD9712B/AD9713B. Signals with small signal bandwidths up to 300 kHz and input swings of 100 mV, or dc signals from −0.6 V to −1.2 V can be applied to the CONTROL AMP input as shown in Figure 2. Because the control amplifier is internally compensated, the 0.1 μF capacitor at Pin 17 can be reduced to 0.01 μF to maximize the multiplying bandwidth. However, it should be noted that settling time for changes to the digital inputs will be degraded.

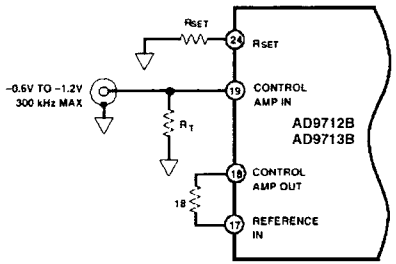


Figure 2. Low Frequency Multiplying Circuit

The REFERENCE IN pin can also be driven directly for wider bandwidth multiplying operation. The analog signal for this mode of operation must have a signal swing in the range of −3.75 V to −4.25 V. This can be implemented by capacitively coupling into REFERENCE IN a signal with a dc bias of −3.75 V to −4.25 V, as shown in Figure 3; or by driving REFERENCE IN with a low impedance op amp whose signal swing is limited to the stated range.

Outputs

As indicated earlier, D_1–D_4 (four MSBs) are decoded and drive 15 discrete current sinks. D5 and D6 are binarily weighted; and D_7–D_{12} are applied to the R-2R network. This segmented architecture reduces frequency domain errors due to glitch impulse.

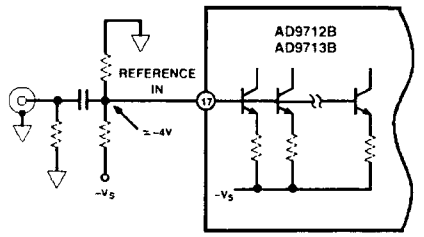


Figure 3. Wideband Multiplying Circuit

The Switch Network provides complementary current outputs I_{OUT} and $\overline{I_{OUT}}$. These current outputs are based on statistical current source matching which provides 12-bit linearity without trim. Current is steered to either I_{OUT} or $\overline{I_{OUT}}$ in proportion to the digital input code. The sum of the two currents is always equal to the full-scale output current minus one LSB.

The current output can be converted to a voltage by resistive loading as shown in Figure 4. Both I_{OUT} and $\overline{I_{OUT}}$ should be loaded equally for best overall performance. The voltage which is developed is the product of the output current and the value of the load resistor.

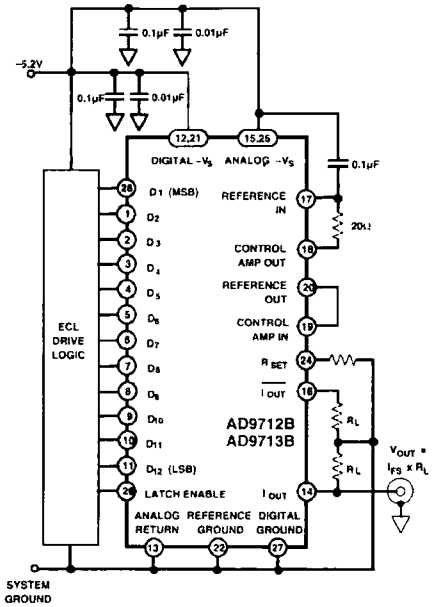


Figure 4. Typical Resistive Load Connection

An operational amplifier can also be used to perform the I to V conversion of the DAC output. Figure 5 shows an example of a circuit which uses the AD9617, a high speed, current feedback amplifier.

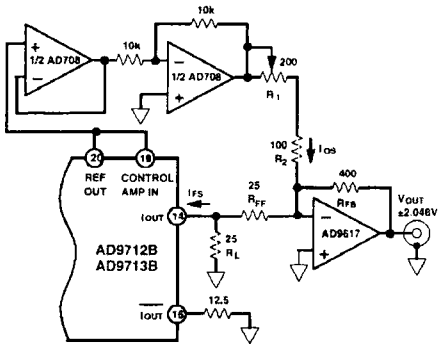


Figure 5. I/V Conversion Using Current Feedback

DAC current across feedback resistor R_{FB} determines the AD9617 output swing. A current divider formed by R_L and R_{FF} limits the current used in the I-to-V conversion, and provides an output voltage swing within the specifications of the AD9617. Current through R_2 provides dc offset at the output of the AD9617. Adjusting the value of R_L adjusts the value of offset current. This offset current is based on the reference of the AD9712B/AD9713B, to avoid coupling noise into the output signal.

The resistor values in Figure 5 provide a 4.096 V swing, centered at ground, at the output of the AD9617 amplifier.

Power and Grounding

Maintaining low noise on power supplies and ground is critical for obtaining optimum results with the AD9712B or AD9713B. DACs are most often used in circuits which are predominantly digital. To preserve 12-bit performance, especially at conversion speeds up to 100 MSPS, special precautions are necessary for power supplies and grounding.

Ideally, the DAC should have a separate analog ground plane. All ground pins of the DAC, as well as reference and analog output components, should be tied directly to this analog ground plane. The DAC's ground plane should be connected to the system ground plane at a single point.

Ferrite beads such as the Stackpole 57-1392 or Amidon FB-43B-101, along with high frequency, low-inductance decoupling capacitors, should be used for the supply connections to isolate digital switching currents from the DAC supply pins. Separate isolation networks for the digital and analog supply connections will further reduce supply noise coupling to the output.

Molded socket assemblies should be avoided even when prototyping circuits with the AD9712B or AD9713B. When the DAC cannot be directly soldered into the board, individual pin sockets such as AMP #6-330808-0 (knock-out end), or #60330808-3 (open end) should be used. These have much less effect on inter-lead capacitance than do molded assemblies.

DDS Applications

Numerically controlled oscillators (NCOs) are digital devices which generate samples of a sine wave. When the NCO is combined with a high performance D/A converter (DAC), the combination system is referred to as a Direct Digital Synthesizer (DDS).

The digital samples generated by the NCO are reconstructed by the DAC and the resulting sine wave is usable in any system which requires a stable, spectrally pure, frequency-agile reference. The DAC is often the limiting factor in DDS applications, since it is the only analog function in the circuit. The AD9712B/AD9713B D/A converters offer the highest level of performance available for DDS applications.

DC linearity errors of a DAC are the dominant effect in low-frequency applications and can affect both noise and harmonic content in the output waveform. Differential Nonlinearity (DNL) errors determine the quantization error between adjacent codes, while Integral Nonlinearity (INL) is a measure of how closely the overall transfer function of the DAC compares with an ideal device. Together, these errors establish the limits of phase and amplitude accuracy in the output waveform.

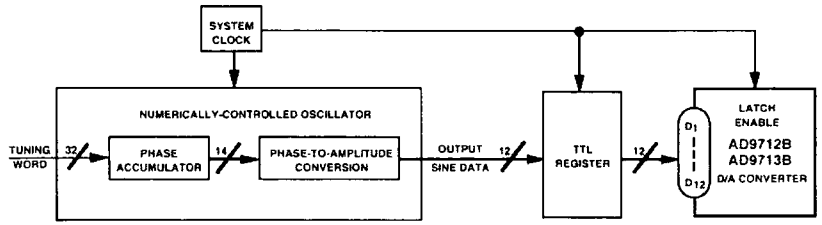


Figure 6. Direct Digital Synthesizer Block Diagram

When the analog frequency (f_A) is exactly f_C/N and N is an even integer, the DDS continually uses a small subset of the available DAC codes. The DNL of the converter is effectively the DNL error of the codes used, and is typically worse than the error measured against all available DAC codes. This increase in DNL is translated into higher harmonic and noise levels at the output.

Glitch impulse, often considered a figure of merit in DDS applications, is simply the initial transient response of the DAC as it moves between two output levels. This nonlinearity is commonly associated with external data skew, but this effect is minimized by using the on-board registers of the AD9712B/AD9713B converters (see Digital Inputs/Timing section). The majority of the glitch impulse, shown below, is produced as the current in the R-2R ladder network settles, and is fairly constant over the full-scale range of the DAC. The fast transients which form the glitch impulse appear as high-frequency spurs in the output spectrum.

While it is difficult to predict the effects of glitch on the output waveform, slew rate limitations translate directly into harmonics. This makes slew rate the dominant effect in ac linearity of the DAC. Applications in which the ratio of analog frequency (f_A) to clock frequency (f_C) is relatively high will benefit from the high slew rate and low output capacitance of the AD9712B/AD9713B devices.

Another concern in DDS applications is the presence of aliased harmonics in the output spectrum. Aliased harmonics appear as spurs in the output spectrum at frequencies which are determined by:

$$Mf_A \pm Nf_C$$

where M and N are integers.

The effects of these spurs are most easily observed in applications where f_A is nearly equal to an integer fraction of the clock rate. This condition causes the aliased harmonics to fold near the fundamental output frequency (see Performance Curves.)

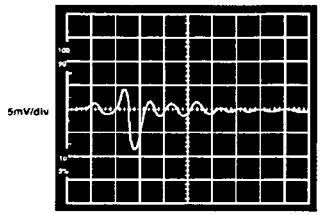


Figure 7. AD9712B/AD9713B Glitch Impulse

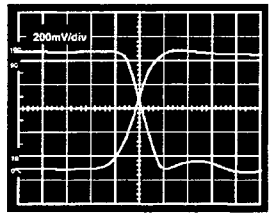


Figure 8. Rise and Fall Characteristics

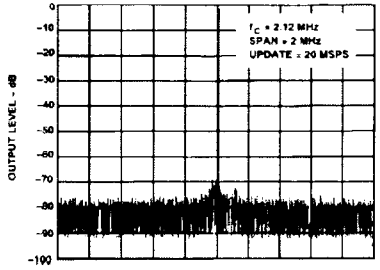


Figure 9a.

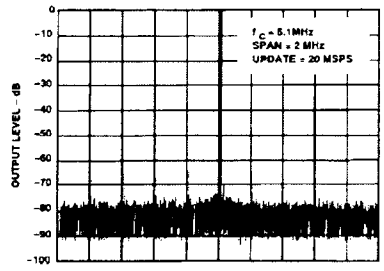


Figure 9b.

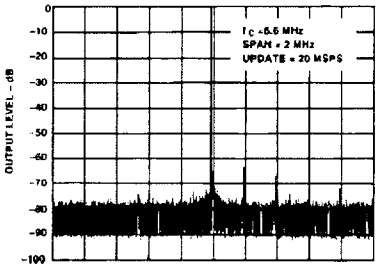


Figure 9c.

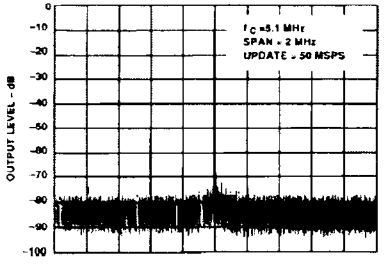


Figure 9d.

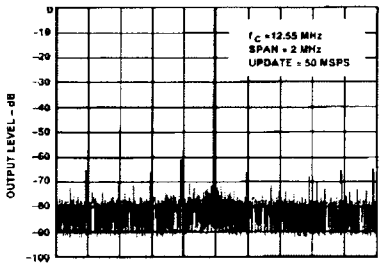


Figure 9e.

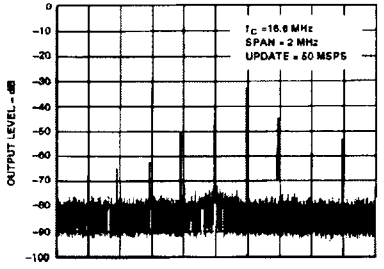


Figure 9f.

Figure 9. Typical Spectral Performance

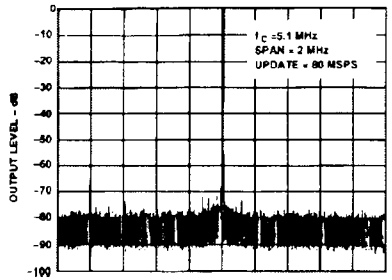


Figure 10a.

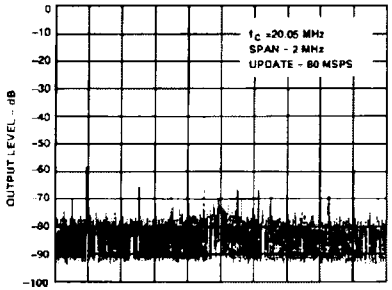


Figure 10b.

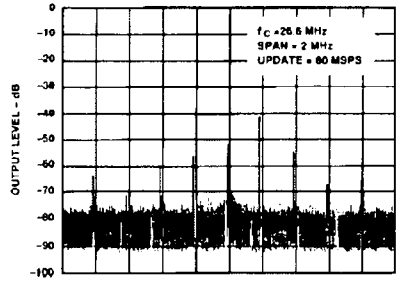


Figure 10c.

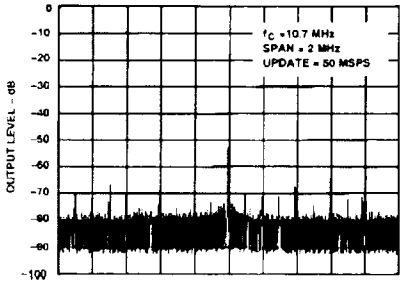


Figure 10d.

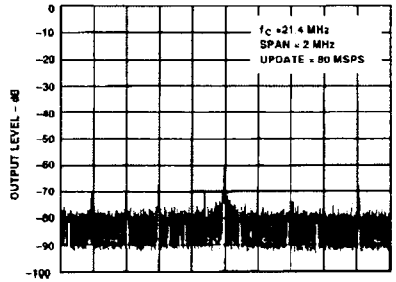
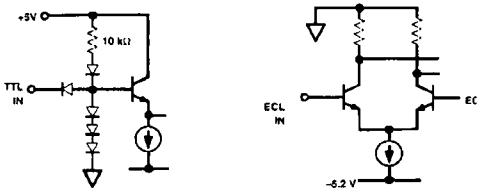
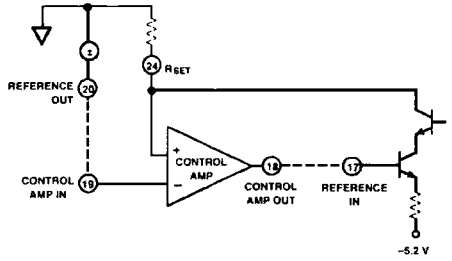


Figure 10e.

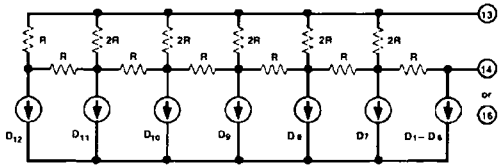
Figure 10. Typical Spectral Performance



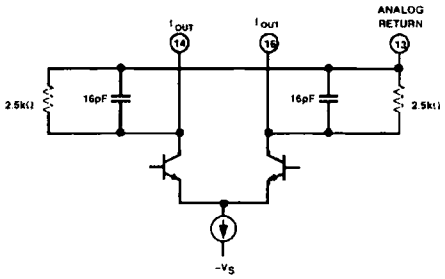
TTL Input Buffer ECL Input Buffer



Full-Scale Current Control Loop



R-2R DAC (for 6 LSBs)



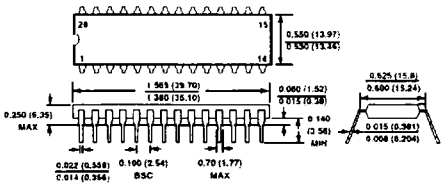
Output Circuit

Figure 11. Equivalent Ci

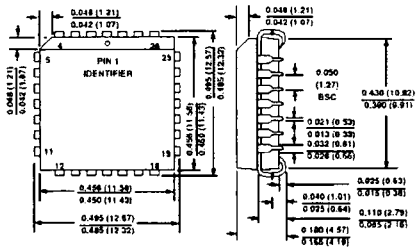
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

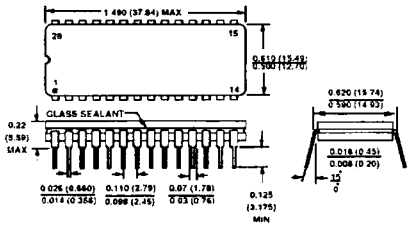
28-Pin Plastic DIP (Suffix N)



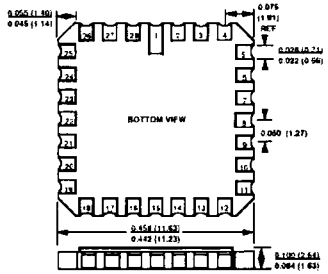
28-Pin Plastic Leaded Chip Carrier (Suffix P)



28-Pin Cerdip (Suffix Q)

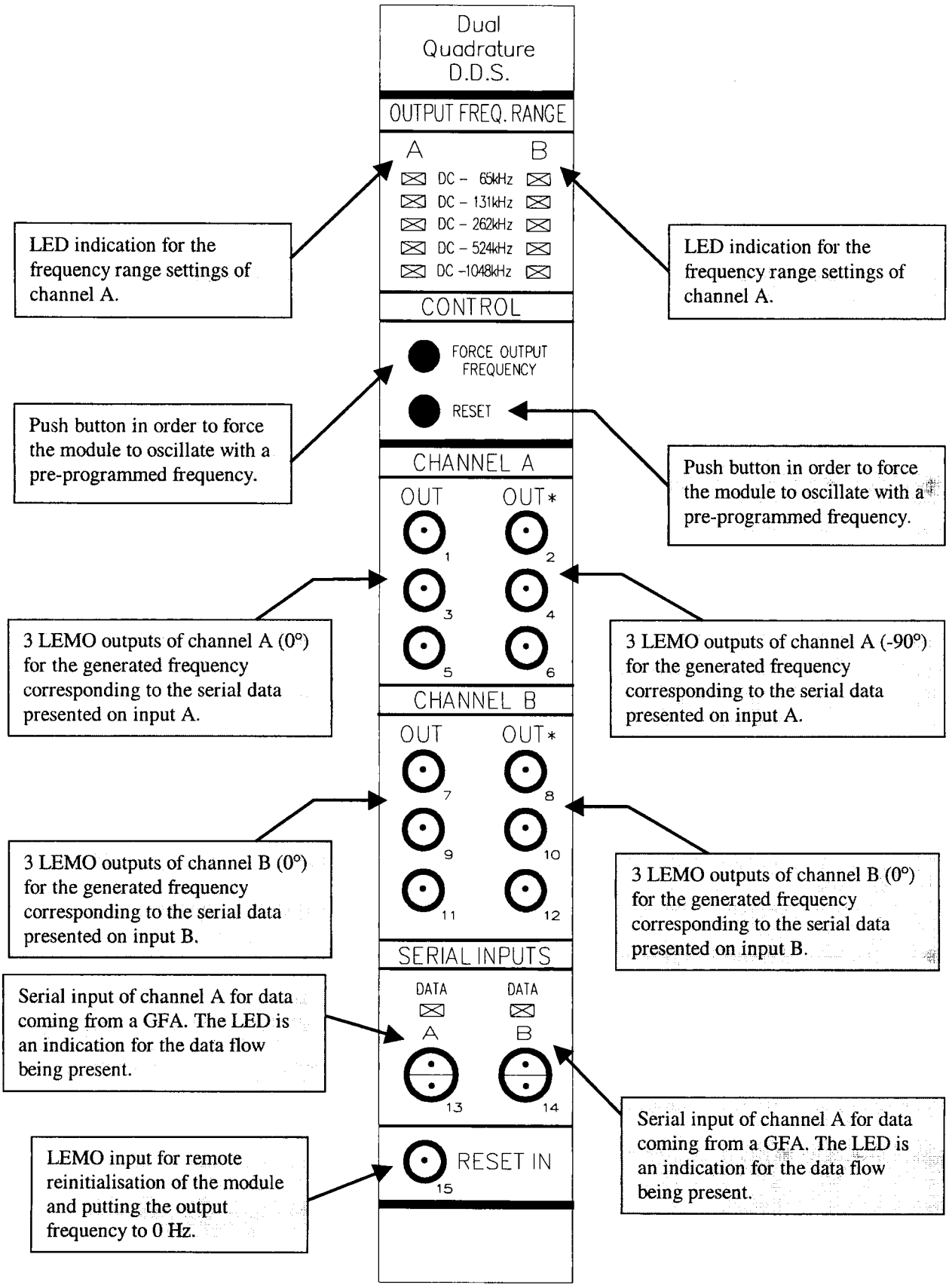


28-Pin LCC Package (Suffix E)



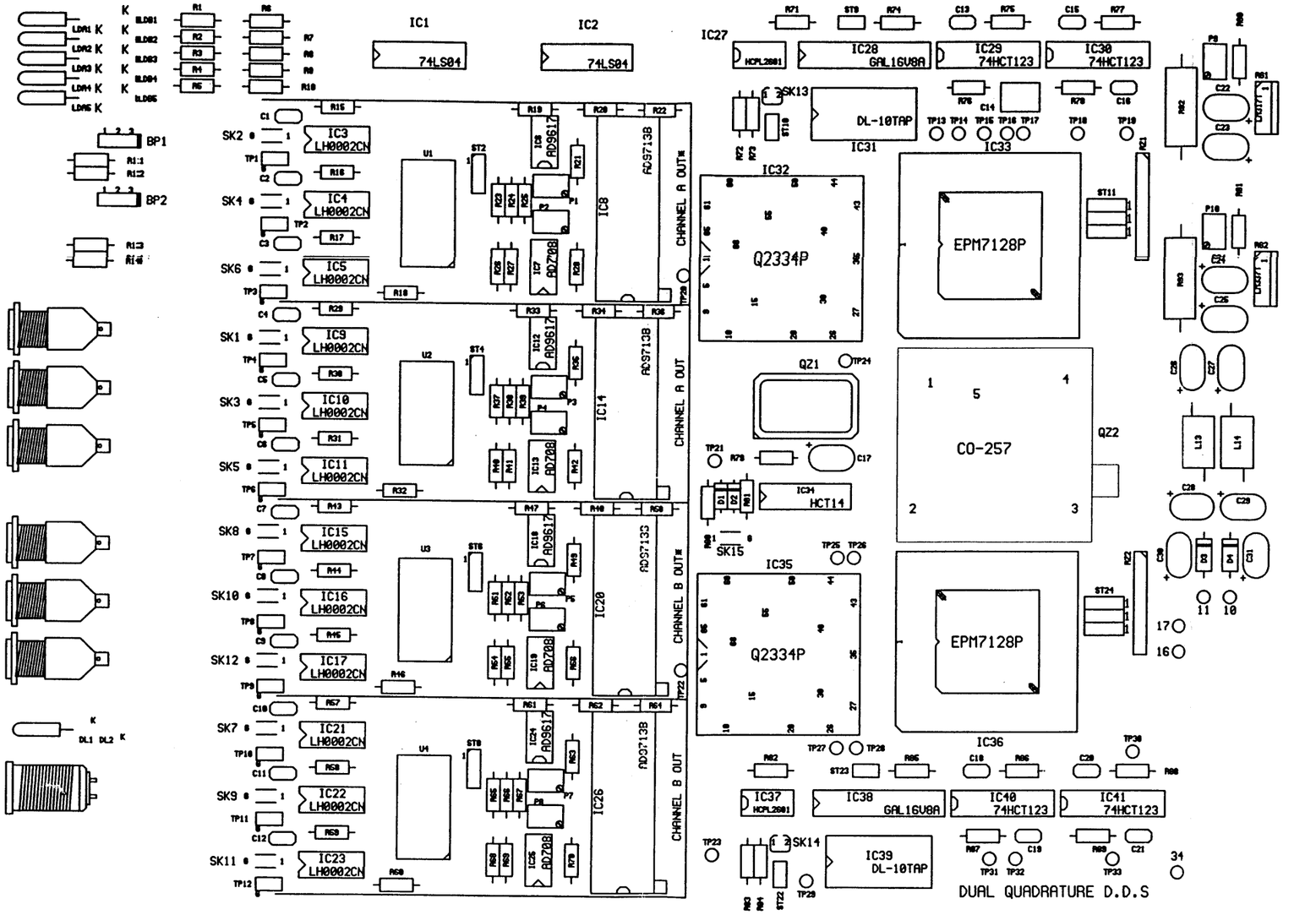
Annex 5.

The Dual Quadrature Direct Digital Synthesizer module front panel.


Dual
Quadrature
D.D.S.
OUTPUT FREQ. RANGE
A
B
DC - 65kHz
DC - 131kHz
DC - 262kHz
DC - 524kHz
DC -1048kHz
CONTROL
FORCE OUTPUT FREQUENCY
RESET
CHANNEL A
OUT
OUT*
1
2
3
4
5
6
CHANNEL B
OUT
OUT*
7
8
9
10
11
12
SERIAL INPUTS
DATA
A
DATA
B
13
14
RESET IN
15
LED indication for the frequency range settings of channel A.
LED indication for the frequency range settings of channel A.
Push button in order to force the module to oscillate with a pre-programmed frequency.
Push button in order to force the module to oscillate with a pre-programmed frequency.
3 LEMO outputs of channel A (0°) for the generated frequency corresponding to the serial data presented on input A.
3 LEMO outputs of channel A (-90°) for the generated frequency corresponding to the serial data presented on input A.
3 LEMO outputs of channel B (0°) for the generated frequency corresponding to the serial data presented on input B.
3 LEMO outputs of channel B (0°) for the generated frequency corresponding to the serial data presented on input B.
Serial input of channel A for data coming from a GFA. The LED is an indication for the data flow being present.
Serial input of channel A for data coming from a GFA. The LED is an indication for the data flow being present.
LEMO input for remote reinitialisation of the module and putting the output frequency to 0 Hz.

Annex 6.

The Printed Circuit Board component view.



CERN ECP/PES	PS 680-3130-050	A	Nbre de couche : 4
	DESS	STEERENBERG_R LOPEZ_N CEGELEC	Ep. du cuivre : 35u
			Ep. du circuit : 1,6
	DATE	04 II 1999	Matiere du CI : EPOXY

SERIGRAPHIE C-SIDE