PS/RF/Note 90-9
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PROGRAMMABLE DELAY CIRCUIT
AD9501 TEST CIRCUIT

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Contents

1. Introduction to Kickers and Septa in the PS accelerator.

1.1 General Description

Particle beam injection or ejection from the PS accelerator is acheived using combinations of **kicker** and **septum** magnets. At any point in time, there can be 20 bunches of particles within the PS accelerator constituting the particle beam. The travel time of one bunch is 30ns and one cycle of the accelerator takes approximately 2.1μs. To eject a bunch of particles, a magnetic field is established using a kicker magnet which forces the beam into betatronic oscillation. In effect, what this does is to produce a beam oscillation which results in an abnormal path of travel for the beam. At a calculated point, the displaced beam will travel into the influence of a septum magnet which will pull the required bunch of particles out of the beam. The selected bunch of particles will then pass along a transfer line to their required destination.

1.2 Kicker Magnet Pulses

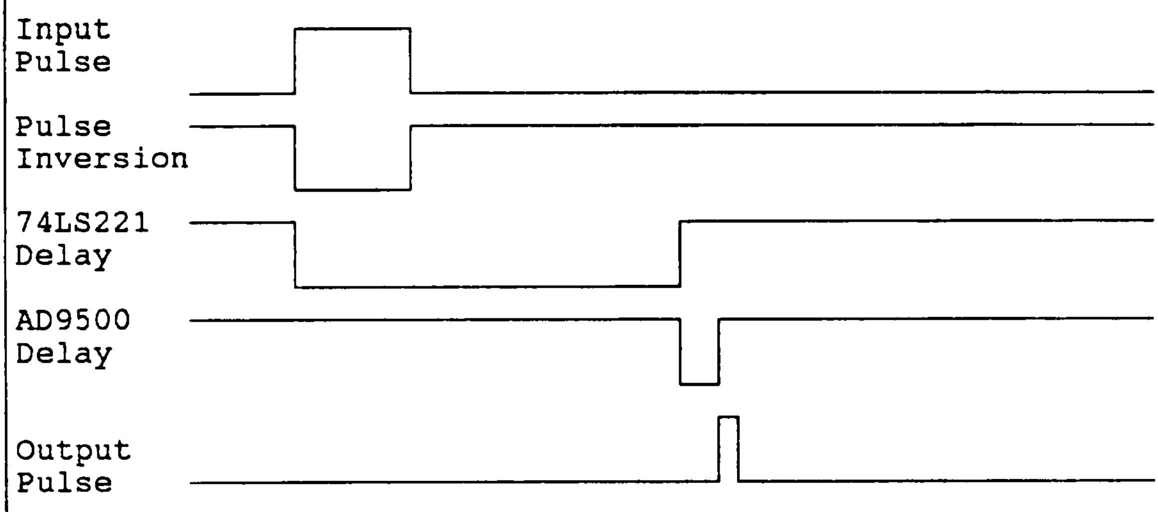
Because of the short time separation between successive bunches, a very fast pulse rise-time much be acheived. Hence, if a magnet is to be used, inductance must be minimal. Within the PS complex, **delay-line magnets** are used to this effect, with PFN's being used to supply pulses at 30kV-80kV. A **thyratron** is used to switch the charged PFN to the kicker magnet. Two thyratrons, connected at either end of the PFN, can be used to produce pulse widths of varying duration.

2. Introduction to the Dual Programmable Delay Circuit

2.1 Description of the original circuit

The **Dual Programmable Delay Unit** was originally designed to allow the selection of a delay period Ts, where the value of Ts was in the range **0 - 2.225μs.** The delay period Ts was the time between the triggering edge of a positive input pulse and a delayed output pulse of very small width. The delay time Ts was manufactured using 74LS221 dual single-shot chips and Analog Device's **AD9500 Digitally Programmable Delay Generator.** Delays of duration 0, 1μs and 2μs could be obtained from the 74LS221 chips through selection via an HEF4051 demultiplexer. The AD9500 was then triggered using the trailing edge of the main delay from the single shot chips. The value of the additional delay from the AD9500 chip was either set manually or by remote control. The timing is shown pictorially in Figure 1.

Figure 1 : Timing Diagram for original dual-delay circuit.



The circuit schematic diagram is contained in Appendix A. The orignal design was based on CIM 25543 cards, and the PCB layout can be found in Appendix B.

3. Dual Delay circuit with AD9501 I.C's

3.1 Comment on AD9501 Programmable Delay generator

The AD9501 Digitally Programmable Delay Generator is the heart of the dual programmable delay circuit. The AD9501 is a successor to the AD9500. There are a number of differences between the two chips, as listed below :

AD9500	AD9501
2.5ns - 100μs FSR	2.5ns - 10μs FSR
+ve and -ve triggering	+ve triggering only
Multiple voltage supply	Single +5V voltage supply
24 pin package	20 pin package
10ps min delay resolution	10ps min delay resolution

The reason for using the AD9501 as a replacement for the AD9500 chip was to investigate whether the jitter problems associated with the AD9500 had been overcome by the re-design. The functional block diagrams for both devices are shown in Figures 2 and 3 below.

Figure 2 : AD9500 Functional Block Diagram

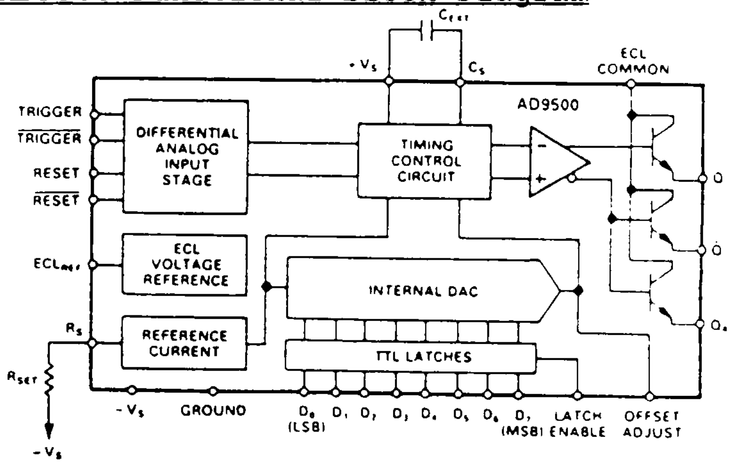
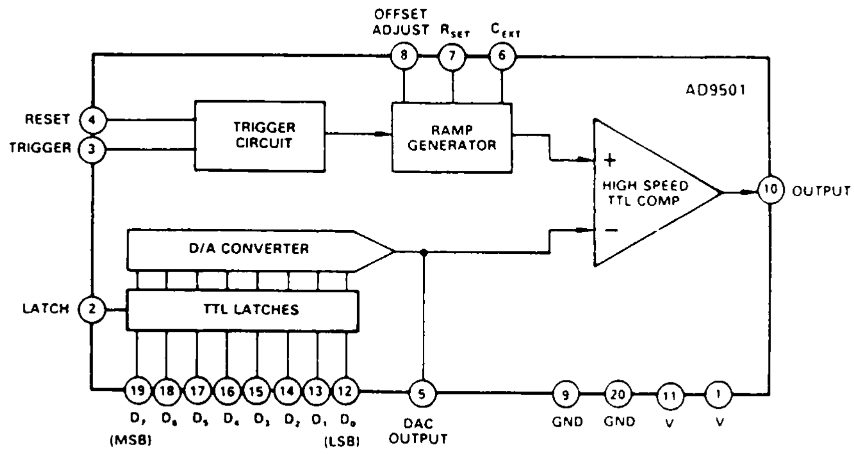


Figure 3 : AD9501 Functional Block Diagram



3. Dual Delay circuit with AD9501 I.C's

The AD9501 would appear to be a simpler version of the AD9500, with the disadvantages of only rising edge triggering and Q outputs, but with the advantage of only 1 +5V power supply requirement compared to +5V, -2V and -5.2V for the AD9500. Some device information from the Analog Devices data sheets is contained in Appendix C.

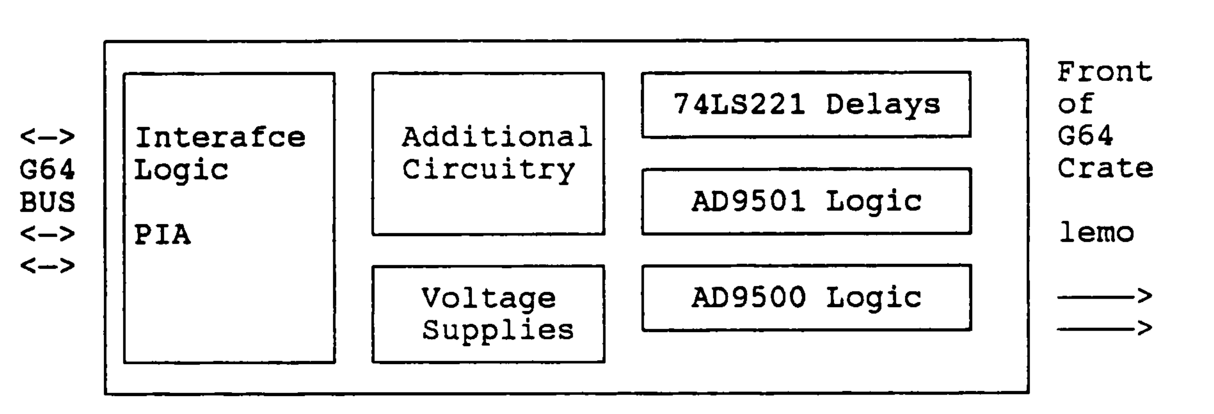
3.2 Objectives of the AD9501 test board

The aim is to build the essential parts of the dual delay circuit, modifying where necessary to incorporate the new AD9501. The circuit contains a single co-axial connector input, the input signal being the standard CERN pulse. This signal is 'shared' by both the AD9500 and the AD9501 circuits on the same board, thus allowing very good comparison of the respective performances. Two seperate co-axial outputs, one for each device, are incorporated into the circuit. Both devices are controlled by the same test software, written in C. **The circuit performance specification is to allow the selection of a delay between the input and output pulses within the range 0 - 2005 ns, with an accuracy of 1ns.**

3.3 Development of the AD9501 test circuit

The test circuit was implemented on a G64 card, giving a useful reduction in size compared to the previous design on CAMAC cards. Because minimal connection lengths were of importance to avoid transmission line effects, an approximate board layout as shown in Figure 4 was produced.

Figure 4 : Delay Circuit approximate layout.



3. Dual Delay circuit with AD9501 I.C's

At first, the use of the 74LS221 I.C's to provide a main delay was used as implemented on the schematic diagram contained in Appendix A. However, upon testing and analysis, it was found that the requirement of allowing the selection of any delay within the range 0 - 2.225μs with 1ns resolution could not be acheived using the design as shown. From the circuit shown in Appendix A, delays could be acheived in the ranges : 0 - 255ns, 1μs - 1.225μs and 2 - 2.225μs, but not continuously. A solution to this problem, giving the choice of any delay between 0 and 4μs, with 1ns accuracy, was proposed using 2 dual 74LS221 single-shot chips. Four delay times would be available from the single-shots... 250ns, 500ns, 1μs and 2 μs. By using a combination of these delays and the 255ns available from the digitally programmable delay generator, any delay within the range 0 - 4μs could be obtained. Upon development of this circuit however, a number of problems were encountered. The control logic for selecting the required delay could not be readily implemented using boolean algebra, because of the requirement that signals be isolated to prevent unwanted triggering. To overcome this, and to also provide a clean path for signals, tri-directional reed relays were selected as the appropriate method for chip selection. However, when testing, a large amount of signal attenuation was discovered across the reed relays. It was suggested that the reason for this was due to voltage drop across the effective contact resistance of the reed relays. NPN transistors were used to boost current levels in an attempt to overcome this, but with little effect.

Having been unable to overcome this problem, an alternative solution was sought. The circuit performance was reduced to give a delay range of 0 - 2.005μs, 1ns resolution, and a more simple solution in terms of both hardware and software was acheived. Four 74LS221 single-shot I.C's, providing main delays in increments of 250ns, with the combination of the AD9500/9501, satisfy the specification, with selection of the main delay being acheived using a 1-8 line demultiplexer.

4. Hardware

4.1 Peripheral Interface Adaptor (PIA)

Interface between the test card and the MC68020 development system was acheived using the Motorola MC6821P PIA. The circuit diagram for the interface is contained in Appendix D.

The MC6821B PIA is interfaces the test card to the development system via two 8-bit bidirectional data buses and four control lines. The control lines are VPA, IRQ, FIRQ and NMI.

VPA = Valid Peripheral Address, tri-state, 48mA.
IRQ = Interupt Request , open-collector, 48mA.
FIRQ = Fast Interupt Request, open collector, 48mA.
NMI = Non maskable Interrupt, open-collector, 48mA.

(IRQ is connected to the PIA via a jumper.)

Both of the 8-bit bidirectional registers of the PIA have been programmed in the output mode. Port B has been selected as the data port for the demultiplexer, and port A is used for AD9500/9501 data.

Initially, data written from the G64 bus is written to a tri-state octal bus transceiver (74LS640) which is designed for asynchronous two-way communication between data buses. Normally, this device is used to transmit data from one bus to another, but in this configuration, the chip transfers data from the G64 bus to the MC6821 PIA. Data which is to be written to the card will either be destined for the demultiplexer or the AD9500/01. Thus the PIA port has to be selected also.

The address for the test card is written into a 74LS2521 eight-bit equal-to comparator. Verification of a valid peripheral address comes from this device. The 74LS2521 is connected to an 8-bit dip switch, the settings of which constitute the test card address. When the card is written to, the equal-to comparator will sense whether the address corresponds to the address on the DIP switches, and operation will be either allowed or denied.

4.2 Circuit voltage supplies

The dual delay circuit requires the following power supply connections : +5V dc, -2V dc and -5.2V dc, earth. The G64 bus allows immediate connection to +5V and earth, but the -2V and -5.2V supplies do not appear on the G64 bus and therefore have to be built into the circuit. Both supplies are obtained by employing LM337 adjustable voltage regulators to reduce the voltage levels as required. The output voltage is set by an external resistor divider arrangment. A potentiometer has been used to allow fine tuning of the output voltage when required, as shown in the circuit schematic diagram contained in Appendix E.

4. Hardware

74LS221 Dual Single Shot Multivibrators

The 74LS221 is a dual monostable multivibrator with Schmitt trigger input. The input to the device can be triggered on either the leading or trailing edge of the input pulse and the output pulse width can range from 30ns to 70s. Within the dual delay circuit, there are 4 74LS221 chips, giving a choice of 8 delays, selected by a 1-8 demultiplexer. The layout of the 221 chips on the test board is shown in Appendix F. The external timing resistors are variable to allow tuning of the output pulse width. The chip connections are contained on the test card schematic diagram in Appendix E.

HEF4051B 1-8 line demultiplexer

Selection of the required 74LS221 single shot pulse as calculated by the software is acheived using the HEF4051B chip. This is dual function device which can be used as either a multiplexer or a demultiplexer. By selecting the appropriate mode of operation, one of 8 independent outputs is connected to a common input by three control bits from the MC6821 PIA. The input pulse, after being inverted by a transistor configuration, passes to the desired single-shot via the deMUX, controlled by the PIA data.

4.5 AD9500 Digitally Programmable Delay Generator

This device can be used to produce pulse delays between 2.5ns and 100μs, with a maximum resolution under certain conditions of 10ps. The delay is selected by an 8-bit digital word, giving 256 possible variations of a base delay which is set by an external resistor-capacitor combination. The pin connections are shown in the circuit schematic diagram in Appendix E. For the external resistor Rs, a potentiometer has been selected to allow tuning of the programmable delay base-value, i.e 1ns. Triggering occurs on the rising edge of the -ve input pulse i.e triggering occurs **after** the delay set by the 221 single-shot's.

4.6 AD9501 Digitally Programmable Delay Generator

This device has been used in exactly the same manner as the AD9500, except for the differences already mentioned in section 3.1. Pin connections are shown on the schematic diagram.

4.7 Test and Measurement Points

The data transfered to the AD9500/9501 chips can be measured or set on the pins indicated on the circuit layout guide in Appendix F. Circuit voltage supplies can also be measured or set on the pins indicated.

5. Software

5.1 General Information

The test program for the dual-delay circuit is called **ADDP8.C** and can be found on the Motorola 68020 Development System hard disk in directory **/h0/STUART/DELAY.** The program has been written in C and can be edited using umacs. The program runs in a continous loop and can be halted by pressing the system reset button on the front panel of the development system.

5.2 PIA Addressing

To enable control of the dual-delay card from the development system a unique address has to be assigned to it. This address is easily set by the DIP switch combination within the PIA on the card. At present, the address is set as 00F Hex. This address has been entered into the SCF device descriptor in the I/O directory. The address in the SCF device descriptor file must correspond to the address set by the DIP switch pattern. If the address requires to be altered, please read the MC68020/OS9 notes written by Lanyu Wang (PS/RF) contained in Appendix G.

5.3 Test Program Structure & Operation

The program listing is contained on the following three pages. The program is made much simpler through the use of the C commands **PATH** and **WRITE** which enable simple defination of paths for the writing of data.

The data which is written to the dual-delay card is stored in a 2 byte buffer called **outputbuf[2].** The program asks the user to entered the required delay. This value should be in nanoseconds. The value which the user enters is stored in a variable called **rawdata.** The program is self-checking and controls the data which can be entered. The following conditions have been set within the program :

(a) The total delay shall not lie outwith the range 0 - 2005 ns inclusive. (b) The total numbers of characters entered by the user shall therefore not exceed 4. (c) The characters entered by the user shall all be numerical digits.

If a non-digit is entered by the user, then the error flag **errflag_1** is SET. Before checking to see if the delay value is within the legal range, the data contained in **rawdata** is converted into an integer an stored in the variable **rawval.** The contents of rawval are then tested and if they lie outside the legal range, then **errflag_2** is SET. If either of the error flags are set, then the user is given an explanation of the error and the program repeats until satisfactory data is entered.

Having established a value of total delay that is required, the program self calculates 2 delay values : a value which will be produced by selection of a 74LS221 single-shot, and a 'top-up' value which is produced by the digitally programmable delay generator chip. The value of the main delay from the single shot is stored in the variable **maindelay** and the value for the AD9500/01

5. Software

```
#include <stdio.h>
#include <ctype.h>
#include <modes.h>

main()
{   /*******************************************************/
    /* Main Program Start.                                  */
    /* Dual Programmable Delay Circuit Test Program         */
    /* Stuart Johnston  12.09.90     Version ADDP8.c        */
    /*                                                      */
    /* Program operation :                                  */
    /* User enters required value of total delay.           */
    /* Program calculates value of maindelay (obtained from */
    /* 74LS221 chips) and programmable delay (obtained from */
    /* AD9500/01 chips).                                    */
    /* Main delay data is stored in outputbuf[1]            */
    /* Programmable delay data is stored in outputbuf[0].   */
    /* The data is then read out to the G64 bus using read  */
    /* and the address $05000000 as defined in the SCF      */
    /* device descriptor.  The device descriptor is called  */
    /* dp.a and is located in the IO directory.             */
    /* Program error conditions:                            */
    /* errflag_1 is set when non-digit data is entered      */
    /* errflag_2 is set when delay is out of range          */
    /*******************************************************/

    char    outputbuf[2], rawdata[5] ;
    int     errflag_1, errflag_2, looprepeat ;
    int     numchars, ch, maindelay, progdelay, path ;
    int     rawval, dummy ;
    looprepeat = 0 ;

    /*******************************************************/
    /* Get value of delay from keyboard using readln.       */
    /* Delay is stored in buffer rawdata                    */
    /*******************************************************/

    do {
    do {
        errflag_1 = 0, errflag_2 = 0 ;

        printf("\n\n. . . . . . . . . . . . . . . . . . . . . . .
      \n") ;
        printf("Pulse Delay = Main Delay + Programmable Delay\n")
;
        printf("Main Delay Range = 0 to 1750ns\n") ;
        printf("Programmable Delay range = 0 to 255ns\n") ;
        printf("\nPlease enter total delay in NANOSECONDS :\n\n")
;
        numchars = readln(0,rawdata,5) ;
        printf(". . . . . . . . . . . . . . . . . . . . . . . .
 ") ;

    /*******************************************************/
    /* Check to see if non-digits were entered.             */
    /* Check contents of rawdata.                           */
```

5. Software

```
/* errflag_1 is set if error occurs.                          */
/*************************************************************/

    for (ch=0 ; ch<(numchars-1) ; ch++) {
        if (isdigit(rawdata[ch]) == 0) {
            errflag_1 = 1 ;
            printf("\n*** ERROR : Non digit entered ***\n") ;
        }
    }

/*************************************************************/
/* Conversion of buffer data into integer variable           */
/* to allow arithmetic operations.                           */
/*************************************************************/

    rawval = atoi(rawdata) ;

/*************************************************************/
/* Verify that total delay is within legal range             */
/*************************************************************/

    if ( rawval < 0 || rawval > 2005 ) {
        errflag_2 = 1 ;
        printf("\n*** ERROR : Delay out of range  ***\n") ;
    }

/*************************************************************/
/* Perform arithmetic to select appropriate values           */
/* for maindelay and programmable delay based on             */
/* the value of the total delay.                             */
/*************************************************************/

    maindelay = 0, progdelay = 0, dummy = -250 ;
    do {
        dummy = dummy + 250 ;
    } while (rawval > dummy+255) ;

    maindelay = dummy ;
    progdelay = rawval - dummy ;

} while (errflag_1 == 1 || errflag_2 == 1 ) ;

printf("\n\nTotal delay from 221 chips = %d",maindelay) ;
printf("\nTotal delay from AD9500/01 = %d",progdelay) ;

/*************************************************************/
/* Calculate correct pattern of control bits for             */
/* deMultiplexer.  Output buffer contains 3 bits.            */
/* Copy values to output buffer outputbuf.                   */
/* It might not be very pretty, but it's really easy to */
/* make specific changes to the control output when you */
/* want to.                                                  */
/*************************************************************/

if (maindelay == 0)
    outputbuf[1] = 0;
```

5. Software

```
else if (maindelay == 250 )
    outputbuf[1] = 1;
else if (maindelay == 500 )
    outputbuf[1] = 2;
else if (maindelay == 750 )
    outputbuf[1] = 3;
else if (maindelay == 1000 )
    outputbuf[1] = 4;
else if (maindelay == 1250 )
    outputbuf[1] = 5;
else if (maindelay == 1500 )
    outputbuf[1] = 6;
else if (maindelay == 1750 )
    outputbuf[1] = 7;

outputbuf[0] = progdelay ;

/*********************************************************/
/* Send data to PIA                                      */
/*********************************************************/

path=open("/dp",2) ;
write(path,outputbuf,2) ;
close(path) ;

while (looprepeat == 0) ;


/*********************************************************/
/* PROGRAM END                                           */
/*********************************************************/
```

is stored in the variable **progdelay.**

Having calculated the individual components of the total delay, the actual data for writing to the G64 bus is calculated. As stated, the output buffer is two bytes in size. Byte zero, i.e outputbuf[0], is used for storing the programmable delay data. Byte one, outputbuf[1], is used for the main delay data. The main delay data is assigned using simple if/then/else statements. This could be written using a repeating loop, but modications can be made more easily when in the form shown. The data assigned as the main delay data are the control bits for the demultiplexor which selects the desired 74LS221 single-shot. The data sent to the digitally programmable delay generator can be used to provide delays up to 255ns in duration, with a resolution of 1ns.

The output data is sent to the card using a simple and very useful set of commands available in C. The path to the card is simply opened using the **PATH** command. Following this, the data is written out using the **WRITE** command. In the listing, the '2' nested within the write command means that the first 2 bytes of the buffer 'outputbuf' shuod be written on the path given.

The program is nested within a continuously repeating loop to allow continuous testing. The first occurance of "do {" at the beginning of the program, and "} while (looprepeat == 0) ;" at the end of the program can be removed to give single operations of the program without the need for a system reset if desired.

5.4 Running the software

Before running the software, the user has to initialize dp and load sc6821 and dp. The file **autor** will automatically do this for you.

When the MC68020 development system has been booted up, and you are located in the root directory, type the following commands to run the software :

autor [RETURN]
addp8 [RETURN]

5.5 Future modifications

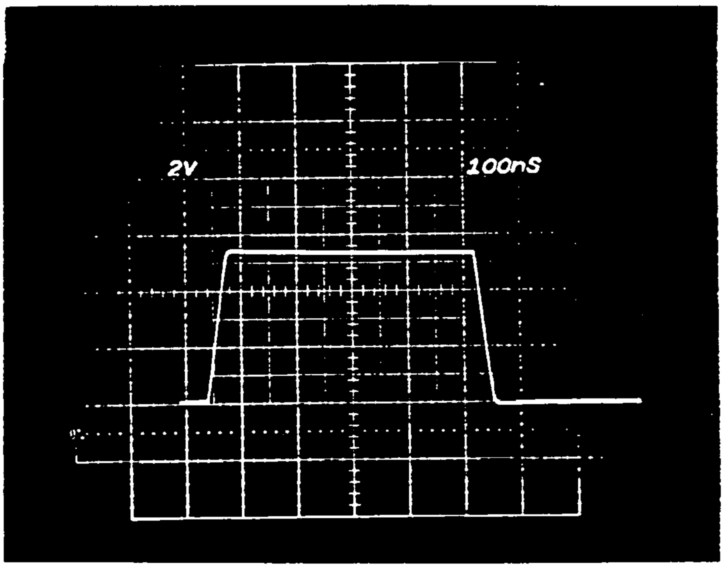
The software as written allows the selection of up to 8 main delay values using a demultiplexer. This can easily be expanded as required with only minor modifications to the software. The code which controls the digitally programmable delay generators should not required to be altered unless compensation for chip delays is introduced.

6. Testing

6.1 Input waveform description

The input pulse wavefrom used to test the circuit bears the characteristics of a standard CERN pulse. A Philips PM 5715 pulse generator is used to generate a pulse as shown in Figure 5. The amplitude of a standard CERN pulse can be as much as 30V, and this circuit will accept such signal levels. Testing was performed with a nominal amplitude of 10V for logic high and 0V for logic low. In Figure 5, the scale is 2V/small division, and 100ns/small division.

Figure 5 : Input pulse characterstics

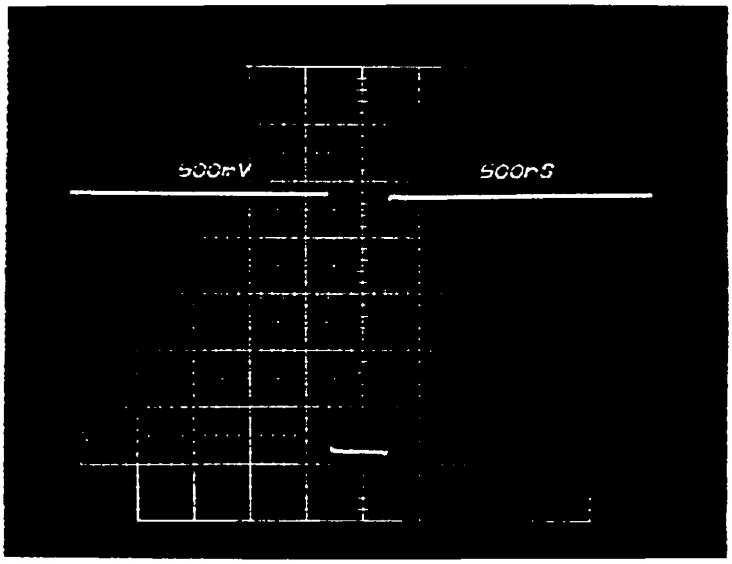


6.2 Input pulse inversion

The input pulse is fed into the base of a 2N2369 NPN transistor, the output being taken off the collector with emitter earthed. The waveform obtained is shown in Figure 6. The circuit design is such that the input pulse is a triggering event and as such does not constitute part of the overall delay period. The next stage of the circuit (74LS221 single shot i.c's) will not re-trigger after an initial triggering event until the set RC delay period has occured. Thus, small oscillations or overshoot in the signal do not produce multiple triggering events at the next stage in the circuit and can be ignored. In this sense, the 74LS221 chips provide some additional immunity to unwanted signals themselves. Clamping diodes are also used on the input, and the optional 50Ω terminating resistor between input signal and input ground was not required.

6. Testing

Figure 6 : Inverted pulse waveform



6.3 Programmable Interface Adaptor

Initially, the PIA would not function. The problem was found to be wrong addressing. It is very important that the PIA is given the same address as contained in the SCF device descriptor file, otherwise data will not be sent to the card and it is difficult to assertain the problem when this occurs. If the circuit fails, please check the condition of the voltages at the output of the basic switch module connected to the 8-bit comparator of the PIA module. The Interrupt Request signal **must** be connected to the MC6821 by a jumper. The circuit layout guide illustrates the necessary jumper position.

6.4 74LS221 Single Shot Multivibrators

The input triggering event for any of the 221 single shot chips is an inverted pulse from the collector of the input transistor, directed to the required 221 I.C by the 1-8 deMUX. There are no notable problems associated with these chips. The trailing edge of the output pulse from one of these chips does rise at an acceptable rate past the necessary threshold for subsequent triggering, and the small transient effect as can be seen in Figs 7 & 8 is not important.

The delay period of these chips is set by an RC combination as shown in the circuit schematic diagram (see Appendix E). The delay period $T_d = 0.7RC$. For calibration purposes, a variable resistor has been used for R. To allow accurate calibration, the value of C should be such that R is small, i.e to enable the use of a smaller valued potentiometer. A smaller change in R when calibrating allows finer tuning of the delay period. Ideally, R should be $< 500\Omega$ variable.

6. Testing

Figure 7 : 250ns delay from 74LS221 single shot

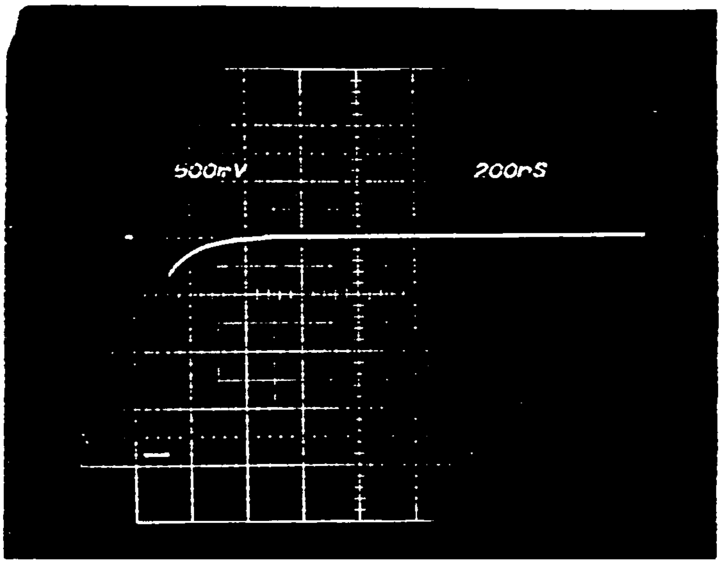
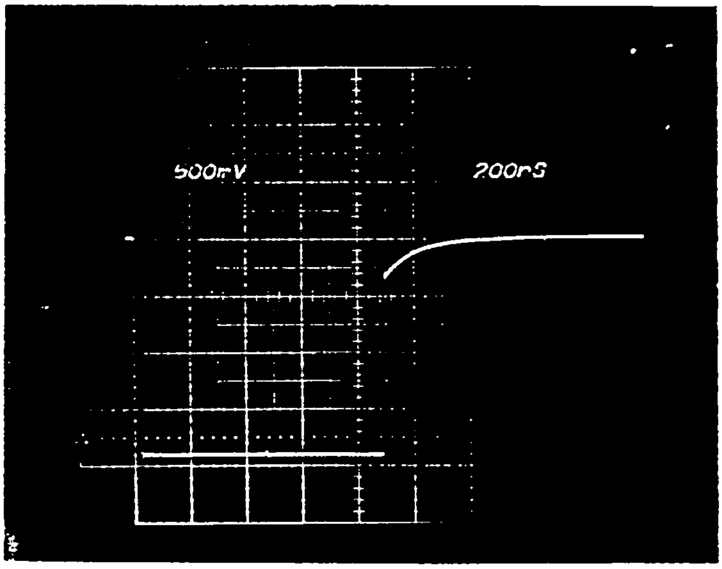


Figure 8 : 1.750μs delay from 74LS221 single shot



6.5 AD9500 Programmable Delay Generator

The resistor/capacitor combination to produce the minimum output delay of 1ns has been carefully calculated to provide accuracy. The output pulse width can be trimmed to 1μs exactly using the variable resistor which is connected to the ECL Voltage Reference pin. The triggering is being used in the opposite mode to the original dual-delay circuit design. In the new design, triggering occurs on the trailing edge of the pulse from the 221 single shot chip, i.e **after** the delay period. The 1μs output pulse will then be produced by the AD9500 after the additional

6. Testing

delay as programmed by the 8-bit digital word. All power supplies to this chip have been capacitively coupled because the device requires a high level of power supply noise immunity. The rising edge of the output pulse is shown with zero delay, and also for 30ns.

Figure 9 : 30ns delayed output from AD9500

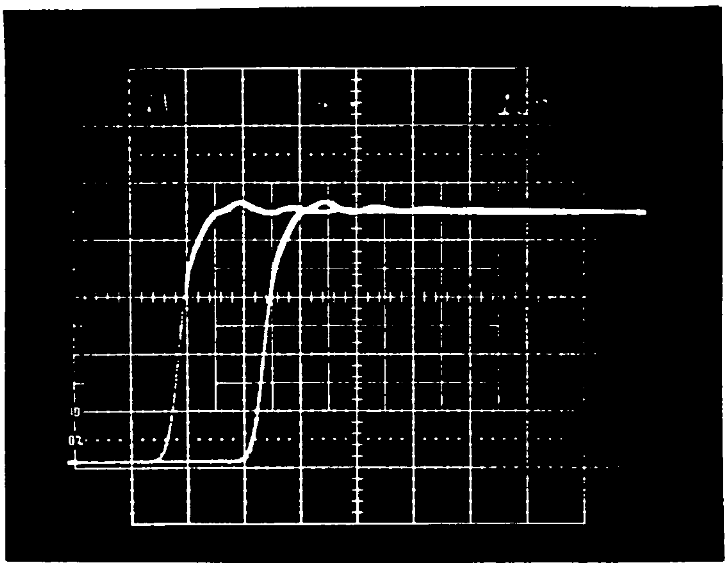


Figure 10 : 2ns delay steps from AD9500

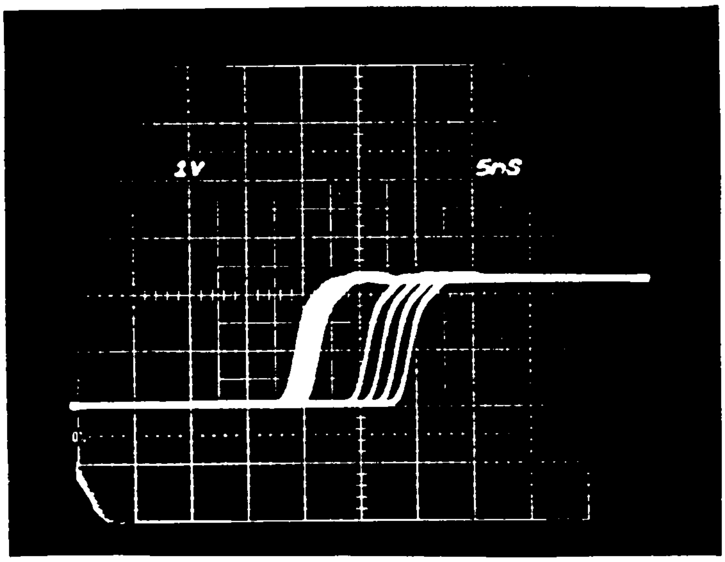


Figure 10 shows a number of different delayed pulses. At first, the delay increment is 2ns, followed by a number of delay increments of 5ns.

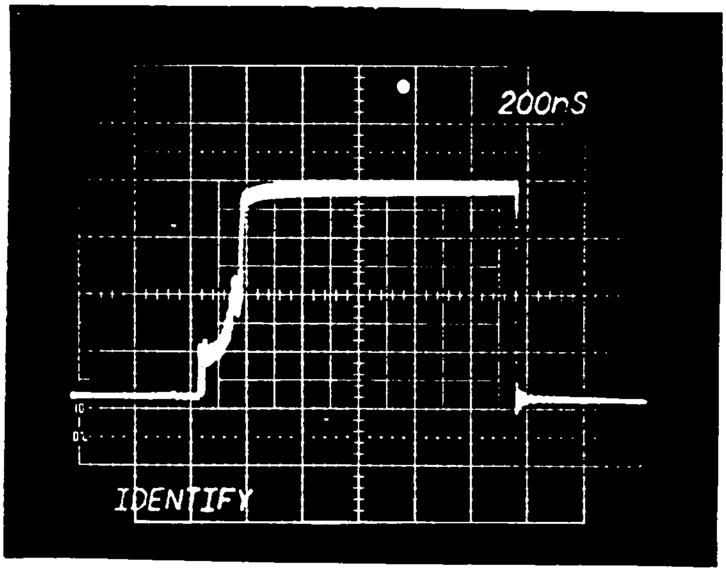
6. Testing

6.6 AD9501 Programmable Delay Generator

Initially, the AD9501 would not function. The reason was that the data sheets for the device are misleading in that they suggest chip RESET occurs on the rising edge of an input pulse to pin 4. However, the RESET is actually level sensitive and therefore some additional problems were encountered providing an appropriate reset signal. Eventually, the solution was to use an additional 74LS221 single shot to produce an external reset. The trigger signal is used to fire a single shot negative pulse delay. The rising edge of this pulse, occuring 1μs later, triggers the second half of the single shot which sends a positive pulse to the reset. Thus, 1μs after being triggered, a positive going pulse is received at the AD9501 RESET which resets the output. Output from the AD9501 is TTL/CMOS compatible and does not required MECL/TTL translation.

Having verified that the chip actually worked, the output signal was found to be of very poor quality, even though connection lengths had been kept to a minimum, as shown in Figure 11.

Figure 11 : Distorted output from AD9501



It is apparent that wire-wrap is not suitable for connections to the AD9501. A soldered circuit with a ground plane should function as required. The circuit as shown is functionally correct and does react properly to the commands from the test software.

Comments

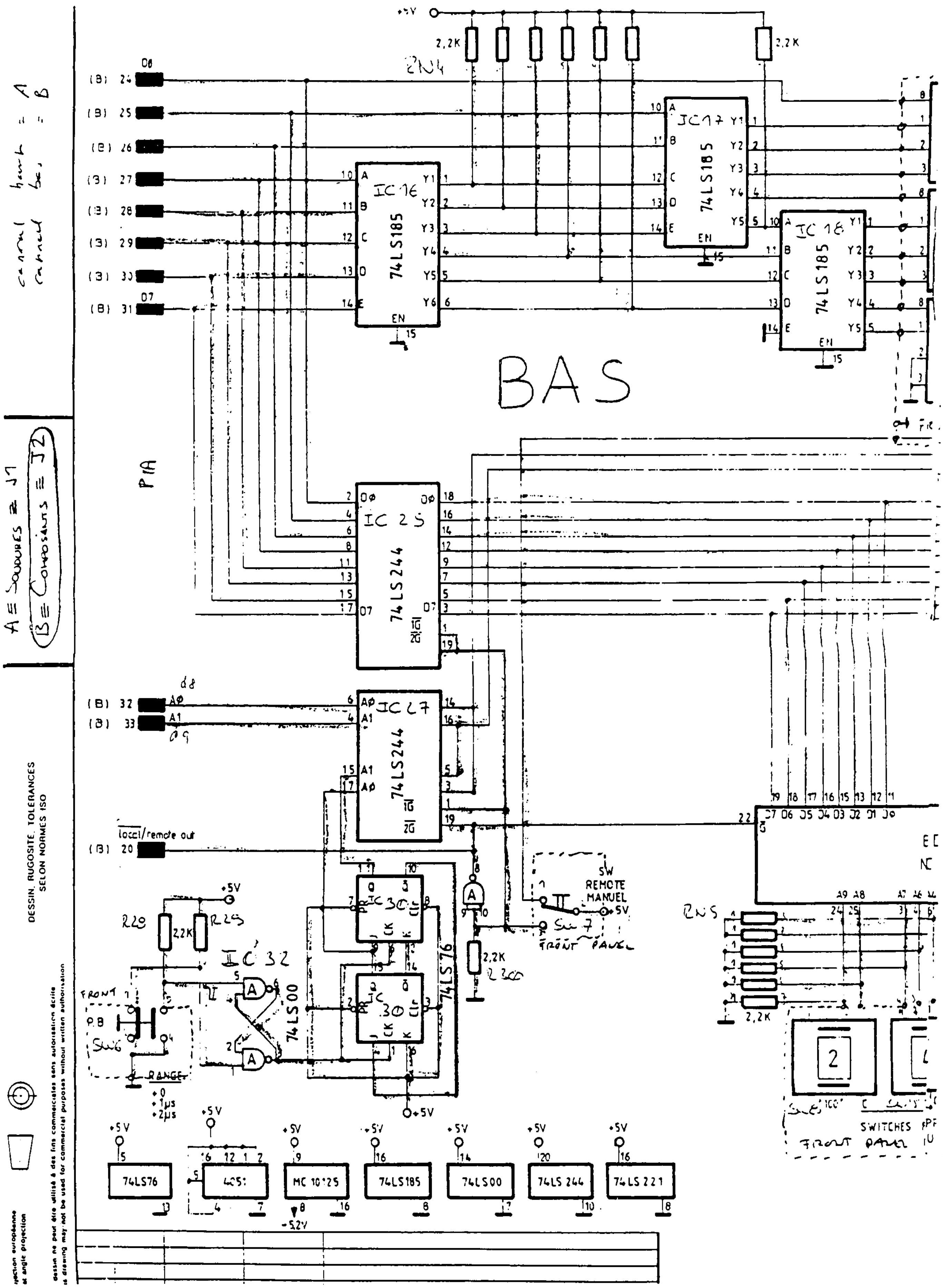
.1 Jitter

Using a 100MHz storage oscilloscope, no jitter was evident n the trace for the AD9500. The AD9500 circuit can be used for est purposes so long as correct cailibration of delay Resistors s carried out.

The AD9501 would appear to also provide jitter free output rom examination of the falling edge of the existing pulse. owever, soldering and capacitive decoupling is absolutely neces- ary.

stribution : Kicker Magnet Section, RF Group

Appendix A - Original circuit schematic diagram



DESSIN, RUGOSITE, TOLERANCES SELON NORMES ISO

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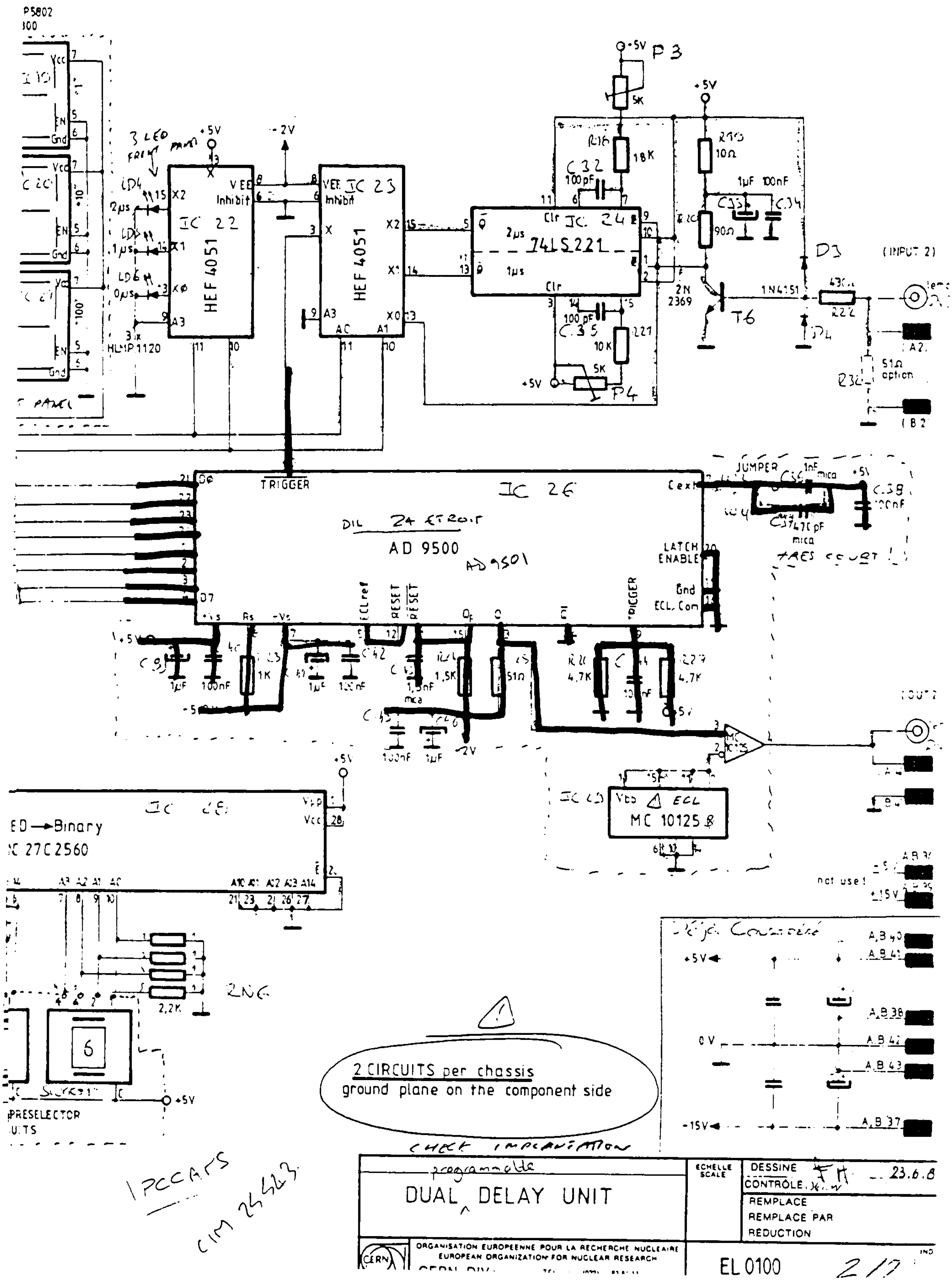
IC 22
HEF 4051
IC 23
HEF 4051
IC 24
74LS221
IC 26
DIL 24 ETROIT
AD 9500
AD 9501
TRIGGER
LATCH ENABLE
IC 25
MC 10125
Vbb
ECL
3 LED FRONT PANEL
3 x HLMP 1120
P3
P4
T6
2N 2369
1N4151
D3
D4
(INPUT 2)
51Ω option
JUMPER
TRES COURT !
2 CIRCUITS per chassis
ground plane on the component side
CHECK IMPLANTATION
BCD→Binary
27C2560
2,2K
PRESELECTOR
not used
+5V
-2V
-5V
+15V
-15V
0 V
programmable
DUAL DELAY UNIT
ECHELLE SCALE
DESSINE
CONTROLE
REMPLACE
REMPLACE PAR
REDUCTION
23.6.8
ORGANISATION EUROPEENNE POUR LA RECHERCHE NUCLEAIRE
EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH
CERN
EL 0100
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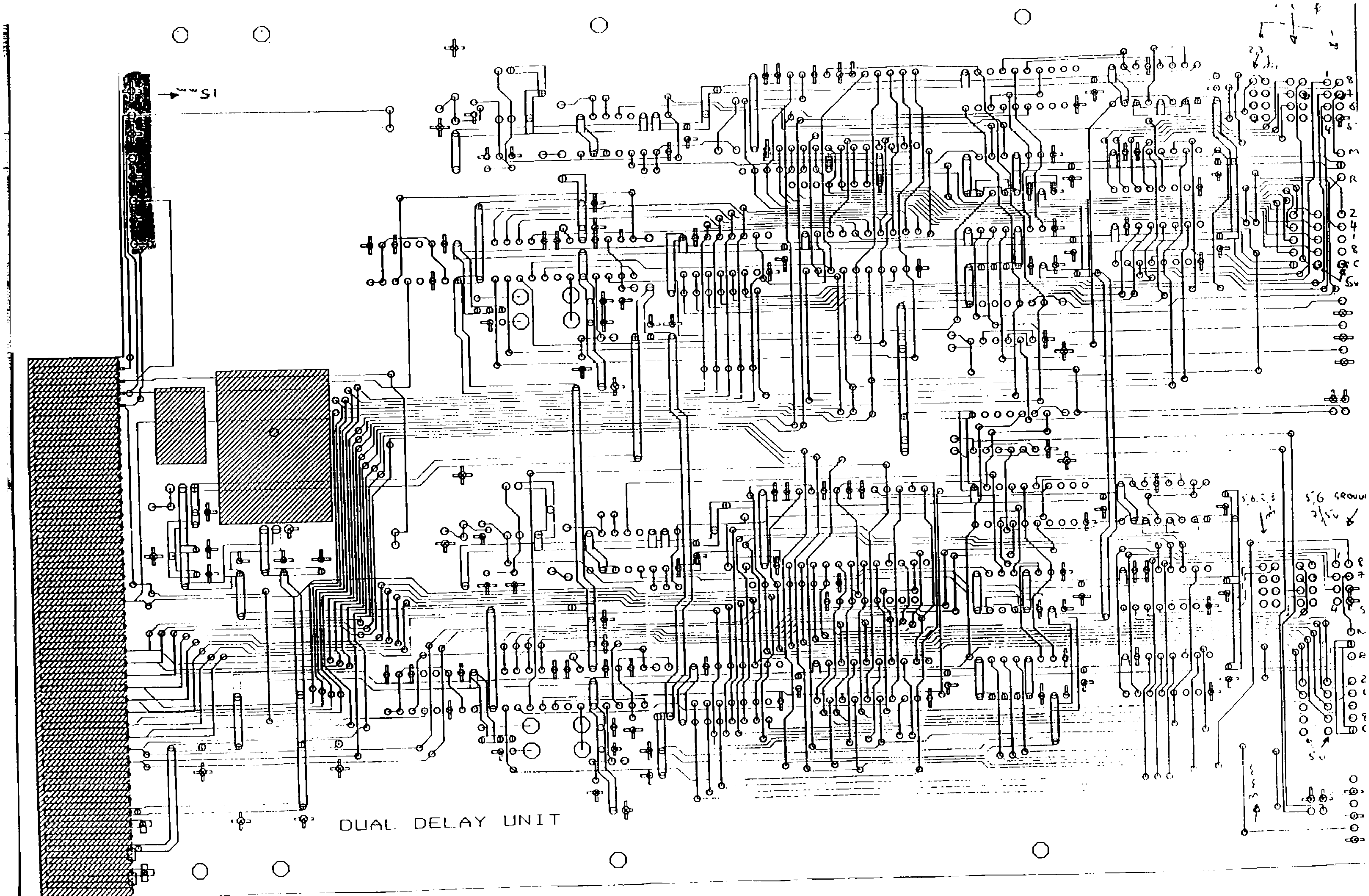
Appendix B - Original PCB Schematic layout



APLTRON SA 1217 MEYRIN
APL 5989 REV
LIAISONS PLAN DE MASSE COTE COMP

Appendix C - AD9500/AD9501 Data Sheets

Stuart Johnston

ANALOG DEVICES

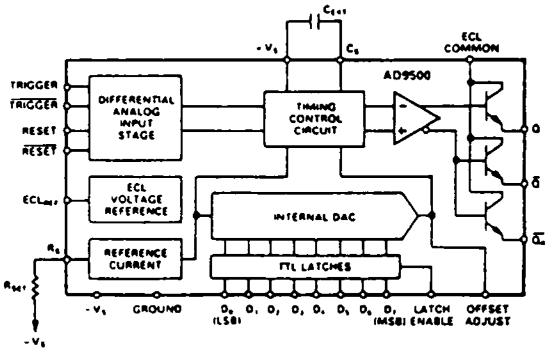
Digitally Programmable Delay Generator

AD9500

FEATURES
10ps Delay Resolution
2.5ns to 100µs + Full-Scale Range
Fully Differential Inputs
Separate Trigger and Reset Inputs
Low Power Dissipation – 310mW

APPLICATIONS
ATE
Pulse Deskewing
Arbitrary Waveform Generators
High-Stability Timing Source
Multiple Phase Clock Generators

AD9500 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

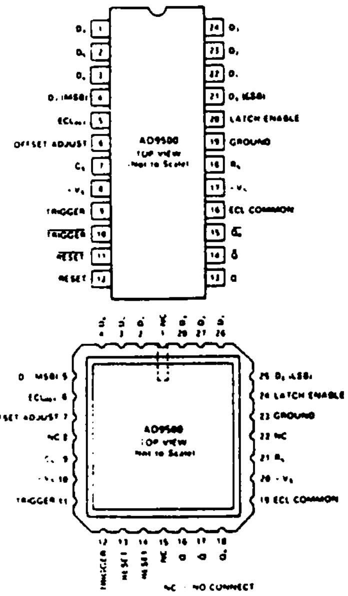
The AD9500 is a digitally programmable delay generator, which provides programmed delays, selected through an 8-bit digital code, in resolutions as small as 10ps. The AD9500 is constructed in a high-performance bipolar process, designed to provide high-speed operation for both digital and analog circuits.

The AD9500 employs differential TRIGGER and RESET inputs which are designed primarily for ECL signal levels but function with analog and TTL input levels. An on-board ECL reference midpoint allows both of the inputs to be driven by either single ended or differential ECL circuits. The AD9500 output is a complementary ECL stage, which also provides a parallel $\overline{Q_R}$ output circuit to facilitate reset timing implementations.

The digital control data is passed to the AD9500 through a transparent latch controlled by the LATCH ENABLE signal. In the transparent mode, the internal DAC of the AD9500 will attempt to follow changes at the inputs. The LATCH ENABLE is otherwise used to strobe the digital data into the AD9500 latches.

The AD9500 is available as an industrial temperature range device, −25°C to +85°C, and as an extended temperature range device, −55°C to +125°C. Both grades are packaged in a 24-pin ceramic "Skinny" DIP (0.3" package width), as well as 28-pin surface mount packages. Contact the factory for MIL-STD-883, revision C, qualified devices.

PIN CONFIGURATIONS



ORDERING INFORMATION

Device	Temperature Range	Description	Package Options*
AD9500BP	−25°C to +85°C	28-Pin PLCC (Plastic), Industrial Temperature	P-28A
AD9500BQ	−25°C to +85°C	24-Pin "Skinny" DIP, Industrial Temperature	Q-24
AD9500TE	−55°C to +125°C	28-Pin LCC, Extended Temperature	E-28A
AD9500TQ	−55°C to +125°C	24-Pin "Skinny" DIP, Extended Temperature	Q-24

*See Section 16 for package outline information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) . . . . +7V
Negative Supply Voltage ($-V_S$) . . . . −7V
ECL COMMON to Ground Differential . . −2.0V to +5.0V
Digital Input Voltage Range . . . . −3.5V to +5.0V
Trigger/Reset Input Voltage Range . . . . ±5.0V
Trigger/Reset Differential Voltage 5.0V
Minimum R_{SET} 220Ω
Digital Output Current (Q and $\overline{Q}$) 30mA
Digital Output Current ($\overline{Q_R}$) 2mA
Offset Adjust Current (Sinking) 4mA
Power Dissipation (+25°C Free Air)[2] 2.62W
Operating Temperature Range
  AD9500BP/BQ . . . . −25°C to +85°C
  AD9500TE/TQ . . . . −55°C to +125°C
Storage Temperature Range . . . . −65°C to +150°C
Junction Temperature . . . . +175°C
Lead Soldering Temperature (10sec) . . . . +300°C

ELECTRICAL CHARACTERISTICS (Supply Voltages $+V_S$ = +5.0V, $-V_S$ = −5.2V; C_{EXT} = 0pF; R_{SET} = 500Ω, unless otherwise stated)

Parameter	Mil[3] Sub Group	Temp	Industrial −25°C to +85°C AD9500BP/BQ Min	Typ	Max	Military −55°C to +125°C AD9500TE/TQ Min	Typ	Max	Units
RESOLUTION			8			8			Bits
ACCURACY[4]									
Differential Linearity	7	+25°C			0.5			0.5	LSB
Integral Linearity	7	+25°C			1.0			1.0	LSB
Monotonicity	7	+25°C		Guaranteed			Guaranteed		
DIGITAL INPUT									
Logic "1" Voltage	7, 8	Full	2.0			2.0			V
Logic "0" Voltage	7, 8	Full			0.8			0.8	V
Logic "1" Current	1, 2, 3	Full			5			5	µA
Logic "0" Current	1, 2, 3	Full			5			5	µA
Digital Input Capacitance	12	+25°C			5.5			5.5	pF
Data Setup Time[5]	12	+25°C		0.4	0.75		0.4	0.75	ns
Data Hold Time[6]	12	+25°C		0.4	0.75		0.4	0.75	ns
Latch Pulse Width (t_{LPW})	12	+25°C	3.0			3.0			ns
RESET/TRIGGER INPUTS[7]									
TRIGGER Input Voltage Range		Full		−2.5; 4.5			−2.5; 4.5		V
RESET Input Voltage Range		Full		−2.5; 2.0			−2.5; 2.0		V
Differential Switching Voltage	7, 8	Full		40	300		40	300	mV
Input Bias Current	1	+25°C		40	50		40	50	µA
	2, 3	Full			75			75	µA
Input Resistance		+25°C		4			4		kΩ
Input Capacitance	12	+25°C		6.5	7.25		6.5	7.25	pF
Minimum Input Pulse Width (t_{TPW}, t_{RPW})		+25°C		2.0			2.0		ns
DYNAMIC PERFORMANCE[8]									
Maximum Trigger Rate	12	+25°C	100			100			MHz
Minimum Propagation Delay (t_{PD})[9]	4	+25°C	5.4	6.4	7.4	5.4	6.4	7.4	ns
Minimum Propagation Delay TC[10]		Full		7.5			7.5		ps/°C
Full-Scale Range TC		Full		0.5			0.5		ps/°C
Delay Uncertainty (Jitter)		+25°C		10			10		ps
Reset Propagation Delay (t_{RD})[11]	4	+25°C	5.4	6.4	7.4	5.4	6.4	7.4	ns
Reset-to-Trigger Holdoff (t_{THO})[12]	4	+25°C	0.2	0		0.2	0		ns
Trigger-to-Reset Holdoff (t_{RHO})[13]	4	+25°C	2.0	1.5		2.0	1.5		ns
Minimum Output Pulse Width		+25°C		3.3			3.3		ns
Output Rise Time	12	+25°C			2.0			2.0	ns
Output Fall Time	12	+25°C			2.0			2.0	ns
Delay Coefficient Settling Time (t_{DAC})[14]		+25°C		29			29		ns
Linear Ramp Settling Time (t_{LRS})		+25°C		22			22		ns

4.2mA

Parameter	Mil[3] Sub Group	Temp	Industrial −25°C to +85°C AD9500BP/BQ Min	Typ	Max	Military −55°C to +125°C AD9500TE/TQ Min	Typ	Max	Units
SUPPORT FUNCTIONS									
ECL_{REF}	1	+25°C	−1.4	−1.3	−1.2	−1.4	−1.3	−1.2	V
ECL_{REF} Voltage Drift[15]		Full		1.1			1.1		mV/°C
Offset Adjust Range		Full		−2			−2		mA
DIGITAL OUTPUTS[8]									
Logic "1" Voltage	1, 2, 3	Full	−1.1			−1.1			V
Logic "0" Voltage	1, 2, 3	Full			−1.5			−1.5	V
POWER SUPPLY[16]									
Positive Supply Current (+5.0V)	1	+25°C		24	28		24	28	mA
	2, 3	Full			30			30	mA
Negative Supply Current (−5.2V)	1	+25°C		37	42		37	42	mA
	2, 3	Full			44			44	mA
Nominal Power Dissipation		+25°C		312			312		mW
Power Supply Rejection Ratio[17]									
Full-Scale Range Sensitivity	7	+25°C		70	300		70	300	ps/V
Minimum Propagation Delay Sensitivity	7	+25°		150	500		150	500	ps/V

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Typical thermal impedance
- 24-Pin Ceramic $\theta_{JA} = 56°C/W$; $\theta_{JC} = 16°C/W$
- 28-Pin PLCC (Plastic) $\theta_{JA} = 60°C/W$; $\theta_{JC} = 22°C/W$
- 28-Pin Ceramic LCC $\theta_{JA} = 69°C/W$; $\theta_{JC} = 25°C/W$

[3]Military subgroups apply to military qualified devices only.

[4]$R_{SET} = 10k\Omega$. (Full-scale delay = 100ns).

[5]The digital data inputs must remain stable for the specified time prior to the LATCH ENABLE signal.

[6]The digital data inputs must remain stable for the specified time after the LATCH ENABLE signal.

[7]The TRIGGER and RESET inputs are differential and must be driven relative to one another. Both of these inputs are ECL compatible, but can also be used with TTL logic families in a limited fashion.

[8]Outputs terminated through 50Ω resistors to −2.0V.

[9]Program Delay = 0.0ps (Digital Data = 00_H). In Operation, any programmed delays are in addition to the Minimum Propagation Delay.

[10]Measured from the 50% transition point of the reset signal input, to the 50% transition point of the resetting output.

[11]Minimum time from falling edge of RESET to triggering input, to insure a valid output event.

[12]Change in total delay through AD9500, exclusive of changes in minimum-propagation delay t_{PD}.

[13]Minimum time from triggering event to rising edge of RESET, to insure a valid output event.

[14]Measured from the LATCH ENABLE input to the point when the AD9500 becomes 8-bit accurate again, after a full-scale change in the programmed delay.

[15]Standard 10K and 10KH ECL families operate with a 1.1mV/°C drift by design.

[16]Supply voltages should remain stable within ±5% for normal operation.

[17]Measured at ±5% of $-V_S$ and $+V_S$.

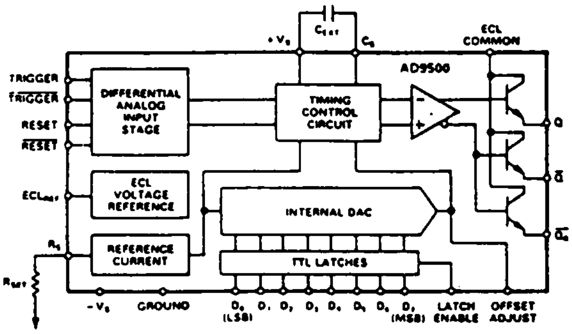
Specifications subject to change without notice.

EXPLANATION OF GROUP A MILITARY SUBGROUPS

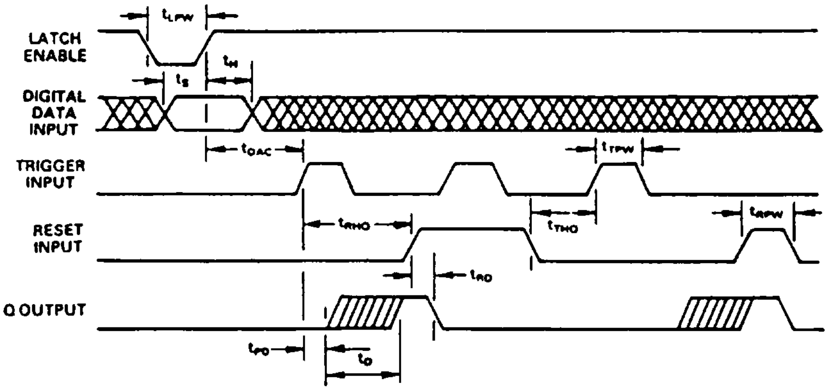
Subgroup 1 – Static tests at +25°C.
Subgroup 2 – Static tests at max rated operating temp.
Subgroup 3 – Static tests at min rated operating temp.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at max rated operating temp.
Subgroup 6 – Dynamic tests at min rated operating temp.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at max and min rated operating temp.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at max rated operating temp.
Subgroup 11 – Switching tests at min rated operating temp.
Subgroup 12 – Periodically sample tested.

FUNCTIONAL DESCRIPTION

PIN NAME	DESCRIPTION
D_4–D_6	– One of eight digital inputs used to set the programmed delay.
D_7(MSB)	– One of eight digital inputs used to set the programmed delay. D_7 (MSB) is the most significant bit of the digital input word.
ECL_{REF}	– ECL midpoint reference, nominally −1.3V. Use of the ECL_{REF}, allows either of the TRIGGER or the RESET inputs to be configured for single-ended ECL inputs.
OFFSET ADJUST	– The OFFSET ADJUST is used to adjust the minimum propagation delay (t_{PD}), by pulling or pushing a small current out of or into the pin.
C_S	– C_S allows the full-scale range to be extended by using an external timing capacitor. The value of C_{EXT}, connected between C_S and $+V_S$, may range from 0pF to 0.1μF+. See R_S ($C_{INTERNAL}$ = 10pF).
$+V_S$	– Positive supply terminal, nominally +5.0V.
TRIGGER	– Noninverted input of the edge-sensitive differential trigger input stage. The output at Q will be delayed by the programmed delay, after the triggering event. The programmed delay is set by the digital input word. The TRIGGER input must be driven in conjunction with the $\overline{\text{TRIGGER}}$ input.
$\overline{\text{TRIGGER}}$	– Inverted input of the edge-sensitive differential trigger input stage. The output at Q will be delayed by the programmed delay, after the triggering event. The programmed delay is set by the digital input word. The $\overline{\text{TRIGGER}}$ input must be driven in conjunction with the TRIGGER input.
$\overline{\text{RESET}}$	– Inverted input of the level-sensitive differential reset input stage. The output at Q will be reset after a signal is received at the reset inputs. In the "minimum configuration," the minimum output pulse width will be equal to the "reset propagation delay," t_{RD}. The RESET input must be driven in conjunction with the $\overline{\text{RESET}}$ input.
RESET	– Noninverted input of the level-sensitive differential reset input stage. The output at Q will be reset after a signal is received at the reset inputs. In the "minimum configuration," the minimum output pulse width will be equal to the "reset propagation delay," t_{RD}. The $\overline{\text{RESET}}$ input must be driven in conjunction with the RESET input.
Q	– One of two complementary ECL outputs. A "triggering" event at the inputs will produce a logic HIGH on the Q output. A "resetting" event at the inputs will produce a logic LOW on the Q output
$\overline{Q}$	– One of two complementary ECL outputs. A "triggering" event at the inputs will produce a logic LOW on the $\overline{Q}$ output. A "resetting" event at the inputs will produce a logic HIGH on the $\overline{Q}$ output.
$\overline{Q_R}$	– $\overline{Q_R}$ output is parallel to the $\overline{Q}$ output. The $\overline{Q_R}$ output is typically used to drive delaying circuits for extending output pulse widths. A "triggering" event at the inputs will produce a logic LOW on the $\overline{Q_R}$ output. A "resetting" event at the inputs will produce a logic HIGH on the $\overline{Q_R}$ output.
ECL COMMON	– The collector common for the ECL output stage. The collector common may be tied to +5.0V, but normally it is tied to the circuit ground for standard ECL outputs.
$-V_S$	– Negative supply terminal, nominally −5.2V.
R_S	– R_S is the reference current setting terminal. An external setting resistor, R_{SET}, connected between R_S and $-V_S$ determines the internal reference current. See C_S ($250\Omega \leq R_{SET} \leq 50k\Omega$).
GROUND	– The ground return for the TTL and analog inputs.
LATCH ENABLE	– Transparent TTL latch control line. A logic HIGH on the LATCH ENABLE freezes the digital. code at the logic inputs. A logic LOW on the LATCH ENABLE allows the internal current levels to be continuously updated through the logic inputs D_0 thru D_7.
D_0(LSB)	– One of eight digital inputs used to set the programmed delay. D_0 (LSB) is the least significant bit of the digital input word.
D_3–D_1	– One of eight digital inputs used to set the programmed delay.



AD9500 Functional Block Diagram

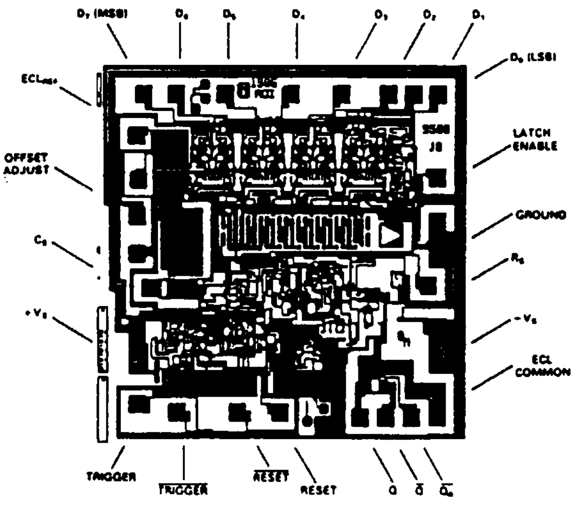


t_S - DIGITAL DATA SETUP TIME
t_H - DIGITAL DATA HOLD TIME
t_{LPW} - LATCH ENABLE PULSE WIDTH
t_{DAC} - INTERNAL DAC SETTLING TIME
t_{PD} - MINIMUM PROPAGATION DELAY
t_{RD} - RESET PROPAGATION DELAY
t_D - PROGRAMMED DELAY
t_{TPW} - TRIGGER PULSE WIDTH
t_{RPW} - RESET PULSE WIDTH
t_{THO} - RESET-TO-TRIGGER HOLDOFF
t_{RHO} - TRIGGER-TO-RESET HOLDOFF

NOTE
A TRIGGERING EVENT MAY OCCUR AT ANY TIME WHILE THE INTERNAL DAC (PROGRAMMED DELAY) IS BEING CHANGED. TRIGGERING EVENTS DURING THE INTERNAL DAC SETTLING TIME MAY NOT GENERATE AN ACCURATE PULSE DELAY.

System Timing Diagram

DIE LAYOUT



MECHANICAL INFORMATION

Die Dimensions	104 × 103 × 18 (max) mils
Pad Dimensions	4 × 4 (min)mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil, Aluminum; Ultrasonic Bonding or 1mil, Gold; Gold Ball Bonding

INSIDE THE AD9500

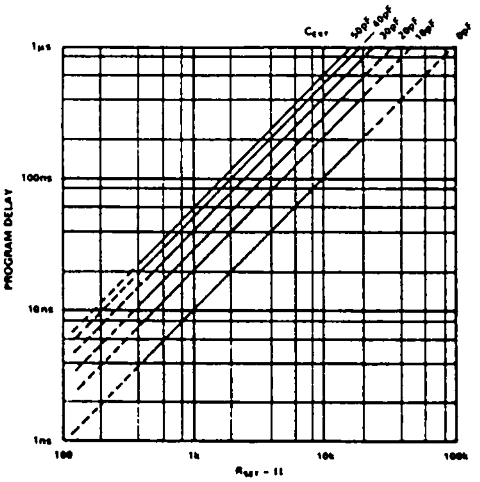
The heart of the AD9500 is the linear ramp generator. A triggering event at the input of the AD9500 initiates the ramp cycle. As the ramp voltage falls, it will eventualy go below the threshold set up by the internal DAC (digital-to-analog converter). A comparator monitors both the linear ramp voltage and the DAC threshold level. The output of the comparator serves as the output for the AD9500, and the interval from the trigger until the output switches is the total delay time of the AD9500.

The total delay through the AD9500 is made up of two components. The first is the full-scale programmed delay, $t_{D\,(max)}$, determined by R_{SET} and C_{EXT}. The second component of the total delay is the minimum propagation delay through the AD9500 (t_{PD}). The full-scale delay is variable from 2.5ns to greater than 1ms. The internal DAC is capable of generating 256 separate programmed delays within the full-scale range (this gives 10ps increments for a 2.5ns full-scale setting).

The actual programmed delay is directly related to both the digital control data (digital data to the internal DAC) and the RC time constant established by R_{SET} and C_{EXT}. The specific relationship is as follows:

Total Delay = Minimum Propagation Delay + Programmed Delay

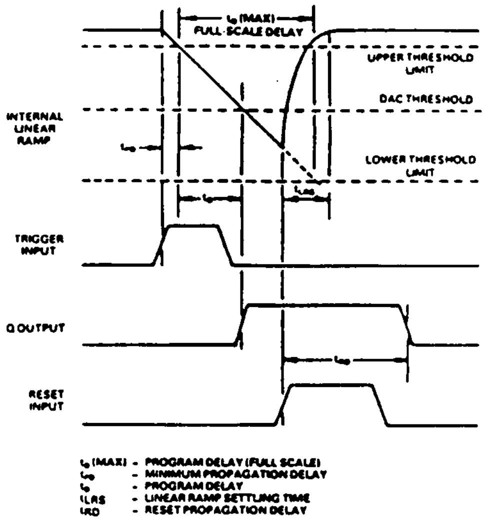
$$= t_{PD} + (\text{digital value}/256)\, R_{SET}\, (C_{EXT} + 10\text{pF})$$



Typical Programmed Delay Ranges

The internal DAC determines the programmed delay by way of the threshold level at its output. The LATCH ENABLE control for the on-board latch is active (latches) logic "HIGH". In the logic "LOW" state, the latch is transparent, and the internal DAC will attempt to follow changes at the digital data inputs.

Both the LATCH ENABLE control and the data inputs are TTL compatible. The internal DAC may be updated at any time, but full timing accuracy may not be attained unless triggering events are held off until after the DAC settling time (t_{DAC}).



Internal Timing Diagram

On resetting, the ramp voltage held in the timing capacitor (C_{EXT} + 10pF) is discharged. The AD9500 discharges the bulk of the ramp voltage very quickly, but to maintain *absolute* accuracy, subsequent triggering events should be held off until after the linear ramp settling time (t_{LRS}). Applications which employ high frequency triggering at a constant rate will not be affected by the slight settling errors since they will be constant for fixed reset-to-trigger cycles.

The RESET and TRIGGER inputs of the AD9500 are differential and must be driven relative to one another. Accordingly, the TRIGGER and RESET inputs are ideally suited for analog or complementary input signals. Single-ended ECL input signals can be accommodated by using the ECL midpoint reference (ECL_{REF}) to drive one side of the differential inputs.

The output of the AD9500 consists of both Q and $\overline{Q}$ driver stages, as well as the $\overline{Q_R}$ output which is used primarily for extending the output pulse width. In the most direct reset configuration, either the Q or the $\overline{Q}$ output is tied to the respective RESET input. This generates a delayed output pulse with a duration equal to the reset delay time (t_{RD}) of approximately 6ns. Note that the reset delay time (t_{RD}) becomes extended for very small programmed delay settings. The duration of the output pulse can be extended by driving the reset inputs with the $\overline{Q_R}$ output through an RC network (see "Extended Output Pulse Width" application). Using the $\overline{Q_R}$ output to drive the reset circuit avoids loading the Q or $\overline{Q}$ outputs.

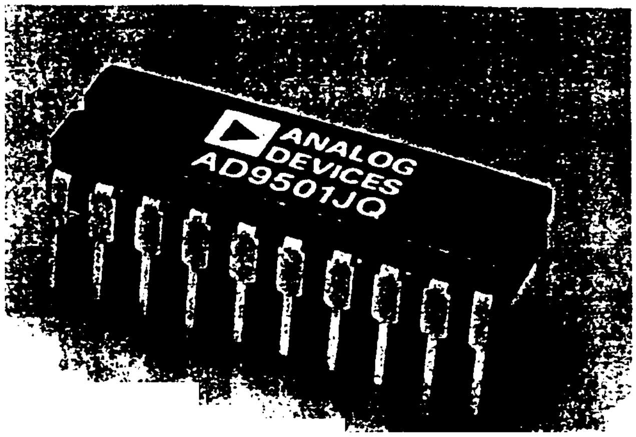
ANALOG DEVICES

Digitally Programmable Delay Generator

AD9501

FEATURES
Single +5 V Supply
TTL and CMOS Compatible
10 ps Delay Resolution
2.5 ns to 10 μs Full-Scale Range
Maximum Trigger Rate 50 MHz

APPLICATIONS
Disk Drive Deskewing
Data Communications
Test Equipment
Radar I & Q Matching

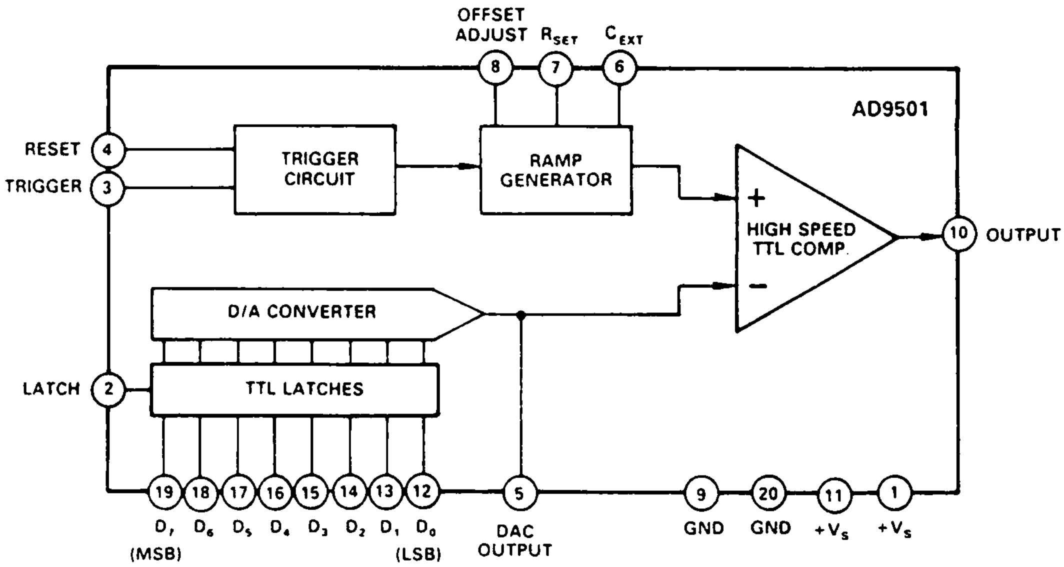


GENERAL DESCRIPTION

The AD9501 is a digitally programmable delay generator which provides programmed time delays of an input pulse. Operating from a single +5 V supply, the AD9501 is TTL- or CMOS-compatible, and is capable of providing accurate timing adjustments with resolutions as low as 10 ps. Its accuracy and programmability make it ideal for use in data deskewing and pulse delay applications, as well as clock timing adjustments.

Full-scale delay range is set by the combination of an external resistor and capacitor, and can range from 2.5 ns to 10 μs for a single AD9501. An eight-bit digital word selects a time delay within the full-scale range. When triggered by the rising edge of an input pulse, the output of the AD9501 will be delayed by an amount equal to the selected time delay (t_D) plus an inherent propagation delay (t_{PD}).

The AD9501 is available for a commercial temperature range of 0 to +70°C in a 20-pin plastic DIP, 20-pin ceramic DIP, and a 20-lead plastic leaded chip carrier (PLCC). Military temperature range devices for operation from −55°C to +125°C are available in ceramic DIPs.



AD9501 Functional Block Diagram

ANALOG DEVICES

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1201 Genève
Tél. 022 / 731 57 60
Télex 289 096
Fax 022 / 731 91 54

Rosenstrasse 13
8600 Dübendorf
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Telex 828 491
Fax 01 / 820 26 01

lorwood, MA 02062-9106 U.S.A.
Twx: 710/394-6577
les: ANALOG NORWOODMASS

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage . . . . +7 V
Digital Input Voltage Range . . . . −0.5 V to $+V_S$
Trigger/Reset Input Volt. Range . . . . −0.5 V to $+V_S$
Minimum R_{SET} . . . . 30 Ω
Digital Output Current (Sourcing) . . . . 10 mA
Digital Output Current (Sinking) . . . . 50 mA
Operating Temperature Range
AD9501JN/JP/JQ . . . . 0 to +70°C
AD9501SQ . . . . −55°C to +125°C
Storage Temperature Range . . . . −65°C to +150°C
Junction Temperature[2] . . . . +175°C
Lead Soldering Temperature (10 sec.) . . . . +300°C

ELECTRICAL CHARACTERISTICS

[$+V_S$ = +5 V; C_{EXT} = Open; R_{SET} = 3090 Ω (Full-scale range = 100 ns); Pin 8 grounded; and device output connected to Pin 4 RESET input unless otherwise noted]

Parameter	Temp	Test Level	COMMERCIAL 0 to +70°C AD9501JN/JP/JQ Min	Typ	Max	M Su	MILITARY −55°C to +125°C AD9501SQ Min	Typ	Max	Units
RESOLUTION			8				8			Bits
ACCURACY										
Differential Nonlinearity	+25°C	I			0.5	7			0.5	LSB
Integral Nonlinearity	+25°C	I			1	7			1	LSB
Monotonicity	+25°C	I		Guaranteed		7		Guaranteed		
GITAL INPUTS										
ogic "1" Voltage	Full	VI	2.0			7, 8	2.0			V
Logic "0" Voltage	Full	VI			0.8	7, 8			0.8	V
Logic "1" Current	Full	VI			60	1, 2, 3			60	μA
Logic "0" Current	Full	VI			3	1, 2, 3			3	μA
Digital Input Capacitance	+25°C	IV			5.5	12			5.5	pF
Data Setup Time (t_S)[4]	+25°C	V		2.5				2.5		ns
Data Hold Time (t_H)[5]	+25°C	V		2.5				2.5		ns
Latch Pulse Width (t_L)	+25°C	V		3.5				3.5		ns
Reset/Trigger Pulse Width (t_R, t_T)	+25°C	V		2				2		ns
DYNAMIC PERFORMANCE										
Maximum Trigger Rate[6]	+25°C	IV	18	22		12	15	22		MHz
Minimum Propagation Delay (t_{PD})[7]	+25°C	I		25	30	4		25	30	ns
Propagation Delay Tempco[8]	Full	V		25				25		ps/°C
Full-Scale Range Tempco	Full	V		36				36		ps/°C
Delay Uncertainty	+25°C	V		53				53		ps
Reset Propagation Delay (t_{RD})[9]	+25°C	I		14.5	17.5	4		14.5	17.5	ns
Reset-to-Trigger Holdoff (t_{THO})[10]	+25°C	V		4.5				4.5		ns
Trigger-to-Reset Holdoff (t_{RHO})[11]	+25°C	V		19				19		ns
Minimum Output Pulse Width[12]	+25°C	V		7.5				7.5		ns
Output Rise Time[13]	+25°C	I		2.3	3.5	9		2.3	3.5	ns
Output Fall Time[13]	+25°C	I		1.0	2.0	9		1.0	2.0	ns
DAC Settling Time (t_{LD})[14]	+25°C	V		30				30		ns
Linear Ramp Settling Time (t_{LRS})[15]	+25°C	V		20				20		ns
DIGITAL OUTPUT										
Logic "1" Voltage (Source 1 mA)	Full	VI	2.4			1, 2, 3	2.4			V
Logic "0" Voltage (Sink 4 mA)	Full	VI		0.24	0.4	1, 2, 3		0.24	0.4	V
POWER SUPPLY[16]										
Positive Supply Current (+5.0 V)	Full	VI		69.5	83	1, 2, 3		69.5	83	mA
Power Dissipation	Full	VI			415	1, 2, 3			415	mW
Power Supply Rejection Ratio[17]										
Full-Scale Range Sensitivity	+25°C	I		0.7	2.0	7		0.7	2.0	ns/V
Minimum Prop Delay Sensitivity	+25°C	I		0.45	1.7	7		0.45	1.7	ns/V

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances: 20-lead plastic leaded chip carrier θ_{JA}=73°C/W; θ_{JC}=29°C/W. 20-pin ceramic DIP θ_{JA}=65°C/W; θ_{JC}=20°C/W. 20-pin plastic DIP θ_{JA}=65°C/W; θ_{JC}=26°C/W.

[3]Military subgroups apply only to military-qualified devices.

[4]Digital data inputs must remain stable for the specified time prior to the positive transition of the LATCH signal.

[5]Digital data inputs must remain stable for the specified time after the positive transition of the LATCH signal.

[6]Programmed delay (t_D)=0 ns. Maximum self-resetting trigger rate is limited to 6.9 MHz with 100 ns programmed delay. If t_D=0 ns and external RESET signal is used, maximum trigger rate is 23 MHz.

[7]Programmed delay (t_D)=0 ns. In operation, any programmed delays are in addition to the minimum propagation delay (t_{PD}).

[8]Programmed delay (t_D)=0 ns. [Minimum propagation delay (t_{PD})]

[9]Measured from 50% transition point of the RESET signal input to the 50% transition point of the falling edge of the output.

[10]Minimum time from the falling edge of RESET to the triggering input to insure valid output pulse, using external RESET pulse.

[11]Minimum time from triggering event to rising edge of RESET to insure valid output event, using external RESET pulse. Extends to 125 ns when programmed delay is 100 ns.

[12]When self-resetting with a full-scale programmed delay.

[13]Measured from +0.4 V to +2.4 V; source=1 mA; sink=4 mA..

[14]Measured from the data input to the time when the AD9501 becomes 8-bit accurate, after a full-scale change in the program delay data word.

[15]Measured from the RESET input to the time when the AD9501 becomes 8-bit accurate, after a full-scale programmed delay.

[16]Supply voltage should remain stable within ±5% for normal operation.

[17]Measured at $+V_S$ = +5.0 V ±5%; specification shown is for worst case.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

EXPLANATION OF MILITARY SUBGROUPS

Subgroup 1 – Static tests at +25°C. (5% PDA calculated against Subgroup 1 for high-rel versions)

Subgroup 2 – Static tests at maximum rated operating temperature.

Subgroup 3 – Static tests at minimum rated operating temperature.

Subgroup 4 – Dynamic tests at +25°C.

Subgroup 5 – Dynamic tests at maximum rated operating temperature.

Subgroup 6 – Dynamic tests at minimum rated operating temperature.

Subgroup 7 – Functional tests at +25°C.

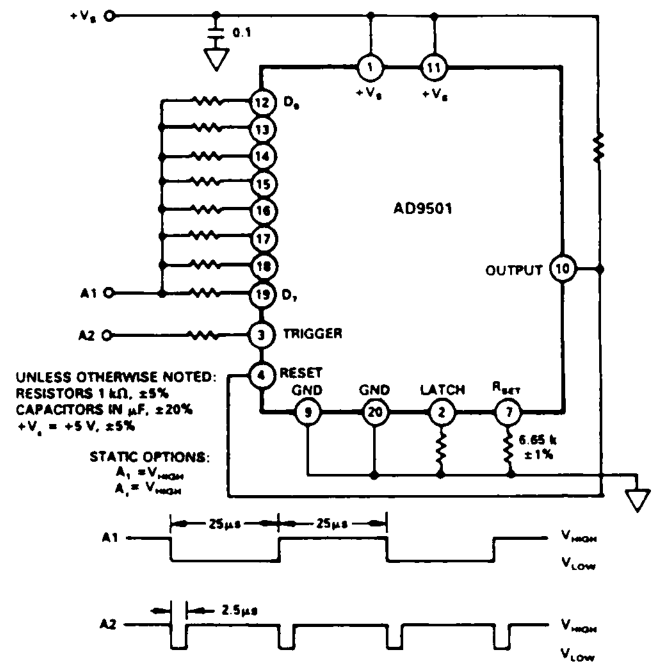
Subgroup 8 – Functional tests at maximum and minimum rated temperatures.

Subgroup 9 – Switching tests at +25°C.

Subgroup 10 – Switching tests at maximum rated operating temperature.

Subgroup 11 – Switching tests at minimum rated operating temperature.

Subgroup 12 – Periodically sample tested.



AD9501 Burn-In Circuit

MIL-STD-883 Compliance Information

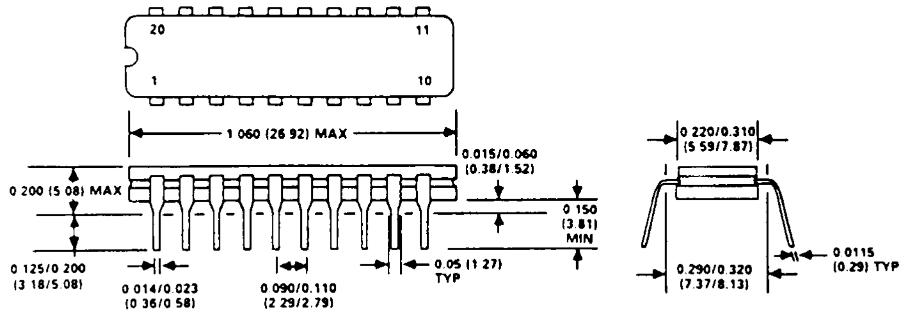
The AD9501 is a time delay generator and is constructed in accordance with MIL-STD-883. The AD9501 is electrostatic sensitive and falls within electrostatic sensitivity classification Class 1. Percent Defective Allowance (PDA) is computed based on Subgroup 1 of the specified Group A test list. Quality Assurance (QA) screening is in accordance with Alternate Method A of Method 5005.

The following apply: Burn-In per 1015; Life Test per 1005; Electrical Testing per 5004. (Note: Group A electrical testing assumes $T_A = T_C = T_J$.) MIL-STD-883-compliant devices are marked with "C" to indicate compliance.

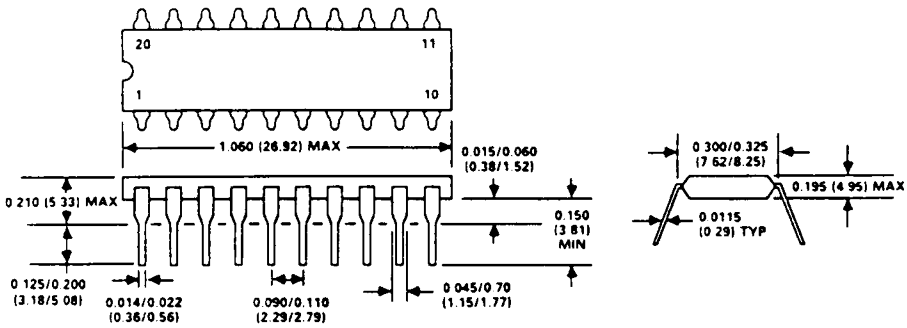
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

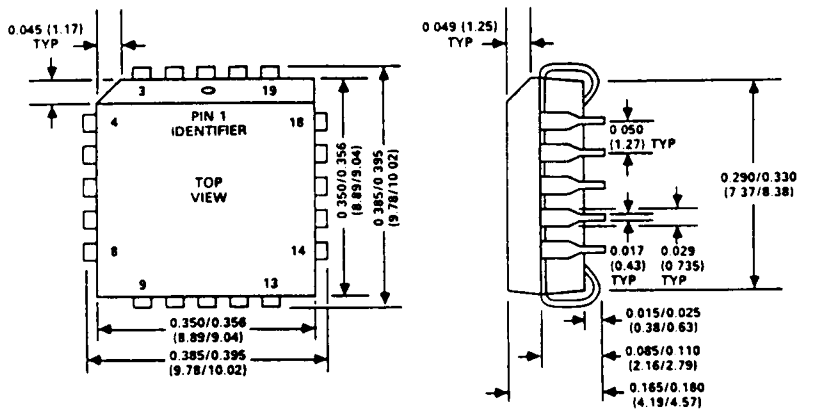
Suffixes JQ and SQ



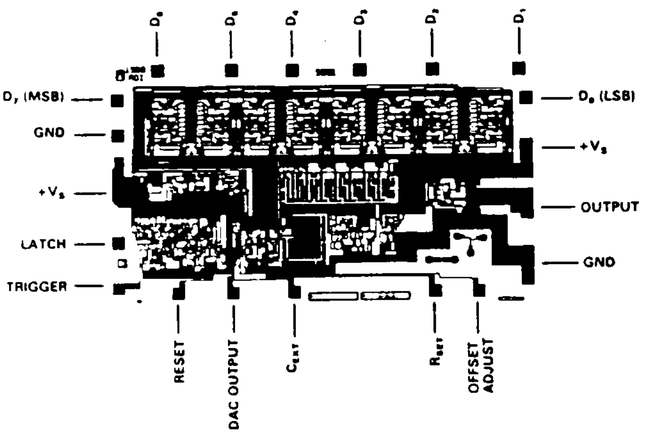
Suffix JN



Suffix JP



DIE LAYOUT AND MECHANICAL INFORMATION

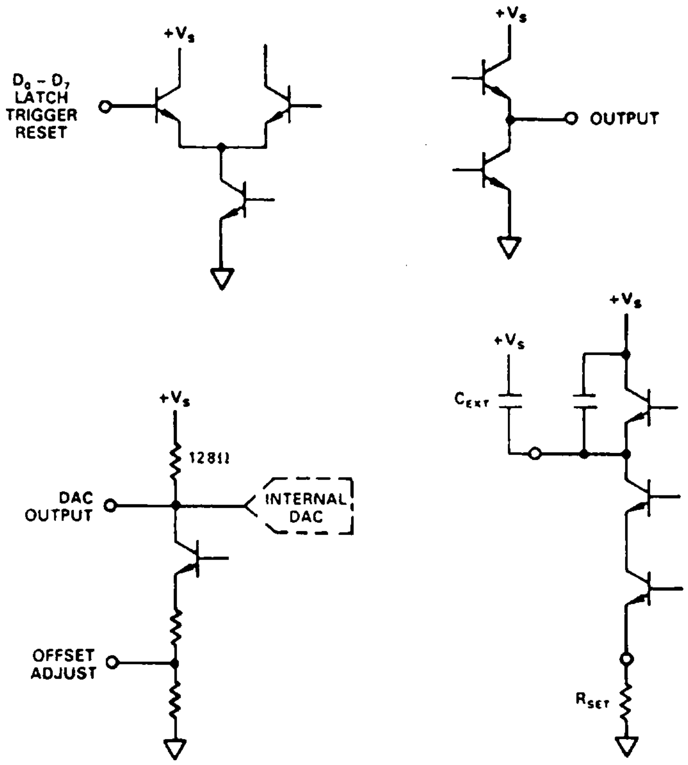


MECHANICAL INFORMATION

Die Dimensions . . . . .89 × 153 × 15 (±2) mils
Pad Dimensions. . . . . .4 × 4 mils
Metalization. . . . . Aluminum
Backing . . . . .None
Substrate Potential . . . . .Ground
Passivation . . . . .Oxynitride
Die Attach . . . . .Gold Eutectic
Bond Wire. . . . . 1.25 mil, Aluminum; Ultrasonic Bonding
or 1 mil, Gold; Gold Ball Bonding

AD9501 PIN DESCRIPTIONS

Pin No.	Name	Function
1	$+V_S$	Positive voltage supply; nominally +5 V.
2	LATCH	TTL/CMOS register control line. Logic HIGH latches input data D_0–D_7. Register is transparent for logic LOW.
3	TRIGGER	TTL/CMOS-compatible input. Rising edge triggers the internal ramp generator, and begins the delay cycle.
4	RESET	TTL/CMOS-compatible input. Logic HIGH resets the ramp voltage and OUTPUT.
5	DAC OUTPUT	Output voltage of the internal digital-to-analog converter.
6	C_{EXT}	Optional external capacitor connected to $+V_S$; used with R_{SET} and 8.5 pF internal capacitor to determine full-scale delay range (t_{DFS}).
7	R_{SET}	External resistor to ground, used to determine full-scale delay range (t_{DFS}).
8	OFFSET ADJUST	Normally connected to GROUND. Can be used to adjust minimum propagation delay (t_{PD}); see Theory of Operation text.
9	GROUND	Circuit ground return.
10	OUTPUT	TTL-compatible delayed output pulse.
11	$+V_S$	Positive voltage supply; nominally +5 V.
12-19	D_0–D_7	TTL/CMOS-compatible inputs, used to set the programmed delay of the AD9501 delayed ouput. D_0 is LSB and D_7 is MSB.
20	GROUND	Circuit ground return.



AD9501 Equivalent Circuits

THEORY OF OPERATION

The AD9501 is a digitally programmable delay device. Its function is to provide a precise incremental delay between input and output, proportional to an 8-bit digital word applied to its delay control port. Incremental delay resolution is 10 ps at the minimum full-scale range of 2.5 ns. Digital delay data inputs, latch, trigger and reset are all TTL/CMOS-compatible. Output is TTL-compatible.

Refer to the block diagram of the AD9501.

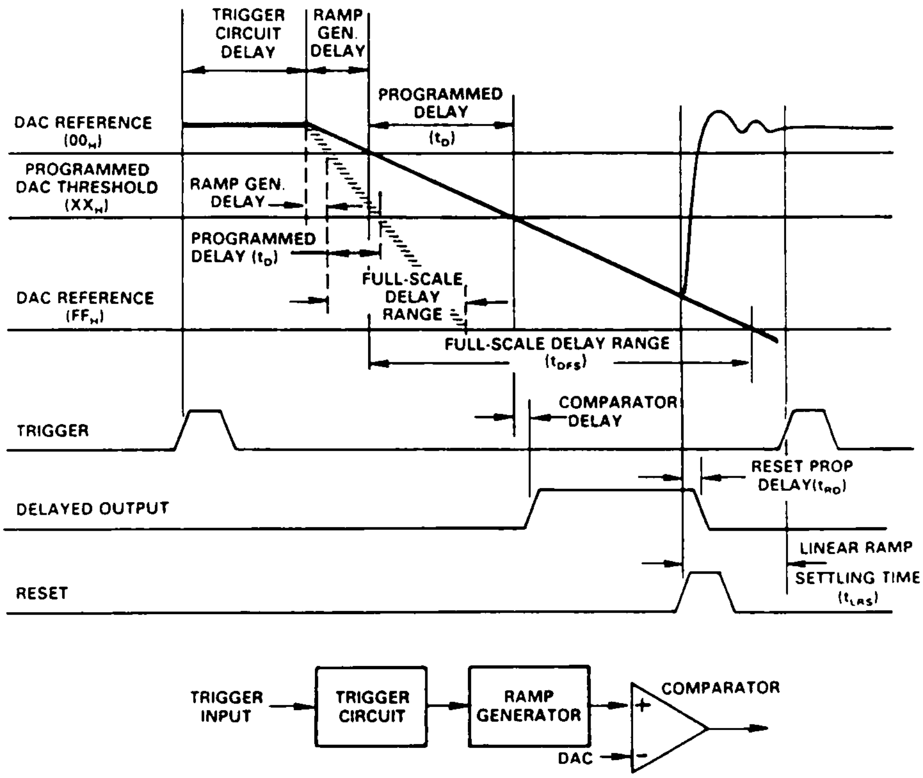
Inside the unit, there are three main subcircuits: a linear ramp generator, an 8-bit digital-to-analog converter (DAC) and a voltage comparator. The rising edge of the input (TRIGGER) pulse initiates the delay cycle by triggering the ramp generator. The voltage comparator monitors the ramp voltage and switches the delayed output (Pin 10) HIGH when the ramp voltage crosses the threshold set by the DAC output voltage. The DAC threshold voltage is programmed by the user with digital inputs.

Figure 1, the AD9501 Internal Timing diagram, illustrates in detail how the delay is determined. Minimum Delay (t_{PD}) is the sum of Trigger Circuit delay, Ramp Generator delay, and Comparator delay.

The Trigger Circuit delay and Comparator delay are fixed; Ramp Generator delay is a variable affected by the rate of change of the linear ramp and (to a lesser degree) the value of the offset voltage described below.

Maximum Delay is the sum of Minimum Delay (t_{PD}) and Full-Scale Program Delay (t_{DFS}).

Ramp Generator delay is the time required for the ramp to slew from its reset voltage to the most positive DAC reference volt- (00_H). The difference in these two voltages is nominally 18 (with OFFSET ADJUST open) or 34 mV (OFFSET ADJU grounded).



MINIMUM PROPAGATION DELAY = (t_{PD}) = TRIGGER CIRCUIT DELAY + RAMP GENERATOR DELAY + COMPARATOR DELAY

MAXIMUM PROPAGATION DELAY = MINIMUM PROPAGATION DELAY(t_{PD}) + FULL-SCALE DELAY RANGE (t_{DFS})

PROGRAMMED DELAY (t_D) = $\left(\frac{\text{DIGITALVALUE}}{256}\right) R_{SET} (C_{EXT} + 8.5\ \text{pF}) (3.84)$

TOTAL DELAY = (t_{PD}) + (t_D)

AD9501 TESTED WITH C_{EXT} = 0 pF, R_{SET} = 3.09 kΩ (100 ns PROGRAMMED DELAY)

Figure 1. AD9501 Internal Timing

Offset between the two levels is necessary for three reasons. First, offset allows the ramp to reset and settle without re-entering the voltage range of the DAC. Second, the DAC may overshoot as it switches to its most positive value (00_H); this could lead to false output pulses if there were no offset between the ramp reset voltage and the upper reference. Overshoot on the ramp could also lead to false outputs without the offset. Finally, the ramp is slightly nonlinear for a short interval when it is first started; the offset shifts the most positive DAC level below this nonlinear region and maintains ramp linearity for short programmed delay settings.

Pin 8 of the AD9501 is called OFFSET ADJUST (see block diagram) and allows the user to control the amount of offset separating the initial ramp voltage and the most positive DAC reference. This, in turn, causes the Ramp Generator delay to vary.

Figure 2 shows differences in timing which occur if OFFSET ADJUST Pin 8 is grounded or open. The variable Ramp Generator delay is the major component of the three components which comprise Minimum Delay (t_{PD}) and, therefore, is affected by the connection to Pin 8.

It is preferable to ground Pin 8 because the smaller offset that results from leaving it open increases the possibility of false output pulses. When grounding the pin, it should be grounded directly or connected to ground through a resistor or potentiometer with a value of 10 kΩ or less.

Caution is urged when using resistance in series with Pin 8. The possibility of false output pulses, as discussed above, is increased under these circumstances. Using resistance in series with Pin 8 is recommended only when matching minimum delays between two or more AD9501 devices; it is not recommended if using a single AD9501. Changing the resistance between Pin 8 and ground from zero to 10 kΩ varies the Ramp Generator Delay by approximately 35%.

The Full-Scale Delay Range (t_{DFS}) can be calculated from the equation:

$$(t_{DFS}) = R_{SET} \times (C_{EXT} + 8.5\ pF) \times 3.84$$

Whenever Full-Scale Delay Range is 326 ns or less, C_{EXT} should be left open. Additional capacitance and/or larger values of R_{SET} increase the Linear Ramp Settling Time, which reduces the maximum trigger rate. When delays longer than 326 ns are required, up to 500 pF can be connected from C_{EXT} to $+V_S$. R_{SET} should be selected in the range from 50 Ω to 10 kΩ. Graph 1 shows typical Full-Scale Delay Ranges for various values of R_{SET} and C_{EXT}.

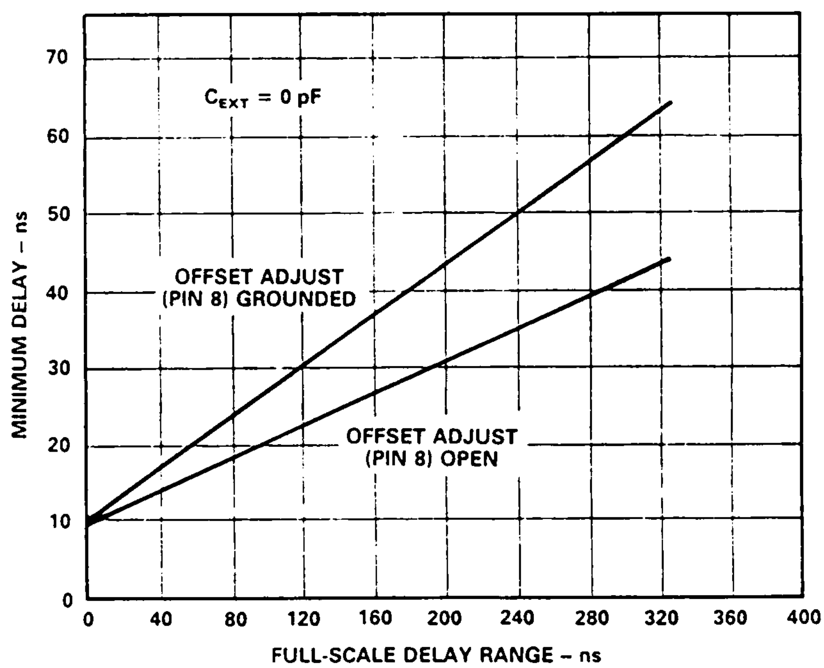
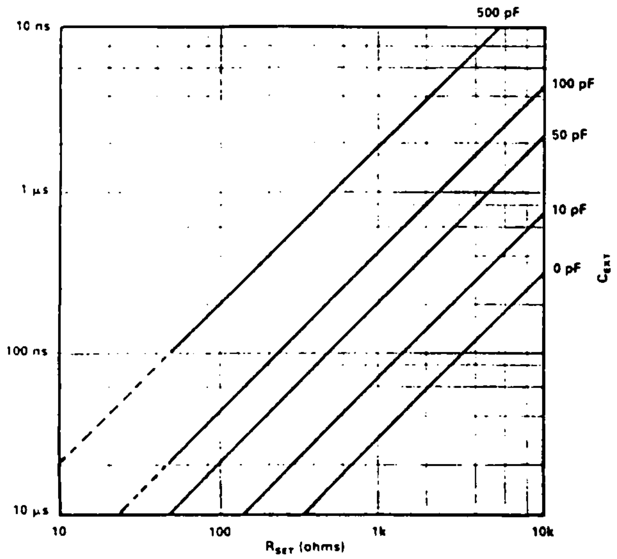


Figure 2. AD9501 Minimum Delay (t_{PD}) vs. Full-Scale Delay Range (t_{DFS})

Ramp charging current and DAC full-scale current are slaved together in the AD9501 to minimize delay drift over temperature. To preserve the unit's low drift performance, both R_{SET} and C_{EXT} should have low temperature coefficients. Resistors which are used should be 1% metal film types.

The programmed delay (t_D) is set by the DAC inputs, D_0–D_7.



Graph 1. RC Values vs. Full-Scale Delay Range (t_{DFS})

The minimum delay through the AD9501 corresponds to an input code of 00_H, and FF_H gives the full-scale delay. Any programmed delay can be approximated by:

$$t_D = (DAC\ code/256) \times t_{DFS}$$

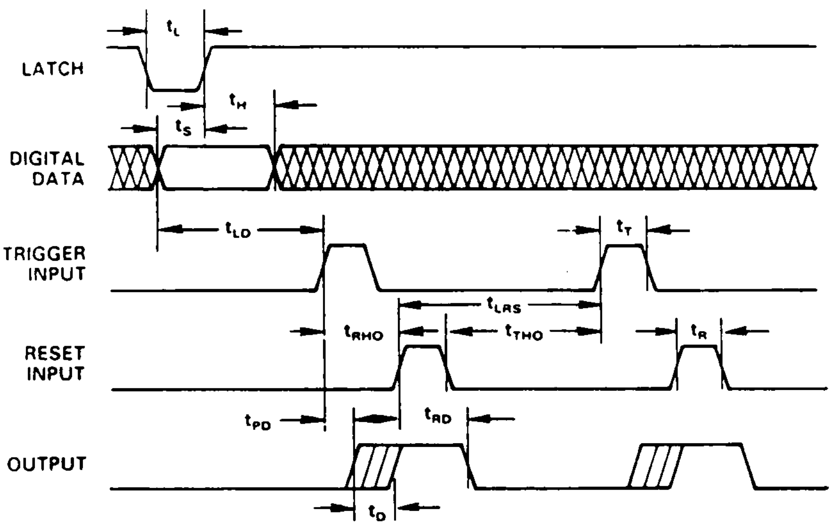
Total delay through the AD9501 for any given DAC code is equal to:

$$t_{TOTAL} = t_D + t_{PD}$$

As shown on the block diagram, TTL/CMOS latches are included to store the digital delay data. Data is latched when LATCH is HIGH. When LATCH is LOW, the latches are transparent, and the DAC will attempt to follow any changes on inputs D_0–D_7.

The System Timing Diagram, Figure 3, shows the timing relationship between the input data and the latch. The DAC settling time (t_{LD}) is approximately 30 ns. After the digital (Programmed Delay) data is updated, a minimum 30 ns must elapse between the time LATCH goes high and the arrival of a TRIGGER pulse to assure rated pulse delay accuracy.

When RESET goes HIGH, the ramp timing capacitor (C_{EXT} + 8.5 pF) is discharged. The RESET input is level-sensitive, and overrides the TRIGGER input. Therefore, any trigger pulse which occurs when RESET is HIGH will not produce an output pulse. As shown on the system timing diagram, Figure 3, the next trigger pulse should not occur before the Linear Ramp Settling Time (t_{LRS}) interval is completed to assure rated pulse delay accuracy.



NOTE: A TRIGGERING EVENT MAY OCCUR AT ANY TIME THE INTERNAL DAC (PROGRAMMED DELAY) IS BEING CHANGED. TRIGGERING EVENTS DURING THE INTERNAL DAC SETTLING TIME MAY NOT GENERATE AN ACCURATE PULSE DELAY.

t_L	- LATCH PULSE WIDTH	t_{RHO}	- TRIGGER-TO-RESET HOLD-OFF
t_H	- DIGITAL HOLD TIME	t_{THO}	- RESET-TO-TRIGGER HOLD-OFF
t_S	- DIGITAL DATA SETUP TIME	t_R	- RESET PULSE WIDTH
t_{LD}	- DAC SETTLING TIME	t_{PD}	- MINIMUM PROPAGATION DELAY
t_T	- TRIGGER PULSE WIDTH	t_{RD}	- RESET PROPAGATION DELAY
t_{LRS}	- LINEAR RAMP SETTLING TIME	t_D	- PROGRAMMED DELAY

Figure 3. AD9501 System Timing

For most applications, OUTPUT can be tied to RESET. This causes the output pulse to be narrow (equal to the Reset Propagation Delay t_{RD}). Alternatively, an external pulse can be applied to RESET. To assure a valid output pulse, however, the delay between TRIGGER and RESET should be equal to or greater than the total delay of t_{PD} + t_D illustrated in the internal timing diagram Figure 1.

As shown in that figure, the capacitor voltage discharges very rapidly and includes a small amount of overshoot and ringing. Rated timing delay will not be realized unless subsequent trigger events are delayed until after the linear ramp settles to its reset voltage value.

The values for the various delay increments in the specification table are based on a Full-Scale Delay Range of 100 ns with OUTPUT tied to RESET (self-resetting operation).

When Full-Scale Delay Range is set for intervals shorter than 100 ns, the rate of change of the linear ramp is increased. This faster rate means the Maximum Trigger Rate shown in the specification table is increased because the Ramp Generator Delay and, consequently, Minimum Propagation Delay t_{PD} become smaller.

Linear Ramp Settling Time t_{LRS} also becomes shorter as Full-Scale Delay Range is decreased. Minimum Delays for various Full-Scale Delay Range values are shown in Figure 2.

APPLICATIONS

The AD9501 is useful in a wide variety of precision timing applications because of its ability to delay TTL/CMOS pulse edges by increments as small as 10 ps.

In Figure 4, the AD9501 typical circuit configuration, the delayed output is tied back to the RESET input. This will produce a narrow output pulse whose leading edge is delayed by an amount proportional to the 8-bit digital word stored in the on-board latches. For the configuration shown, the output pulse width will be equal to the Reset Propagation Delay (t_{RD}). If wider pulses are required, a delay can be inserted between OUTPUT and RESET. If preferred, an external pulse can be used as a reset input to control the timing of the falling edge (and consequently, the width) of the delayed output.

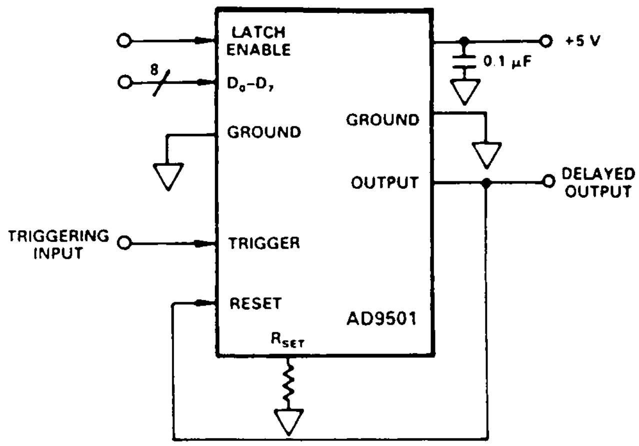


Figure 4. AD9501 Typical Circuit Configuration

Multiple Signal Path Deskewing

High speed electronic systems with parallel signal paths require that close delay matching be maintained. If delay mismatch (time skew) occurs, errors can occur during data transfer. For these situations, the matching of delays is generally accomplished by carefully matching lead lengths.

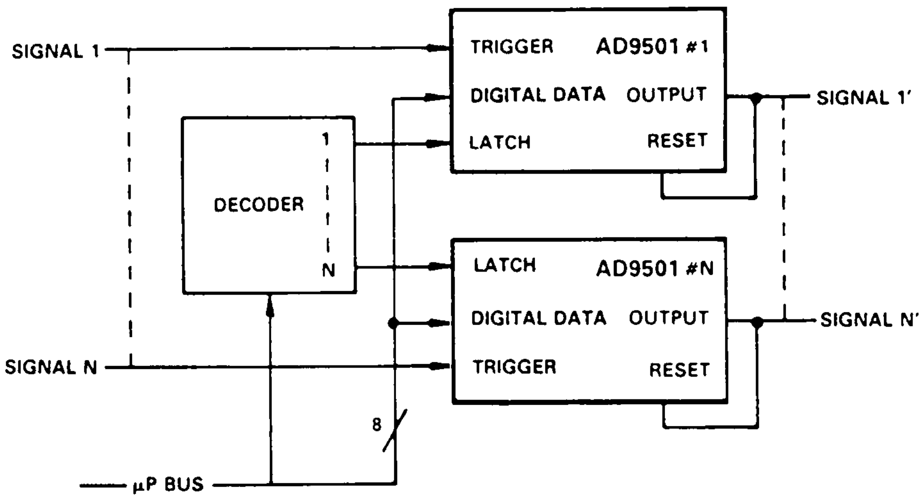
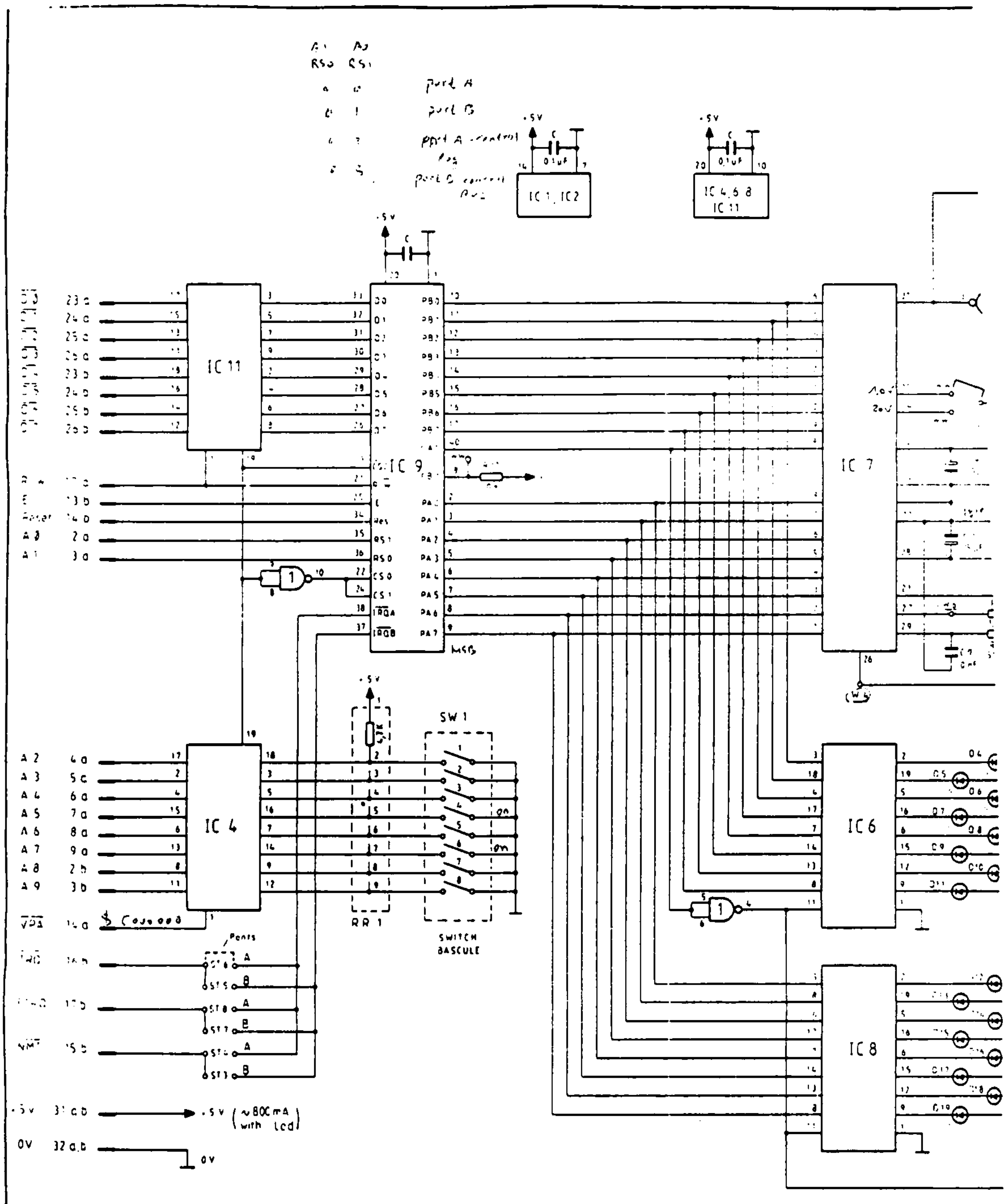


Figure 5. Multiple Signal Path Deskewing

Appendix D - PIA (MC6821B) : Circuit schematic



IC

IC 1,2	4093 BE
IC 3	123
IC 4	25LS 2521
IC 5	OP 27
IC 6,8	374
IC 7	ADC 76 KG
IC 9	PIA 6821
IC 10	TMC S 2 15.120
IC 11	74 LS 640
IC 12	AD 574 AKD

RESISTORS

All Resistors	AB 1/8 W - 5%	except
R 18	AB 1/4 W - 5%	
R9,10,11,12,15,16	Sfernice 0,01%	
R 13	Sfernice 1%	
RR 1 — RR 3	Bourns	

CAPACITORS

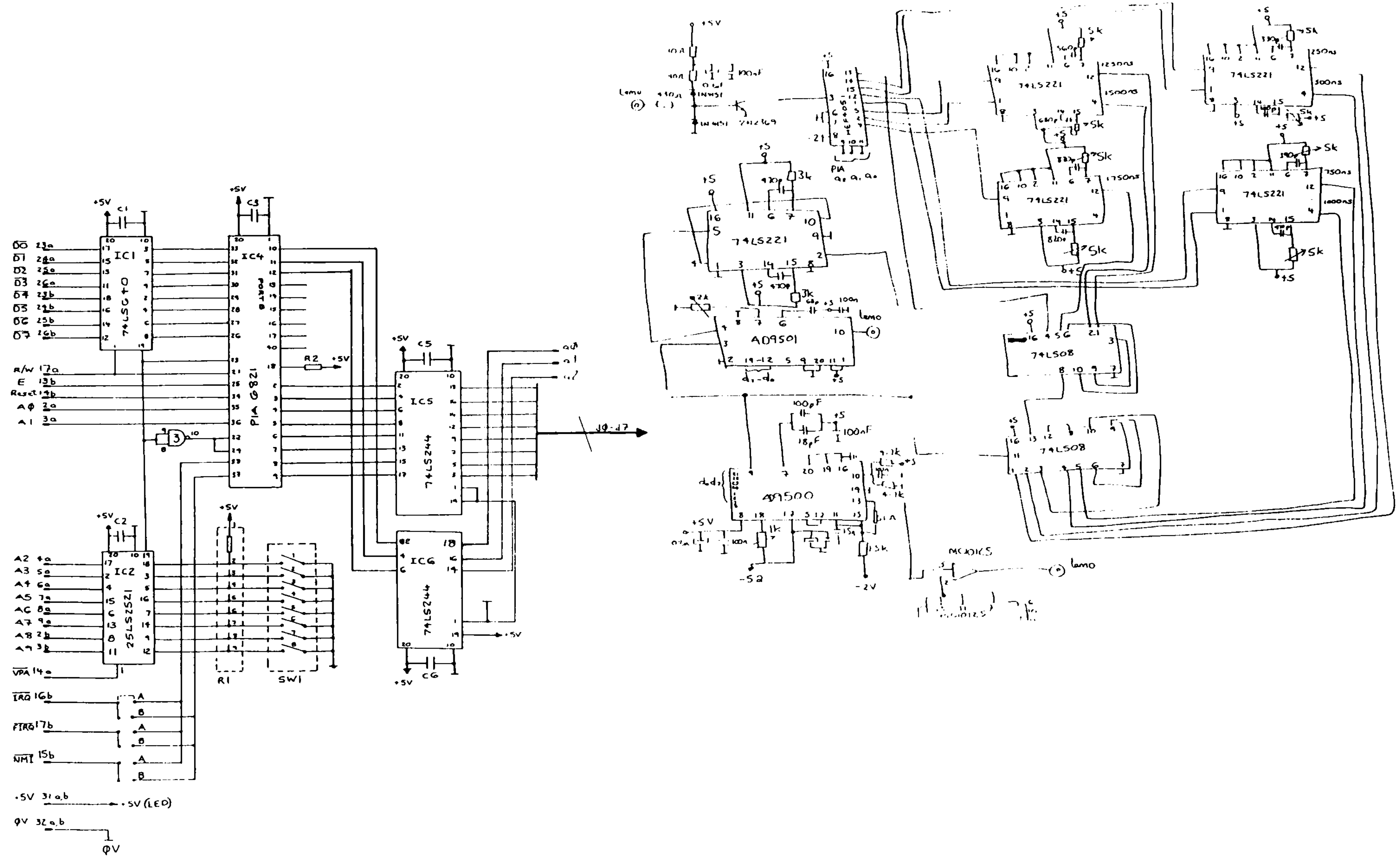
C 0,1µF	Ceramic
All Capacitors	Ceramic exc
C 2,4,11	Tantale perle
C 12	Wima
C 13	Tantale 15V
C7,8,10	Tantale perle

INDICE	DATE	NOM	ZONE	MODIFICATION

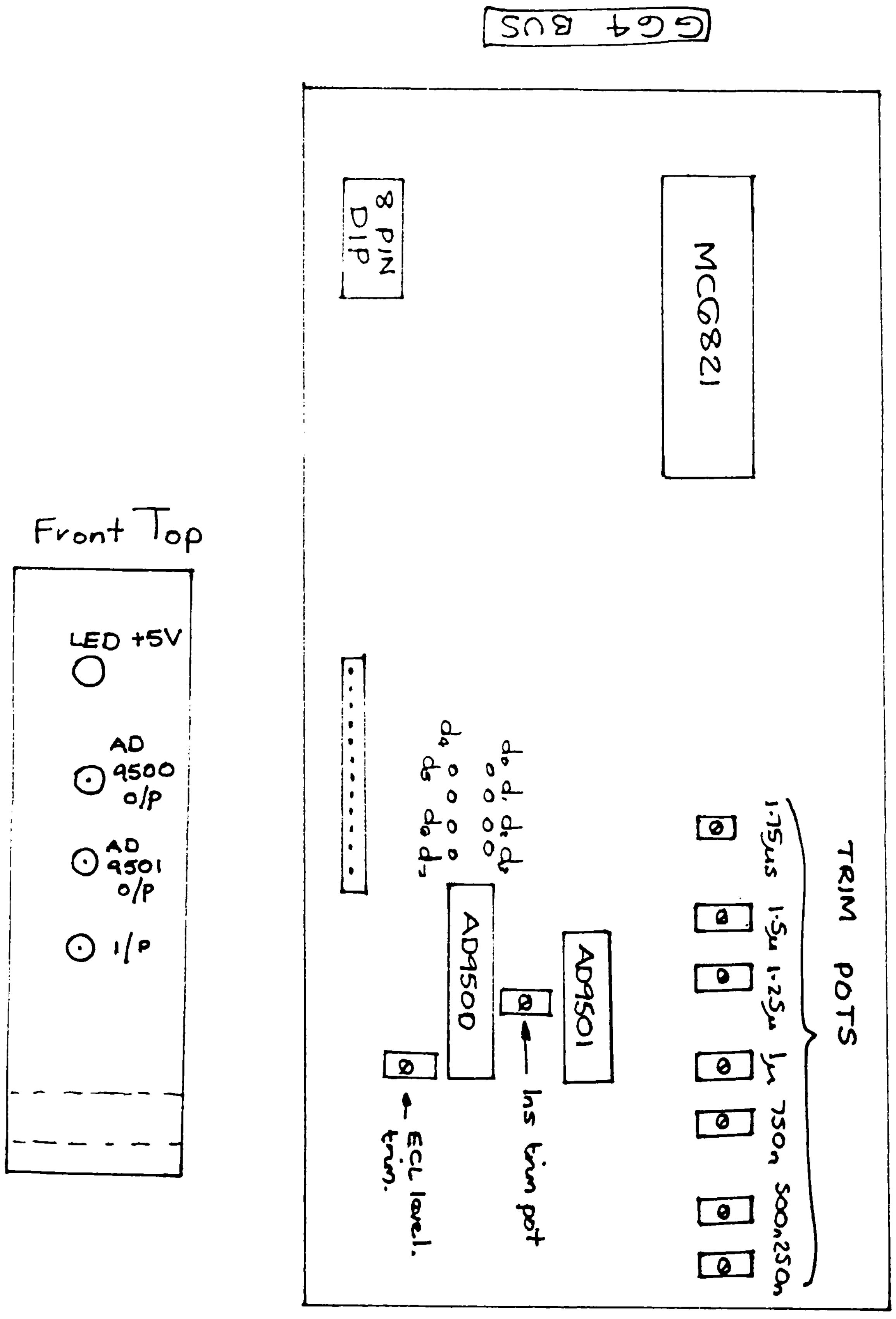
11 10 9 8 7 6

First angle projection
DESSIN HUGOT
SELON I. I - D CES

Appendix E - Test Card Circuit Schematic


IC1
74LS640
IC4
PIA 6821
PORT B
IC5
74LS244
IC6
74LS244
IC2
25LS2521
R1
SW1
R2
C1
C2
C3
C5
C6
D0-D7
+5V
R/W 17a
E 13b
A0 2a
A1 3a
A2 4a
A3 5a
A4 6a
A5 7a
A6 8a
A7 9a
A8 2b
A9 3b
VPA 14a
IRQ 16b
FIRQ 17b
NMI 15b
+5V 31a,b
+5V (LED)
0V 32a,b
0V
74LS221
74LS508
AD9501
AD9500
lemo
PIA
100nF
100pF
18pF
250ns
500ns
750ns
1000ns
-5.2
-2V

Appendix F - Test Card Circuit Layout Guide


GG4 BUS
8 PIN DIP
MC6821
TRIM POTS
1.75μs
1.5μs
1.25μs
1μs
750n
500n
250n
AD9500
AD9501
1ns trim pot
ECL level. trim.
Front Top
LED +5V
AD 9500 o/P
AD 9501 o/P
I/P