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The Timepix4 analog front-end design: Lessons learnt on fundamental limits to noise and time resolution in highly segmented hybrid pixel detectors

R. Ballabriga [a,*], J.A. Alozy [a], F.N. Bandi [a], G. Blaj [b], M. Campbell [a], P. Christodoulou [a,c,d], V. Coco [a], A. Dorda [a,e], S. Emiliani [a,h], K. Heijhoff [f], E. Heijne [a,c], T. Hofmann [a], J. Kaplon [a], A. Koukab [h], I. Kremastiotis [a], X. Llopart [a], M. Noy [a], A. Paterno [a], M. Piller [a,g], J.M. Sallesse [h], V. Sriskaran [a], L. Tlustos [a,c], M. van Beuzekom [f]

[a] CERN, Experimental Physics Department, Meyrin, 1211, Switzerland
[b] SLAC National Accelerator Laboratory, Menlo Park, 94025, CA, United States
[c] IEAP, Czech Technical University in Prague, Prague, 11000, Czech Republic
[d] Department of Biomedical technology, Faculty of Biomedical Engineering, Czech Technical University in Prague, nam. Sitna 3105, Kladno, 272 01, Czech Republic
[e] KIT - Karlsruhe Institute of Technology, Institute for Data Processing and Electronics (IPE), Hermann-von-Helmholtz-Platz 1, Eggenstein-Leopoldshafen, 76344, Germany
[f] Nikhef, Science Park 105, Amsterdam, 1098, Netherlands
[g] Institute of Electronics, Graz University of Technology, Graz, 8010, Austria
[h] Electron Device Modeling and Technology Laboratory (EDLAB), Ecole Polytechnique Federale de Lausanne (EPFL), Lausanne, 1015, Switzerland

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ABSTRACT

This manuscript describes the optimization of the front-end readout electronics for high granularity hybrid pixel detectors. The theoretical study aims at minimizing the noise and jitter. The model presented here is validated with both circuit post layout simulations and measurements on the Timepix4 Application Specific Integrated Circuit (ASIC). The analog front-end circuit and the procedure to optimize the dimensions of the main transistors are described with detail.

The Timepix4 is the most recent ASIC designed in the framework of the Medipix4 Collaboration. It was manufactured in 65 nm CMOS process, and consists of a four side buttable matrix of 448 × 512 pixels with 55 μm pitch. The analog front-end has a gain of ~36 mV/ke$^-$ when configured in *High Gain Mode*, and ~20 mV/ke$^-$ when configured in *Low Gain Mode*. The Equivalent Noise Charge (ENC) is ~68 e$^-_{rms}$ and ~80 e$^-_{rms}$ in *High Gain Mode* and in *Low Gain Mode* respectively. In *event driven mode* the incoming hits can be time stamped within a ~ 200 ps time bin and the chip can deal with a maximum flux of ~ 3.6 MHz mm^{-2} s^{-1}. In *photon counting mode*, the chip can deal with up to ~ 5 GHz mm^{-2} s^{-1}.

The routine designed to optimize the Timepix4 front-end is then used to analyze the performance limits in terms of jitter and noise for Charge Sensitive Amplifiers in pixel detectors.

1. Introduction

Hybrid pixel detectors have led to advances in many fields of science and industrial applications due to the ability for the readout Application Specific Integrated Circuit (ASIC) to process the signal deposited in the sensor by individual particles and extract relevant information. The circuit to readout the small signal induced in the detector electrodes is usually a Charge Sensitive Amplifier (CSA) [1].

In this work the authors present the key parameters involved in the optimization of the analog front-end of a hybrid pixel detector for low jitter and for low noise. The study is based on the development done for the design of the CSA for Timepix4, which is the latest hybrid pixel detector readout chip designed in the framework of the international Medipix Collaborations [2].

The rest of the introduction is dedicated to present the Hybrid Pixel Detector technology, some of its applications and readout ASICs that have been designed with the purpose of precise particle time stamping. In Section 2 the modeling of the sensor is presented with emphasis on describing a simplified model of a widely used planar silicon sensor. Section 3 presents the calculations that are implemented in a routine that has been written to optimize the biasing and the dimensions of the transistors in the CSA. We start with the modeling of the MOS transistors using the EKV model equations [3] and then model the CSA

* Corresponding author.
E-mail address: rafael.ballabriga@cern.ch (R. Ballabriga).

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and the comparator using a small signal circuit analysis. In Section 4 the results from calculations are validated by transistor level simulations and measurements on the Timepix4 chip [4].

The purpose of this study is to give general guidelines on the design of front-ends and to explore the fundamental limits in the noise and time resolution, by analyzing the contribution that is introduced by the front-end electronics in the detection system. The results are based on the studies leading to the design of previous front-ends and, in particular, this article focuses on the specific design of the analog front-end for the Timepix4 ASIC. The final time resolution of the system depends on the convolution of the uncorrelated uncertainties in the time measurement introduced by different elements in the detector chain (e.g. the sensor itself or the Time-to-Digital Converter (TDC)). Although in this paper we briefly mention these effects, and in particular those related to the sensor, it is not in the scope of this manuscript to cover them in detail. Section 5 presents the key simulation results. Section 6 summarizes and concludes with the key findings.

1.1. Hybrid pixel detectors

A Hybrid Pixel Detector is a 2-dimensional matrix of microscopic radiation sensitive semiconductor elements, each of which is connected to its own pulse processing electronics chain. The sensor material and the readout electronics are processed in different substrates and connected together with a fine pitch interconnection technology. The electronics ASIC, that is typically designed for the readout of highly segmented semiconductor material sensors, can also be used to read out the signal from other radiation detectors like Micro Channel Plates (MCPs) [5] or Gas Electron Multipliers (GEMs) [6]. The channel pitch is usually in the order of tens of μm. The detection channel consisting of a sensor and its readout electronics is sensitive to any type of incoming radiation whose interaction with the sensor induces a fast signal that exceeds (typically) a few hundred electrons. The technology has been used to detect X-ray photons [7–10], gamma photons [11,12], visible light photons [5], electrons [13], ions [14,15], neutrons [16], alpha particles [17] and other short lived particles [18].

Fig. 1 shows the cross section of a hybrid pixel detector. The semiconductor sensor material and the readout electronics are shown. They are connected via fine pitch flip-chip technology. The hybrid architecture allows to connect different semiconductor materials to the readout ASIC, for example Si, GaAs, CdTe, CdZnTe, Ge or perovskites [7]. This allows for optimization of the system depending on the requirements for the application in terms of type and energy of the radiation. The electronics can be designed to measure different characteristics of the incoming radiation. One can measure:

- The number of particles deposited during a given exposure.
- The energy deposited by a particle.
- The time of arrival.
- The incoming type of particle, based on the shape of the cluster of pixels responding to a single charge deposition event [15].
- The angle of incidence of the incoming particle based on the difference of time of arrival of the drifting charge in the different pixels [18].

1.2. Applications

Hybrid pixel detectors were first developed for High Energy Physics (HEP) in the late 1980s and beginning of 1990s for the tracking detectors of particle Collider experiments which are the detector elements which are closest to the interaction point. Their purpose is to disentangle the various particle tracks and to assign them to primary or secondary vertices. The very high track density together with a high beam crossing rate lead to the following requirements:

- Good spatial resolution (in the micrometer range) to distinguish closely separated tracks.
- The ability to tag hits to single bunch crossings (bunch crossings in the Large Hadron Collider (LHC) [19] are separated by 25 ns).
- The ability to store the data on pixel or on chip permitting triggering and data reduction.
- Low effective mass in order not to disturb particle identification in the outer detectors.
- Low power consumption to minimize the cooling infrastructure.
- High radiation tolerance for the detectors and readout electronics.
- Short readout time to cope with high event rates.

In High Energy Physics, the "objects" to be imaged are the interactions (events) between colliding particles, which result in a number of other particles originating at the collision point. The ionization created by these particles in a suitable medium (e.g. semiconductor material or gas) makes possible the reconstruction of the particle tracks [20]. Hybrid pixel detectors were first tested in a three pixel chip telescope in 1991 [21] and successfully used in the lead beam experiment WA97 [22]. That experiment demonstrated the potential of the technology in terms of high Signal to Noise Ratio (SNR) and detection efficiency of the system. Currently the ATLAS (A Toroidal LHC ApparatuS), CMS (Compact Muon Solenoid), and LHCb (Large Hadron Collider beauty) experiments at the LHC are equipped with inner tracking detectors based on hybrid pixels. During runs 1 and 2, the LHCb experiment had a photon detector system which also used hybrid pixels in its readout. All these systems have proven to provide vital data contributing to the discovery of the Higgs boson by the ATLAS and the CMS experiments at the LHC that validated the Englert–Brout–Higgs mechanism explaining the origin of mass of the subatomic particles in the standard model. This lead to the award of the Nobel Prize in physics (2013) to François Englert and Peter Higgs for their theoretical prediction of the mechanism.

With some modifications of the ASIC architecture, the same technology that was developed to "image" the collisions between particles has been transferred to other applications and has contributed to advances in many fields of science.

Hybrid pixel detectors have played a key role in synchrotron and Free Electron Laser (FEL) applications which revolutionized fields like biology, medicine or material science [10,23].

Another example of a field where hybrid pixel detectors implementing photon counting architecture are contributing to a "revolution" is spectral Computed Tomography (CT) in medicine [24]. The technology allows to optimize the Contrast-to-Noise Ratio (CNR) compared to Energy Integrating Detectors obtaining better image quality and reduction in dose. It allows for reduction of beam hardening artifacts. Hybrid pixel detectors also provide intrinsically a better spatial resolution with respect to scintillator based technologies, whose resolution is in the order of 1 mm. Spectral photon counting CT has the potential for quantitative multiple k-edge imaging, which has been demonstrated in both phantom and in vivo studies [25].

The technology of hybrid pixel detectors has been transferred to many other research and industrial fields like medical imaging [7], synchrotron applications [8,9], and Free Electron Lasers [10] X-ray inspection, material analysis using X-rays, electron microscopy [13], mass spectrometry [14], dosimetry (including dosimetry in space [15]), adaptive optics, education [17], neutron imaging [16] and other.

Some applications, like HEP and mass spectrometry, require a precise time stamping of the incoming particle hits. In HEP, at the High Luminosity LHC, the number of collisions per beam crossing is going to increase to ~ 200 (pile up events) [26]. This leads a challenge in particle track reconstruction and assignment to primary vertices. Adding precise timing within the bunch crossing can lead to recover the precision of the vertex reconstruction. In other HEP applications, precise particle timing can also lead to the reduction of events from background or reflections [27]. In mass spectrometry, an improvement in the time resolution of the arrival time of incoming ions to the detector leads to an improved mass resolution.

These applications have different requirements in terms of sensor type, pixel size, power consumption, sensor leakage current (before and after detector irradiation), etc. This paper aims at presenting a routine as well as the key equations related to the optimization of the front-end readout electronics for highly segmented (from ∼ 10 µm to 200 µm pitch) hybrid pixel detector readout chips.

1.3. State of the art designs

A number of hybrid detector readout chips have been designed to time stamp the time of arrival of the incoming particles. The Timepix chip [28], designed in 0.25 µm CMOS, contains a matrix of 256 × 256 pixels, each 55 µm × 55 µm, in which a 100 MHz clock is distributed from the pixel periphery along the columns. The time bin is 10 ns. The pixel can be configured to measure either (1) event counts per acquisition time, (2) time of arrival (ToA) by means of counting clock ticks from the time the discriminator is fired until the shutter closes or (3) energy by counting clock ticks while the preamplifier output exceeds the threshold (Time over threshold (ToT)). The readout of the chip is frame based, i.e. the 14-bit counters of all the pixels are read out sequentially after the shutter is closed.

The Timepix3 chip [29] has the same matrix and pixel dimensions as its predecessor. It was designed in a 130 nm CMOS technology and included a data driven architecture in which when a pixel is hit, it initiates the process to send the data off chip. When the discriminator fires, it latches a 14-bit time stamp provided by an on chip 40 MHz gray-encoded ramp counter. It also starts a ring oscillator at 640 MHz which increases a fine time stamp counter until the next clock rising edge, providing a 1.56 ns fine time bin. The output data packet contains 48 bits which include ToA and ToT information as well as the coordinates of the hit pixel. The voltage controlled ring oscillator is shared between a group of 8 pixels.

TDCpix [30] is a hybrid pixel detector chip designed for the readout of the GigaTracker of the NA62 experiment at CERN. It contains a matrix of 40 × 45 pixels with 300 µm pitch. The dynamic range of the front-end is from 0.8 fC to 10 fC. The overall response of the front-end is equivalent to a CR-RC^3 shaping function. The discriminated signal from the pixel is sent differentially through a transmission line to the periphery of the chip where there is a bank of Time-to-Digital Converters (TDCs) with ∼ 100 ps time bin. The full system measured a time resolution of ∼ 72 ps_{rms} when the sensor was illuminated with a laser impinging at the center of the pixel and inducing a signal corresponding to 2.4 fC.

tPix [31] is a hybrid pixel detector developed for momentum spectroscopy experiments at the Linac Coherent Light Source (LCLS). The pixel pitch is 100 µm. The time critical signals, such as the global clock, are distributed to the pixels through a balanced hierarchical signal tree. After the incoming hit deposits a signal above the threshold, the output of the comparator is fed to a 16-cells ring oscillator until the arrival of the next global clock rising edge. At this point, the state of the internal phases of the oscillator are sampled providing fine time measurement. The number of cycles of the signal within the ring oscillator are counted and represent other 2 (normal mode) or 6 (high dynamic range mode) coarse bits. The delay elements in the ring oscillator determine the time bin and are implemented with fully differential delay cells. The measured time resolution is 100 ps (the measurement range is 26 µs).

The Timespot INFN project [32] aims at developing a complete demonstrator of a tracking device, from sensors to track reconstruction. The project includes the design of a radiation-hard highly segmented hybrid pixel detector. The 55 µm pixel contains an analog front-end and a dedicated Vernier TDC with its two Digital Controlled Oscillators (DCOs) running at a frequency close to 1 GHz. Measurements on the first prototype standalone were done and showed a TDC resolution below 50 ps, with an average of 23 ps. The resolution of the analog front-end was quantified to be below 100 ps with an average of 43 ps. The power consumption of the front-end, for these measurements, was kept below 40 µW [33].

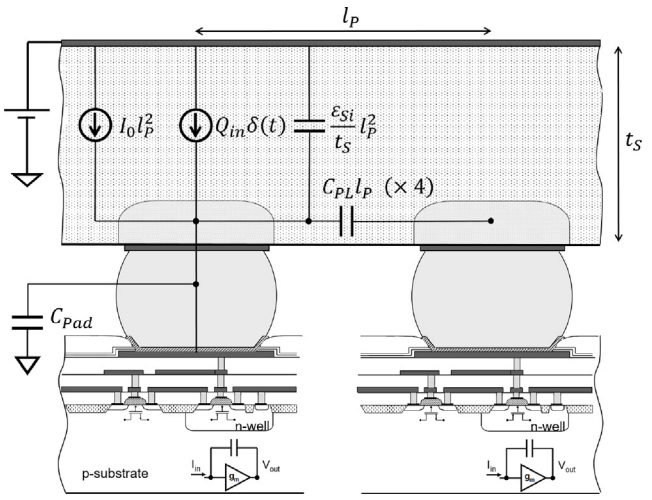

Fig. 1. Sensor geometry and modeling for a semiconductor planar sensor (not to scale).

ALTIROC1 is a hybrid pixel detector readout ASIC that is designed for the High Luminosity-LHC upgrade [34]. ALTIROC1 contains 25 channels and is designed in 130 nm CMOS technology for the readout of 1.3 mm pitch Low Gain Avalanche Diodes (LGADs) of the ATLAS High-Granularity Timing Detector (HGTD) detector. Test bench measurements on the prototype chip showed a jitter lower than 35 ps_{rms} at 4 fC using the internal calibration test pulse (with the sensor connected), and a threshold that could be set as low as 2 fC. The power consumption per channel is 4.5 mW.

2. Sensor geometry modeling

For the calculations presented in this paper, the sensor is modeled with a current source that delivers a Dirac Delta pulse representing the current induced in the presence of a particle interacting with the sensor and also a DC component representative of the detector leakage current. The current source is in parallel with the intrinsic detector capacitance. The detector capacitance is modeled with three components (1) a fixed value capacitance that depends on the geometry of the pixel, (2) a capacitance which is directly proportional to the pixel pitch and (3) a capacitance proportional to the pixel area. No inductance element is accounted for due to the intimate interconnection of the sensor with the readout electronics. This leads to a sensor model which can be adapted to different sensor geometries, from silicon planar sensors (see Fig. 1) to configurations in which the detector operates with an MCP in vacuum (see Fig. 2).

The signal from the sensor is read out by a circuit consisting of a CSA followed by a comparator. This is valid and representative of highly segmented hybrid pixel detectors [2,8,32,35]. The signal processing chain of typical readout circuits for semiconductor detectors usually contains a pulse shaper, that is an analog filter which defines the *shape* of the signal at the output of the analog chain and defines its signal to noise ratio [1]. A shaper circuit has not been accounted for in this work because in complex fine-pitch pixel detectors, there is not enough area in the pixel to integrate this electronic circuit in the space allocated to the analog front-end. This has implications on the relations between performance and circuit parameters. The discriminator in this work is considered to compare the signal with the threshold on the leading edge.

The model presented here is aimed at calculating the contribution to the jitter and to the noise introduced by the analog readout electronics for a given detector geometry.

2.1. Silicon planar sensor geometry

Fig. 1 illustrates the modeled components for the particular case of a silicon planar sensor. Two current sources represent (1) the pulse generated by the incoming radiation and (2) the sensor leakage current. The pitch of a square pixel is denoted by the variable l_p. The induced charge is represented by Q_{in}.

The sensor leakage current is modeled by a current source delivering a current that is proportional to the pixel area (l_p^2). I_0 represents the sensor leakage current per unit area.

The capacitances and their dependence on the geometry are also shown in the picture. The detector capacitance is calculated as a combination of three components with different dependence on the pixel pitch:

$$C_D = C_0 + C_1 l_p + C_2 l_p^2 = C_{PAD} + 4C_{PL} l_p + \frac{\epsilon_{Si}}{t_s} l_p^2 \quad (1)$$

where C_D is the total capacitance per pixel. C_0 represents the component which is independent of the pixel pitch, that is dominated by parasitic metal to metal capacitances in the readout ASIC. The exact value of this component depends on the chip architecture and on the Back End Of Line (BEOL) of the selected CMOS process. Its value can range from ∼20 fF for small pixels in the order of ∼50 µm [36] to ∼80 fF for the latest state of the art architectures in which the sensor pads are connected to the pixels through a redistribution layer (RDL) as is the case for the Timepix4 chip. C_1 represents the interpixel capacitance due to the side wall capacitance of the diodes (although this value depends on the sensor geometry, for example, on the distance between the pixel implants, an approximation is taken as 1 pF cm^{-1} [37]. C_2 is the capacitance from the pixel to the backside electrode. In this model, and for simplicity, the infinite parallel plate capacitance model is considered and in consequence $C_2 = \epsilon_{Si}/t_s$, where ϵ_{Si} is the permittivity of silicon and t_s the sensor thickness.

2.1.1. High energy charged particle detection

In [38], the time resolution of silicon detectors was derived for high energy particles that deposit energy along their entire path through the sensor and perpendicular to the sensor plane. The energy deposition follows a Landau distribution. For thin (50 µm) sensors in which the sensor voltage is biased such that the carriers move at velocity saturated speeds (>200 V), the electrons take ∼0.6 ns to traverse the sensor and the holes ∼0.8 ns. The time resolution in the induced current by a Minimum Ionizing Particle (MIP) is ∼10 ps. This is based on the calculation of the center of gravity of the current time signal.

For 200 µm sensors in which the sensor voltage is biased such that the carriers move at velocity saturated speeds, the signal develops in less than ∼3 ns. The time resolution in the induced current in that case is ∼30 ps.

In highly segmented hybrid pixel detectors, given the values of the intrinsic capacitances in the sensor and in the readout electronics (in the order of a few tens of fF), and for the level of power consumption of a matrix of elements (in the order of 1 W cm^{-2}), the time constant of the rise time of the signal at the preamplifier output will be >3 ns. This justifies the assumption that from now on, the procedure to optimize the electronics assumes that the peaking time of the electronics response to a delta pulse is larger than the sensor pulse (i.e. there is no ballistic deficit). This assumption is valid for calculating the contribution from the electronics to the jitter of the system.

However, in systems aiming at particle time stamping at the ∼10 ps level, sensor effects degrading the timing should be accounted for. The first effect is that the dependency of the weighting field shape on the position of the interaction in the detector leads to position dependent differences in the pulse shape. These variations cannot be accurately compensated for with ToT [39]. The second effect is charge straggling [40] that means that fluctuations in the number of electron/hole pairs created along the path of the particle introduce fluctuations on the shape of the induced signal. As a practical example of the impact of the two effects, the full time resolution of the TDCpix [39] was measured to be 71 ps$_{\text{rms}}$. The measurement was done with a laser pulse shining the center of a pixel and inducing a well reproducible signal corresponding to ∼ 2.4 fC. The test beam with minimum ionizing particles showed a time resolution of 115 ps$_{\text{rms}}$ [39].

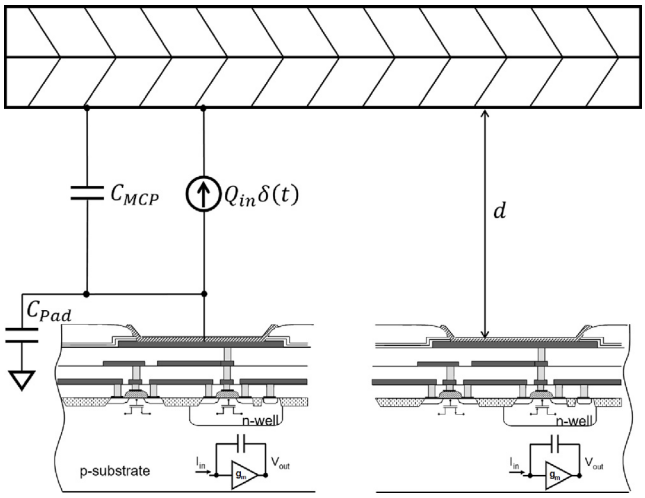

Fig. 2. Sensor geometry and modeling for a hybrid pixel readout chip configured to read the signal from an MCP (not to scale).

The small pixel effect in pixels in which the pitch is small with respect to the sensor thickness combined with the ability of those pixels to measure time, allows to reconstruct the ionization path of charged particles inside the detector using the same detection principles used in a Time Projection Chamber (TPC) [18,41].

2.1.2. X-ray photons

Precise X-ray photon time stamping with planar sensors is a challenge. The energy of X-ray photons, when interacting through photoelectric effect, is deposited as a cloud of electron hole pairs, near the interaction point. The probability distribution of interaction depths is an exponential decay, depending on photon energy. This results in both large drift times (for typical n-type, 10 kΩ cm 300 µm sensors biased at 200 V the drift time from the front to the back of the sensor is ∼13 ns) and large differences in drift times when the photons interact at different depths in the sensor [42]. The jitter is also in the order of 0 ns to 13 ns. The charge shape and implicitly the induced pulse shape at the pixel readout pads depends on the interaction depth and on the physical location on the pixel surface in which the deposition took place, up to about 1 ns FWHM [42]. Thinner planar sensors would lead to a decrease in the jitter, for example, in a 75 µm p-type sensor biased at 200 V the photon jitter would drop down to ∼ 1.4 ns but at the expense of reduced detector efficiency.

2.2. Extension to other sensor geometries

Note that other types of sensors can also be studied using the simplified sensor model presented above. For example 3D silicon sensors [43] could be modeled by changing the values of the components C_1 and C_2 to account for the specific geometry of this detector. A photocathode detector with an MCP as an amplification layer could also be modeled with the components $C_1 \to 0$, $C_2 \to 0$ and Q_{in} accounting for the charge amplified by secondary electron emission in the MCP pores [5].

3. Electronics modeling

The electronics for the readout of very fine pitch hybrid pixel detectors usually consists of a CSA followed by a discriminator. The amplifier

integrates the charge delivered by the sensor into a capacitance producing a pulse with an amplitude proportional to the energy deposited by the incoming particle. The discriminator compares the pulse with an energy threshold which is set above the intrinsic electronics noise. This allows noise hit free measurements. Before analyzing the CSA circuit and showing the steps in the optimization procedure, the complete modeling of the input transistor is reviewed.

3.1. Input transistor

The circuit has been modeled using the charge-based EKV transistor model [3,44] and following a design procedure inspired by the methodology presented in [45–48]. The method has been adapted to the particularities of CSA design for hybrid pixel detectors. For example, in [45], the starting point in choosing the transistor dimensions and drain current is the assumption that the gain bandwidth product and the output capacitance are known for the circuit under design. Our approach relies on the optimization of the input transistor dimensions and operating point based on the assumption that a given current is available for the analog front-end which is determined from a given power density budget ($\mathrm{W\,cm^{-2}}$) allocated at a system level to the pixel matrix.

A brief description of the model used and its equations are presented for completeness. In the EKV model, the parameter that is used to evaluate the operation region of a transistor is the *Inversion Coefficient* (IC), which is a measurement of the inversion level of the channel of a MOS transistor. The IC is also an indicator of how efficiently we use current to generate gain (transconductance) [48]. This parameter replaces the overdrive voltage ($V_{OV} = V_{GS} - V_T$) and enables a continuous and accurate model even for moderate and weak inversion. This is especially important in very deep submicron processes in which the strong inversion region is shrinking with technology downscaling.

In the following, and for simplicity, the transistors to be optimized will be considered in the saturation region. The inversion coefficient is defined as [49]:

$$IC = \frac{I_D}{I_{SPEC}} \tag{2}$$

where (I_{SPEC}) is the specific current [49]:

$$I_{SPEC} = 2nU_T^2\mu C_{OX}\frac{W}{L} = I_{spec\square}\frac{W}{L} \tag{3}$$

and $n = 1 + C_{Dep}/C_{OX}$ is the slope factor. C_{Dep} is the channel bulk depletion capacitance per unit area and C_{OX} is the oxide capacitance, also per unit area. $U_T = K_BT/q$ is the thermodynamic voltage, μ is the low field mobility in the channel region and W and L are the transistor width and length respectively.

An $IC > 10$ corresponds to the strong inversion region of operation and is usually chosen for high speed (high transit frequency (f_t)) or for improved matching in current mirrors. An $IC < 0.1$ corresponds to the transistor operating in weak inversion region. This operating point is typically used in low-power low-voltage applications, where V_{DSsat} is minimum. Weak inversion is also chosen to maximize the transconductance that can be achieved for a given current and also to minimize the offset mismatch in differential input pairs.

The region between the two i.e. $0.1 < IC < 10$ corresponds to moderate inversion which provides a good trade off between speed, current efficiency and circuit area.

The following equation gives the expression for the small signal MOS transconductance for a given current. The equation includes velocity saturation effects [49,50].

$$\frac{g_m}{I_D} = \frac{1}{nU_T}\frac{\sqrt{(\lambda_C IC+1)^2+4IC}-1}{IC(\lambda_C(\lambda_C IC+1)+2)} \tag{4}$$

where $\lambda_C = L_{sat}/L$ is the fraction of the channel in full velocity saturation, $L_{sat} = 2\mu_0 U_T/v_{sat}$ is the length of the channel which is in velocity saturation and v_{sat} is the velocity saturation of carriers.

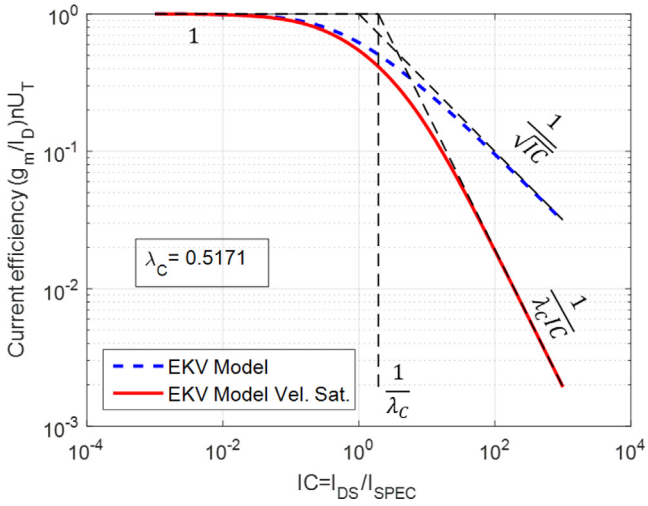

Fig. 3. Normalized g_m/I_D for the model with and without including velocity saturation.

A plot of the value of g_m/I_D normalized by nU_T is shown in Fig. 3. The plot shows the model with and without accounting for velocity saturation effects. The only input parameter for the plot is λ_C. The calculation of this parameter was assumed for a commercial 65 nm CMOS process for a 100 nm transistor length. The transistor length in the following calculations is chosen larger than the minimum allowed by the technology in order to obtain an increased DC gain (g_m/g_{ds}) in the design of analog circuits. Choosing a non-minimal gate length is also beneficial to obtain a decreased noise excess factor [51]. Note that the model provides a continuous function from very deep weak inversion to strong inversion and velocity saturation regions. It can be observed from the plot that the velocity saturation effect creates a decrease in the current efficiency. Also note that the region corresponding to strong inversion is very small in the case that the velocity saturation effects taking place on short transistors are accounted for in the model.

The MOS capacitances are modeled as [52]:

$$C_{GS} = \frac{WLC_{OX}}{\frac{3}{2}+\frac{1}{ICf(IC)}} + W\Delta LC_{OX} \tag{5}$$

where

$$f(IC) = \frac{1}{0.5(\sqrt{1+4IC}+1)} \tag{6}$$

$$C_{GB} = \frac{n-1}{n}\left(1-\frac{(3/2)ICf(IC)}{(2/3)+ICf(IC)}\right)WLC_{OX} \tag{7}$$

$$C_{GD} = C_{OV}W \tag{8}$$

where C_{OV} is the overlap capacitance C_{OV} ~0.69 $\mathrm{fF\,\mu m^{-1}}$. This value has been extracted from transistor level simulations. The second term in Eq. (5) corresponds to the contribution of the overlap capacitance to C_{GS}.

$$C_{DB} = C_{JSW}(2W+2L_{diff}) + C_{JS}(WL_{diff}) \tag{9}$$

where L_{diff} is the diffusion length. In the presented model, the value of C_{DB} was approximated by the product of the transistor width and a constant ($0.84\,\mathrm{fF\,\mu m^{-1}}$). The value was extracted from transistor simulation results using the models provided by the foundry.

The gate referred noise voltage spectrum of the CMOS transistor is

$$S_e^2(f) = S_W^2 + \frac{K_f}{C_{ox}WL}\frac{1}{f^{\alpha_f}} \tag{10}$$

The first term is the thermal white noise of the transistor and the second term is the flicker noise contribution. The thermal white noise is given by

$$S_W^2 = 4K_BT\frac{\Gamma}{g_m} \tag{11}$$

where $\Gamma = \alpha_w n\gamma$. α_w is the noise excess factor, which for 65 nm CMOS technology was measured as $\sim$ 1.09 for NMOS transistors and $\sim$ 1.04 for PMOS transistors (for devices longer than the minimum available length) [51]. n is the slope factor and γ is a coefficient which also depends on the Inversion Coefficient and goes from 1/2 in weak inversion region to 2/3 in strong inversion region and can be approximated as

$$\gamma = \frac{\frac{1}{2} + \frac{2}{3}IC}{1 + IC} \tag{12}$$

The second term in (10) represents the $1/f$ noise. K_f is a process parameter and α_f is a parameter close to unity. The Gate Induced Current (GIC) noise [53,54], that originates from the coupling of local fluctuations in the channel to the gate through C_{GS} is not accounted for in this work as its contribution is negligible due to the small dimensions of the input transistor.

3.2. CSA equations

The charge sensitive amplifier is modeled with the simplified circuit in Fig. 4. The sensor model presented earlier can be identified from the current source I_{DET} in parallel with the capacitance C_{DET}. M_0 represents the input transistor that is biased with a current I_{BIAS}. The first amplifier stage consists of a common source with a cascoded PMOS input transistor. The choice of the PMOS flavor is made in order to allow the circuit to load the output capacitance C_O without slew rate limitations when reading out negative polarity sensors (the impact of slew rate limitations on the measured jitter will be shown, later in Section 4). The bias current I_{BIAS} depends on the pixel area and the specified power density (W cm^{-2}). The cascode increases the gain of the amplifier and also avoids the gate to drain capacitance (C_{GD}) of the input transistor (M_0) to appear in parallel with the feedback capacitance C_{FB} in which the charge delivered by the sensor is integrated. The increase in gain achieved with the cascode technique (and, as previously mentioned, choosing the length of the transistor larger than the minimum available by the technology) helps decreasing the input impedance of the amplifier. This increases the percentage of the charge that is delivered by the sensor that is effectively integrated in the feedback capacitor. Note also that the cascode bias voltage V_{BIAS} might be generated by a feedback loop that samples and amplifies (with a negative gain) the voltage at v_Y in order to increase further the low frequency gain of the stage (the circuit would be referred as a regulated cascode [55]). The implementation of the current source labeled $(1-K)I_{BIAS}$ allows to obtain both a high transconductance for transistor M_0 and a large output impedance in node v_X. This increases the gain of the amplifier at low frequencies. The amplifier is followed by a unity gain buffer that is typically implemented with a common drain stage. Keeping the requirement presented previously to amplify the signal delivered by negative polarity sensors without slew rate limitations, the input transistor of the common-drain buffer should be an NMOS transistor because the pulses at nodes v_X and v_{OUT} have positive polarity [1]. The buffer decouples the high impedance node from the output of the CSA from the load of the circuit. R_{FB} is a high value resistance in parallel with C_{FB} that resets the voltage at the capacitor after a pulse has developed. The function of this resistance is usually implemented with active circuits [56].

As it can be seen in the simplified schematic in Fig. 4, the feedback loop contains an NMOS transistor (M_2) in parallel with the feedback capacitance. This transistor allows to extend the dynamic range of the time over threshold measurement in the positive polarity. It acts as a non-linear capacitor which presents a low capacitance in response to small pulses, as long as the preamplifier pulse amplitude is smaller than the threshold voltage of the transistor. When the pulse amplitude exceeds the threshold voltage, its channel becomes inverted and the capacitance increases to $C_{OX}WL$. To minimize the gate-to-drain and the gate-to-source overlap capacitances, which would appear in parallel

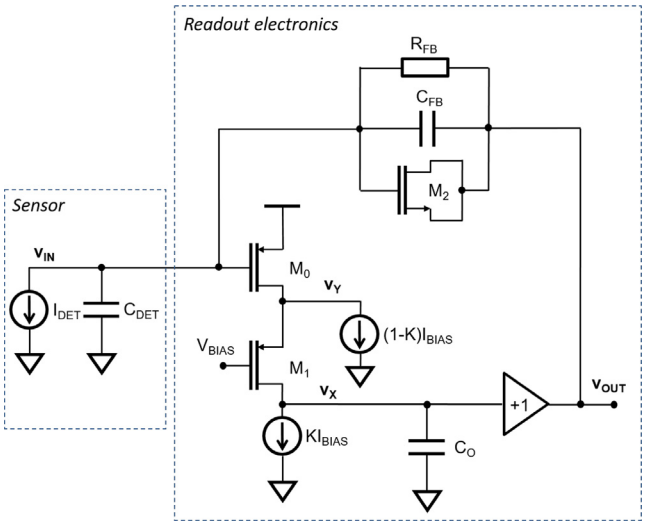

Fig. 4. Simplified schematic of the charge sensitive amplifier.

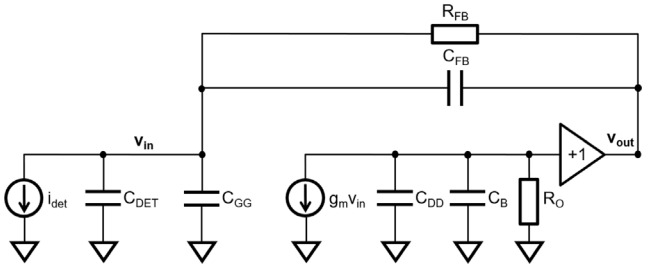

Fig. 5. CSA small signal model.

with the feedback capacitance, the transistor is sized long and narrow. The technique was presented by Manghisoni in a design developed for X-ray Free Electron Laser experiments [57].

Fig. 5 shows the small signal model of the charge sensitive amplifier. We can define the input capacitance as

$$C_{IN} = C_{DET} + C_{GG} + C_{FB} \tag{13}$$

where $C_{GG} = C_{GS} + C_{GB} + C_{GD}$ of the input transistor. We define the output capacitance as

$$C_O = C_{DD} + C_B \tag{14}$$

where C_{DD} is the capacitance of the cascode transistor (M_1 in Fig. 4). C_B is the input impedance of the buffer and also includes the parasitic capacitance from the interconnection of the amplifier with the level shifter.

With respect to the unity gain buffer, a level shifter (common drain stage) is considered and in consequence, the input capacitance is equal to the $C_{GD}+C_{GB}$ of its input transistor. The C_{GS} of this transistor is not accounted for as, at a first approximation, it is bootstrapped. Strictly speaking, this capacitance vanishes from the equations if the body effect and the channel length modulation effects are not accounted for, which is the case for the calculations presented here. In the case the two effects were taken into account in the equations, a fraction of C_{GS} would have to be included in C_B. The main transistor of the level shifter is assumed to be dimensioned to operate in the moderate inversion region ($IC = 1$) as a trade off between speed, drain to source saturation voltage optimization and minimization of the parasitic capacitances of the device which might lead to a decrease in the slope of the voltage and in consequence, to a degradation of the jitter [47].

3.2.1. Signal analysis

In response to a Dirac Delta pulse at the input, corresponding to the induced signal from the detector in the input pad, the transfer function from the CSA is

$$H(s) = \frac{v_{out}}{i_{det}}(s) = \frac{R_{FB}}{(1+\tau_f s)(1+\tau_r s)} \tag{15}$$

where $\tau_r = (C_{IN} + C_{FB})C_O/g_m C_{FB}$ is the time constant associated to the rise time of the signal. Note that $1/\tau_r$ is the gain bandwidth product of the amplifier's open loop gain. $\tau_f = R_{FB}C_{FB}$ is the time constant associated to the fall time (i.e. the time constant for the output of the charge amplifier to return to the baseline after a pulse has developed). In order to obtain the expression (15), the dominant pole approximation has been used i.e. $\tau_f > \tau_r$.

The time response, for a Dirac Delta pulse carrying a charge Q_{in} is then,

$$v_{out}(t) = \frac{Q_{in}R_{FB}}{\tau_f - \tau_r}\left(e^{-\frac{t}{\tau_f}} - e^{-\frac{t}{\tau_r}}\right) \tag{16}$$

In very fine granularity hybrid pixel detectors, it is not practical to implement the feedback element with a resistor, as it was shown in Fig. 4, and different solutions have been implemented with active devices [56]. In some cases this could lead to a deviation of the measured response with respect to the small signal model which is based on the linearization of the circuit around a specific operating point. Some of these non-linearities might be *beneficial* for the purpose of the measurements. For example, in the commonly known Krummenacher feedback [58], when the pulse at the output of the amplifier exceeds the thermodynamic voltage (U_T), the reset of the feedback capacitor is done at a constant current and this leads to a pulse duration at the preamplifier output which is linear with the injected signal at the input. This leads to a linear energy measurement by registering the time duration for which the signal at the preamplifier output is above threshold [59]. This deviation in the shape of the pulse during the return to zero has a negligible impact on the rise time part of the pulse unless the front-end is designed and biased for high flux applications where τ_f and τ_r are no longer well separated.

If we calculate the derivative of the time waveform at the time it crosses a threshold voltage V_{th}, then we have the slope dv/dt of the signal. This is required for the jitter calculation since the time uncertainty σ_t is the voltage noise σ_v over the slope of the signal $\sigma_t = \sigma_v/(dv/dt)$.

$$\frac{dv_{out}(t)}{dt} = \frac{Q_{in}g_m}{C_O(C_{IN}+C_{FB})}\frac{\frac{Q_{in}}{C_{FB}} - V_{th}}{\frac{Q_{in}}{C_{FB}}} \tag{17}$$

The Eq. (17) is obtained by assuming that the time constant associated with the fall time is significantly longer than ($\tau_f \gg \tau_r$). The high frequency poles in the circuit are neglected (for example the pole associated with the cascode or the pole related to the output impedance of the unity gain buffer) and this might lead to a small error in the calculation of the slope of the signal, in particular for threshold values which are very small. The simplification, which has been validated both with simulations and also with measurements [59], leads to expressions which help the designer to get insight on the circuit. The second term in Eq. (17) modulates the impact of the threshold on the slope of the signal. In this manuscript, this term is referred to as *normalized overdrive*. For very small thresholds compared to the signal amplitude (Q_{in}/C_{FB}) this term is close to unity. The term becomes close to zero when the amplitude of the incoming pulse is slightly above the threshold. In order to maximize the slope (and then minimize the time uncertainty) one can (1) maximize the input charge (for example using sensors with intrinsic gain), (2) maximize the transconductance (which is related to the drain current and the dimensions of the input transistor) or (3) minimize both the total input and output capacitances in the circuit. Decreasing the threshold (i.e. increasing the overdrive) also helps maximizing the slope but within some limits since for very low threshold values, the impact of the non dominant poles on the transfer function might lead to a decrease in the slope of the CSA output voltage signal in the time domain.

3.2.2. Noise analysis

The main noise sources in the circuit have been identified and their contributions to the Equivalent Noise Charge have been calculated. The first noise source is the thermal noise from the input transistor. This noise source is in series with the input and referred to as series noise. Its value, expressed in e^-_{rms} is:

$$ENC_S = \sqrt{\frac{K_B T \Gamma (C_{IN}+C_{FB})C_{FB}}{\beta C_O q^2}} \tag{18}$$

In Eq. (18), β is a parameter, smaller than one. It accounts for the impact of the degree of separation of the rise and fall time constants on the amplitude of the signal at the CSA output.

$$\beta = max\left(e^{-\frac{t}{\tau_1}} - e^{-\frac{t}{\tau_2}}\right), \text{for } t > 0 \tag{19}$$

An important conclusion from Eq. (18) is that, provided the rise time and the fall time constants are well separated (i.e. $\beta \approx 1$), the series noise due to the input transistor does not depend on its transconductance g_m and as a consequence, it is independent on the CSA's power consumption (since most of the power goes to the input transistor). The reason for this effect is that when the current in the input transistor is increased, its thermal noise decreases by the same amount as the bandwidth over which the thermal noise is integrated increases, the two effects canceling each other out. If the device operates in a low count rate environment substantial reductions in power consumption can be obtained with little or no noise penalty by reducing the bias current of the input transistor provided a good separation between the preamplifier rise and fall times is ensured [59].

A similar non-dependence of the series thermal noise with the input transistor's transconductance was presented for the readout of a monolithic pixel detector based on circuit based on a source follower to readout the small sensor diode [60].

Eq. (18) also shows that an increase in the output capacitance C_O can lead to a decrease in the series noise at the expense of degrading the jitter.

The non-dependence of the series thermal noise with the input transistor's transconductance is not observed in systems in which the charge sensitive amplifier is followed by a shaper. In that case, the noise is inversely proportional to the square root of the input transistor's transconductance [61].

From Eq. (18) it can be observed that the series noise does not strongly depend on technological parameters. The advantage of process downscaling in minimizing the component of the jitter related to the series noise comes through a potential reduction of C_0, that leads to an increase in the slope of the signal. However this potential advantage has to be evaluated on the specific selected process taking into account considerations for analog design like (1) transistor layout, (2) transistor mismatch or (3) additional noise sources related to downscaling [62].

The flicker noise of the input transistor is neglected here due to the broad band of the CSA circuit.

The second noise source considered here is the noise from the sensor diode. The sensor diode leakage current I_{leak} produces shot noise that can be modeled with a current source in parallel with the input with a one-sided power spectral density $2qI_{leak}$. Its contribution to the output, expressed in e^-_{rms} is:

$$ENC_{P_{det}} = \sqrt{\frac{(2qI_{leak})C_{FB}R_{FB}}{4\beta q^2}} = \sqrt{\frac{(2qI_{leak})C_{FB}2}{4\beta q^2 g_{mFB}}} = \sqrt{\frac{I_{leak}C_{FB}}{q\beta g_{mFB}}} \tag{20}$$

The third contribution considered comes from the feedback resistor element. In this study, we consider the implementation of the feedback reset network with active devices using the Krummenacher topology [58] which contains two feedback networks. The first network is responsible for resetting the CSA output voltage. The second, working

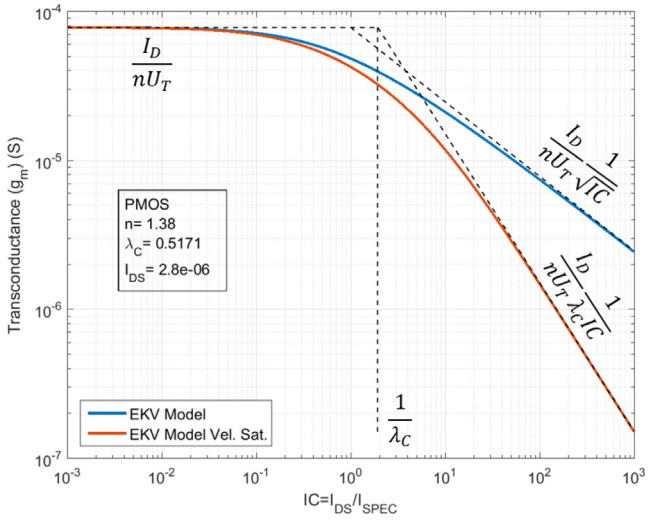

Fig. 6. Transconductance that can be obtained for the input transistor as a function of the Inversion Coefficient (IC), for a fixed bias current $I_{DS} = 2.8\,\mu A$. The asymptotes for the velocity without and with velocity saturation are shown.

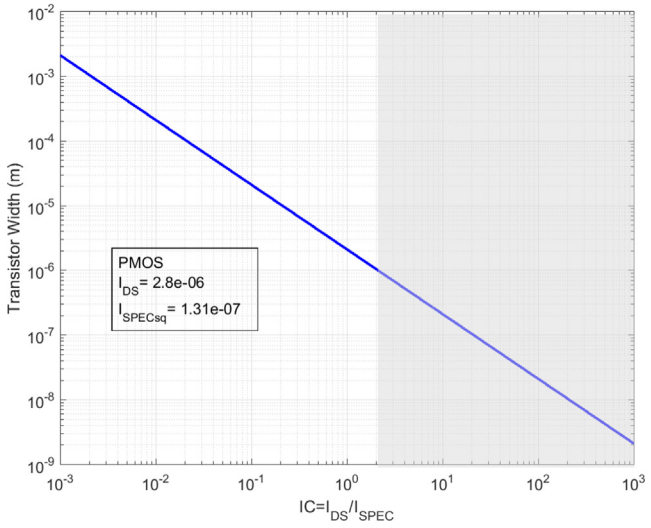

Fig. 7. Input transistor width as a function of the Inversion Coefficient (IC). (Transistor length (L) fixed to 100 nm, $I_{DS} = 2.8\,\mu A$.). The range of ICs for which the transistor width is below the minimum value chosen $W = 1\,\mu m$ is shown in gray.

at low frequencies, is responsible for compensating for the detector leakage current. For resetting the preamplifier output, the equivalent resistance R_{FB} is equal to $2/g_{mFB}$, where g_{mFB} is the transconductance of the transistors in the active feedback network. Its contribution to the total noise (expressed in e^-_{rms}) is:

$$ENC_{P_{MOS}} = \sqrt{\frac{2 \times 4K_B T n \gamma C_{FB}2}{4\beta q^2}} = \sqrt{\frac{4K_B T n \gamma C_{FB}}{q^2 \beta}} \quad (21)$$

As we can see from Eq. (18), (20) and (21), reducing the feedback capacitance C_{FB} is effective in reducing the ENC from different sources. However, for the different applications, the value of this capacitance is determined by the CSA gain and its dynamic range. Its lower value is limited by (1) the input impedance of the front-end, that is designed to integrate the charge delivered by the sensor and (2) the stability of the system for some front-end topologies like the commonly used Krummenacher architecture [58,63].

The total noise is then, the sum in quadrature of the three previously shown contributions

$$ENC_{Total} = \sqrt{ENC_S^2 + ENC_{P_{det}}^2 + ENC_{P_{MOS}}^2} \quad (22)$$

3.2.3. Jitter analysis

The jitter (expressed in s_{rms}) can be then expressed as the noise (V_{rms}) divided by the slope ($V\,s^{-1}$):

$$Jitter = \frac{qENC_{Total}}{\frac{dv_{out}(t)}{dt} C_{FB}} \quad (23)$$

3.3. Example of optimization procedure

The procedure for the optimization of the dimensions of the input transistor starts with generating a plot for the transconductance that can be obtained as a function of the input transistor's inversion coefficient. The drain to source current for this transistor is considered fixed, for the moment, and equal to 2.8 μA, which could be representative of a low power amplifier for a pixel with a size ∼ 50 μm. The plot is shown in Fig. 6.

The aspect ratio of the transistor can be directly calculated from combining Eqs. (2) and (3). The transistor width can then be calculated by fixing a value for the length. In this routine, the transistor length chosen was 100 nm (The minimum allowed by the CMOS process is 60 nm). Fig. 7 shows the function:

$$W = \frac{LI_D}{IC2nU_T^2 \mu C_{OX}} \quad (24)$$

Note from Fig. 7, that the value for the width of the transistor decreases with increasing the Inversion Coefficient. Working in weak inversion can yield very high values for the width of the transistor (leading to a large area for the implementation of the CSA). Please note as well that, for the bias current that has been chosen in this particular example (2.8 μA), there is an IC range for which the calculated width cannot be physically implemented because it is smaller than the minimum allowed dimension from the technology. This range is indicated in gray in the figures. In practice, the designer should not choose values that are too small, below ∼ 1 μm, because this could lead to a degradation of the circuit performance related to (1) decreased transistor mismatch, (2) flicker and Random Telegraphic Noise (RTN) [64] and (3) decreased radiation tolerance [65]. Also, it is a common practice to design the transistor width to allocate space for a minimum number of contacts in both the polysilicon and the transistor active areas. The multiplicity of contacts has a positive impact on the reliability of the integrated circuit. Also, the use of the Enclosed Layout Transistor (ELT) geometry is often used for the design of hybrid pixel detector readout chips in order to minimize the cumulative effects from radiation on the electronics. The use of these devices impacts the aspect ratio of the transistors [65].

The input transistor capacitances are shown in Fig. 8. Even though for a transistor of a fixed dimensions, C_{GS} increases with the inversion coefficient (IC), Fig. 8 shows a decrease in the capacitances with the inversion coefficient due to a decrease of the transistor dimensions. Note also that in the plot, it can be observed that the weight of C_{GS} increases with respect to the other capacitances in the transition from weak to strong inversion, which is also expected from the modeling.

With these elements we can now calculate the parameters of the circuit. Fig. 9 shows the slope of the preamplifier output voltage as a function of the inversion coefficient of the input transistor. As it can be observed in the figure, there is a maximum in the region of moderate inversion for the transistor. Starting from the left hand side of the plot, as the IC is increased, the area of the transistor is decreased (the drain to source current is fixed). The decrease in area leads to a decrease in the value of the intrinsic capacitances of the device leading to an increased slope. The reason why, after the peak, the slope drops

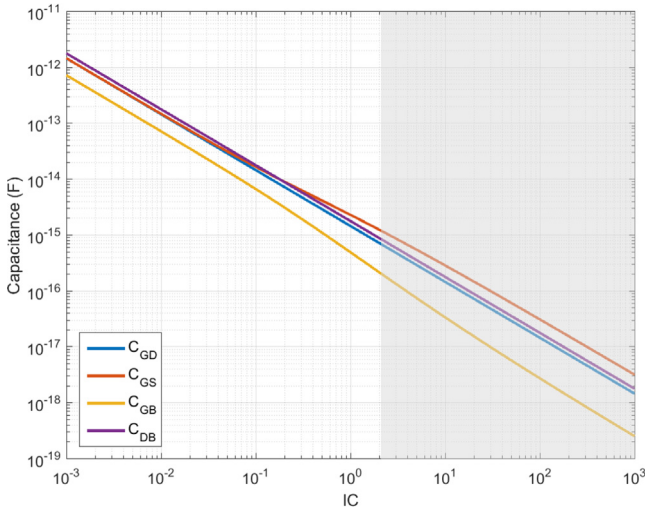

Fig. 8. Input transistor capacitances as a function of the Inversion Coefficient (IC). The values were calculated using equations in Section 3.1. (Transistor length (L) fixed to 100 nm, $I_{DS} = 2.8\,\mu$A.).

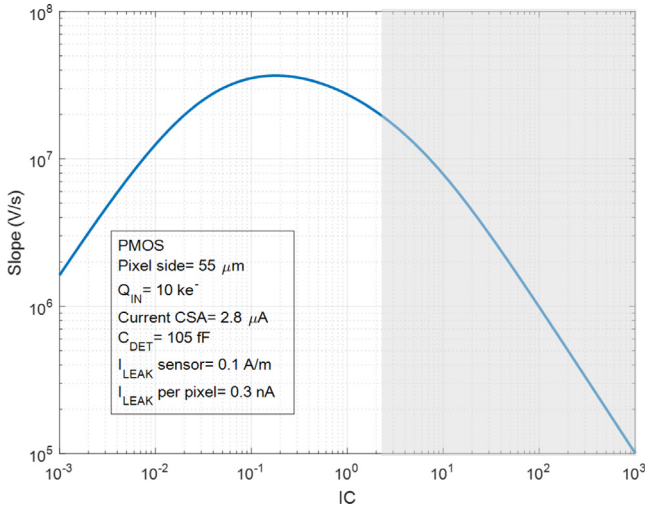

Fig. 9. Slope of the preamplifier output voltage as a function of the Inversion Coefficient (IC) of the input transistor. (Transistor length (L) fixed to 100 nm. Input charge chosen as 10 ke⁻.).

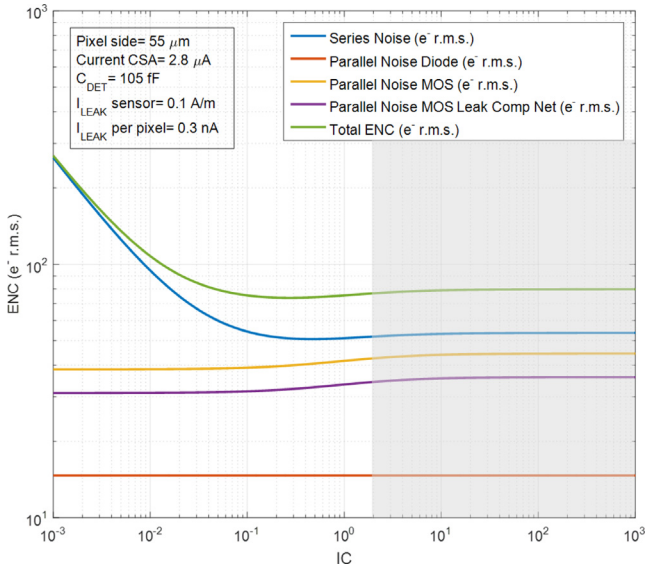

Fig. 10. Equivalent Noise Charge (ENC) expressed in e^-_{rms} as a function of the Inversion Coefficient (IC) of the input transistor. (Transistor length (L) fixed to 100 nm. The leakage current taken for this particular plot is 0.3 nA.).

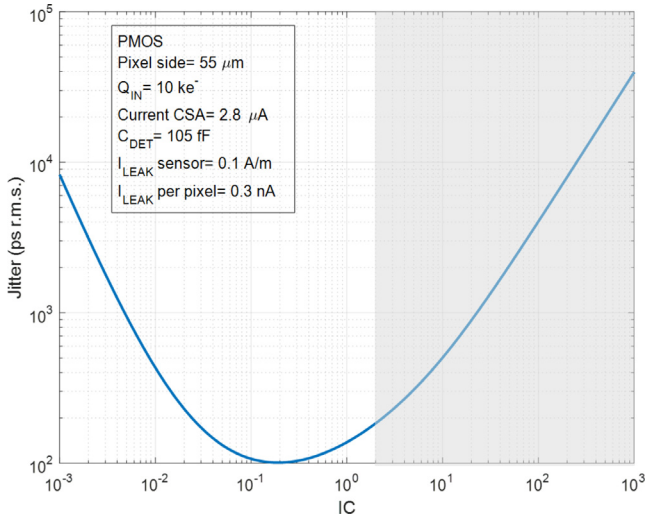

Fig. 11. Jitter at the preamplifier output expressed in ps_{rms} as a function of the Inversion Coefficient (IC) of the input transistor. (Transistor length (L) fixed to 100 nm. Input charge chosen as 10 ke⁻.).

with increasing the inversion coefficient is due to the decrease of the transconductance efficiency starting at moderate inversion (see Fig. 3).

The noise as a function of the inversion coefficient is shown in Fig. 10. For small values of the inversion coefficient, the large width of the input transistor leads to a large input capacitance which degrades the series noise of the system. A plateau is reached when the capacitance of the input transistor becomes small with respect to the sum of the detector capacitance and the internal metal to metal capacitance on the ASIC.

Fig. 11 shows the jitter for a 10 ke⁻ input charge. A minimum is shown for $IC \sim 0.2$. Fig. 12 shows the jitter at the preamplifier output as a function of the input charge. The jitter, as it can be observed from the plot, is inversely proportional to the input charge.

Table 1 summarizes the result of the optimization for the input transistor. The input transistor is biased with 2.8 µA current and the pixel pitch is 55 µm. The design assumes a silicon planar sensor with the model presented in Section 2. The chip includes an integrated redistribution layer for allowing the design to be tilable seamlessly on four sides [2,4]. This leads to an increase in the input capacitance with respect to the traditionally laid out three-side-buttable hybrid pixel detectors [29] whereby the pixel in the sensor matches the pixel in the readout electronics. The excess in capacitance impacts both the noise and the jitter. In the table, C_{IN} accounts for the sensor capacitance, the capacitance introduced by the redistribution layer and also the intrinsic capacitances of the input transistor. The operating point is the result of the optimization for jitter ($IC \sim 0.2$, $W \sim 10\,\mu$m). The transistor is at the limit between weak and moderate inversion which, in general, is a good trade off between speed, noise, drain to source saturation voltage, transconductance efficiency and circuit area.

3.4. Timepix4 comparator model

The Timepix4 comparator consists of a transconductance followed by a fast current mode amplifier [66]. A simplified schematic is shown in Fig. 13 (A), and the simplified small signal equivalent circuit is shown in (B). The schematic shows (1) the OTA (with gain $g_{m,comp}$) that

Table 1
Input transistor and system optimization. The input transistor is biased with 2.8 µA current. The values for the transistor capacitances were calculated using equations in Section 3.1. The input charge is 10 ke⁻. The pixel is connected to a 100 µm thick silicon sensor.

Symbol	Value	Units
C_{IN}	105	fF
W	11.16	µm
L	0.1	µm
g_m	64	µS
C_{GS}	9.5	fF
C_{GB}	3.3	fF
C_{GD}	7.7	fF
C_{DB}	9.4	fF
$V_{DS_{sat}}$	126	mV
$Noise$	73	e⁻ r m s
$Jitter$	100	ps r m s

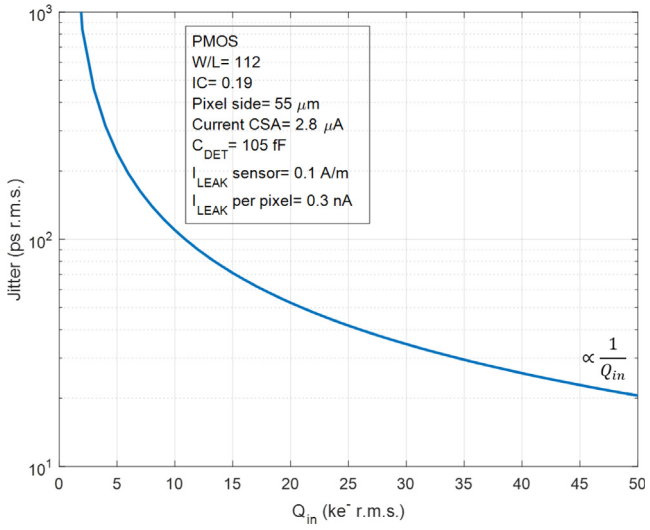

Fig. 12. Jitter at the preamplifier output expressed in ps_{rms} as a function of the input charge. (Transistor length (L) fixed to 100 nm. $I_D = 2.8$ µA.).

amplifies the difference between the output of the CSA and a voltage that represents the threshold and generates a current at its output, (2) a programmable 5-bit binary weighted current source Digital-to-Analog Converter (DAC) to correct from the random voltage offset in both the CSA and the OTA that leads to pixel-to-pixel threshold mismatch and (3) a zero crossing current amplifier [66].

The transfer function of the comparator, from the differential input to the single ended output is:

$$\frac{v_{out}}{v_{in}}(s) \sim \frac{g_{m,comp}R_{FB,comp}}{1+(C_{O,comp}+K_A C_{FB,comp})(R_{FB,comp}/K_A)s} \tag{25}$$

The jitter of the comparator was calculated as:

$$\sigma_t = \frac{\sigma_n}{\frac{dv}{dt}} = \frac{\sqrt{2}\sqrt{\frac{K_B T \gamma n g_{m,comp} R_{FB,comp}}{C_{FB,comp}}}}{\frac{\Delta_{in} g_m}{C_{FB,comp}}} \tag{26}$$

The expression assumes that the main noise source in the comparator are the transistors in the differential input pair of the transconductance amplifier (OTA in Fig. 13). $g_{m,comp}$ is the transconductance of the input stage of the comparator and Δ_{in} is the amplitude of the pulse at the output of the CSA, which is fed to the comparator input. This parameter is calculated using Eq. (27) in order to account for saturation effects on

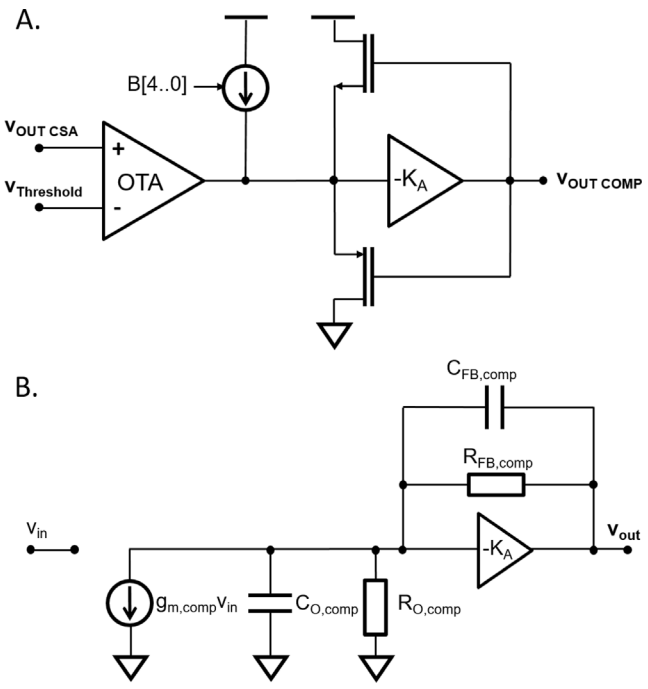

Fig. 13. A. Comparator simplified schematic. B. Small signal model.

the CSA output pulse:

$$\Delta_{in} = min\left(\frac{Q_{in}}{C_{FB,CSA}}, V_{sat,CSA}\right) \tag{27}$$

where $V_{sat,CSA}$ is the voltage at which the amplitude at the output of the CSA saturates. The routine also accounts for a limitation in the slope (denominator in (26)) due to slew rate effects.

Although the measurements match with the calculations for the comparator, this block will not be accounted for in the study in the next sections for three reasons. The first is that there are different comparator topologies that have been used in the past [1,67–69] and it is difficult to define a generic model relating the comparator power consumption with its time uncertainty. The second is the fact that the simplified model for the comparator presented above includes the transconductance (g_m), and as a consequence power dissipation, of only a subset of the transistors in the signal path. For example, the OTA in Fig. 13 might be implemented with a folded cascode architecture. In terms of Eq. (26), the important is to maximize the transconductance of the input transistors in order to maximize the slope and minimize the jitter. However, it is also necessary to allocate some power budget for the current mirrors which is difficult to account precisely in the generic model. Third, the non-linearities in the comparator are very difficult to model with a small signal circuit that is based on the linearization of the circuit around a quiescent operating point. For example, in Fig. 13, the feedback element of the second stage is based on two transistors whose transconductance might vary orders of magnitude during a comparator output state transition.

4. The Timepix4 analog front-end design and routine validation

The calculations with the small signal analysis have been validated with transistor level simulations and with measurement results from Timepix4. The chip, that was manufactured in a standard 65 nm CMOS process, consists of a matrix of 448 × 512 pixels with 55 µm pixel pitch. The novel aspects of this chip with respect to its predecessors are (1) the implementation of an architecture that allows the chip to be tiled seamlessly on four sides, (2) its reticle-sized dimensions (the chip measures 24.7 × 30 mm^2) and (3) the ∼ 200 ps time bin which leads

Table 2
Measurements on Timepix4 in High and Low Gain mode.

Measurement	High Gain Mode	Low Gain Mode	Units
Gain	~ 36	~ 20	mV/(ke$^-$)
Gain Variation	<2	<2	% min–max
Linearity	~ 7	~ 12	ke$^-$
ENC (mean value)	~ 68	~ 80	e$^-$ $_{rms}$
Threshold dispersion	<35	<60	e$^-$ $_{rms}$
Minimum Threshold	~450	~650	e$^-$

to a time resolution of $\sim 60\,\mathrm{ps}_{rms}$ (the time resolution is calculated as the standard deviation of the error in the measurement i.e. $200/\sqrt{12}$). Timepix4 can operate in data driven mode, in which the hit pixel sends off chip its coordinates, the measured energy and time information. In this mode of operation, the incoming hits can be time stamped and the maximum flux the chip can deal with is $\sim 3.6\,\mathrm{MHz\,mm^{-2}\,s^{-1}}$. The chip can also operate in photon counting mode with a frame-based data readout. In this mode, the chip can deal with up to $\sim 5\,\mathrm{GHz\,mm^{-2}\,s^{-1}}$. The data readout is done via a programmable number of serializers (from 2 to 16) each running at a configurable frequency between 40 Mbps and 10 Gbps.

The analog front-end consists of a CSA in which the value of the feedback capacitance is programmable in order to optimize the dynamic range for a given application. The front-end can deal with both, positive and negative polarity signals [58]. A non-linear MOS gate capacitance can also be programmed [57], in parallel with the feedback capacitance, in order to extend the linear range of the energy measurement up to the MeV when the front-end is configured in the positive collection polarity.

Some measured parameters for the analog front-end in the Timepix4 chip are presented in Table 2. The parameters in the table, are evaluated on the amplitude of the pulse at the CSA output for the negative polarity configuration and with a bare chip. Electrical test pulses were injected at the CSA input node. The parameters presented in Table 2 are also valid for the operation in positive polarity. The linearity measurement is defined as the input signal for which the amplitude of the output pulse deviates 5 % from the linear fit at low energies. The conversion from voltage to charge was measured on a Timepix4 ASIC bump bonded to a silicon planar sensor using X-ray photons.

Fig. 14 shows the measured map of the ENC, expressed in e$^-$ $_{rms}$. The ENC was measured using the s-curve method [70]. The mean value is ~68 e$^-$ $_{rms}$ and the standard deviation ~5.9 e$^-$ $_{rms}$. The pixels for which their sensor connection is above the area where the *periphery electronics* is located have an increased noise of ~10 e$^-$ $_{rms}$ due to an increase in their input capacitance of ~30 fF. The increase of the input capacitance is due to an additional level of shielding for those lines connecting the pads to the readout electronics in order to prevent signal crosstalk. In the Timepix4 chip the *peripheral circuitry* is located in the top and bottom edges, and also in the center of the chip. These are the locations where Through Silicon Vias (TSV) landing pads are also located [4]. These regions can be identified in Fig. 14 by an increase in noise. Only 30 pixels in the full matrix have a noise above 90 e$^-$ $_{rms}$. No systematic effects are observed in the matrix. The value calculated for the noise in the same geometry with the routine matches the mean value with an error ~1.5%.

Fig. 15 shows the comparison of the jitter calculated by the routine as a function of the input charge when the input transistor is biased at 2.8 μA. The red dashed line corresponds to the transistor level simulation of the post-layout circuit. The calculation used in the routine described in this manuscript matches well, for small input charges, with the full post layout simulation of the front-end. There is an error below 15 % for large charges in which the routine underestimates the jitter. The discrepancy between the routine and the transistor level simulation lies in the fact that the routine uses a linearized model around the transistor quiescent point whereas the transistor level simulations account for effects related to the deviation from the linearity, second order transistor effects and also slew rate effects.

Fig. 16 shows the jitter as a function of the input charge for the routine modeling (blue solid line), and for the mean time resolution measured on the Timepix4. A full description of the measurement setup including further results is presented in [71]. The routine included a description of the behavior of the comparator that was briefly described (Section 3.4). The contributions to the time uncertainty from the front-end and from the comparator were added in quadrature. The measurements were done based on electrical test pulses on a bare chip and setting the threshold to 800 e$^-$. This value is above the intrinsic random electronics noise and allows operating the chip without noise induced hits. For each amount of injected charge, the jitter was determined by measuring the arrival-time distribution of analog test pulses. In order to isolate the analog front-end from the TDC, S-curves of the transitions between TDC time bins were measured by careful control of the test-pulse arrival time in steps of 20 ps with respect to the system clock. In the present configuration, it is not possible to inject charges larger than 20 ke$^-$ on the front-end due to the limited dynamic range of the electrical test pulse because a small (~ 3.2 fF) test capacitance was implemented. The measurement is shown for the signals on two polarities: e$^-$ (red curve) and h$^+$ (magenta dashed line). It is clearly shown that, the two measured curves match for low input charges. However in the positive polarity curve, the jitter enters a plateau region above ~ 10 ke$^-$. This is due to the fact that for positive polarity, C_O in Fig. 4 has to discharge through a fixed value current source (KI_{BIAS}) which sets a limitation on the slope of the pulse at the CSA voltage output (i.e. the front-end enters a slew rate limited regime above ~ 10 ke$^-$ for positive polarity sensors). The design choice was taken to avoid entering a slew rate limited regime for negative polarity sensors (see Section 3.2). The simulation and the measurements for negative polarity sensors match well over the whole range.

5. Simulations

The jitter and the noise are calculated in this section for different input parameters for the routine. In Section 3.2, the jitter (σ_t) was approximated to the noise (σ_n) divided by the slope (dv/dt) of the time waveform taken at time that the preamplifier output crosses the threshold. The *normalized overdrive* was introduced in order to account for the impact of the threshold value on the slope of the signal. If the normalized overdrive is considered equal to unity (this assumption is valid when the amplitude of the preamplifier output is much larger than the threshold voltage i.e. $Q_{in}/C_{FB} \gg V_{th}$) then the jitter can be expressed normalized by the input charge:

$$Jitter\ Q_{in} = \frac{qENC_{Total}C_O(C_{IN}+C_{FB})}{g_m C_{FB}} \tag{28}$$

For example, Fig. 17 shows the *normalized jitter* at the CSA output (expressed in ps_{rms} ke$^-$) as a function of the input capacitance for different values of the analog power density. The parallel noise due to sensor leakage current was not included in this particular calculation. The input capacitance in the x-axis includes the sensor capacitance and the internal metal-to-metal capacitance on the chip. The analog power density accounts for the power density allocated to the analog CSA, the comparator and the on-pixel threshold adjustment DAC (the power consumption of the comparator and of the threshold adjustment DAC is estimated as 50 % of the power budget).

The values for the power consumption density were chosen considering that, as a rule of thumb, and for design at room temperature operation without active cooling, the power consumption density of an ASIC (including analog and digital) should be kept below $1\,\mathrm{W\,cm^{-2}}$.

From Fig. 17, we can read that for a 50 fF input capacitance and an analog power density of $0.5\,\mathrm{W\,cm^{-2}}$, the normalized jitter is ~ $400\,\mathrm{ps}_{rms}$ ke$^-$ i.e. the jitter for a 10 ke$^-$ input charge would be ~ $40\,\mathrm{ps}_{rms}$. Increasing the power consumption improves the jitter through the increase of the transconductance. For example, for an analog power

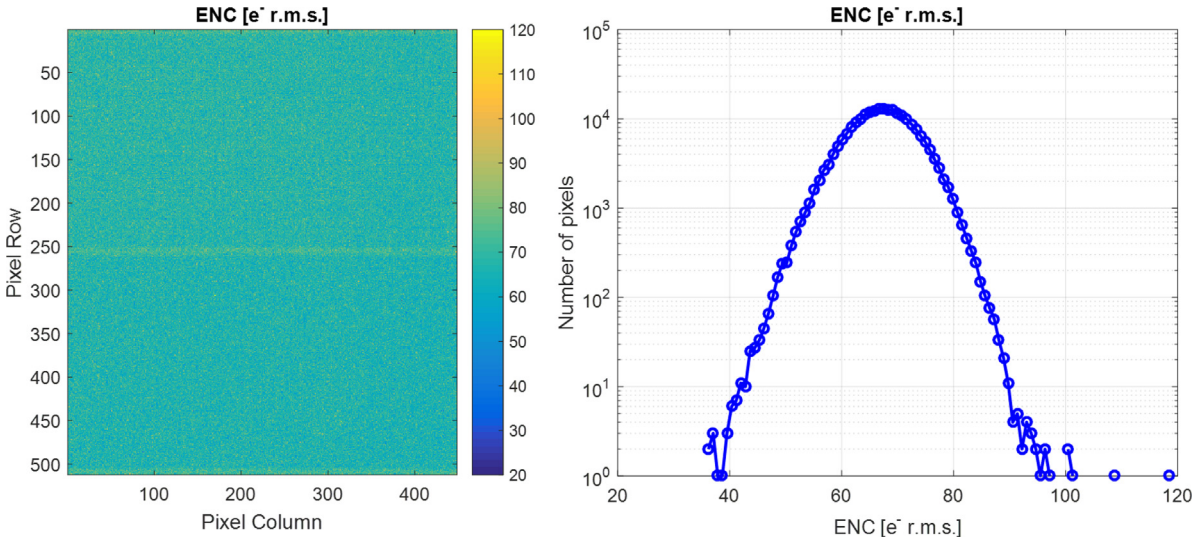

Fig. 14. Left: Map of the ENC measured in the Timepix4 chip, expressed in e^-_{rms}. The pixels for which their input pad is above the area where the periphery electronics is located have an increased noise of $\sim 10\,e^-_{rms}$. Right: Histogram of the pixel noise. The mean value is $\sim 68\,e^-_{rms}$ and the standard deviation $\sim 5.9\,e^-_{rms}$.

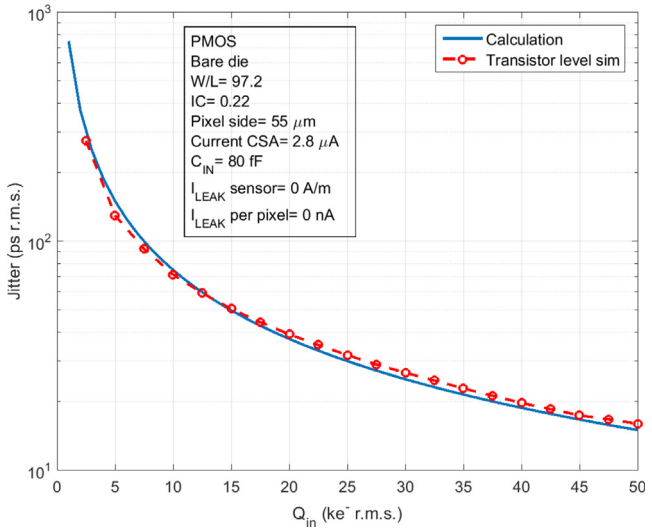

Fig. 15. Comparison of the routine jitter simulation at the preamplifier output, as a function of the input charge with a transistor level post-layout simulation of the circuit.

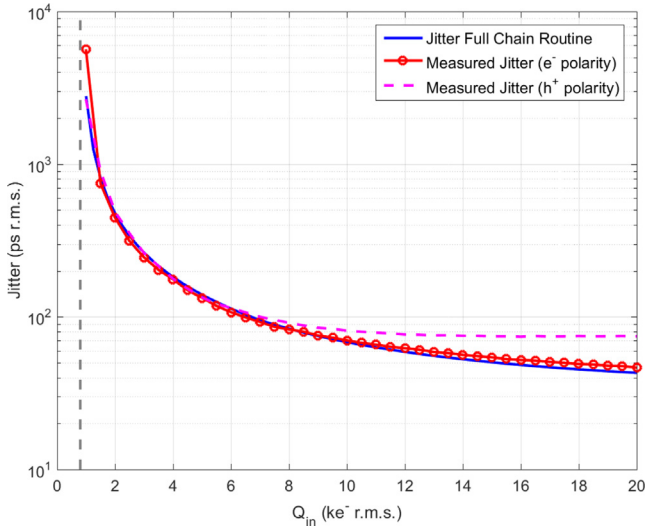

Fig. 16. Jitter simulation at the comparator output, as a function of the input charge for the operation point representative of the Timepix4 chip implementation when the front-end is biased at 4.7 µA and the threshold fixed at $800\,e^-$ (blue). The red line represents measured data on the Timepix4v1 chip using the same operating point in negative polarity. In magenta, the measurements are shown for the front-end configured in positive polarity. The slewing of the front-end is shown in this mode.

density of $1\,W\,cm^{-2}$, the jitter for a $10\,ke^-$ input charge would be $30\,ps_{rms}$. The figure also shows that the increase in capacitance leads to an increase in both, jitter and noise. Please also note that increasing the power consumption does not improve significantly the noise due to the fact that, as explained in 3, the decrease in the noise of the input transistor is counter balanced by the increase in the bandwidth over which the noise is integrated.

Fig. 18 shows the power consumption of the detector channel for published hybrid pixel detector readout chip designs [7] versus the channel density (in number of pixels per cm^2). Three lines are drawn, corresponding to the power consumption of the channel for constant values of the density of power consumption ($0.1\,W\,cm^{-2}$, $1\,W\,cm^{-2}$ and $10\,W\,cm^{-2}$). The lowest level, $0.1\,W\,cm^{-2}$, corresponds roughly to the limit of heat flux that can be removed by natural air convection with 10 C temperature rise [72]. As it can be seen from the plot, the density of power consumption for the densest designs available is below $1\,W\,cm^{-2}$. In the absence of active cooling, increasing the power consumption could lead to an increase in temperature in the detector system, leading to temperature induced leakage currents in the sensor that might lead to a degradation in both noise and time resolution. These are aspects that should be accounted for at system level design [73].

To account for the modulation of the threshold on the slope at the comparator crossing point the result should be corrected by the function $N_{OV}/(N_{OV}-1)$ where N_{OV} is the number of times that the amplitude at the output of the CSA is larger than the threshold voltage. This function is plotted in Fig. 19. For $N_{OV} = 1+\epsilon$ the slope of the signal is very small because the signal at the preamplifier output is just slightly above the threshold. As the signal increases with respect to the threshold, the correction function approaches the asymptote 1.

Fig. 17 also includes three reference points for illustrating the capacitance of detectors that have been used while read out by high granularity hybrid pixel detectors. MCPs operate in vacuum and do not introduce a significant capacitance to the electronics input (~ 25 fF was considered as metal-to-metal input capacitance). They provide a large

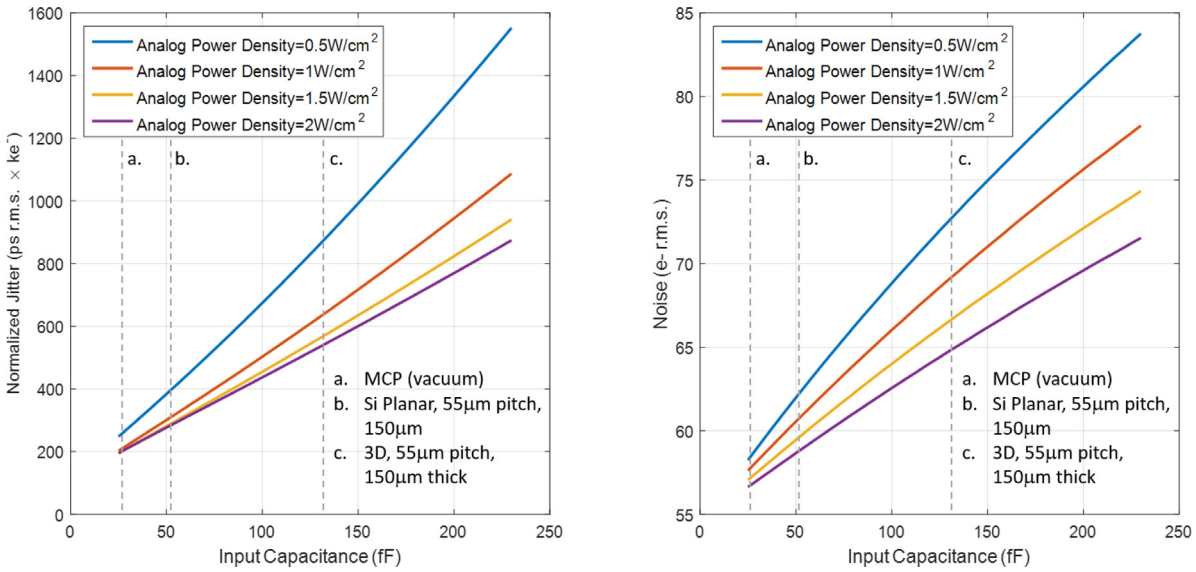

Fig. 17. Normalized jitter (left) and noise (right) as a function of the input capacitance for different values of the power density.

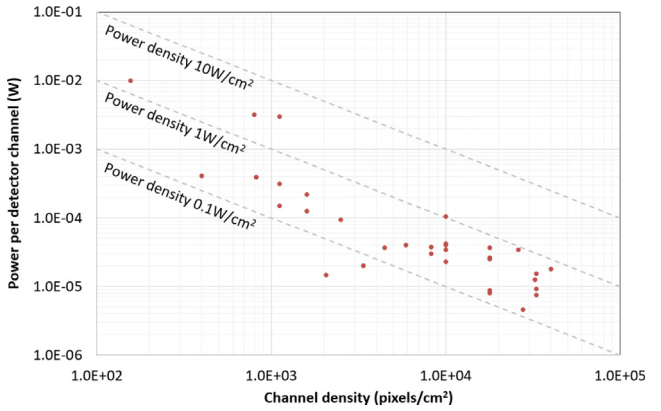

Fig. 18. Power consumption per detector channel as a function of the channel density for existing hybrid pixel detector readout ASICs. Data extracted from [7].

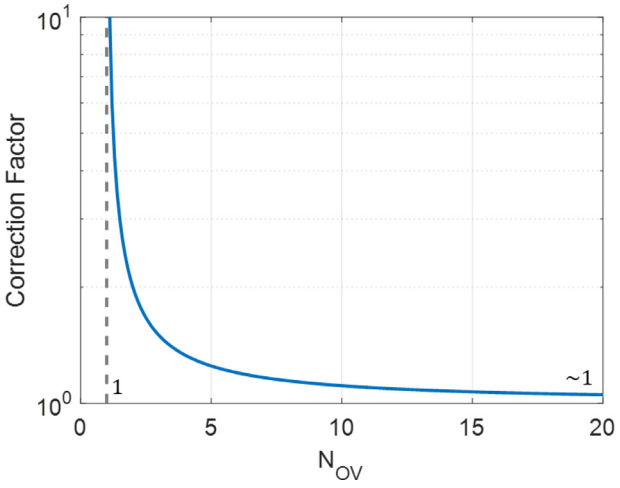

Fig. 19. Correction function as a function of the number of times the amplitude of the charge sensitive amplifier output pulse is larger than the threshold.

and prompt signal and their Transit Time spread can be very small (∼ 20 ps) [5]. The plot also shows, as reference, the capacitance for a silicon planar detector [37] and the capacitance for a 3D detector [43], which is a candidate detector for precise timing particle tracking in future High Energy Physics experiments due to its prompt signal induction. However its capacitance is intrinsically large (∼ 110 fF for a 55 µm pixel [43]).

Figs. 20 and 21 show the normalized jitter at the CSA output as a function of the pixel pitch for different values of the analog power density. The simulation includes a 100 µm thick planar silicon sensor which has a leakage current of 0.1 A m^{-2} (10 µA cm^{-2}). Fig. 20 takes into account the integration of a redistribution layer in the ASIC to bring the signals from the sensor pads to the pixel input transistor. The RDL adds parasitic capacitance at the input node. In Fig. 21, it is considered that the sensor pixel matches the readout electronics pixel and that the connection between the sensor and the readout electronics is optimized. This is the case in the traditionally designed three side buttable pixels. In both cases, an optimum is seen for the jitter as a function of the pixel pitch. When decreasing the pixel pitch, the current available for the input transistor decreases (for a constant power density, the power consumption per pixel decreases) and this leads to a decrease in the slope of the signal at the CSA output voltage and an increase in the jitter. When moving towards larger pixels, the current allocated to the input transistor increases. However the input capacitance increases as well due to the larger pixel geometry and as a consequence both noise and jitter degrade. For a system with no redistribution layer, 50 µm pixel pitch and 0.5 W cm^{-2}, the normalized jitter is ∼410 ps$_{rms}$ ke$^-$ i.e. the jitter for a 10 ke$^-$ input charge would be ∼41 ps$_{rms}$. For a pixel of 40 µm pitch, we would expect a jitter of 54 ps$_{rms}$ for a 10 ke$^-$ input charge (at 0.5 W cm^{-2}).

Increasing the power consumption to 1 W cm^{-2} on a 50 µm pixel pitch would lead to a jitter of 25 ps$_{rms}$ for a 10 ke$^-$ charge. In the case of a system with RDL and under the same conditions, the expected jitter would be ∼ 40 ps$_{rms}$. We can conclude that, in order to optimize the system for jitter, the input capacitance has to be minimized as much as possible. Furthermore, there is a penalty in jitter (or in power consumption) for designing a system with an architecture allowing it to be tiled seamlessly on four sides.

In Fig. 20 and 21 on the right, the CSA noise is plotted as a function of the pixel pitch. The noise was computed for the dimensions of the input transistor that minimize the jitter. The noise increases with the pixel pitch due to an increase in the input capacitance when designing larger pixels (see Eq. (18)). Also the series noise is independent of the transconductance of the input transistor (and as a consequence of the power consumption) and this can be also seen in the figure

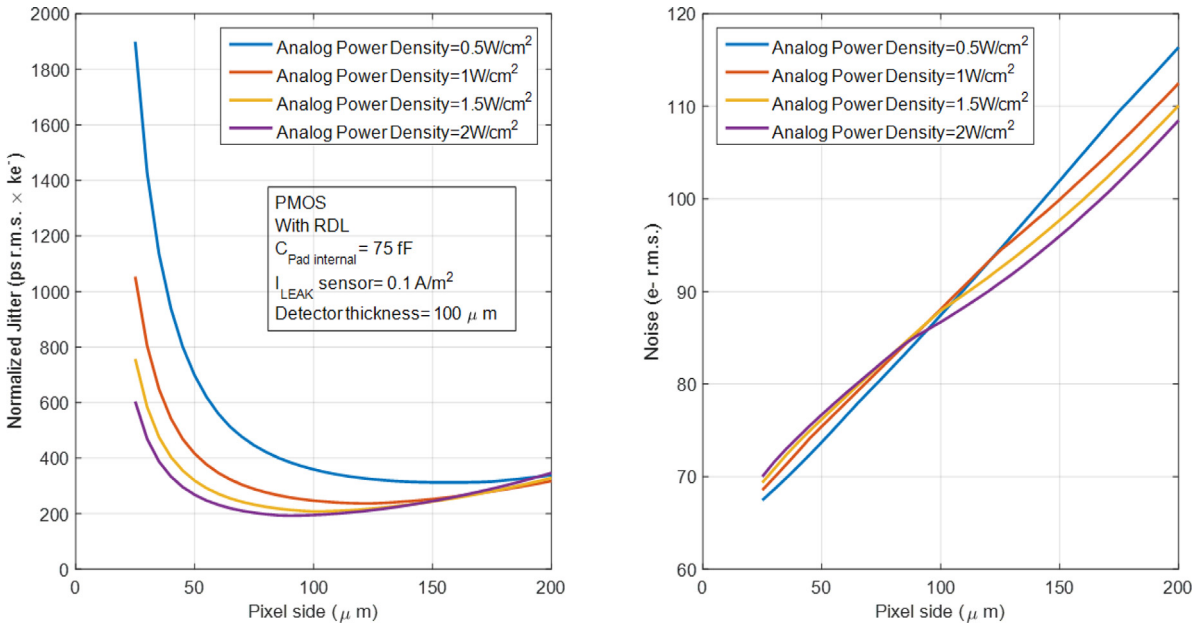

Fig. 20. Normalized jitter (left) and noise (right) as a function of the pixel pitch for different values of the power density. The input capacitance is taken considering an internal redistribution line from the sensor pads to the pixel electronics for a four-side buttable design.

(Section 3.2). A second order effect is seen in the plots that leads to a slightly higher noise for increased power consumption in the region of the plot corresponding to small pixels. This effect is related to the operating point for the input transistor which, for a given pixel pitch, varies with the power density. The optimal Inversion Coefficient for the input transistor that minimizes the jitter is calculated to be in the moderate inversion region but its value slightly increases with an increase in the drain to source current. This leads to larger transistor dimensions and to an increase in the input capacitance and in the noise. Increasing the Inversion Coefficient for the input transistor also leads to an increase of the γ factor in Eq. (12) which also contributes to the increase of noise with the IC but the impact of this parameter in the overall noise is negligible.

The normalized jitter at the CSA output and the noise are plotted in Fig. 22 as a function of the sensor leakage current on a 55 μm pixel pitch with redistribution line. Both the noise and the jitter increase with the sensor leakage current because the parallel noise increases. Increasing the power consumption reduces the jitter although it does not contribute to reduce the noise.

6. Summary and conclusions

This paper presents the analog front-end of the Timepix4 hybrid pixel detector readout chip and some electrical characterization results. The calculations that led to the optimization of the transistors in the analog circuits are shown as well. The same routines, which have been validated with post-layout simulations and measurements, are used to extract information on fundamental limits to noise and time resolution on highly segmented pixel detectors.

The novel aspects of this chip, manufactured in 65 nm CMOS process, are (1) the implementation of an architecture that allows the chip to be tiled seamlessly on four sides, (2) its reticle-sized dimensions (the chip measures 24.7×30 mm^2) and (3) the ~ 200 ps time bin which leads to a time resolution of ~ 60 ps$_{\text{rms}}$.

The analog front-end has a gain of ~ 36 mV/ke$^-$ when configured in *High Gain Mode*, and ~ 20 mV/ke$^-$ when configured in *Low Gain Mode*. The Equivalent Noise Charge (ENC) is $\sim$68 e$^-_{\text{rms}}$ and $\sim$80 e$^-_{\text{rms}}$ in *High Gain Mode* and in *Low Gain Mode* respectively. The residual offset and the noise do not present systematic variations across the matrix.

In the calculations presented in this manuscript, we aim at understanding the parameters leading to a minimization of both the ENC and the time jitter introduced by the CSA in the full detector chain. We present a simple detector model that, although it was designed for the geometry of planar sensors, it can be extended to other detector layouts. The transistors are modeled using the EKV model [3] and the CSA equations have been calculated from basic principles using a small signal analysis. The EKV model provides a continuous and accurate transistor parameter modeling from the weak to the strong inversion regions.

To minimize the time uncertainty in the measurement, the noise of the system has to be minimized. In addition, the slope of the voltage time waveform at the output of the CSA when a pulse develops has to be maximized.

With respect to the noise, we concluded that, in a system consisting of a CSA (without a shaping circuit), the series noise is independent of the transconductance (g_m). The reason is that increasing the transconductance the power spectral density of the noise decreases, but the bandwidth over which it is integrated increases by the same factor. The two effects cancel each other. As a consequence and in a first order calculation, the noise of the system does not depend on the power consumption of the CSA. The series noise can be minimized by (1) decreasing the value of the input capacitance, by (2) decreasing the value of the feedback capacitance (there are limitations to the lower limit in terms of stability of the front-end) and (3) by increasing the value of the output capacitance of the front-end (at the penalty of a decreased slope and increased jitter). A system designed to be tiled seamlessly on four sides requires a redistribution layer in order to bring the signals from the sensor pads to the readout electronics. That leads to an increase of the capacitance at the input node of the CSA leading to a penalty in the noise and jitter (an increase in jitter of $\sim 37.5\,\%$ was calculated for 50 μm pixels).

In order to maximize the slope, the designer can (1) maximize the input charge (for example using sensors with intrinsic gain), (2) maximize the transconductance (g_m) (that is related to (a) the drain current (and as a consequence to the power consumption) and (b) to the dimensions of the input transistor) or (3) minimize both the total input and output capacitances in the circuit.

Although not covered in detail in this work, we saw that the sensor contributions should be accounted for when aiming for time resolutions

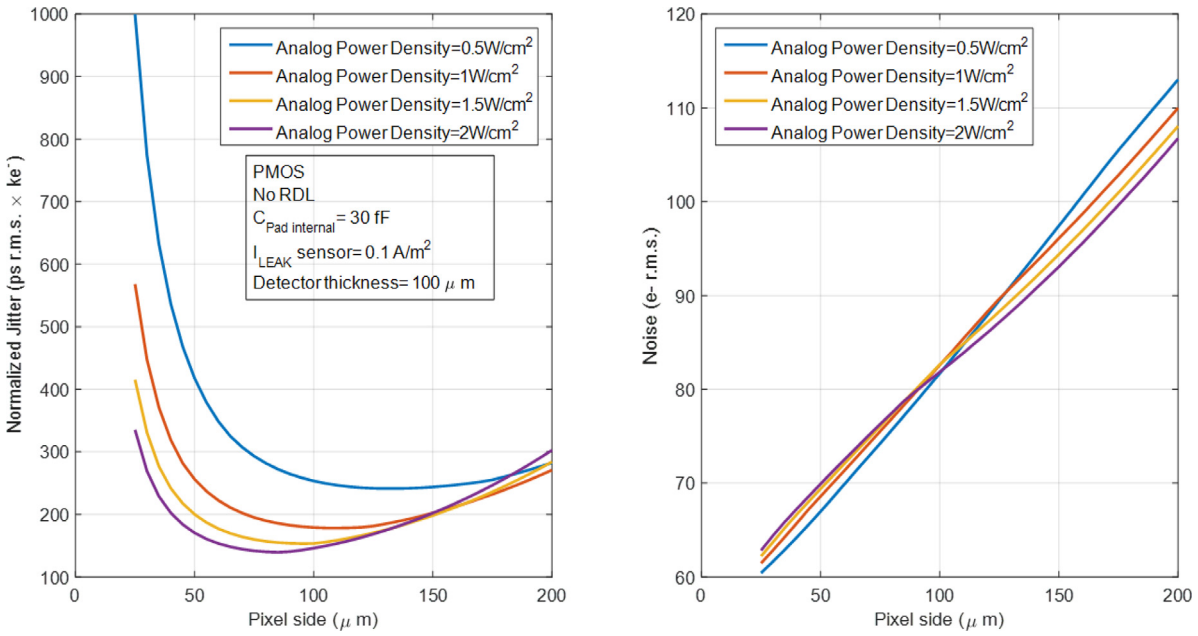

Fig. 21. Normalized jitter (left) and noise (right) as a function of the pixel pitch for different values of the power density. The input capacitance is taken considering an optimized connection from the sensor pad to the readout electronics. In this case the ASIC would be laid out as the traditional three sides buttable designs.

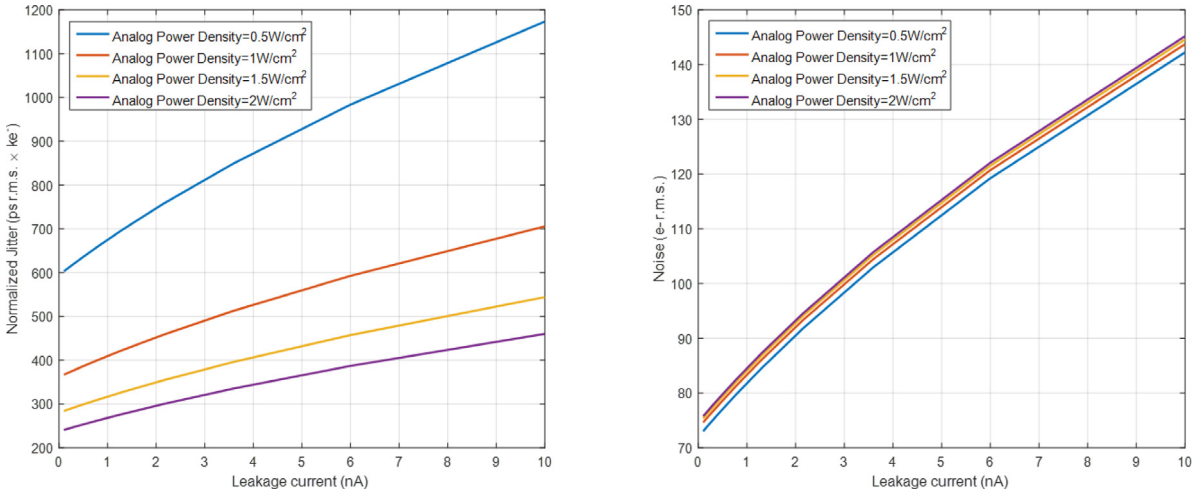

Fig. 22. Normalized jitter (left) and noise (right) as a function of the leakage current for different values of the power density for a 55 μm pixel pitch. The input capacitance is taken considering the presence of a redistribution layer for four side buttable system.

in the order of tens of ps. We saw in particular that the pulse shape from event to event might change depending on the physical location of the deposition leading to inaccuracies in the time walk correction. Charge straggling also introduces fluctuations on the shape of the induced signal. We can conclude that codesign of sensor and readout electronics is key in precise timing systems.

Finally, we concluded that for very highly segmented detectors, with 50 fF input capacitance and an analog power density of $0.5\,\mathrm{W\,cm^{-2}}$ (so that the ASIC can operate without active cooling) the limit for the jitter introduced by the front-end for a $10\,\mathrm{ke^-}$ input charge would be $\sim 40\,\mathrm{ps_{rms}}$.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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