Prepared for submission to JINST

TWEPP 2022
19/09/2022-23/09/2022
Bergen, Norway

# BETSEE: Testing for System-Wide Effects of Single Event Effects on ITk Strip Modules

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Abstract: The Inner Tracker silicon strip detector (ITk Strip) is a part of the ATLAS upgrade for the HL-LHC. The detector readout and control is accomplished by the interaction of three on-module custom ASICs (ABCStarv1, HCCStarv1 and AMACstar). All ASICs are designed with protections against Single Event Errors. Their resilience at the system-level can be tested using the Board for Evaluation of Triple-chip Single Event Effects (BETSEE). This special board places all three ASICs into the beam-spot concurrently and allows for module-like operation. The results from irradiating BETSEE with heavy ions and protons will be presented.

Keywords: Radiation-hard detectors, Front-end electronics for detector readout, Digital electronic circuits

ATL-ITK-PROC-2022-030
20 October 2022

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## Contents



## 1 HL-LHC and ATLAS ITk

The High Luminosity LHC (HL-LHC) is next phase of the LHC program. Expected to begin operation in 2029 and deliver 3 times the instantaneous luminosity of the LHC, the HL-LHC will deliver a total of 4000 $fb^{-1}$ over its lifetime. The maximum pileup at the HL-LHC is expected to surpass 200 and the radiation environment is harsher, including a lifetime dose of 50 MRad in the strip detector. To reach the desired physics performance in these conditions, the ATLAS experiment will replace the current Inner Detector with a new all silicon Inner Tracker (ITk) with improved granularity, data rate, and radiation hardness [1][2].

The outer section of ITk will consist of 4 (6) barrel (endcap) layers of silicon strip detectors consisting of 17,888 individual modules. The hybrid modules of the ITk strip detector consist of front-end electronics glued to silicon strip sensors with a 75.5 $\mu$m pitch. The front end electronics use a parallel powering scheme with on module DC-DC conversion and regulation. Most of the functionality of the module is implemented in three Application Specific Integrated Circuits (ASICs). The Autonomous Measurement and Control Chip (AMAC) handles power switching and analog monitoring for the module. The ATLAS Binary Chip (ABC) handles the analog front-end, digitization, and readout of 256 channels. The Hybrid Control Chip (HCC) controls up to 11 ABCs, providing the control information to and combining the data output from these chips. Each module carries 1 AMAC, 1 or 2 HCCs, and up to 20 ABCs.

## 2 SEE Mitigation in ITk Strip ASICs

The harsh radiation environment of the HL-LHC requires the ITk strip ASICs to be protected against Single Event Effects (SEEs) — prompt effects of radiation on the detector electronics. We mostly consider three flavors of SEEs: Single Event Upsets (SEUs) in which a bit flips in a chip's internal registers, Single Event Transients (SETs) in which a transient signal on the chip's logic

lines changes its state, and Single Event Latch-Ups (SELs) in which a transistor is forced open resulting in high operating current and potential permanent damage. The primary design methods used to prevent SEUs and SETs from affecting the operation of the chips are triplication of the logic and encoding of key command and data signals. The triplication uses a majority voter system with triplicated voters operating on three separate clock domains. All registers and control logic have been triplicated in the ITk Strip ASICs, but large buffers in the data paths have not been triplicated due to space and power constraints. Control lines to the HCC are 6b8b encoded and passed on to the ABC with the encoding. The data output from the HCC is 8b10b encoded. These encodings provide DC balance and allow the detection of SETs. Hamming codes are used to protect event metadata.

The SEE mitigation techniques have been tested with a rigorous simulation campaign detailed further in [3]. Additionally, each chip has undergone SEE test beam campaigns using specially designed single chip carrier cards [4]. These tests allow precise measurement of the expected rates of various SEEs in the ATLAS detector and allow observation of command and data lines which are usually internal to a module.

## 3 Testing for System Level Effects

In addition to the chip level SEE tests, we have performed a module level test for SEEs. The goal of this test is to operate all three ASICs in a module like configuration in a test beam environment. This allows sensitivity to SEEs arising from interactions between the chips, including SETs on the connections and accumulating SEEs across the whole module. Additionally, the hardware and software setups are independent of the single chip tests, granting additional coverage and verification with a focus on effects relevant for detector operations.

These tests are performed with a specially designed board — the Board for Evaluation of Triple chip Single Event Effects (BETSEE). The main design consideration for BETSEE is placement of all three ASICs within a 2.5 cm diameter to accommodate the beam spot size at test beam facilities. To achieve this, the AMAC is placed as usual on a separate PCB called the powerboard with the DCDC converters. The HCC and ABC are glued and wire bonded directly to the BETSEE PCB near AMAC as shown in Figure 1. The powering, control, and inter-chip connections are exactly as in a module — only the number of ABCs and the geometrical placement of ABC and HCC are changed.

BETSEE is interfaced to the DAQ PC through an FPGA and powered at 12V using a USB controlled power supply. HCC and AMAC are connected separately to the FPGA, which is capable of handling up to 8 BETSEE cards simultaneously. The DAQ PC runs three separate processes to control and monitor the power supply, AMAC, and HCC. The power supply loop monitors the module's current consumption. The AMAC process continuously reads out AMACs internal configuration and uses AMACs monitoring capabilities to track board temperatures and current consumption. The HCC data loop continuously reads all HCC and ABC registers and sends a trigger which reads out a predetermined pattern of hits to test for SEEs in the data path. The inner loop runs more than twice a second with a full reset of chip registers occurring every minute. We use the MonEater Python module to perform online data analysis and save processed data points to an InfluxDB database. The database is connected to a GrafAna instance running on the DAQ PC

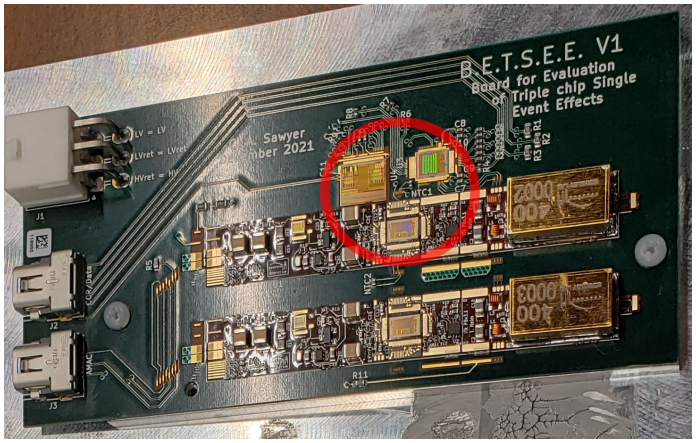


**Figure 1**. Photograph of BETSEE board mounted to cooling plate used during heavy ion running. The red circle shows the rough location of the beam spot with the AMAC, ABC, and HCC inside.

| Ion | Energy [MeV] | LET [MeV/(mg/cm$^2$)] | Fluence [particles/cm$^2$] |
|---|---|---|---|
| $^{27}Al^{8+}$ | 250 | 5.7 | $3.00 \times 10^7$ |
| $^{53}Cr^{16+}$ | 505 | 16.1 | $1.25 \times 10^8$ |
| $^{84}Kr^{25+}$ | 769 | 32.4 | $1.50 \times 10^8$ |
| $p^+$ | 480 | N/A | $6.35 \times 10^{13}$ |

**Table 1**. Fluences, energies, and LET of different species used in test beam SEE runs with BETSEE. Proton collisions have a broad spectrum of LET rather than a narrow peak.

which allows real time remote monitoring of SEEs and the board's operational status during testing. The live monitoring setup is crucial to be able to react to unforeseen issues either with the setup or from SEEs, and to ease changes to the tests when we find a gap in our SEE coverage.

## 4 SEE Testing with BETSEE at Test Beams

We have operated BETSEE during two test beam campaigns alongside the single chip tests. We ran a single BETSEE module in a heavy ion beam at UCLouvain's Heavy Ion Facility and two BETSEE modules in a proton beam at TRIUMF's Proton Irradiation Facility. The energies and collected fluences of each species are detailed in Table 1. The heavy ion running allowed us to search for effects that will only happen with rare, high LET events, as heavy ions deposit more energy in the chips. The proton running allowed us to better extrapolate event rates to the HL-LHC, as proton collisions produce events with a spectrum of LET via the same mechanism as the HL-LHC environment.

The boards ran successfully at both tests without requiring external resets or power cycling due to SEEs. At TRIUMF we encountered some setup issues not attributable to the chips or to SEEs, including some resets of the FPGA and the failure of the DAQ PC's power supply. The latter issue resulted in a reduced data set from running with protons.

| Chip | Observed Corrected SEUs (Kr) | $\sigma_{\mathrm{SEU}}$(Kr) [cm$^2$/ion/bit] | Observed Corrected SEUs ($p^+$) | $\sigma_{\mathrm{SEU}}(p^+)$ [cm$^2$/ion/bit] |
|---|---|---|---|---|
| ABC | 31225 | $2.5 \times 10^{-7}$ | 19642 | $2.2 \times 10^{-13}$ |
| HCC | 5749 | $3.4 \times 10^{-7}$ | 4324 | $7.5 \times 10^{-13}$ |

**Table 2**. Counts and cross sections for corrected SEUs with protons and Krypton for ABC and HCC.

## 5 Observed SEEs

SEUs corrected by the triplicated voter system raise a flag, allowing us to count these corrected bit flips and use them to verify that the chip is receiving radiation. The measured cross section of corrected SEUs in the three chips is shown in Table 2. SEUs which are not corrected by the triplication can be observed comparing the read values of the configuration registers to the expected values; no uncorrected SEUs are observed over all three chips and both test beam campaigns. Additionally, we look at the monitored temperatures and current usage and note that there are no sudden changes in temperature or current which could indicate an SEL or power cycling of the chips. The temperature stability as measured by AMAC's monitoring capabilities is shown in Figure 2. The final data analysis consists of scanning all monitored values for anomalies and scrutinizing the full raw data stream from the module for unexpected behavior using a manual parsing code that flags and categorizes unparsable data.

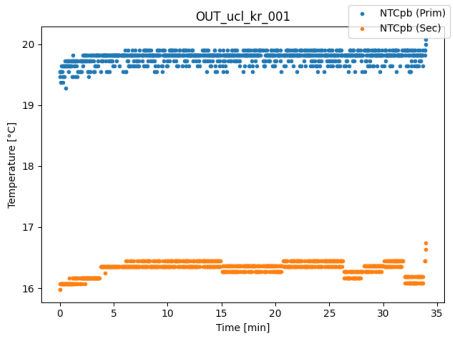


**Figure 2**. Temperatures measured on two powerboards showing warm-up on start and stability during running.

The most common observed SEEs, aside from corrected SEUs, are errors on the command input and output lines to HCC and ABC. These data paths are 6b8b encoded, and bit flips in the data are caught by the decoding mechanism, which can become unlocked from the signal if too many consecutive packets are affected. These bit flips can arise from SETs on the transmission lines, or for the ABC inputs, from SEEs in the transmission circuit of the HCC. Additionally, the HCC command input is passed on to the ABC even when there is an error. As a result, the ABC error counter increments whenever the HCC counter does and often on its own; this behavior can be seen in Figure 3. The rate of these communication errors at HL-LHC dose rates is expected to be negligible and the errors produced no observable impact on module functionality.

The most intrusive error observed was an interruption in communication on the R3L1 input to the HCC, which is used to send trigger info. The associated error counter immediately filled as

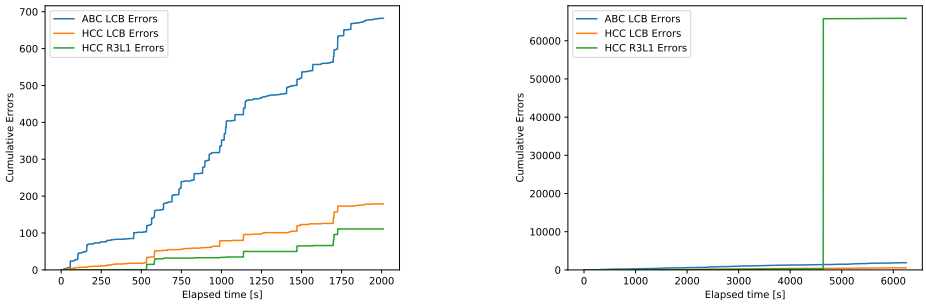


**Figure 3**. Cumulative communications errors on ABC (blue) and HCC (orange and green) inputs during two runs with Kr. The run shown on the left shows normal behavior of the error counters. The run pictured on the right shows the sudden spike of errors associated with the R3L1 interruption.

shown on the right side of Figure 3. A 3 bit shift of the internally stored frame of the R3L1 input signal occurs simultaneously with these errors. The final symptom is a loss of physics data. All symptoms cleared after approximately 5 minutes asynchronously from any regularly issued reset. The error occurred only once when running with Krypton, the highest LET ion used. This effect has thus far not been replicated in simulation or on the lab bench. If it is a radiation effect, we expect minimal detector impact based on the rarity. We also expect, based on the symptoms shown, that the error could be resolved by simply sending reset or power cycle to the module in order to reduce down time.

## 6 Conclusions

We have devised a system level SEE test of the three ASICs developed for use in the ATLAS ITk Strip detector planned for the Phase 2 upgrade in preparation for the HL-LHC. The BETSEE test placed all three chips into beams of protons and heavy ions and operated them in a detector-like configuration to improve coverage of potential SEEs that may impact detector operations. BETSEE is particularly sensitive to any effects which arise from the interactions of the chips, whereas the single chip tests are not sensitive to these. A combination of live monitoring and offline data analysis allowed swift reaction times and thorough study and allowed us to identify a small number of SEEs. With the exception of corrected SEUs, these SEEs are all expected to be rare in detector operations, and the most intrusive effect is expected to be correctable with a fast reset. The successful completion of these tests has indicated minimal impact on detector operations from SEEs and allowed the production of these chips to proceed.

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