PS/BR/OP 76-22
18 January 1977

THE CONTROLS OF THE NEW PSB MULTIPOLES

G. Baribaud, G.P. Benincasa, J. Donnat, B. Frammery, F. Giudici and P. Horne

ABSTRACT

The controls of the new multipoles of the PSB are implemented from the existing IBM 1800 control computer using STAR as the data transmission system. The implementation of hardware and software is the result of a close collaboration between all people involved in the project, in the operation, and in the maintenance, of the new multipoles. Some new features have been incorporated in the design: a flexible power supply-magnet connection with identification, some equipment monitoring facilities, and a built-in analogue observation system automatically controlled from the KNOBS system.

Provisions have been made for future extension, and easy and inexpensive transition ot the forthcoming new computer system if serial CAMAC is used.

The report deals with both hardware and software implementations.

Geneva
1977

CONTENTS

1. INTRODUCTION

Ninety-six new multipoles have been added to the PS Booster to compensate the stopbands in order to improve high-intensity beam qualities[1].

As the 96 new magnets will not be used simultaneously, at least for the time being, the number of power supplies was limited to 56 units. A manually operated switching system is provided so that any multipole can be connected to any unused power supply at will. This new feature implies the implementation of some identification process to update the computer data bank automatically whenever the connection pattern is modified by the operator.

The control software must be such that no difference can be noticed between the operation of the conventional old multipoles and the new ones (see Section 3.1). Owing to some delay in the implementation of the new PS computer system, it was decided to control the new multipoles from the existing IBM 1800.

The control hardware is built in CAMAC technology. CAMAC will probably be used for the new PS computer system[2] and many CAMAC modules are now available either from commercial firms or from other groups within CERN. The CAMAC Analogue Acquisition System (CAAS), developed in the PS Division (CCI group) in collaboration with SPS for the memory part, is used in this project (see Section 2.4 for more detailed descriptions).

A close collaboration between all people involved in the project and in the future operation of the multipoles led to the elaboration of some equipment monitoring facilities and an automatic analogue observation system.

A new VARILOG facility using microprocessor in a CAMAC crate is also provided.

The implementation of the new multipoles is based on the use of new technologies to improve operation, reliability, and maintenance. The transition from the present control computer to the new one is also taken into account throughout the design. Only two serial CAMAC crate controllers will be required to interface these 96 new elements to a CAMAC serial loop system (provided serial CAMAC is selected). The present software is implemented to cope with up to 104 new multipoles and up to 96 power supplies; the number of new multipoles can be expanded if enough room can be found in the PSB data bank. The present control hardware is designed to provide complete acquisition and control facilities for up to 72 power supplies; at the moment 60 power supplies are actually installed. Ninety-six new multipoles and 56 power supplies were requested in the project.

2. DESCRIPTION OF THE CONTROL HARDWARE

2.1 General layout

2.1.1 Control hardware schema

The control hardware schema of the new multipoles is shown in Fig. 1. Apart from some new features to improve the operation, the control hardware of a power supply is rather well known and it is extensively used at the PS Booster.

The analogue reference voltage at the input of the power supply amplifier is the product of an analogue function and a 10-bit digital word stored in a local memory. The analogue function is supplied by the Varian-620i-driven Function Generator for the time being. It will be replaced by some GFAs (Générateurs de Fonction Autonomes) in the new computer system; provision is made to cope with the difference in analogue output voltages of the various types of analogue function generators.

The contents of the local memory is controlled by the IBM 1800 via STAR C and CAMAC (see below); the specifications of the control word are given in Section 2.2.1. The shunt current of each power supply is processed to be interfaced to CAAS for acquisition, on the one hand, and is fed to an analogue observation multiplexer system, on the other hand.

Status bits can be directly acquired by the computer (STATUS ACQUISITION); they can also be surveyed locally by an equipment surveyor which detects any variation in the status bit pattern (see Section 2.7: Equipment surveyor). A part of the status words is formed by the identification word.

2.1.2 Hardware layout

The 60 power supplies to be controlled are in fact divided into two identical groups; the two control equipments are installed in the racks BAT 17 and BAT 60. As the two groups are identical, we shall describe only one.

Though the electronics of the regulator of the power supplies are built in a modular form, they cannot be put into CAMAC modules for the following reasons:

i) CAMAC power would not be used efficiently.

ii) Too many STAR adddresses would be required (see STAR-CAMAC crate controller in Section 2.1.3).

iii) The electronics of the power supply regulators must be isolated, while the common point of CAMAC power supplies is connected to ground.

It was then decided to house the electronics of the regulators of the power supply in isolated CIM crates equipped with adequate auxiliary power supplies. The electronics for six regulators can be plugged into one CIM crate; they occupy 24 CAMAC units in space, leaving one unit to interface the CIM crate to the CAMAC

dataway. In such a way five CIM crates are required per group to control 30 power supplies. The hardware layout is shown in Fig. 2. The analogue processing of the shunt currents is also performed in a separate CIM crate.

Analogue signals are treated in this CIM crate to be interfaced to the CAAS system (in CAMAC) for acquisition by the computer (see Section 2.4) and to the analogue observation system (see Section 2.5).

The status surveyor and the microprocessor are both installed in the CAMAC crates. The microprocessor is an auxiliary controller having access to the CAAS through the CAMAC dataway.

The power supply hardware is dealt with in a separate report[3].

The layout of the hardware in the CAMAC crate is shown in Fig. 3, together with the main interconnections between CAMAC and CIM crates (for rack BAT 17).

2.1.3 STAR-CAMAC crate controller

As the control hardware is built in CAMAC technology (see Fig. 2) it was necessary to interface the CAMAC crates to the IBM 1800 control computer, since we could not wait until the new computer is operational. The simplest way was to interface CAMAC and STAR by means of a specially designed CAMAC crate controller proposed and built by the CCI group[4]. We use two such crate controllers.

This crate controller performs all CAMAC functions on the 16 leftmost positions in the crate[5]. Blocks of 128 STAR A addresses and blocks of 128 STAR C addresses can be provided independently to equip eight successive CAMAC positions. A STAR-CAMAC crate controller can utilize up to 256 STAR A addresses and 256 STAR C addresses for a fully equipped crate (16 stations).

It should also be noticed that there is no LAM handling facility with the STAR-CAMAC crate controller, but there is no need for it in our application. The STAR-CAMAC crate controller gives access to the "N" lines via a rear-panel connector; this allows the implementation of auxiliary controllers in the CAMAC crate. This feature is used by the microprocessor which can access the Analogue-to-Digital Converter (ADC) and the analogue multiplexers (MPX) of the CAAS through the CAMAC dataway[6].

The HOLD[7] function is also implemented in the STAR-CAMAC crate controller; it is used for the acquisition of the status words, identification words, and test words.

The lists of the STAR A and STAR C addresses are given in Tables A1 to A4 of Appendix 1 for racks BAT 17 and BAT 60, respectively. These lists are edited by G. Surback. Each CAMAC crate is equipped with 256 STAR C addresses and with 128 STAR A addresses.

A special CAMAC hardware test[8] is provided to facilitate interaction with modules installed in those two CAMAC crates; a third crate used for Q calculation is also concerned. Up to 12 CAMAC dataway operations can be performed sequentially from a list of parameters (C, N, A, and F, and data for $F \geq 16$) specified by the user through the console, either in the Main Control Room (MCR) or from the mobile in the Booster building.

2.2 Control word, identification word, and status word specifications

In this section we define clearly all transfer words implemented in the design. The exact definition of these terms is indispensable for the coordination of the work of various teams (power hardware, control hardware and software).

2.2.1 Control word

The control word is stored in a local memory which drives a digital-to-analogue converter (DAC) whose reference voltage is connected to the output of an analogue function generator. Only one local memory is provided; anyhow, pulse-to-pulse intensity modulation (PPM) can be achieved directly from the IBM 1800 for the time being. In the future two more possibilities can be envisaged with the new computer system:

i) a local digital modulator can be incorporated in the CAMAC crate[9];
ii) GFAs can be installed in large quantities to replace the Varian computer.

The format of the control word is given in Fig. A1 of Appendix 2 (MEMORY CONTROL WORD): it can be read by the computer for data transfer analysis (see Section 2.2.5). The local memory is physically located in the power supply electronics[3] as well as the DAC; they will not be described in this report.

2.2.2 Identification word

Each new multipole has its own hardwired identification number as shown on Fig. A2 in Appendix 2, Bit 1 (LSB) is used as a continuity test to detect whether a power supply multipole connection is actually done; the next eight bits (2 to 9) are used to code up to 256 multipoles per group.

Bit 11 to bit 16 are used to code the identification number of the analogue function, which is connected to the power supply and hence to the multipole. The coding of these two identification numbers is implemented in the hardware of the power supply, so it is described in a separate note[3].

The acquisition of these identification words by the computer is done via the hardware address of the power supply. They are used to modify the data-bank configuration and are displayed on the screen of the PDS 1 as connection tables (see Section 3.3).

Though the philosophy of the manual connection system was to reduce the number of useful power supplies, it can also be used for quick repair in case of failure of one power supply; we have to keep in mind that the time devoted to machine experiment is rather limited. With the help of the equipment monitoring facility, it is easy to localize a fault, so a suspected power supply can be replaced by an unused one and the data bank rebuilt.

2.2.3 Power supply status word

A 10-bit status word is provided per power supply. The format of the status word is the same for all power supplies, as is shown in Fig. A3 of Appendix 2. A close collaboration between all people involved in the design (power hardware, control hardware, software, and operation) was necessary to define the meaning of every bit of that status word. This does not mean at all an attempt to standardize status words; they depend on the application we deal with, up to 15 independent status bits can be incorporated in a single status word.

This status word is used as input for an equipment monitoring program (see Section 3 for Software and display of results).

2.2.4 Test word

In order to increase the efficiency of fault diagnostic, a manually programmable 16-bit test word is hardwired in each power supply. This test word can be acquired by the control computer and compared to a reference test word; this allows a fast test of the digital acquisition system. The use of local digital displays (on CAMAC dataway as an example), in conjunction with a local mobile console, helps to localize faults. The acquisition of the test word is carried out by the following CAMAC commands:

a) HOLD MODE A(0,5)·F(14) for first CIM crate
A(8,13)·F(14) for second CIM crate

b) NORMAL MODE A(0,5)·F(14) + A(0,5)·F(1) for first CIM crate
A(8,13)·F(14) + A(8,13)·F(1) for second CIM crate

2.2.5 Reading of the control word (local control memory)

The contents of the control word stored in the local memory can be read by the computer. This facility combined with the test word (Section 2.2.4) can be used to test fully the digital data transmission system.

The acquisition of the contents of the local control memory is carried out by the following CAMAC commands:

a) HOLD MODE A(0,5)·F(6) for first CIM crate
A(8,13)·F(6) for second CIM crate

b) NORMAL MODE A(0,5)·F(30) + A(0,5)·F(6) for first CIM crate
A(8,13)·F(30) + A(8,13)·F(6) for second CIM crate

2.2.6 READY/ON/OFF status word

To facilitate the use of the knobs (see Section 3.2.2) the READY and ON/OFF status bits are grouped in a single word. As only six power supplies are found in a CIM crate the READY/ON/OFF status word contains only six bits of each. The MSB (bit 16) is a status bit generated by the common power rectifier when current overload is reached. The bit pattern is shown in Fig. A4 of Appendix 2.

2.2.7 Crate equipment monitoring configuration

A complementary 8-bit status word is defined in each crate for equipment monitoring purposes. The format of the word is shown in Fig. A5 of Appendix 2. Not all those equipment monitoring facilities are fully used with the present computer system; they are ready for the implementation of a more elaborate equipment monitoring program to be developed within the forthcoming computer system.

2.3 Equipment interface for control

2.3.1 Transceiver and Control Unit modules

As mentioned earlier, the electronics of the power supplies could not economically be housed in CAMAC crates (see Section 2.1.2). Figure 4 shows the block diagram of the hardware required to interface CAMAC dataway to the interconnection bus in the CIM crate (for six power supplies). Two complementary modules were designed to perform this interface.

The first module, called Transceiver, is a one-unit-wide CAMAC module which can interface two different CIM crates referred to as crate 1 and crate 2. This feature allows a rather good utilization of CAMAC power, since up to 12 power supplies can be controlled from a single CAMAC slot.

The second module, called Control Unit (CU), was designed as a complement to the Transceiver; it is a one-unit-wide module installed in the 25th position of a CIM crate (see Fig. 3). Both modules are described in detail in a separate note by Hallgren[10]; we only list the CAMAC functions performed by the Transceiver in Appendix 3. The galvanic isolation between the CAMAC and the CIM crates is achieved through the use of fast optocouplers in the Transceiver and in the CU. An ESAU program was written to perform a computer-driven test of the Transceiver and CU connected together.

2.3.2 Description of the interconnection bus

The interconnection bus in each CIM crate is worth describing, since it was used as a "team interface" between control hardware designers and power hardware designers during the project. The technology used is low-power Schoottky TTL; the layout of the bus is shown in Fig. 5, with timing references and logical levels in Fig. 6. We will describe all parts of this interconnection bus.

2.3.2.1 Data bus (1)

Referred to as (1) in Fig. 5, it is a bidirectional bus using a tri-state circuit to transfer 16-bit data words from CU to a selected power supply or vice versa.

2.3.2.2 Function bus (2)

This 3-parallel-line bus is controlled by CU and specifies which function will be performed in the selected power supply. These functions are derived from CAMAC functions; they are listed in Appendix 3 [reprinted from Hallgren's note][10].

2.3.2.3 Strobe line (3)

This single line is used to synchronize the operations on the interconnection bus as shown in Fig. 6.

2.3.2.4 Address lines (4)

These six individual lines are controlled by CU; they are used to address directly the power supplies; they correspond to the "N" lines of CAMAC.

2.3.2.5 READY lines (5)

The six READY lines are generated by the six power supplies; they represent the sum of all status bits of the concerned power supplies (see Fig. 6). Each READY line is routed towards two different paths:

i) to CU to be grouped in a single word for computer acquisition (see Section 2.2.6), to be compatible with the present KNOBS system.
ii) to a rear-panel connector for equipment monitoring purposes (see Section 2.7).

The logical levels are as follows:

READY = 0 V (TTL logical-zero level)
NOT READY = 5 V (TTL logical-one level)

2.3.2.6 ON/OFF lines (6)

The six ON/OFF lines are generated by the six power supplies; they are grouped in CU in a single word for computer acquisition (see Section 2.2.6) to be compatible with the present KNOBS system.

The logical levels are as follows:

ON = 5 V (TTL logical-one level)
OFF = 0 V (TTL logical-zero level)

2.3.2.7 Sign lines (7)

The six sign lines are generated by the six power supplies; they represent the state of the current inverter; they are patched to a rear-panel connector C1 for digital computer acquisition and analogue observation of shunt currents. C1 is connected to the CIM crate for analogue processing (see Fig. 2 and Sections 2.4 and 2.5).

2.3.2.8 Analogue lines (8)

The six analogue lines are in fact twisted pairs patched to the rear-panel connector C2 for connection to the analogue processing CIM crate (Fig. 5). The analogue voltage on each twisted pair is proportional to the shunt current of the corresponding power supply. These voltages are used for digital computer acquisition and for analogue observation in the MCR (see Sections 2.4 and 2.5).

2.3.2.9 Analogue input test line

An analogue signal (0 to +10 V) can be applied on an isolated LEMO connector placed on the front panel of CU. This signal is also patched to connector C2 and will be processed as a shunt current; this feature can be used to calibrate or to check the digital computer acquisition system.

2.3.2.10 CIM crate power supply surveyor

The auxiliary power supplies to power electronics in the CIM crates are continuously monitored by a special circuit. Whenever the +5 V power supply is distributed, the volatile memories can be modified accidentally. The power supply monitor circuit indicates all possible disturbances to the control computer which can then refresh the contents of the local memories. The output of the power supply monitor circuit is patched in the crate status word (see Fig. A5 in Appendix 2). Another bit is set when all auxiliary power supplies are on. The power supply monitor circuit is described in detail in Section 2.7.2.

2.3.2.11 Initial reset line (11)

Whenever the auxiliary CIM power supplies are turned on, the power supply monitor generates a pulse which resets all local memories in the CIM crate. This precaution prevents an accidental overload of the main rectifier as well as a perturbation of the circulating beams.

2.3.2.12 Monitor reset line (12)

This line is used to reset the power supply monitor; it is under computer control.

2.4 Analogue-to-digital conversion and computer data acquisition hardware

2.4.1 Generalities

Two identical computer data acquisition systems are provided in racks BAT 17 and BAT 60, to acquire the 30 analogue shunt signals from the 30 power supplies of each group (see Section 2.1). The unipolar analogue shunt signals with their corresponding sign bit (state of the polarity inverter) are provided to the acquisition hardware on separate cables; up to 36 analogue shunt signals can be processed per system. The analogue shunt signals are multiplexed for analogue-to-digital conversion and mixed for storage.

The system operates either in sequential mode or in random mode, depending on the occurrence of an external START pulse (standard Booster pulse or preset counter output). Some extra test signals are provided to check the quality of the analogue-to-digital conversion and the digital data transmission system (see Section 2.3.2.9).

2.4.2 General layout of the computer acquisition system

Twisted pairs are used to transmit the analogue shunt signals. Twelve shunt signals, one test signal and a ground level signal are patched to the same connector to be multiplexed by 3 AMX 16/1 CAMAC analogue multiplexers developed for CAAS (CAMAC Analog Acquisition System) by the CCI group[11] for the new computer system. The outputs of the analogue MPXs are linked to a common analogue bus connected to the input of a 12-binary-bit ADC whose conversion time is 7 μsec.

A specially designed CIM module, called Sign Multiplexer, used both for computer acquisition and analogue observation systems, collects sign bits through a 14-pin Hughes connector. The Sign Multiplexer unit receives INIT. and INCREMENT pulses from CAAS through the mixer unit.

Sign bits are sent to the CAMAC memory interface unit through the mixer unit so that both the sign and corresponding 12-binary-bit digital value are stored in the corresponding address of the 256-word buffer memory.

The contents of the buffer memory can be read in a random addressing mode by the computer through the memory interface unit and the STAR-CAMAC crate controller (see Sections 2.1.3 and 2.4.3.5).

Timing pulses (standard Booster pulses or pulse trains) are level-translated within the mixer unit, which also generates a fixed-duration BUSY signal to warn other CAMAC equipment users (see Section 2.6). The sequential analogue-to-digital conversion process is the highest-priority task, though it does not use the CAMAC dataway except for computer acquisition.

Two dual preset counters and one 256-word buffer memory (48 words are required at the moment) have been provided for future improvements such as sampling. At the moment, the analogue-to-digital conversion is triggered by standard Booster pulse RTPS04, which is also used for the old multipoles.

Remark: Some units are involved both in the computer data acquisition system and in the analogue observation system; they will be described partly in this section and partly in the next.

2.4.3 Technical characteristics

In this section it is not intended to give a complete detailed description, but every unit will be described as a block diagram with relevant technical information on inputs and outputs (see Fig. 7).

TTL and MOS-TTL compatible technologies are used to implement the hardware, and most of the CIM units contain on-card power regulators to fit with NIM standard power supplies.

2.4.3.1 The Sign Multiplexer

This four-unit NIM plug-in contains a mother board to which up to four 16-signal input boards can be connected.

RANDOM ACCESS bit and BUSY bit are sent by the mixer unit to enable the ADC to control the Sign Multiplexer (see Fig. 7). The INIT. pulse will reset the address counter; INCREMENT pulses will increment the 8-binary-bit synchronous counter. Each input card is equipped with a 4-bit address and one strobe signal. Input signals are galvanically isolated by optocouplers and selected through a 16 to 1 data selector MPX.

Buffer memory and 13 front-panel LEDs, mainly used in conjunction with the analogue observation system, are provided in this unit.

Eight 14-pin Hughes connectors located on the rear panel of the CIM crates are used to input the sign bits from the power supplies.

2.4.3.2 The mixer

The mixer is a CIM unit performing the following functions:

i) it delays and shapes the START pulse (from a CAMAC preset counter or a standard Booster pulse) to initialize the ADC and the Sign Multiplexer;

ii) it generates the 400 μsec BUSY signal to warn the microprocessor (see Section 2.6.2);

iii) it gates and shapes the INCREMENT pulse from the ADC for the Sign Multiplexer;

iv) it translates the standard 30 V/1 μsec pulse into TTL levels;

v) it supplies a fixed-duration MARK pulse to be mixed with the analogue signal to ease analogue observation in the MCR;

vi) it temporarily buffers SIGN bits for the memory interface.

This unit can easily be modified to cope with some new requirements.

2.4.3.3 The AMX 16/1 analogue multiplexer

The analogue observation MPX (see Section 2.5) units process the analogue shunt signals for analogue observation and send 12 of these signals to each AMX 16/1 analogue MPX in view of the analogue-to-digital conversion. Each AMX 16/1 either gates the INCREMENT pulses for its own use or sends them to the next AMX 16/1. The mixer unit has been placed in the control loop between the ADC and the first AMX 16/1 to get all INCREMENT pulses generated by the ADC. This unit is fully described in Ref. 11 and a block diagram is shown on Fig. 11.

2.4.3.4 The analogue-to-digital converter (ADC)

The basic ADC unit developed for the CAAS has been modified to house a 12-bit, 3.5 μsec, ADC module from Hybrid Systems. It is now registered as MPS/BR 861 7002. It is used as a unipolar ADC with a 10 V input range and it performs a conversion every 7 μsec; half of this time is required for analogue signal selection and for data storage in the memory buffer.

2.4.3.5 The memory interface

A 3-unit-wide CAMAC module was necessary to house rather simple electronics because of the characteristics of CAMAC, which allocate a maximum of 16 random acquisition addresses for slot-in random mode on function F(0). Three CAMAC units are then required to provide 48 addresses. Tri-state buffers, controlled by BUSY signal through MODE input, transmit data and sign bits to the buffer memory. A CLEAR MEMORY ADDRESS signal and a STROBE pulse are sent with data bits by the ADC; these two bits are used to settle the internal address counter of the buffer memory. The transmission of data between the memory interface, the ADC, and the buffer memory is done through 52-pin Cannon connectors on front panels.

During the data acquisition procedure by the crate controller, an NAF command is generated on the CAMAC dataway; this command is fully decoded in the memory interface module to create the internal address to retrieve the relevant data from buffer memory. The data are transmitted to the dataway through open collector buffers gated by the NAF decoder. Access to stored data is done in a random fashion to be compatible with the present KNOBS system.

2.4.3.6 The memory buffer

Two slight modifications were made to the module developed by the SPS[12]; these two modifications do not alter the standard functions of the device; they concern the following parts:

i) Input mode is controlled by the BUSY signal through the front panel Cannon connector instead of internal jumper.

ii) The memory chips used are of Totem Pole type; otherwise internal pull-up resistors have to be added to the output of all memory chips.

2.5 Analogue signal observation system

2.5.1 Analogue observation in the Main Control Room (MCR)

The analogue observation of shunt currents in the MCR on conventional oscilloscopes is indispensable for the easy operation of an accelerator, although all parameters of the machine can be controlled and acquired through digital form. In view of these operational requirements a built-in analogue observation MPX is implemented in the controls of the new multipoles.

As hardware is shared in two parts, two analogue MPXs had to be provided. One of these systems acts as the master receiving the outputs of the slave as cascade input. The system allows the simultaneous observation of four bipolar analogue shunt signals; it is controlled by the central control computer through STAR and CAMAC. Hooking a knob to a multipole automatically selects the corresponding analogue shunt signals on the MPX outputs for observation on an oscilloscope in the MCR (see Section 3.2.2 for software modification in the KNOBS system).

2.5.2 General layout of the analogue observation system

A multipole Transceiver (see Section 2.3.1) sends a control word to the bus driver (see Fig. 8) specifying the desired signal and channel of the MPX to be used. The bus driver stores this control word and transmits it sequentially on a digital bus referred to as a CIM digital bus in this section; it also sends a clock pulse to synchronize read-write operation on the bus.

As long as the BUSY signal generated by the mixer unit is not active, the Sign Multiplexer selects the sign bit and the concerned analogue MPX selects the corresponding analogue shunt signal. The selected analogue signal (on a high-impedance analogue bus) and the selected sign bit are fed to the analogue driver unit to restore bipolar signals on coaxial cables to the MCR. If the selection deals with some signals from the slave subsystem, a CLEAR control signal is first transmitted to the master system to enable the cascade input of the analogue driver to be linked to the output in the MCR.

The format of the control word is as follows

Bit 1 : crate number
Bits 2 to 4 : module number
Bits 5 and 6 : output channel
Bits 7 to 10 : signal address
Bits 11 to 16 : unused

The crate bit is usually one, except when a CLEAR signal is sent to the master subsystem.

2.5.3 Technical characteristics

2.5.3.1 Transceiver

This CAMAC unit is already used to control the multipoles (see Section 2.3.1). It is used to send one control word per channel to the bus driver unit; the HOLD function of the Transceiver is not used in this application.

2.5.3.2 Bus driver

Channel bits are used to select locations where other significant bits of control words will be stored in 4 × 4 register files allowing simultaneous read-write operations. When the storage is done, a pulse is returned to the transceiver to finish up the transmission.

Those registers are sequentially scanned at a rate of 1 kHz and their contents are sent to the CIM digital bus through MPXs and buffers. Clock pulses derived from the internally generated 1 kHz clock synchronize writing operations in the other CIM units. The CIM digital bus is connected to the OMX 16/4 MPXs, to the analogue driver, and to the Sign Multiplexer.

Test facilities through front-panel switches and LEDs are provided. In TEST position, data can be simulated by means of 10 front-panel switches and stored in registers by pushing a button. A flashing LED warns the user when the TEST is on.

2.5.3.3 Analogue observation multiplexer OMX 16/4

The analogue part of the CIM unit consists of low-bandwidth unity gain amplifiers to convert balanced signals into COMMON mode analogue signals prior to multiplexing. Each amplifier drives four identical 16 to 1 MOS MPXs corresponding to the four output channels. These MPXs have ENABLE CONTROL features which allow high impedance output.

The analogue signals are entered through twisted pairs on two 14-pin Hughes connectors mounted on the rear panel (each of them contains six analogue shunt signals, one analogue test signal, and a ground level signal). The analogue signals are directly linked to front-panel Hughes connectors for direct connection to the AMX 16/1 analogue MPXs for analogue-to-digital conversion (see Section 2.4.3).

The digital part of the board consists of:

i) A decoder processing control bits from the bus driver. Four bits are provided for module location instead of the three bits in the bus driver: for future uses of this unit one can envisage up to 256 analogue signals. A multiple switch on the card has to be set according to the location the plug-in occupies in the CIM crate.

ii) A buffer storing channel bits and generating ENABLE signals for the MPX circuits and displaying the selected channels on LEDs. Four other buffers each store the signal address bits to be sent to the MPX. Four of these MPXs are used in each CIM crate in the multipole system. The analogue outputs are linked together per channel and entered in the analogue driver.

2.5.3.4 Sign Multiplexer

When the BUSY signal from the mixer unit is down, the control of the Sign Multiplexer is performed through the CIM digital bus.

The control bits select the sign address and store it in the register corresponding to the involved channel. Thirteen front-panel LEDs indicate the used output channels, the binary address of the signal (crate, module, signal bits), and the sign of the selected address.

The MPX is used in a random fashion in the analogue observation system, while it is used in sequential mode for the analogue-to-digital conversion.

2.5.3.5 Analogue driver

This CIM unit essentially consists of four programmable amplifiers (PRAM) followed by complementary pairs of transistors to drive 50 Ω cables for analogue voltages in the range of ±10 V.

The MARK pulse (600 mV, 600 μsec) generated by the mixer unit is added to the output signals to indicate when the analogue-to-digital conversion takes place: in case of automatic selection according to the knob specifications, the digital value of the shunt current measured at RTPS04 follows the name of the multipole on the screen of the console (PDS-1), so an immediate comparison can be made by the operator between the digital computer acquisition path and the actual analogue parameter.

Three of the four inputs of the PRAMs are used as follows:

i) one with unity gain (+1);
ii) one with inverted unity gain (-1);
iii) one with direct unity gain.

Two bits control the selection of the PRAM input: the first two inputs correspond to analogue bus signals, the sign bit from the Sign Multiplexer selecting the right one; the last one is dedicated to cascade input for signals from the other crate. The selection of this input is made with the crate bit of the control word. The bandwith of this unit exceeds 100 kHz.

The analogue signals are transmitted to the MCR in a COMMON mode, so the receiving amplifiers in the MCR eliminate 50 Hz ripple and compensate for losses in the cables. This rather simple system achieves a signal-to-noise ratio better than 4×10^{-4}.

2.6 VARILOG using microprocessor

2.6.1 VARILOG for power supplies driven by an analogue function

A proposal for the use of a microprocessor in the new PSB multipole power supply control system has already been presented[13], and arose from the need to measure the shape of the function produced by each of the 60 power supplies. In this application it is known that a simple area measurement will give a good approximation to the function, but requires the acquisition of some 3840 values (64 samples per power supply) each Booster cycle. With a serial crate system, each acquisition takes approximately 50 μsec, and therefore the total transmission time would be nearly 200 msec, which represents a large part of the Booster cycle. By introducing a microcomputer facility locally, in the CAMAC crate responsible for monitoring the power supplies, it is possible to perform all the necessary calculations to obtain the areas and then only transmit 60 values.

This microcomputer facility is in the form of CODOC 1 [14] and its interface to CAMAC, which acts as an auxiliary controller. Such an "intelligent" auxiliary controller in the CAMAC crate also allows us to perform equipment status monitoring and provides this information as data to be acquired by the central computer, thus once again reducing the data transmission rate.

For the moment only one microprocessor and its associated CAMAC interface have been built and tested; the second crate will be equipped with an identical microprocessor in 1977.

2.6.2 Implementation

The equipment to monitor these supplies is in the two CAMAC crates used for control and acquisition (see Sections 2.3 and 2.4). The MPX and ADC with memory are already used by the acquisition system once per cycle so that the auxiliary controller must be informed when the equipment is not available (by a BUSY signal, see Section 2.4.3.1). Further, the CAMAC crate is also used $\sim$ 30 times/cycle for the transmission of the control word (see Section 2.2.1) to the DAC driving the power supplies. The microcomputer must therefore be interrupted if it is in the process of using the dataway when the controller also requires its use. These two interrupts are the only change in context of the task required during its otherwise simple operation.

A block diagram of the monitoring system is shown in Fig. 9 and consists of three MPXs, an ADC, and the auxiliary controller (CODOC 1 + interface). The task of the auxiliary controller is to set the MPXs to the required address (see Fig. 10) and read the digitized data from the ADC. This is repeated 64 times for each power supply during the Booster cycle, commencing at STB1 and finishing before EBC. [See Timing system for the PSB[15].]

To control the MPX (see Fig. 11) and ADC, a daisy-chain connection of the equipment is required, such that on writing an address [F(16)A(Ø)] to an MPX [or an increment function F(25)A(0)], the ADC will also be triggered. The hardware internal to the ADC copes with the necessary set-up time of the MPX address before triggering the conversion. Also, in this configuration, when writing to one MPX the others are automatically cleared, and incrementing one MPX until overflow occurs will cause the next MPX in the chain to be incremented. Thus by only controlling the first MPX, the analogue signals on all of them can be accessed. The only time the other two MPXs need to be accessed directly is after an interrupt by either CAMAC or the BUSY signal.

2.6.2.1 Software implementation

The software to perform this VARILOG resides in PROM memory on the CODOC 1 module and is written in the ASSEMBLER language of the INTEL 8080 microprocessor. The development of this program was performed on the INTELLEC 8/MOD 80 MCS development system which was acquired by the Booster group.

As mentioned previously, the task is to acquire 64 samples from the power supplies during each Booster cycle, calculate the area, and supply these results as integer values (range 0-32768) to be acquired by the central computer. A status word will also be generated by the program, which will give the validity of the results and the status of the equipment controlled by the task.

The sequence of events required of the program is as follows:

i) Power up in a state ready to accept the STB1 signal;

ii) Monitor the multipole power supplies, sampling each one 64 times during the Booster cycle.

   a) If CAMAC is busy (B enabled), halt any auxiliary controller operation in progress and interrupt the program. When CAMAC is free, return to the main program with all hardware set to the condition it was in before the interrupt.

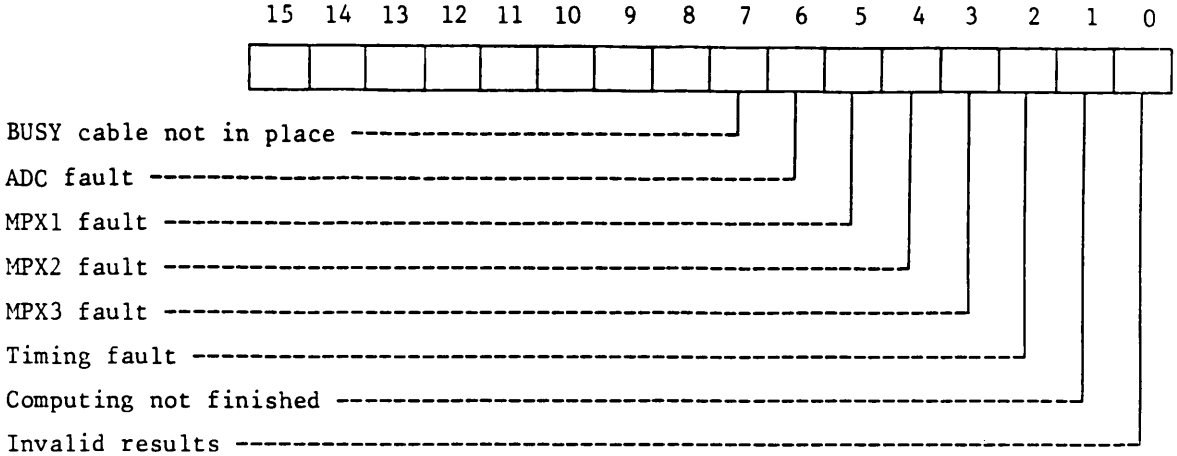
   b) If the MPXs or the ADC are used (BUSY signal enabled), interrupt the program. Count the time spent, in the interrupt routine, waiting for the BUSY signal to be disabled. When the equipment is free, return to the main program with all hardware set to the condition it was in before the interrupt occurred.

   c) If STB1 occurs, initiate a PROGRAM RESTART.

iii) When the task is finished, put the processor in the HALT state and wait for the next STB1.

A detailed description of this program is given in the listing in Appendix 4.

There are seven possible errors that may occur during the operation of this VARILOG program, and this information will be placed in a status word to be acquired by the central computer along with the results. The definitions of the status words and the errors are:



If the cable for the BUSY signal is not in place, the program will not commence and this error bit (7) will be set. A "Timing fault" will occur if the program is interrupted too many times during one Booster cycle, as the rate at which the power supplies are sampled will be too unevenly spaced leading to unpredictable results. The "Computing not finished" error bit is set at the beginning of the program and is only reset when the results are available to be acquired by the central computer. Finally, the "Invalid result" bit is of course just the OR of all other bits (the ADC and MPX faults are not yet implemented).

2.6.2.2 Acquisition of results using the CAMAC/STAR system

To acquire the results from CODOC 1 in a single step mode, the following sequence of operations must be performed:

1) Perform the CAMAC command N(9)A(7)F(16) with data = FBFF (hexadecimal):
   STAR C - address = 08A1 with data = FBFF.
   This operation puts the microprocessor in the HALT mode and loads the DMA address register with 0400; it also reads the first result into the CAMAC READ register in CODOC 1.

2) Do the CAMAC command N(9)A(1)F(0) (READ RESULT) 31 times to read the 30 results and the status word:
   STAR A - address = 4940.

3) The final command is to remove the HOLD signal from the microprocessor by performing the CAMAC function N(9)A(6)F(16) with data = 0.
   STAR C - address = 48A1 with data = 0000.

For the second microprocessor, the above addresses must be changed as follows: 08A1 to 08E1, 4940 to 4980, and 48A1 to 48E1.

The IBM VARILOG program using these results as input is described in Section 3.3.6; the PPM facility still has to be implemented.

2.7 Hardware for equipment monitoring

2.7.1 Monitoring by the 64-Line Surveyor module

All READY bits (sum of all internal status bits) can be monitored continuously through a 64-Line Surveyor CAMAC module*).

We only summarize the main features of this one-unit-wide CAMAC module also used in the new Linac project:

i) 64 different status bits (TTL level, open collector) are continuously scanned.

ii) As soon as a bit is found in the wrong state, scanning is stopped.

iii) By reading the module output, one gets the address (and the state) of the wrong status line.

iv) Faulty status bits can be masked if necessary.

We use one such module in each CAMAC crate; the bits to be monitored are galvanically isolated in a separate chassis.

The status of the 60 power supplies is then limited to two bits to be tested by the computer. The state of the +5 V power supplies is also monitored through the power supply monitor circuit described below and the 64 Line Surveyor. At the moment there is no active survey of the status bits by the IBM 1800 for the multipoles. The hardware is installed and the equipment monitoring facilities will be implemented with the forthcoming new PS computer system. It was felt that manpower should now be reserved for the new computer system.

2.7.2 Power supply monitor circuit

In the present state of the art of memory technology, local memories used in computer control application are based on bipolar or MOS circuits. These memories are cheap, fast, and reliable, but they are volatile; this means that any lack of power supply destroys the contents of the memories; this is rather bad when the power network is prone to noticeable disturbances (industrial, thunderstorms, etc.).

Non-volatile memories such as magnetic core memories or bubble memories are not fitted for small local memory applications. Other new technologies will be available soon; the MNOS (Metal Nitrure Oxide Silicon) seem to be limited as far as the number of WRITE operations is concerned, while the DIFMOS (Double Injection Floating-grid Metal Oxide Silicon from Texas Instruments) require a writing time of 100 msec or so.

---

*) Designed and manufactured by the Société d'Electronique nucléaire (SEN).

For the new multipoles, TTL memories were the only possible solution to implement local control memories; a power supply monitor circuit is associated with all +5 V power supplies.

The power supply monitor circuit is shown on Fig. 12 with its transfer characteristic in Fig. 13. The +5 V power supply (V_{cc}) to be monitored is also used to power the operational amplifier which acts as voltage comparator. The operational amplifier can operate correctly with a single power supply in the range from +2.5 V to +18.0 V (characteristics published by NSC). When V_{cc} is larger than 4.75 V, the Q_1Q_2 flip-flop on Fig. 12 can be reset by the RESET pulse; if V_{cc} gets into the +2.0 V to 4.75 V range, the Q_1Q_2 flip-flop will be set to one, and will remain in that state even if V_{cc} returns to the 4.75 V to 5.25 V range. The power supply monitor output can be sensed by the computer, which can refresh all relevant local memories and reset the Q_1Q_2 flip-flop.

Two such circuits can be combined to monitor a power supply in a defined range (e.g. 4.75 V to 5.25 V). All other power supplies (not connected to memories) are monitored by conventional relays whose contacts are placed in series to create the power supply on (PS ON) status bit shown in Fig. A5 of Appendix 2.

The power supply monitor circuit is housed in a module plugged into the auxiliary power supply crate.

3. DESCRIPTION OF SOFTWARE

3.1 Generalities

As already mentioned, it has been agreed to have in this project[16] the minimum control facilities compatible with an easy operation. This implies:

i) no sophisticated treatments of the multipoles, e.g. no harmonics, non-linear couplings, etc.;

ii) use, when possible, of the existing control systems, e.g. KNOBS system, data bank, etc.

This second item permits the operator to deal with new multipoles in the same way as it was accustomed to deal with other PSB parameters and, first of all, to control at the same time the new and the old multipoles.

An implication of this solution is that an important part of the software consists in modifications of the existing control programs. These modifications permit the adaptation of programs to the peculiarities of the new multipoles in a way that is, as far as possible, transparent to the user. The functional aspect of the software is intimately related to the operation of the new multipoles. However we have tried here to separate the two things and all operational aspects are dealt with elsewhere[17-18].

3.2 Modification of the existing software

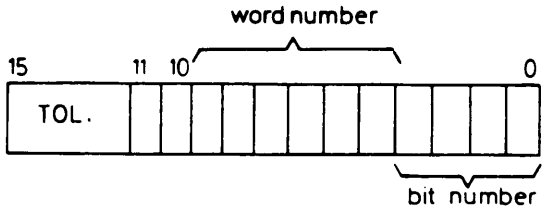
3.2.1 Data bank

The new multipoles are organized[19] in 28 groups, each one containing two or four elements: the number of one element represents the period in which the multipole is installed (between 1 and 16). Owing to the organization of the PSB data bank[20], the elements must be numbered progressively and room must be reserved on disk for all elements from the lowest to the highest numbered ones, no matter whether they exist physically or not.

In our case that means we need $16 \times 28 \times 10 = 4480$ words on disk (each element specification takes 10 words). Unfortunately, that much free room does not exist in the PSB data bank. This difficulty has been overcome in the following way. The elements in each group are numbered only from 1 to 4 (or 1 to 2): the data bank management programs (see Section 3.2.2) provide the translation from the user name (1 to 16) to the data bank name (1 to 4). For example, the group containing the elements (periods) 4, 9, 13, 16 is translated into a group containing the elements 1, 2, 3, 4. The "trick" is transparent to the user. This "compression" permits the storage of the element specifications of the 104 multipoles in only 1040 words (Fig. 14). The user numbers are in parentheses. No problems exist for storing

of the group specifications (28 × 10 = 280 words). The group and element specifications are the same as for the other PSB parameters except for the ON-OFF and READY bits position words[20]. In these two words the bits 10 and 11 have a new signification:

- bit 10 = 1 means element is a new multipole
- bit 11 = 1 means element is not connected



STATUS BIT POSITION WORD

DATA BANK MANAGEMENT PROGRAMS

3.2.2 Data bank management programs

i) The SOFTC routine

This routine permits the link between the name of a parameter and its specifications on data bank. It has been modified to permit the translation mentioned before between user and data bank names.

ii) The IN-CORE status word table

This table, which is updated at each PSB cycle, contains information about the status of most of the PSB elements (READY, ON-OFF, polarity conditions, etc.). Twelve acquisition words have been added for the new multipoles. Each word refers to a CIM crate and contains the ON-OFF and READY conditions for six power supplies (see Section 2.1). It also contains the overflow conditions for a bank of transistors.

iii) The READY and ON-OFF routines

These two routines are very similar: following the instructions contained in the data bank (position of the READY and ON-OFF bits, see Section 3.2.1) they read in the table mentioned in (ii) if the parameter is READY (ON) or not.

If the element is not connected (bit 11 in the status bit position word, see Section 3.2.1) the answer NOT READY or OFF is given without reading in that table.

3.2.3 The KNOBS system

Two new functions have been added to this system[21]. They are activated at each machine cycle if the element connected to a knob is recognized as a new multipole (bit 10 in the status bit position word, see Section 3.2.1):

i) The WARNING RECTIFIER bit of the CIM crate to which the multipole belongs is tested and, if ON, the message OUT OF RANGE is sent to the display (PDS 1).

ii) The analogue MPX is activated (see Hardware, in Section 2.4) and the current function corresponding to the selected multipole is sent to the four-trace oscilloscope in the MCR. The number of the chosen trace on the oscilloscope is the same as the one of the selected knob.

3.2.4 Other modifications

The programs PRINT DATA BANK and UPDATE DATA BANK have been modified to treat also the new multipoles. The output of the first one is printed from the data bank names. The second one allows interaction with the data bank through the user name (see Section 3.2.1).

3.3 New programs

3.3.1 The NEW MULTIPOLES program

The functional flow chart of this program is shown in Fig. 15. The main tasks of this program are to build the connection table (see Section 3.3.2) between multipoles and power supplies[17] (Fig. 16a) and to execute a status information treatment (Section 3.3.3 and Fig. 16b).

The connection table can be, on request, either simply displayed, or stored on disk and used to update the data bank. The last table stored on disk can be displayed using the first option of the program.

One important treatment concerns the error detection (see Section 3.3.2). Errors are checked, classified according to their type[17,18], and displayed. If their number is unacceptable, the data bank is not updated.

3.3.2 The IDENT routine (Fig. 17)

The input for this routine is a table of 60 identification words, acquired from each power supply (in the future 96 power supplies are foreseen) and containing the identification word (see Section 2.2.2) of the multipole and of the analogue function driving the power supply. The output is a table of 120 words, each one assigned to a multipole (for the moment only 104 exist) and containing the reference number of the power supply and of connected analogue function.

This table is called the connection table. During the execution of this kind of table inversion, each acquired word is checked for three types of errors[17,18]:

- the reference number of the multipole is not within the limits of 1 to 52 and 65 to 116 representing the two groups existing at present;
- the same multipole number is found on two or more power supplies;
- the reference number of the analogue function is not within the limits of 34 to 48.

The multipoles affected with errors of the first two types are considered as non-connected. The connection and the error tables are returned to the main program and used as explained before.

3.3.3 The update new multipoles DATA BANK program (Figs. 18 and 19)

The PSB data bank is organized[20] in groups and elements specifications: both of these are usually fixed and are defined at the moment of the design. This is no longer true for the new multipoles: owing to the freedom in connections, four element specifications must be updated after each modification in the connections.

These specifications are (Fig. 18):

- the acquisition address
- the control address
- the READY bit position word
- the ON-OFF bit position word.

The program reads the element specifications of all new multipoles into core (1040 words for the 104 elements; see Fig. 14). The four concerned specifications are first filled with dummy or special values:

- acquisition address = /0000 (dummy address)
- control address = /0215 (dummy address)
- READY word = /0800 (not connected)
- ON-OFF word = /0800 (not connected).

Then, following the instructions contained in the connection table, the program fills the actual four specifications only in those multipoles that are connected without identification errors (see Section 3.3.2). Finally, the updated data bank is stored on disk.

3.3.4 The STATUS DISPLAY program (Figs. 20 and 16b)

The program provides the user with detailed information on the power supplies behaviour.

In fact the NOT READY message occurring in certain cases on the KNOBS display[21] is only an OR-ed sum of many conditions; each one of them can stop the supply.

Nine NOT READY, one WARNING, and one OFF condition per power supply are checked and displayed. This information is contained in status words, one per power supply;

they are acquired at the beginning of the program. At the same time identification words are acquired (see Section 3.3.2) to attribute multipole names on the display. The display is divided into four pages, each one referring to a group of power supplies.

If a multipole number error is detected (see Section 3.3.2) the message FAULT replaces the multipole name in front of the corresponding power supply reference number. After the display of the last page (page 4) it is possible to come back to page 1: in this case a new acquisition is done permitting one to follow the evolution of the status bits when hardware is being repaired.

3.3.5 The CURRENTS HISTOGRAM program (Figs. 21 and 16c)

This program concerns the new and the old multipoles (except for the zero-harmonic multipoles).

An identification process, similar to that described in Section 3.3.2, permits the attribution to each new multipole of the acquisition address of the power supply to which it is connected.

Three pages of histograms are available, one for the quadrupoles, another for the sextupoles, and a third one for octupoles. On each page the four rings of the PSB are represented separately. The currents are acquired in a selected Intensity Programme Line (IPL). The initial value of the full-scale histogram is ±30 A and the acquisition timing corresponds to a B-value of 1260 G.

By turning knobs 4 and 3 respectively, it is possible to change these two parameters during the execution of the program: this avoids the tedious preselection of the starting values.

Knobs are used in the incremental mode with reset after each reading, i.e. $P_1 = P_0 + \Delta P$, where P_1 and P_0 are buffered in the computer memory and ΔP is the knob's acquired value.

MIN (±1 A) and MAX (the selected full scale) values are checked by software, and if a current exceeds these limits its representation in the histogram is truncated to these limits and a message is given.

A similar limiting check is done for timing.

3.3.6 Other programs

A LOG program which permits one to have:

- printed information on the new multipoles in a form similar to that of other PSB elements;
- a VARILOG*) program (see Section 2 and Fig. 16d). This program compares the actual acquired current value of each multipole with a reference value. If a

*) The analysis of this program has been done by John Stark[22].

difference exceeding a predefined tolerance or a status change are detected, alarm messages are displayed as in Fig. 16d.

Two message pages exist for the two groups of power supplies.

The acquired values and the reference values concern time-integrated current area measurements as explained in Section 2 and in Ref. 13. For this reason the displayed values can be totally different from these given by the KNOBS or LOG programs.

Acknowledgements

This work was carried out in continuous collaboration with many of our colleagues involved in the project. We would like to thank G. Nassibian, K.H. Reich and H. Schindl for their help in defining the system, the BR/power team members P. Burla, M. Métais, R. Gailloud, J.P. Royer and F. Völker for their close collaboration, J. Stark for his help in the VARILOG and the STAR maintenance team, and J. Philippe and G. Surback for the installation and the test of the two STAR-CAMAC controllers.

REFERENCES

1) K. Schindl, A quoi servent les nouveaux multipôles du PSB, PS/BR Note 76-23 (1976).

2) The working party of the CPS controls, Improvement programme for the CPS controls, PS/CCI Note 76-33 (1976).

3) P. Burla, L'électronique de commande et régulation pour les alimentations des nouveaux multipôles PSB, PS/BR/76-16 (1976).

4) J. Philippe et G. Surback, Contrôleur STAR-CAMAC, MPS/CCI Note 75-5 (1975).

5) G. Surback, Caractéristiques et particularités du contrôleur STAR-CAMAC, MPS/CCI Note 75-19 (1975).

6) G. Baribaud, G. Benincasa, P. Horne and D. Williams, Microprocessors help in control and beam observation at the CERN PS Booster, to appear.

7) F. Bel et al., CAMAC timing with special reference to crate controller timing, CERN-NP CAMAC, Note 3800 (1971).

8) F. Giudici, Note technique test CAMAC, October 1976.

9) G. Baribaud, Mémoires locales pour le PPM, PS/BR Note 76-19 (1976).

10) B. Hallgren, The transceiver and the control unit for the control of the new PSB multipoles using CAMAC MPS/BR Note 75-20 (1975).

11) E. Marcarini, Convertisseur analogique digital, PS/CCI/Note 76-13 (1976).

12) C. Guillaume, Mémoire 256 × 16 mots, Lab. II CO/CC/Int. Note/CG/75-6 (1975).

13) G. Benincasa and B. Hallgren, Using a microprocessor in an improved VARILOG facility, MPS/BR Note 75-2 (1975).

14) P. Horne, CODOC 1, Computing device for CAMAC, PS/BR Note 76-4 (1976).

15) G. Gelato, Timing system for the PSB, SI/Note EL/70-3 (1970).

16) G. Baribaud, G. Benincasa, G. Gelato, P. Heymans, K.H. Reich and K.H. Schindl, Computer control requirements for the control of the PSB multipoles, the pulse to pulse intensity modulation and the PSB equipment monitoring, MPS/BR Note 74-22 (1974).

17) F. Giudici, Table de connexion des alimentations des nouveaux multipôles du PSB, MPS/BR Note 75-24 (1975).

18) G. Benincasa et F. Giudici, Opération par ordinateur des nouveaux multipôles du PSB, PS/BR Note 76-21 (1976).

19) G. Benincasa, Proposition de "baptêmes" des nouveaux multipôles du PSB, MPS/BR memorandum 27.11.74.

20) D. Daneels, A data bank for on-line process control, CERN/SI/Int. DL. 72-3 (1972).

21) G. Benincasa, Le système KNOBS pour le contrôle du PSB, SI/BR Int. 72-3 (1972).

22) J. Stark, The PSB varilog, MPS/BR Note 73-16 (1973).

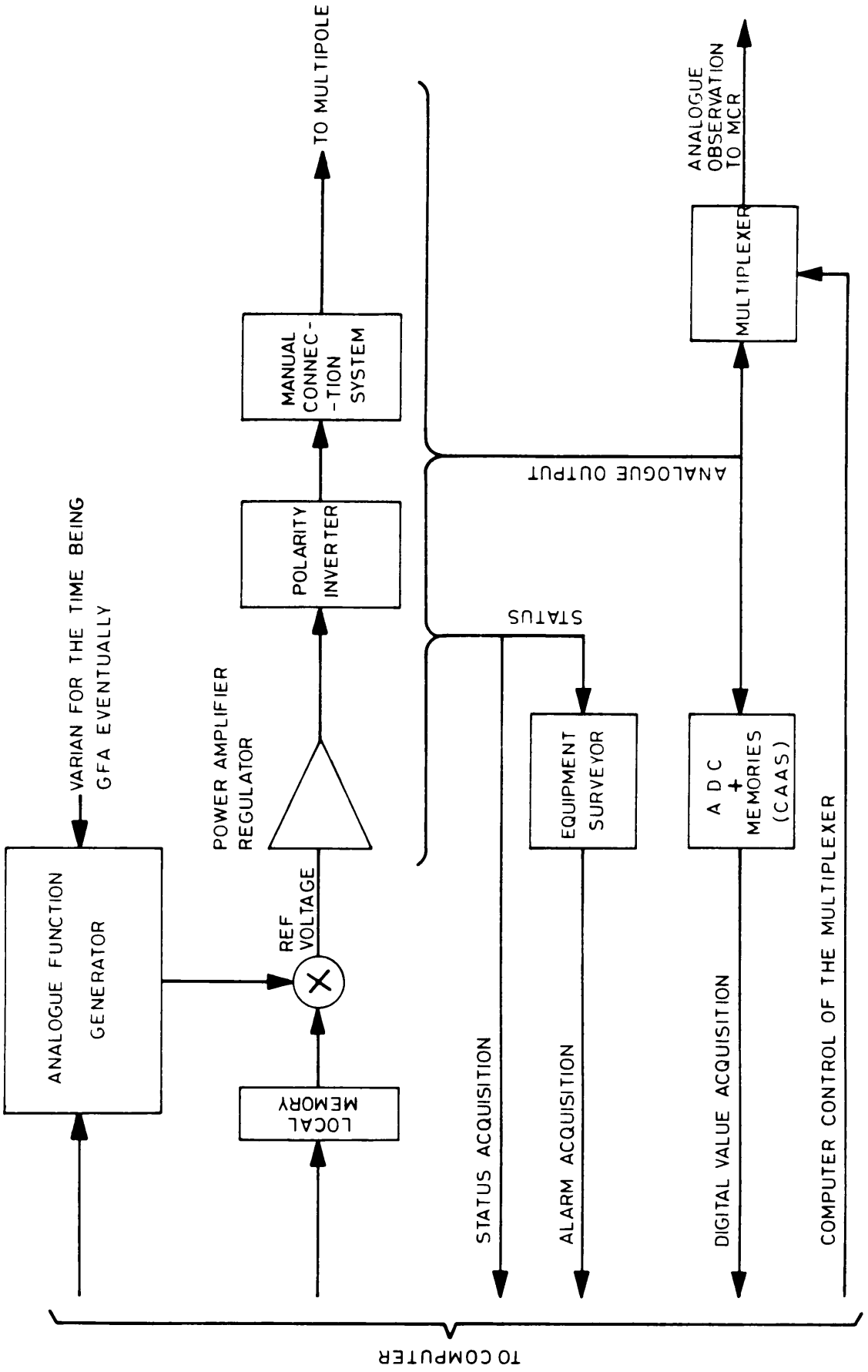


FIG. 1 CONTROL SHEMA OF THE NEW MULTIPOLES

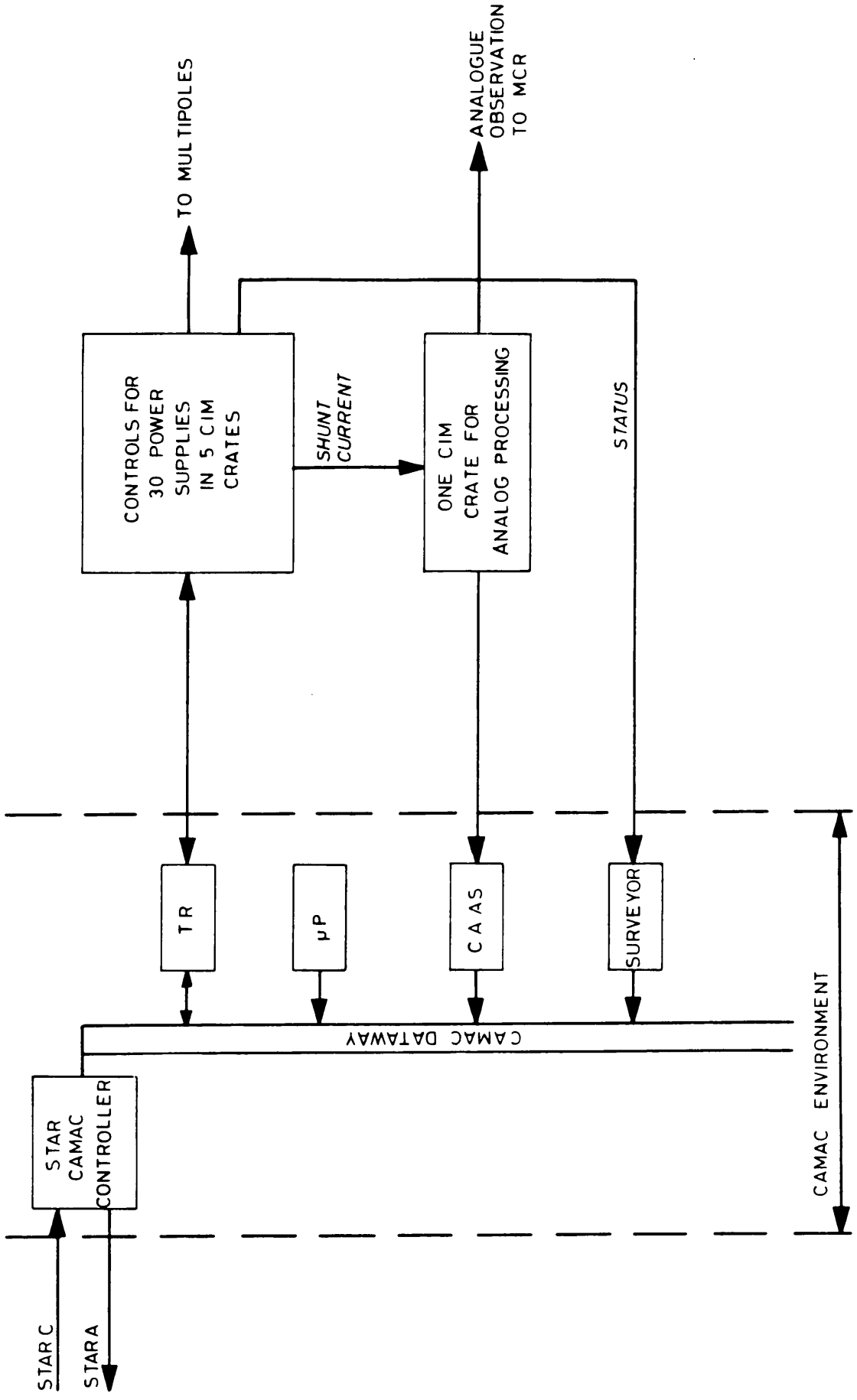


FIG.2. HARDWARE LAYOUT FOR ONE GROUP

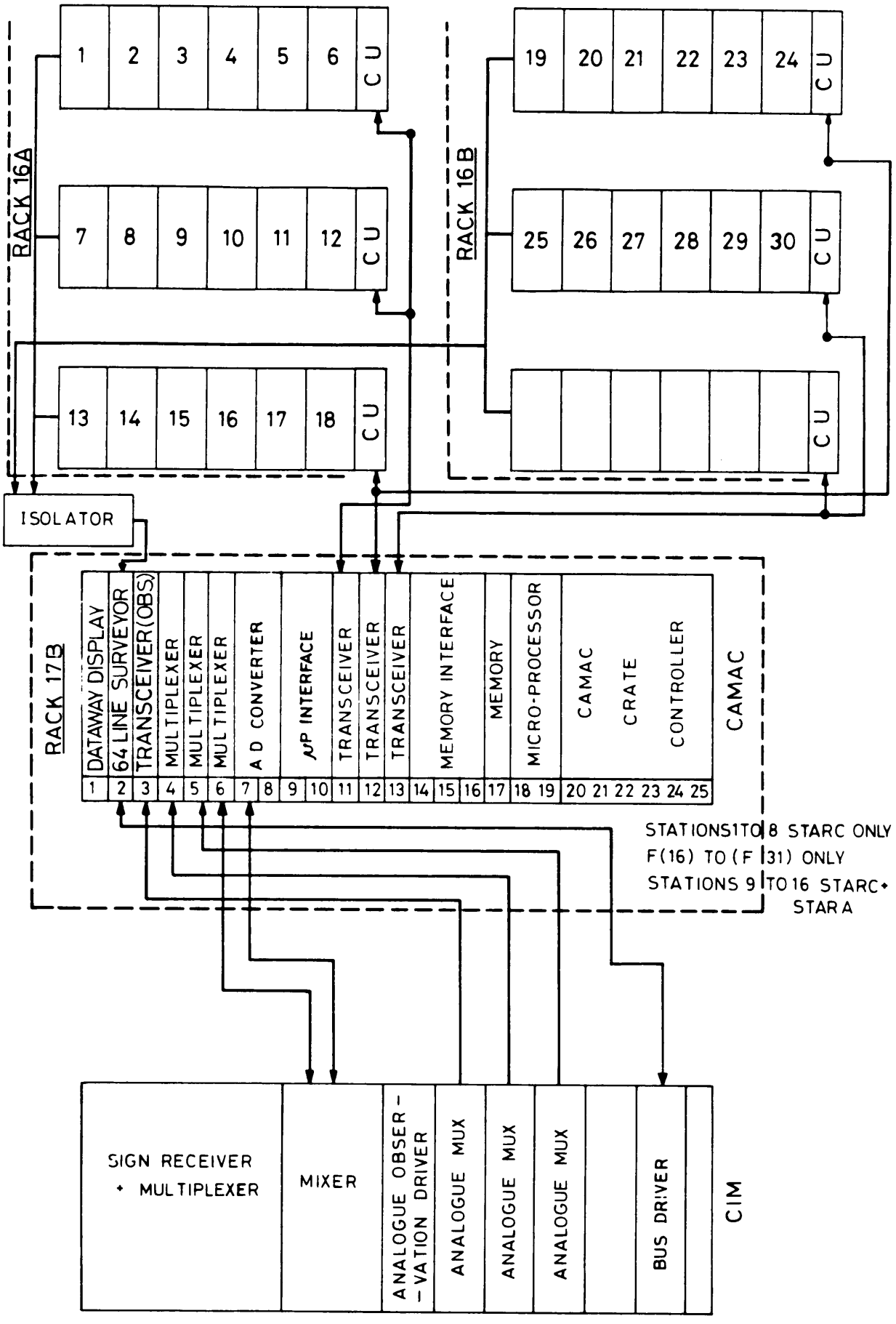


FIG. 3. FINAL LAYOUT OF THE HARDWARE

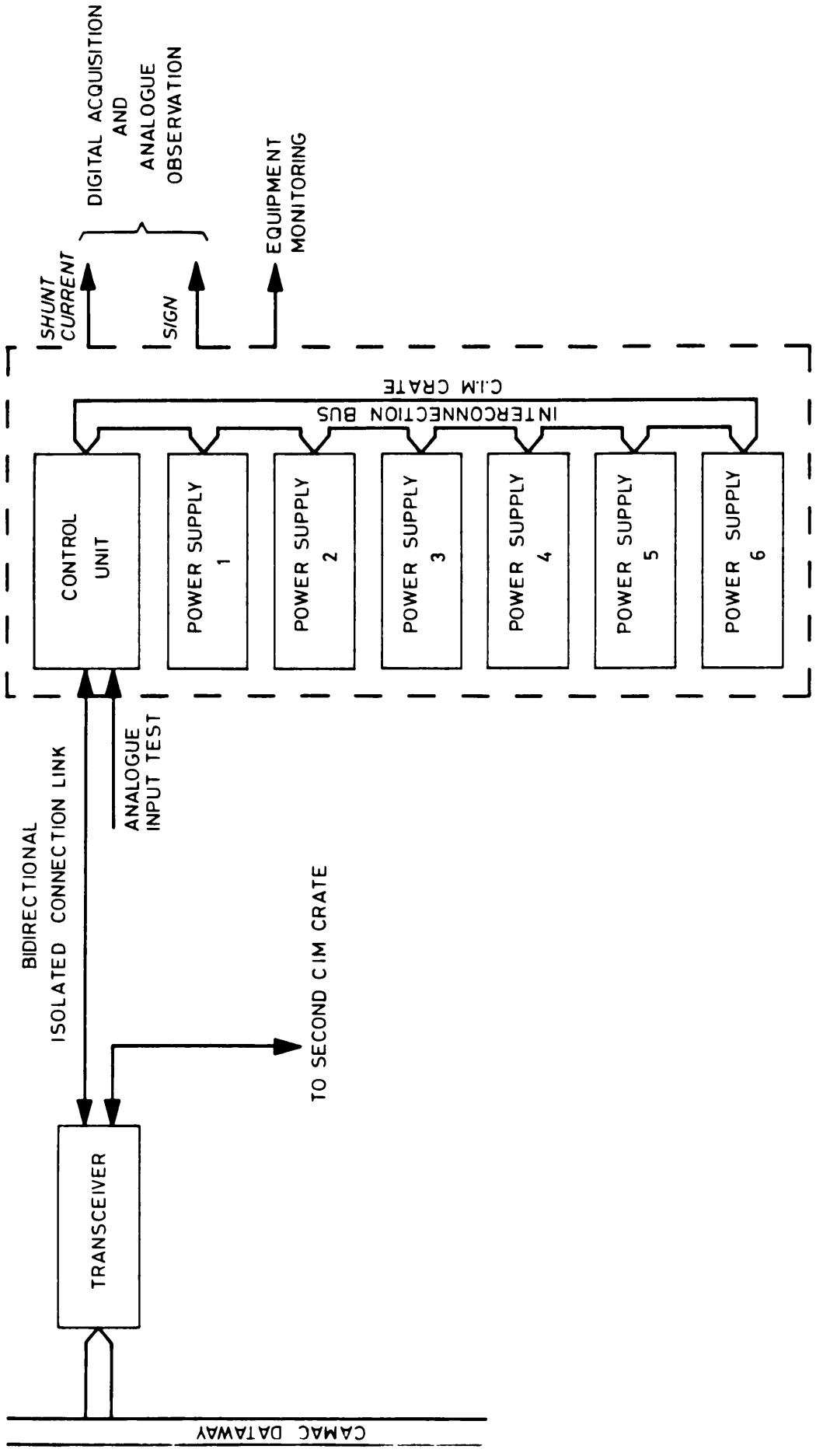


FIG. 4. CAMAC - CIM INTERFACE LAYOUT

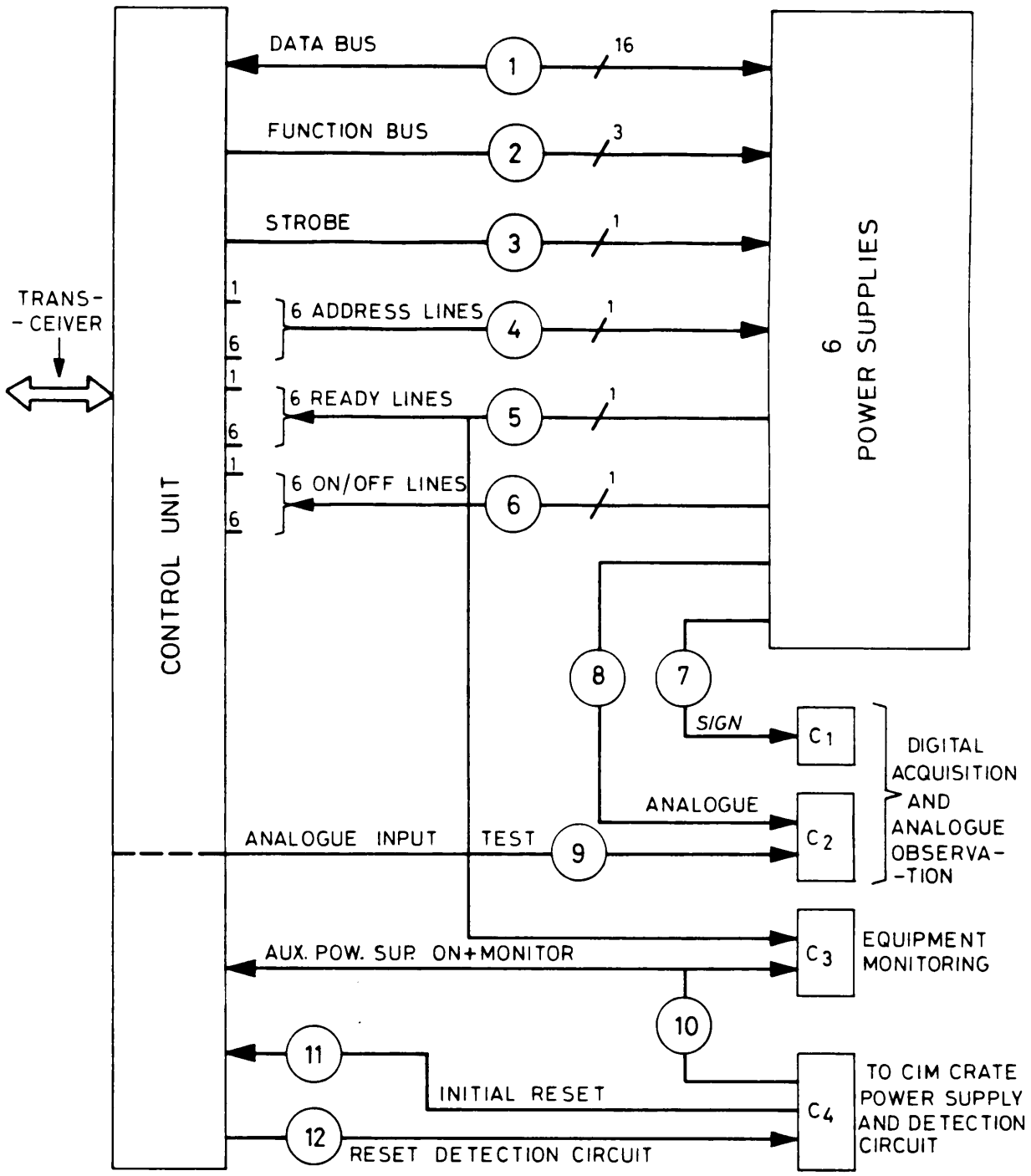
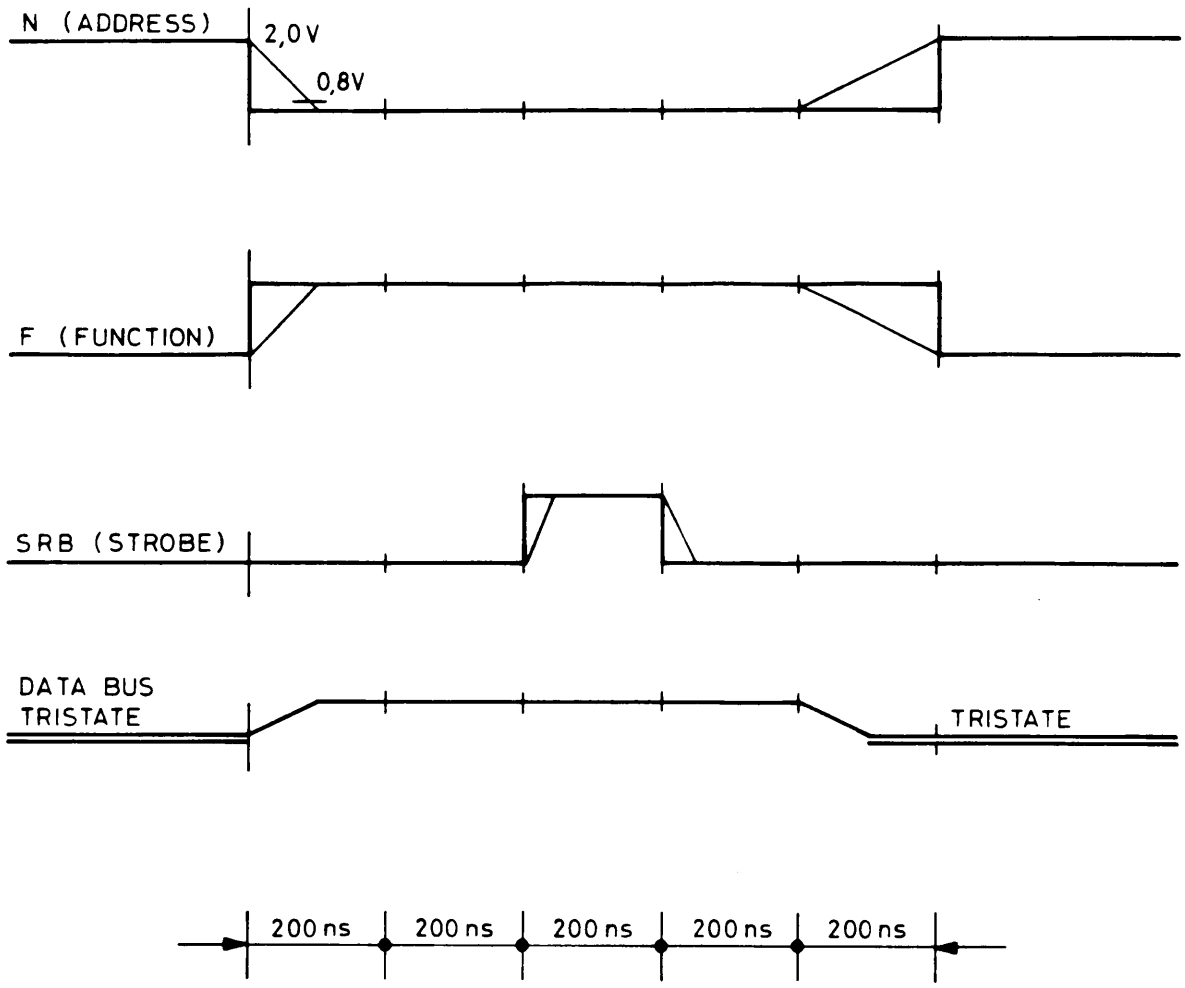


FIG. 5. INTERCONNECTION BUS



N: TTL OPEN COLLECTOR, NEGATIVE LOGIC
DATA TTL TRISTATE POSITIVE LOGIC (9 TTL LOADS)
FUNCTIONS AND STROBE: TTL TOTEM POLE POSITIVE LOGIC
(29 TTL LOADS)

FIG. 6. TIMING AND LOGICAL LEVELS
FOR THE INTERCONNECTION BUS

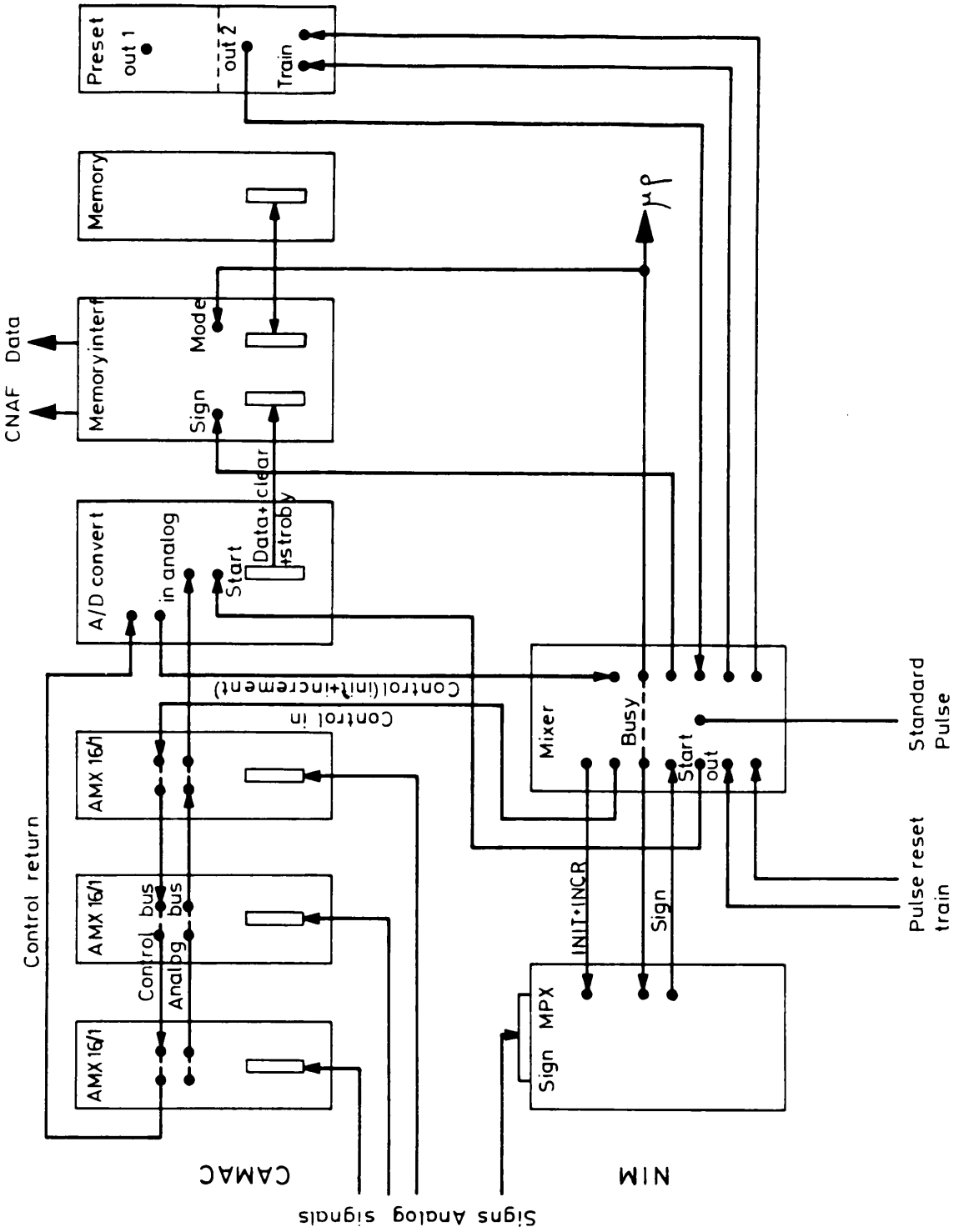


FIG. 7 A/D Conversion and acquisition layout

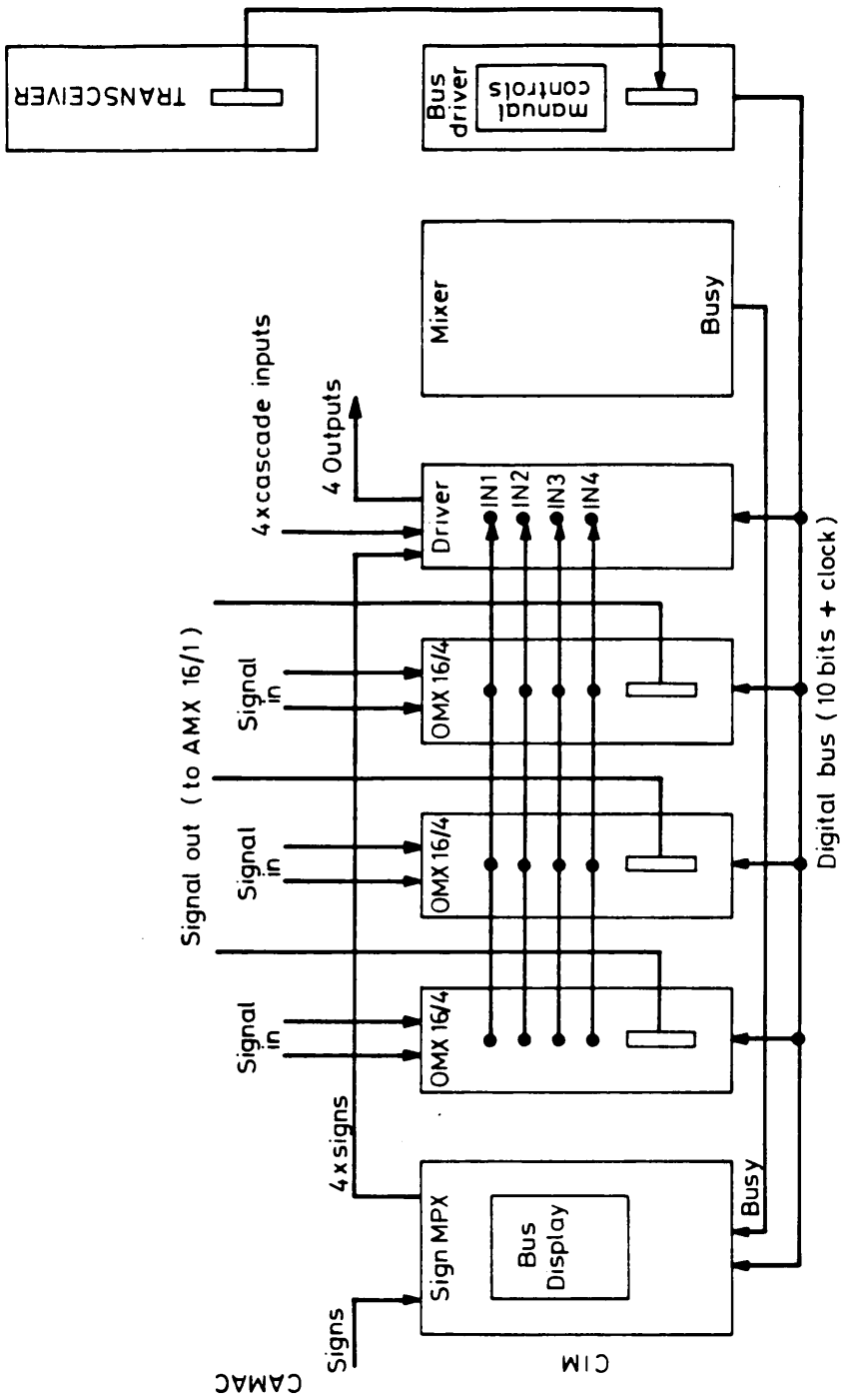


FIG. 8. Analog signal observation layout

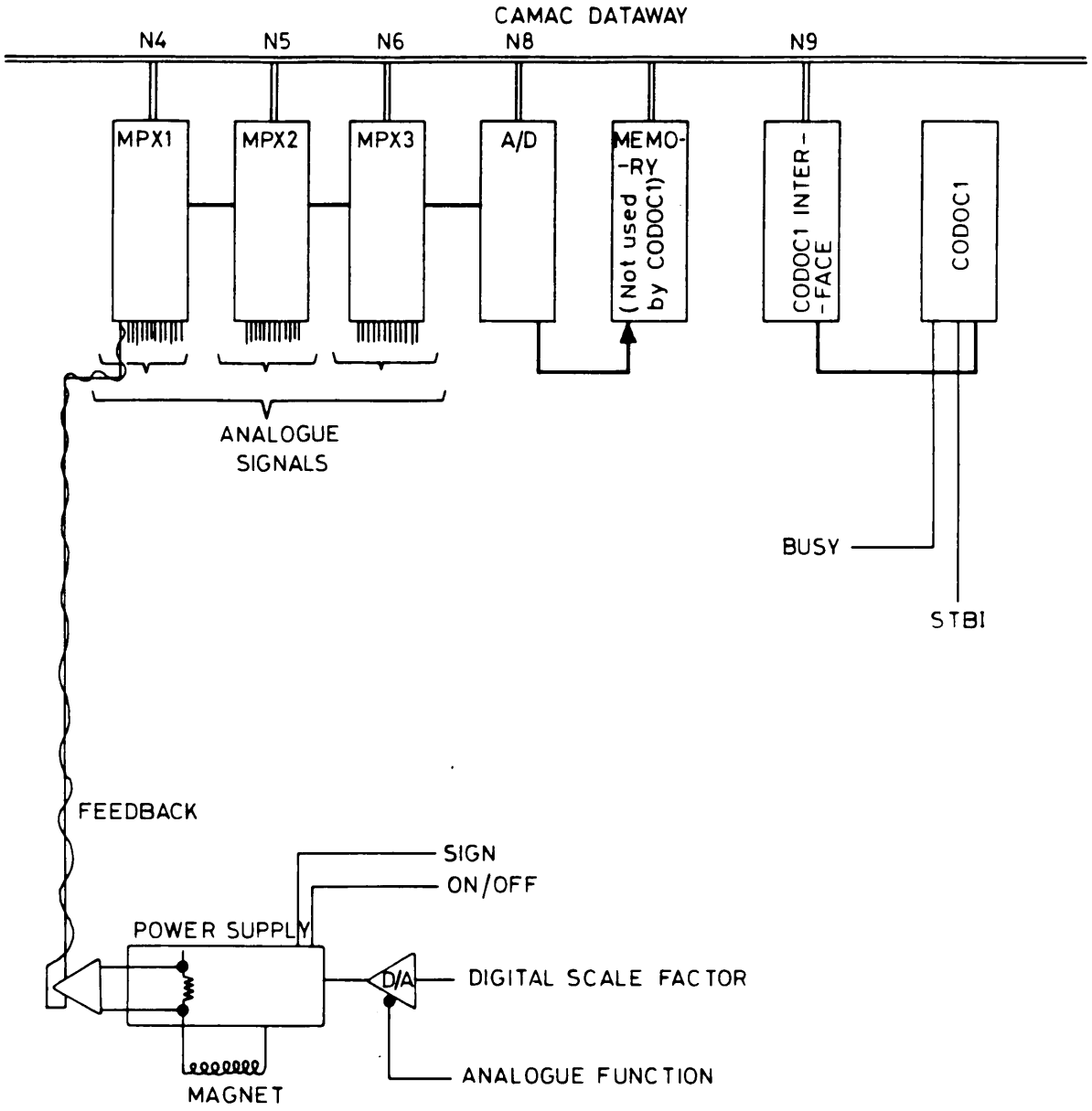


FIG. 9. MULTIPOLE MICROPROCESSOR VARILOG (HARDWARE)

POWER SUPPLY	MPX	ADDRESS (MPX)
1	1	0
2	"	1
3	"	2
4	"	3
5	"	4
6	"	5
7	"	7
8	"	8
9	"	9
10	"	10
11	"	11
12	"	12
13	2	0
14	"	1
15	"	2
16	"	3
17	"	4
18	"	5
19	"	7
20	"	8
21	"	9
22	"	10
23	"	11
24	"	12
25	3	0
26	"	1
27	"	2
28	"	3
29	"	4
30	"	5

FIG. 10. MULTIPLEXER / POWER SUPPLY CONNECTION

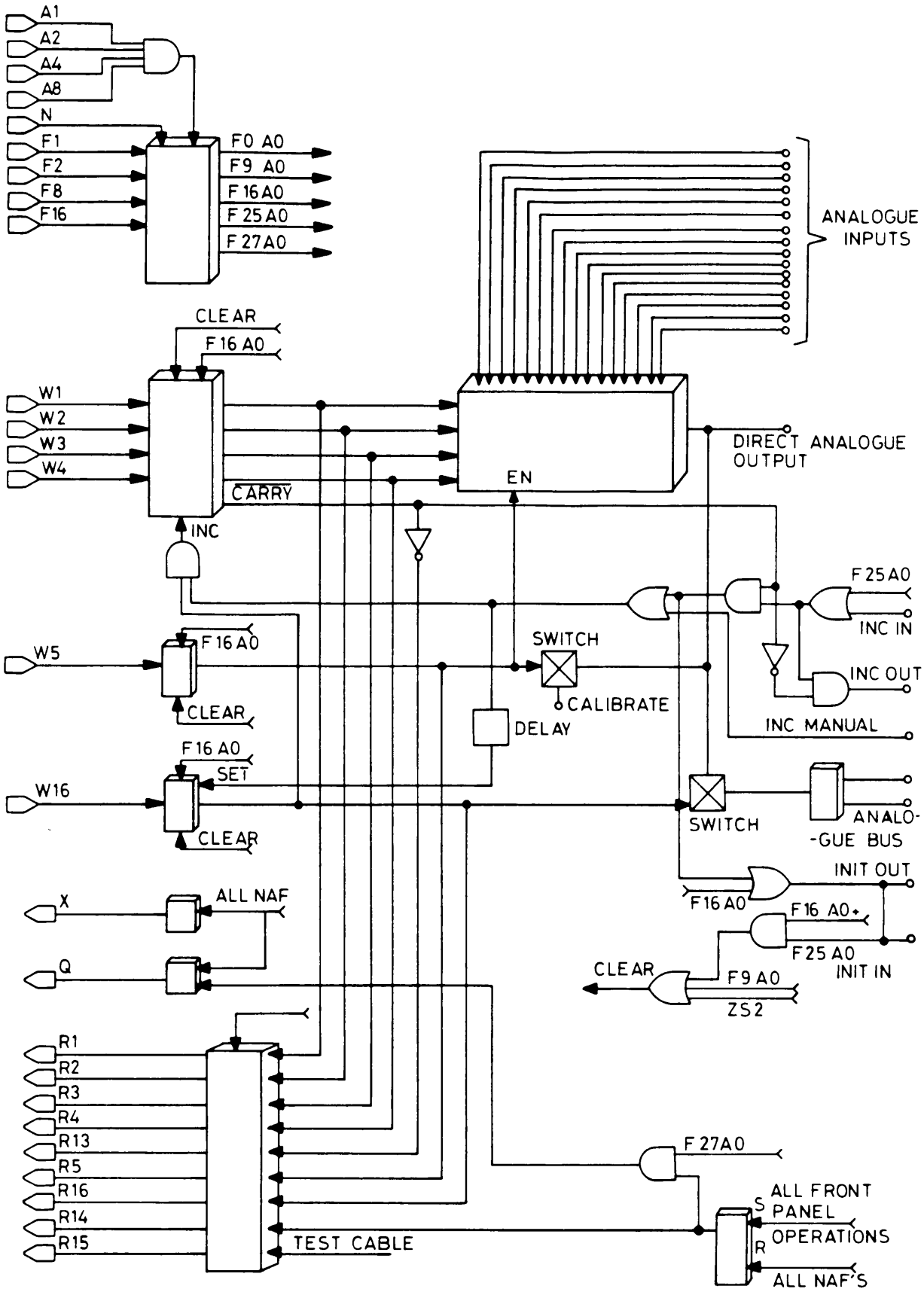


FIG. 11. ANALOG MULTIPLEXER 16/1

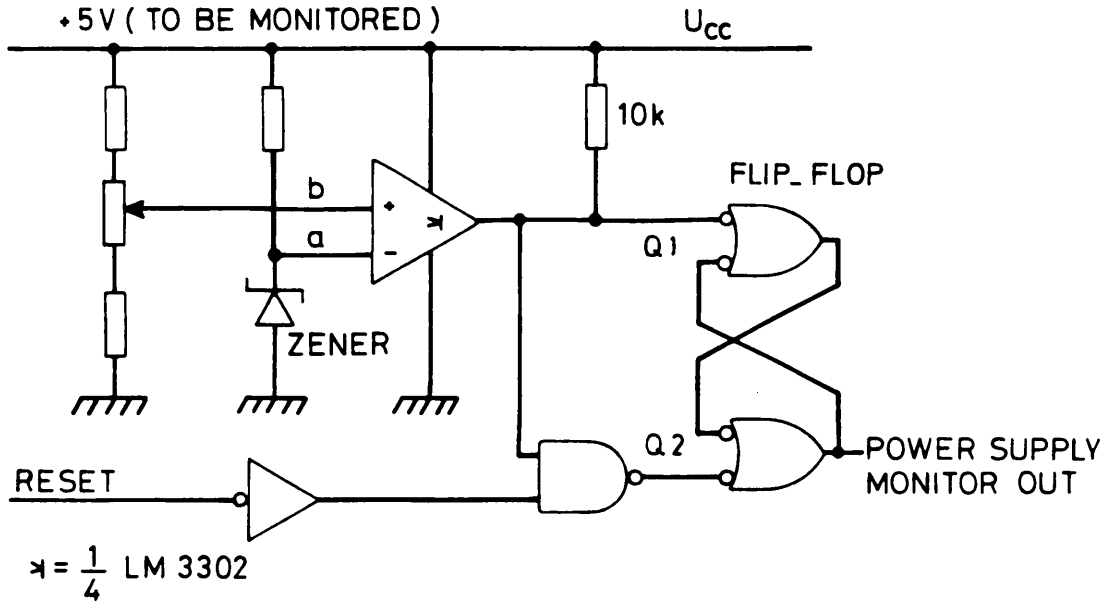


FIG. 12. POWER SUPPLY MONITOR CIRCUIT

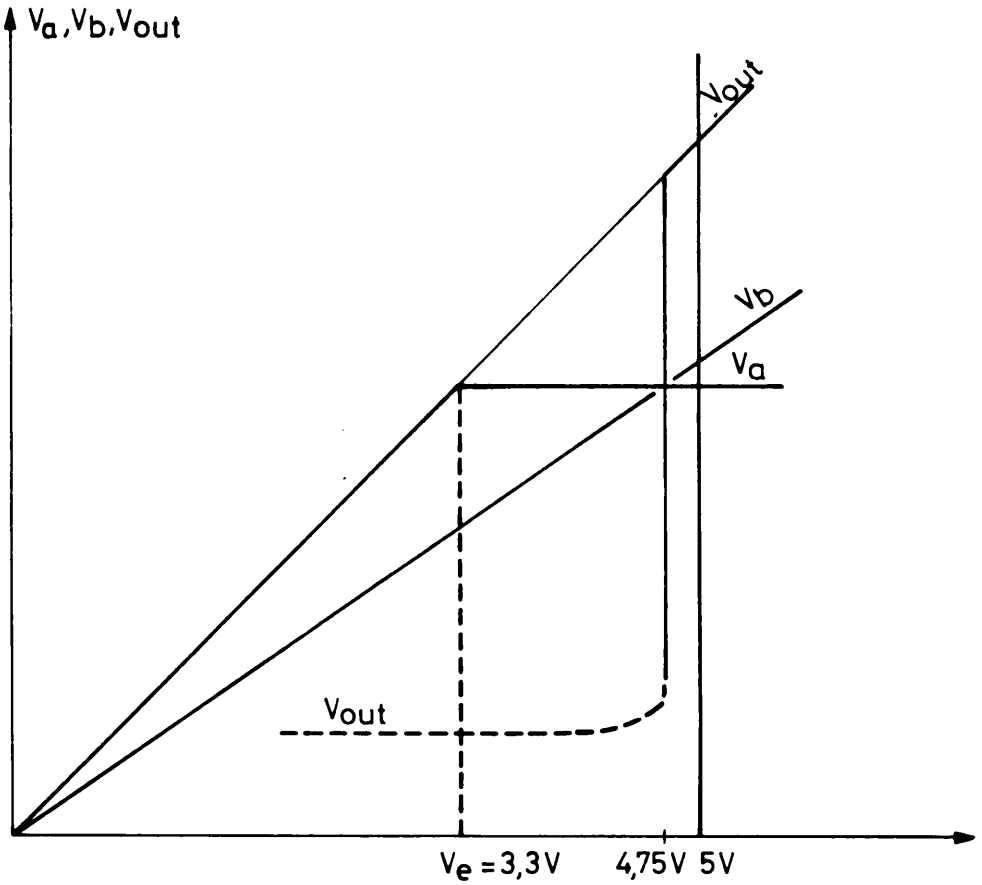


FIG. 13. TRANSFER CHARACTERISTICS OF THE POWER SUPPLY MONITOR CIRCUIT

PSB DATA BANK
ELEMENT SPECIFICATIONS

NEW MULTIPOLES

(FILE 12) DDF60

	(SOFT CODE)						
1	1	8	8	1	1SSL	(04)	Ø1
2	1	8	8	2		(06)	Ø2
3	1	8	8	3		(09)	Ø3
4	1	8	8	4		(12)	Ø4
5	1	9	0	1	1SNL	(04)	Ø1
6	1	9	0	2		(06)	Ø2
7	1	9	0	3		(09)	Ø3
8	1	9	0	4		(12)	Ø4
9	1	9	8	1	1OSL	(04)	Ø1
10	1	9	8	2		(06)	Ø2
11	1	9	8	3		(09)	Ø3
12	1	9	8	4		(12)	Ø4
13	1	A	Ø	1	1ONL	(04)	Ø1
14	1	A	Ø	2		(06)	Ø2
15	1	A	Ø	3		(09)	Ø3
16	1	A	Ø	4		(12)	Ø4
17	1	A	8	1	1SSS	(02)	Ø1
18	1	A	8	2		(06)	Ø2
19	1	A	8	3		(11)	Ø3
20	1	A	8	4		(12)	Ø4
21	1	B	Ø	1	1OSS	(02)	Ø1
22	1	B	Ø	2		(06)	Ø2
23	1	B	Ø	3		(11)	Ø3
24	1	B	Ø	4		(12)	Ø4
25	1	B	8	1	1SNS	(03)	Ø1
26	1	B	8	2		(12)	Ø2
27	1	C	Ø	1	2SSL	(04)	Ø1
28	1	C	Ø	2		(06)	Ø2
29	1	C	Ø	3		(09)	Ø3
30	1	C	Ø	4		(12)	Ø4
31	1	C	8	1	2SNL	(04)	Ø1
32	1	C	8	2		(06)	Ø2

(FILE 13) DDF61

	(SOFT CODE)						
33	1	C	8	3		(09)	Ø3
34	1	C	8	4		(12)	Ø4
35	1	D	Ø	1	2OSL	(04)	Ø1
36	1	D	Ø	2		(06)	Ø2
37	1	D	Ø	3		(09)	Ø3
38	1	D	Ø	4		(12)	Ø4
39	1	D	8	1	2ONL	(04)	Ø1
40	1	D	8	2		(06)	Ø2
41	1	D	8	3		(09)	Ø3
42	1	D	8	4		(12)	Ø4
43	1	E	Ø	1	2SSS	(02)	Ø1
44	1	E	Ø	2		(06)	Ø2
45	1	E	Ø	3		(11)	Ø3
46	1	E	Ø	4		(12)	Ø4
47	1	E	8	1	2OSS	(02)	Ø1
48	1	E	8	2		(06)	Ø2
49	1	E	8	3		(11)	Ø3
50	1	E	8	4		(12)	Ø4
51	1	F	Ø	1	2SNS	(03)	Ø1
52	1	F	Ø	2		(12)	Ø2
53	1	F	8	1	3SSL	(04)	Ø1
54	1	F	8	2		(06)	Ø2
55	1	F	8	3		(09)	Ø3
56	1	F	8	4		(12)	Ø4
57	7	9	8	1	3SNL	(04)	Ø1
58	7	9	8	2		(06)	Ø2
59	7	9	8	3		(09)	Ø3
60	7	9	8	4		(12)	Ø4
61	7	A	Ø	1	3OSL	(04)	Ø1
62	7	A	Ø	2		(06)	Ø2
63	7	A	Ø	3		(09)	Ø3
64	7	A	Ø	4		(12)	Ø4

(FILE 14) DDF62

	(SOFT CODE)						
65	7	A	8	1	3ONL	(04)	Ø1
66	7	A	8	2		(06)	Ø2
67	7	A	8	3		(09)	Ø3
68	7	A	8	4		(12)	Ø4
69	7	B	Ø	1	3SSS	(02)	Ø1
70	7	B	Ø	2		(06)	Ø2
71	7	B	Ø	3		(11)	Ø3
72	7	B	Ø	4		(12)	Ø4
73	7	B	8	1	3OSS	(02)	Ø1
74	7	B	8	2		(06)	Ø2
75	7	B	8	3		(11)	Ø3
76	7	B	8	4		(12)	Ø4
77	7	C	Ø	1	3SNS	(03)	Ø1
78	7	C	Ø	2		(12)	Ø2
79	7	C	8	1	4SSL	(04)	Ø1
80	7	C	8	2		(06)	Ø2
81	7	C	8	3		(09)	Ø3
82	7	C	8	4		(12)	Ø4
83	7	D	Ø	1	4SNL	(04)	Ø1
84	7	D	Ø	2		(06)	Ø2
85	7	D	Ø	3		(09)	Ø3
86	7	D	Ø	4		(12)	Ø4
87	7	D	8	1	4OSL	(04)	Ø1
88	7	D	8	2		(06)	Ø2
89	7	D	8	3		(09)	Ø3
90	7	D	8	4		(12)	Ø4
91	7	E	Ø	1	4ONL	(04)	Ø1
92	7	E	Ø	2		(06)	Ø2
93	7	E	Ø	3		(09)	Ø3
94	7	E	Ø	4		(12)	Ø4
95	7	E	8	1	4SSS	(02)	Ø1
						(06)	Ø2

(FILE 15) DDF63

	(SOFT CODE)						
97	7	E	8	3		(11)	Ø3
98	7	E	8	4		(12)	Ø4
99	7	F	Ø	1	4OSS	(02)	Ø1
100	7	F	Ø	2		(06)	Ø2
101	7	F	Ø	3		(11)	Ø3
102	7	F	Ø	4		(12)	Ø4
103	7	F	8	1	4SNS	(03)	Ø1
104	7	F	8	2		(12)	Ø2

FIG. 14

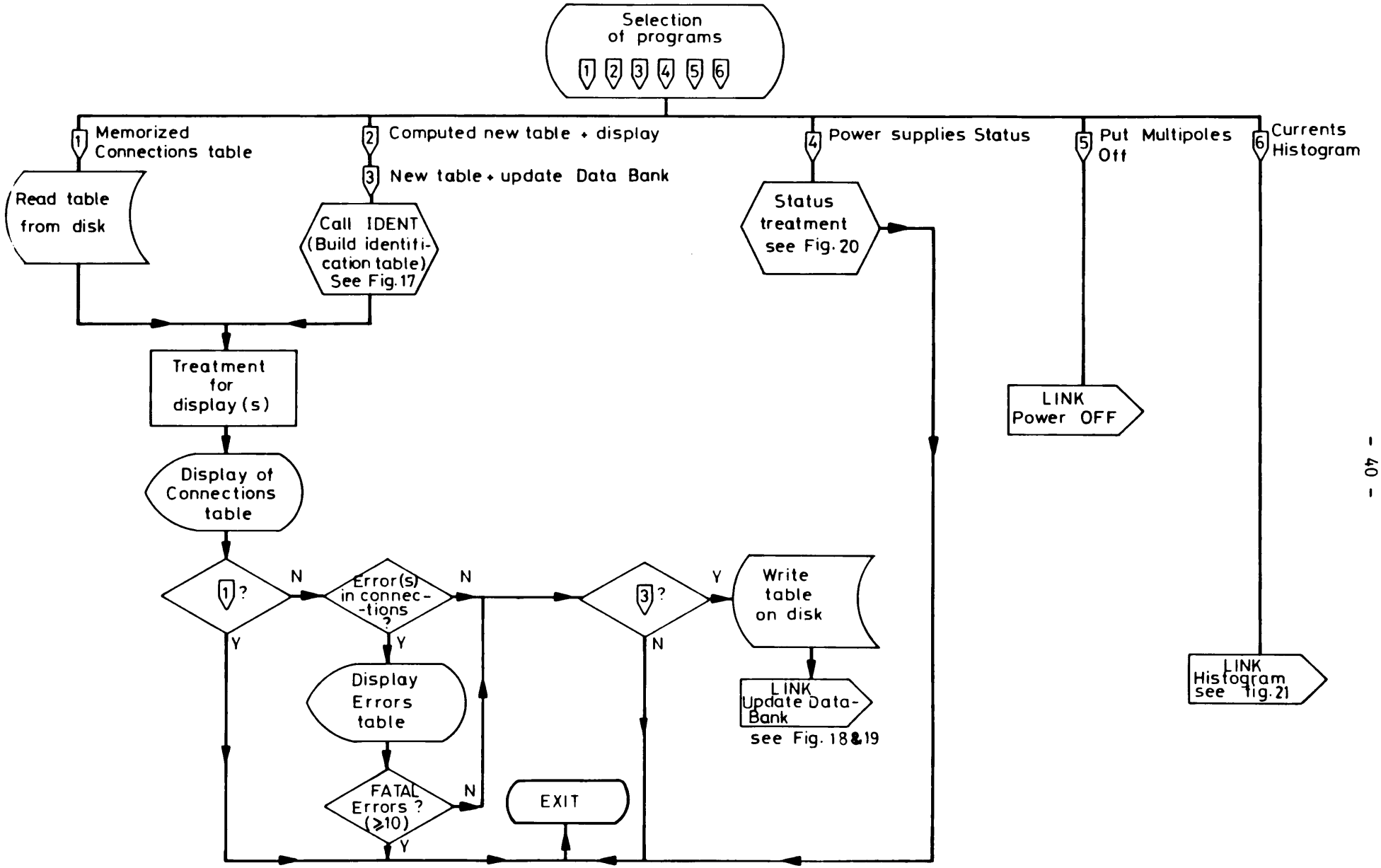
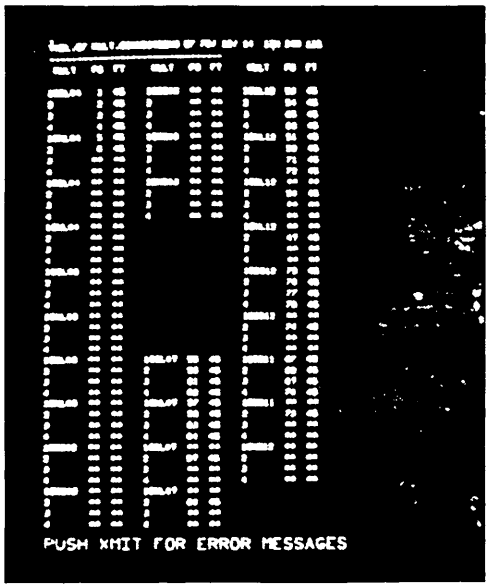
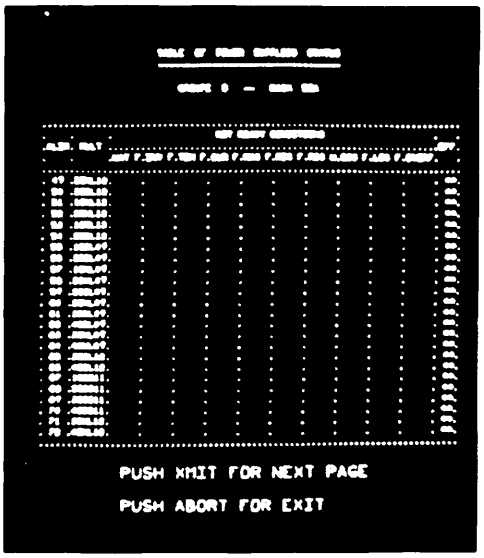


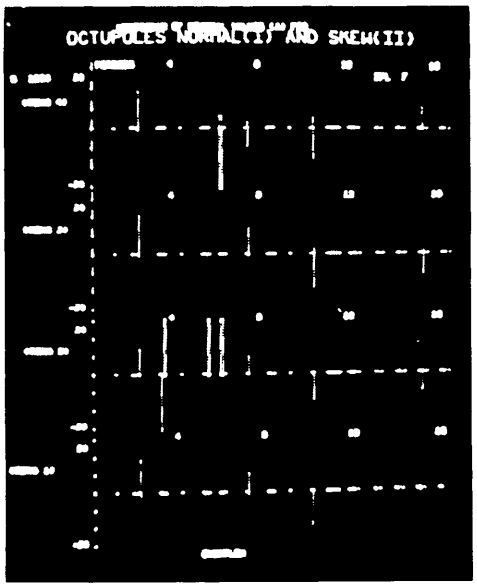
FIG. 15. NEW MULTIPOLES PROGRAM (BST 19 on P.R.U)



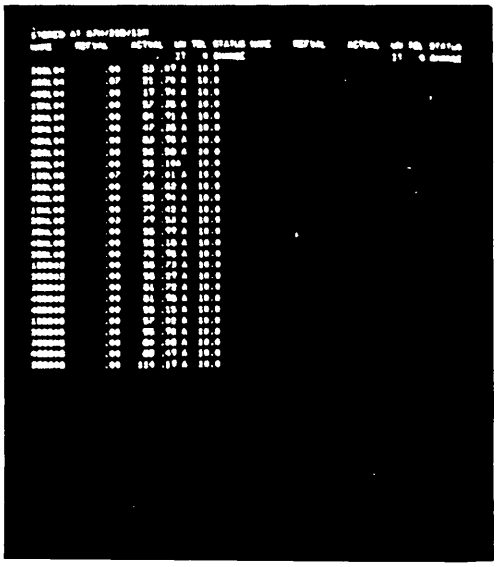
a) Connection Table Display



b) Status Display



c) Current Histogram Display



d) Varilog Display

Fig 16

PS= POWER SUPPLY NUMBER
FT= VARIAN FUNCTION NUMBER
NM= MULTIPOLE NUMBER

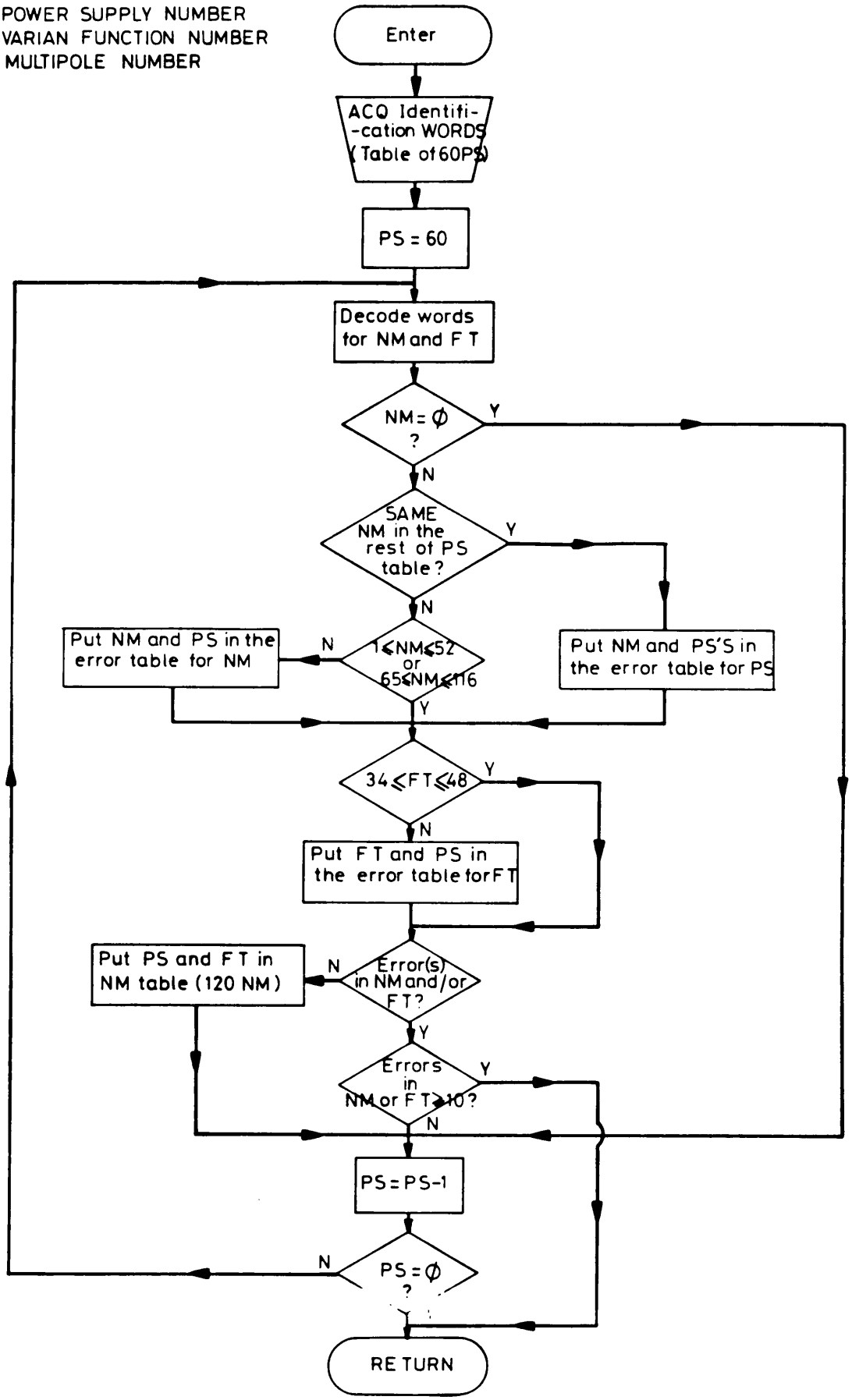


FIG. 17 "IDENT" subroutine

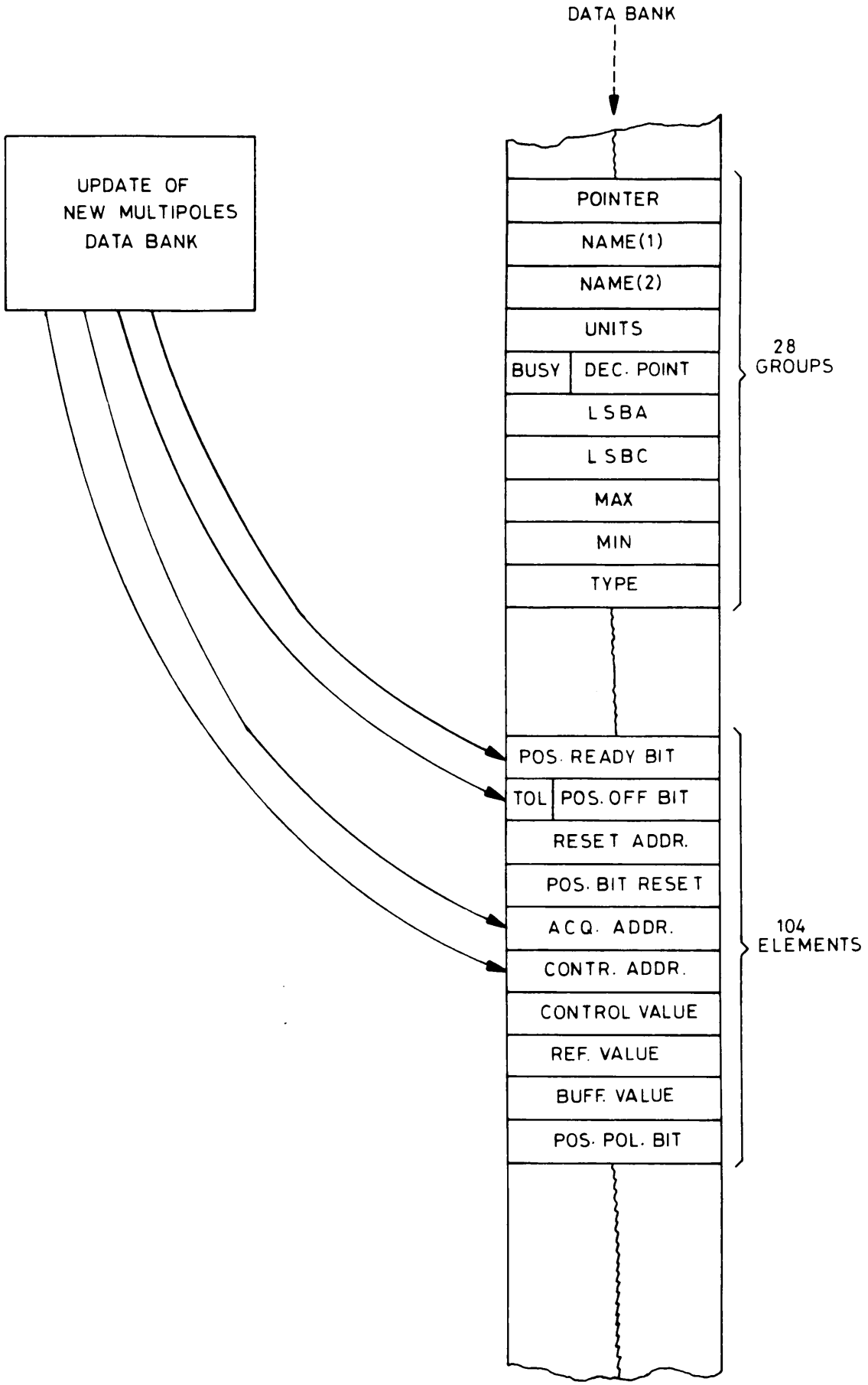
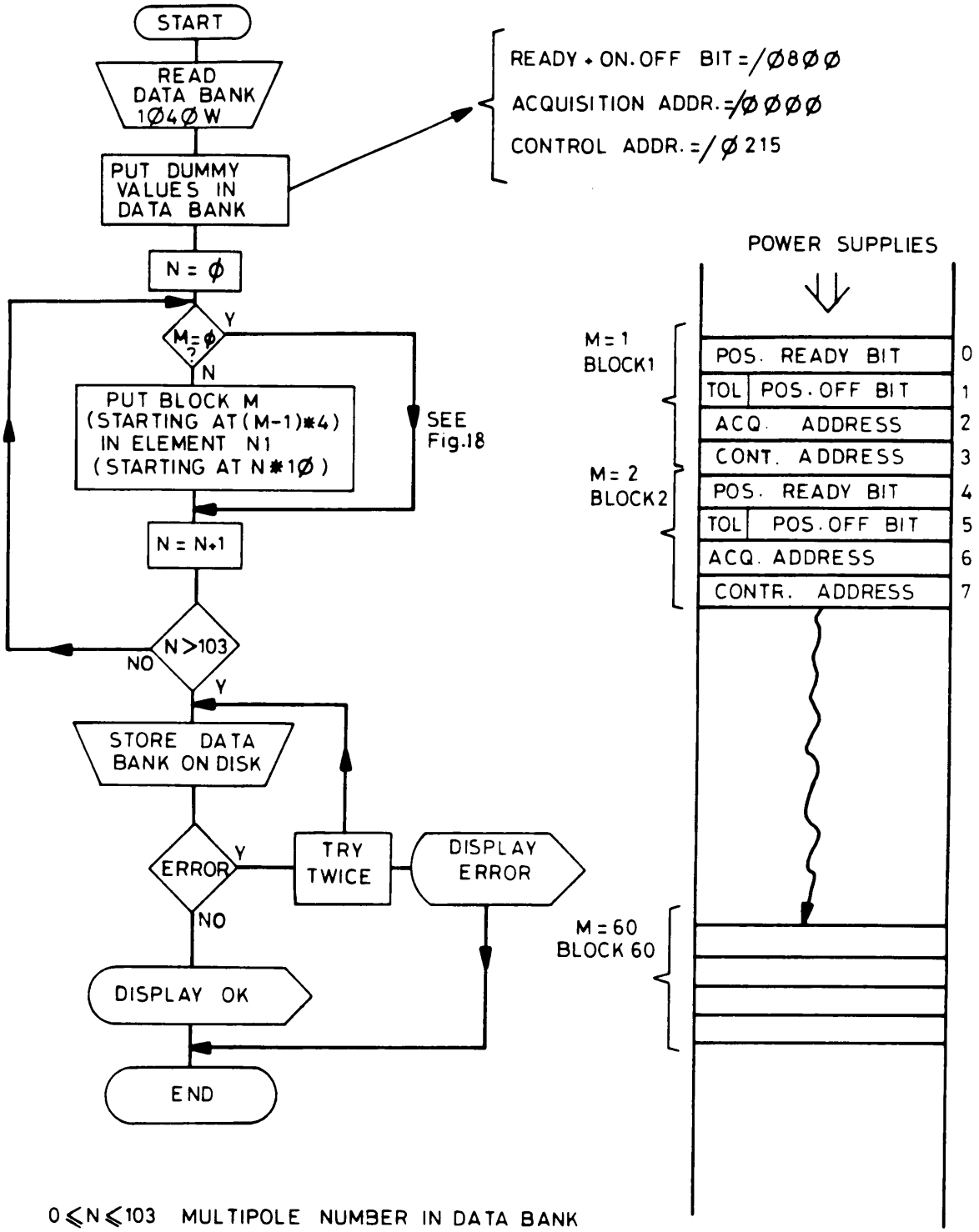


FIG. 18. DATA BANK UPDATING



$0 \leqslant N \leqslant 103$ MULTIPOLE NUMBER IN DATA BANK

$1 \leqslant M \leqslant 60$ POWER SUPPLY NUMBER (Ø = NOT CONNECTED)

FIG. 19. UPDATE DATA BANK

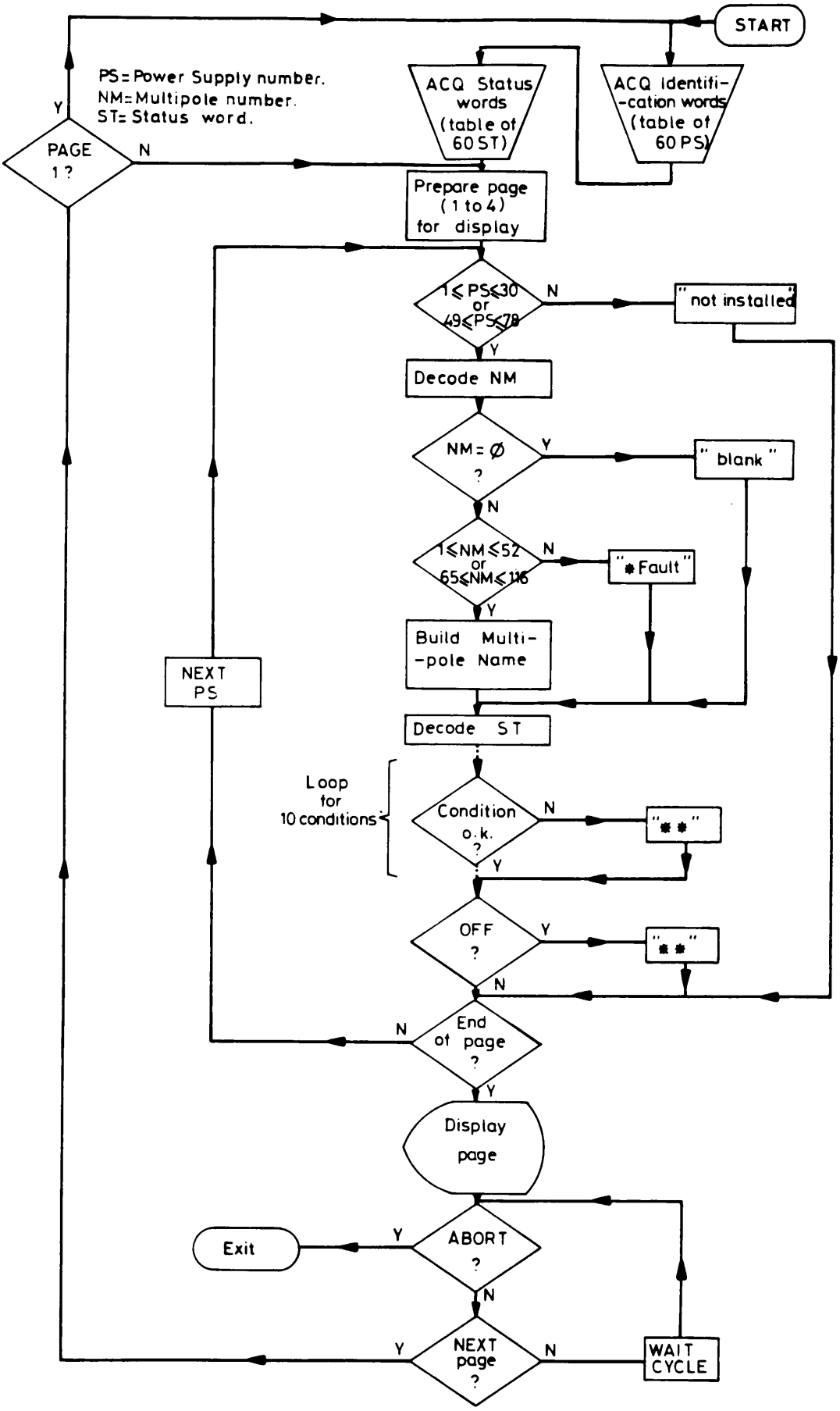


FIG. 20. STATUS DISPLAY

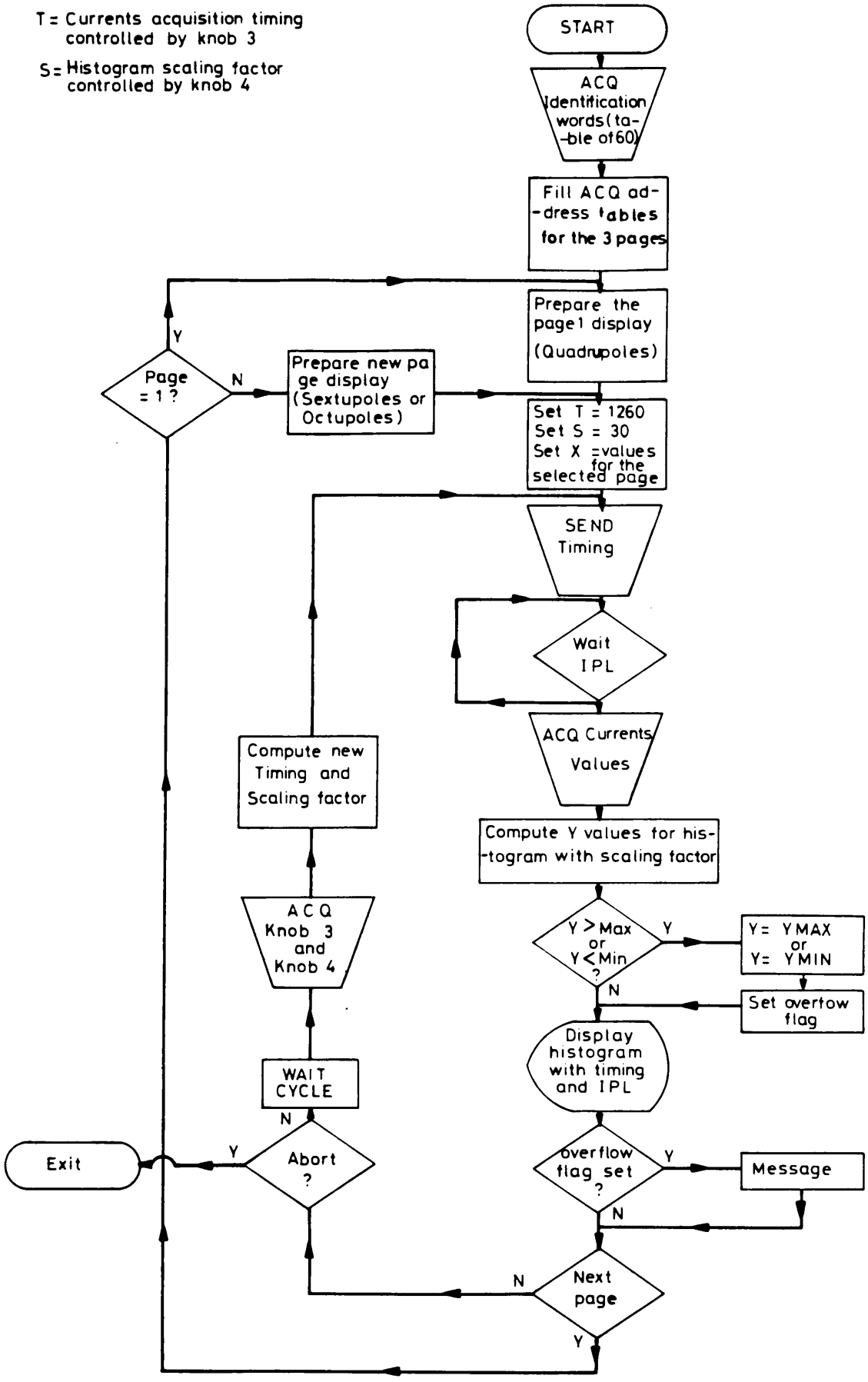


FIG. 21. CURRENT HISTOGRAM

Table A1

Addresses STAR A for STAR-CAMAC controller-SC1-BAT 17																
Sub-address	N_1	N_2	N_3	N_4	N_5	N_6	N_7	N_8	N_9	N_{10}	N_{11}	N_{12}	N_{13}	N_{14}	N_{15}	N_{16}
A_0									/0940	/0948	/0950	/0958	/0960	/0968	/0970	/0978
A_1									/4940	/4948	/4950	/4958	/4960	/4968	/4970	/4978
A_2									/0941	/0949	/0951	/0959	/0961	/0969	/0971	/0979
A_3									/4941	/4949	/4951	/4959	/4961	/4969	/4971	/4979
A_4									/0942	/094A	/0952	/095A	/0962	/096A	/0972	/097A
A_5									/4942	/494A	/4952	/495A	/4962	/496A	/4972	/497A
A_6									/0943	/094B	/0953	/095B	/0963	/096B	/0973	/097B
A_7									/4943	/494B	/4953	/495B	/4963	/496B	/4973	/497B
A_8									/0944	/094C	/0954	/095C	/0964	/096C	/0974	/097C
A_9									/4944	/494C	/4954	/495C	/4964	/496C	/4974	/497C
A_{10}									/0945	/094D	/0955	/095D	/0965	/096D	/0975	/097D
A_{11}									/4945	/494D	/4955	/495D	/4965	/496D	/4975	/497D
A_{12}									/0946	/094E	/0956	/095E	/0966	/096E	/0976	/097E
A_{13}									/4946	/494E	/4956	/495E	/4966	/496E	/4976	/497E
A_{14}									/0947	/094F	/0957	/095F	/0967	/096F	/0977	/097F
A_{15}									/4947	/494F	/4957	/495F	/4967	/496F	/4977	/497F

Table A2

Addresses STAR C for STAR-CAMAC controller-SC1-BAT 17																
Sub-address	N_1	N_2	N_3	N_4	N_5	N_6	N_7	N_8	N_9	N_{10}	N_{11}	N_{12}	N_{13}	N_{14}	N_{15}	N_{16}
A_0	/6880	/6884	/6888	/688C	/6890	/6894	/6898	/689C	/68A0	/68A4	/68A8	/68AC	/68B0	/68B4	/68B8	/68BC
A_1	/2880	/2884	/2888	/288C	/2890	/2894	/2898	/289C	/28A0	/28A4	/28A8	/28AC	/28B0	/28B4	/28B8	/28BC
A_2	/4880	/4884	/4888	/488C	/4890	/4894	/4898	/489C	/48A0	/48A4	/48A8	/48AC	/48B0	/48B4	/48B8	/48BC
A_3	/0880	/0884	/0888	/088C	/0890	/0894	/0898	/089C	/08A0	/08A4	/08A8	/08AC	/08B0	/08B4	/08B8	/08BC
A_4	/6881	/6885	/6889	/688D	/6891	/6895	/6899	/689D	/68A1	/68A5	/68A9	/68AD	/68B1	/68B5	/68B9	/68BD
A_5	/2881	/2885	/2889	/288D	/2891	/2895	/2899	/289D	/28A1	/28A5	/28A9	/28AD	/28B1	/28B5	/28B9	/28BD
A_6	/4881	/4885	/4889	/488D	/4891	/4895	/4899	/489D	/48A1	/48A5	/48A9	/48AD	/48B1	/48B5	/48B9	/48BD
A_7	/0881	/0885	/0889	/088D	/0891	/0895	/0899	/089D	/08A1	/08A5	/08A9	/08AD	/08B1	/08B5	/08B9	/08BD
A_8	/6882	/6886	/688A	/688E	/6892	/6896	/689A	/689E	/68A2	/68A6	/68AA	/68AE	/68B2	/68B6	/68BA	/68BE
A_9	/2882	/2886	/288A	/288E	/2892	/2896	/289A	/289E	/28A2	/28A6	/28AA	/28AE	/28B2	/28B6	/28BA	/28BE
A_{10}	/4882	/4886	/488A	/488E	/4892	/4896	/489A	/489E	/48A2	/48A6	/48AA	/48AE	/48B2	/48B6	/48BA	/48BE
A_{11}	/0882	/0886	/088A	/088E	/0892	/0896	/089A	/089E	/08A2	/08A6	/08AA	/08AE	/08B2	/08B6	/08BA	/08BE
A_{12}	/6883	/6887	/688B	/688F	/6893	/6897	/689B	/689F	/68A3	/68A7	/68AB	/68AF	/68B3	/68B7	/68BB	/68BF
A_{13}	/2883	/2887	/288B	/288F	/2893	/2897	/289B	/289F	/28A3	/28A7	/28AB	/28AF	/28B3	/28B7	/28BB	/28BF
A_{14}	/4883	/4887	/488B	/488F	/4893	/4897	/489B	/489F	/48A3	/48A7	/48AB	/48AF	/48B3	/48B7	/48BB	/48BF
A_{15}	/0883	/0887	/088B	/088F	/0893	/0897	/089B	/089F	/08A3	/08A7	/08AB	/08AF	/08B3	/08B7	/08BB	/08BF

Table A3

Addresses STAR A for STAR-CAMAC controller-SC2-BAT 60																
Sub-address	N_1	N_2	N_3	N_4	N_5	N_6	N_7	N_8	N_9	N_{10}	N_{11}	N_{12}	N_{13}	N_{14}	N_{15}	N_{16}
A_0									/0980	/0988	/0990	/0998	/09A0	/09A8	/09B0	/09B8
A_1									/4980	/4988	/4990	/4998	/49A0	/49A8	/49B0	/49B8
A_2									/0981	/0989	/0991	/0999	/09A1	/09A9	/09B1	/09B9
A_3									/4981	/4989	/4991	/4999	/49A1	/49A9	/49B1	/49B9
A_4									/0982	/098A	/0992	/099A	/09A2	/09AA	/09B2	/09BA
A_5									/4982	/498A	/4992	/499A	/49A2	/49AA	/49B2	/49BA
A_6									/0983	/098B	/0993	/099B	/09A3	/09AB	/09B3	/09BB
A_7									/4983	/498B	/4993	/499B	/49A3	/49AB	/49B3	/49BB
A_8									/0984	/098C	/0994	/099C	/09A4	/09AC	/09B4	/09BC
A_9									/4984	/498C	/4994	/499C	/49A4	/49AC	/49B4	/49BC
A_{10}									/0985	/098D	/0995	/099D	/09A5	/09AD	/09B5	/09BD
A_{11}									/4985	/498D	/4995	/499D	/49A5	/49AD	/49B5	/49BD
A_{12}									/0986	/098E	/0996	/099E	/09A6	/09AE	/09B6	/09BE
A_{13}									/4986	/498E	/4996	/499E	/49A6	/49AE	/49B6	/49BE
A_{14}									/0987	/098F	/0997	/099F	/09A7	/09AF	/09B7	/09BF
A_{15}									/4987	/498F	/4997	/499F	/49A7	/49AF	/49B7	/49BF

Table A4

Addresses STAR C for STAR-CAMAC controller-SC2-BAT 60																
Sub-address	N_1	N_2	N_3	N_4	N_5	N_6	N_7	N_8	N_9	N_{10}	N_{11}	N_{12}	N_{13}	N_{14}	N_{15}	N_{16}
A_0	/68C0	/68C4	/68C8	/68CC	/68D0	/68D4	/68D8	/68DC	/68E0	/68E4	/68E8	/68EC	/68F0	/68F4	/68F8	/68FC
A_1	/28C0	/28C4	/28C8	/28CC	/28D0	/28D4	/28D8	/28DC	/28E0	/28E4	/28E8	/28EC	/28F0	/28F4	/28F8	/28FC
A_2	/48C0	/48C4	/48C8	/48CC	/48D0	/48D4	/48D8	/48DC	/48E0	/48E4	/48E8	/48EC	/48F0	/48F4	/48F8	/48FC
A_3	/08C0	/08C4	/08C8	/08CC	/08D0	/08D4	/08D8	/08DC	/08E0	/08E4	/08E8	/08EC	/08F0	/08F4	/08F8	/08FC
A_4	/68C1	/68C5	/68C9	/68CD	/68D1	/68D5	/68D9	/68DD	/68E1	/68E5	/68E9	/68ED	/68F1	/68F5	/68F9	/68FD
A_5	/28C1	/28C5	/28C9	/28CD	/28D1	/28D5	/28D9	/28DD	/28E1	/28E5	/28E9	/28ED	/28F1	/28F5	/28F9	/28FD
A_6	/48C1	/48C5	/48C9	/48CD	/48D1	/48D5	/48D9	/48DD	/48E1	/48E5	/48E9	/48ED	/48F1	/48F5	/48F9	/48FD
A_7	/08C1	/08C5	/08C9	/08CD	/08D1	/08D5	/08D9	/08DD	/08E1	/08E5	/08E9	/08ED	/08F1	/08F5	/08F9	/08FD
A_8	/68C2	/68C6	/68CA	/68CE	/68D2	/68D6	/68DA	/68DE	/68E2	/68E6	/68EA	/68EE	/68F2	/68F6	/68FA	/68FE
A_9	/28C2	/28C6	/28CA	/28CE	/28D2	/28D6	/28DA	/28DE	/28E2	/28E6	/28EA	/28EE	/28F2	/28F6	/28FA	/28FE
A_{10}	/48C2	/48C6	/48CA	/48CE	/48D2	/48D6	/48DA	/48DE	/48E2	/48E6	/48EA	/48EE	/48F2	/48F6	/48FA	/48FE
A_{11}	/08C2	/08C6	/08CA	/08CE	/08D2	/08D6	/08DA	/08DE	/08E2	/08E6	/08EA	/08EE	/08F2	/08F6	/08FA	/08FE
A_{12}	/68C3	/68C7	/68CB	/68CF	/68D3	/68D7	/68DB	/68DF	/68E3	/68E7	/68EB	/68EF	/68F3	/68F7	/68FB	/68FF
A_{13}	/28C3	/28C7	/28CB	/28CF	/28D3	/28D7	/28DB	/28DF	/28E3	/28E7	/28EB	/28EF	/28F3	/28F7	/28FB	/28FF
A_{14}	/48C3	/48C7	/48CB	/48CF	/48D3	/48D7	/48DB	/48DF	/48E3	/48E7	/48EB	/48EF	/48F3	/48F7	/48FB	/48FF
A_{15}	/08C3	/08C7	/08CB	/08CF	/08D3	/08D7	/08DB	/08DF	/08E3	/08E7	/08EB	/08EF	/08F3	/08F7	/08FB	/08FF

APPENDIX 2

CONTROL AND ACQUISITION FORMATS

	BIT	NAME	SPECIFICATIONS
LSB	1	$2^0 = 1$	
	2	$2^1 = 2$	
	3	$2^2 = 4$	
	4	$2^3 = 8$	
	5	$2^4 = 16$	10 BIT WORD = ABSOLUTE VALUE OF THE MULTIPLIER
	6	$2^5 = 32$	
	7	$2^6 = 64$	
	8	$2^7 = 128$	
	9	$2^8 = 256$	
	10	$2^9 = 512$	
	11		
	12		
	13		
	14		
	15	ON / OFF	CONTROLS THE STATE OF THE POWER SUPPLY
MSB	16	SIGN	CONTROLS THE STATE OF THE POLARITY REVERSAL SYSTEM

TRANSMITTED ON CAMAC ADDRESSES AND FUNCTION

A(0,5) . F(16) ON FIRST CRATE
A(8,13) . F(16) ON SECOND CRATE
} CONNECTED TO THE SAME TRANSCEIVER

FIG. A1 MEMORY CONTROL WORD (ONE SUCH WORD PER POWER SUPPLY)

	BIT	NAME	SPECIFICATIONS
LSB	1	C.O.K.	CONNECTION O.K. (CONTINUITY TEST)
	2	I D 1	8 BIT WORD FOR MULTIPOLE IDENTIFICATION (0→255 POSSIBILITIES FOR FUTURE EXTENSION)
	3	I D 2	
	4	I D 3	
	5	I D 4	
	6	I D 5	
	7	I D 6	
	8	I D 7	
	9	I D 8	
	10		DON'T CARE
	11	A F 1	6 BIT WORD FOR ANALOGUE FUNCTION IDENTIFICATION (0→63 POSSIBILITIES 0 = NO CONNECTION AT ALL)
	12	A F 2	
	13	AF 3	
	14	AF 4	
	15	A F 5	
MSB	16	AF 6	

CAMAC ACQUISITION

a) HOLD MODE
A(0,5). F(12) FOR FIRST CRATE
A(8,13). F(12) FOR SECOND CRATE
} CONNECTED TO THE SAME TRANSCEIVER

b) NORMAL MODE
A(0,5). F(12) + A(0,5). F(0) FOR FIRST CRATE
A(8,13). F(12) + A(8,13). F(0) FOR SECOND CRATE
} CONNECTED TO THE SAME TRANSCEIVER

FIG. A2 IDENTIFICATION WORD (ONE PER POWER SUPPLY)

	BIT	NAME	SPECIFICATIONS
LSB	1	WAT F	WATER COOLING FAULT
	2	INV F	INVERTER FAULT
	3	TEM F	TEMPERATURE FAULT
	4	CUR F	CURRENT FAULT
	5	MAG F	MAGNET FAULT
	6	REC F	RECTIFIER FAULT
	7	REC W	RECTIFIER WARNING (ϵ REF TO HIGH)
	8	DCC F	DC CONNECTOR FAULT
	9	LOC C.	LOCAL CONTROL
	10	OVER F	OVERFLOW (REF OF THE REGULATOR 'S HARD WIRED LIMITAT. IN THE REGULATOR)
	11		
	12		
	13		
	14		
	15		
MSB	16	READY	SUM OF ALL STATUS BITS

CAMAC ACQUISITION

HOLD { A(0,5).F(4) FIRST CRATE
A(8,13).F(4) SECOND CRATE

NORMAL { A(0,5).F(28) + A(0,5).F(4) FIRST CRATE
A(8,13).F(28) + A(8,13).F(4) SECOND CRATE

FIG. A3 REGULATOR STATUS WORD (ONE SUCH WORD PER POWER SUPPLY)

	BIT	NAME	SPECIFICATIONS
LSB	1	RDY 1	
	2	RDY 2	
	3	RDY 3	6 READY BITS
	4	RDY 4	
	5	RDY 5	
	6	RDY 6	
	7		
	8		
	9	ON/OFF 1	
	10	ON/OFF 2	
	11	ON/OFF 3	6 ON/OFF BITS
	12	ON/OFF 4	
	13	ON/OFF 5	
	14	ON/OFF 6	
	15		
MSB	16	WARNING RECTIFIER	

CAMAC ACQUISITION
A(6).F(0) FOR FIRST CRATE
A(14).F(0) FOR SECOND CRATE

FIG. A4 READY/ON/OFF STATUS WORD
(ONE SUCH STATUS WORD PER CIM CRATE)

	BIT	NAME	SPECIFICATIONS	
LSB	1	RDY 1		
	2	RDY 2		
	3	RDY 3		8BIT WORD UNDER SURVEILLAN-
	4	RDY 4		-CE BY 64 LS
	5	RDY 5		
	6	RDY 6		
	7	PS ON	POWER SUPPLY ON	
	8	PSF	POWER SUPPLY MONITOR	
	9			
	10			
	11			
	12			
	13			
	14			
	15			
MSB	16			

CAMAC ACQUISITION

HOLD | A(6) . F(1) First Crate
A(14) . F(1) Second Crate

NORMAL | A(6) · F(14)+ A(6) F(1) First Crate
A(14) · F(14)+ A(6) F(1) Second Crate

FIG. A5 CRATE EQUIPMENT MONITORING CONFIGURATION

APPENDIX 3

TRANSCEIVER MODULE AND INTERCONNECTION BUS FUNCTIONS

LIST OF ALL CAMAC FUNCTIONS PERFORMED BY THE TRANSCEIVER MODULE

Without HOLD option (switch OFF) the following pair of commands are needed:

F(12) A(0-5) F(0) A(0-5)	Read Q=1 — identification word CRATE 1, power supply module 1 to 6.
F(12) A(6) F(0) A(6)	Read Q=1 — ready on/off status word in CRATE 1
F(12) A(8-13) F(0) A(8-13)	Read Q=1 — identification word CRATE 2, power supply module 1 to 6
F(12) A(14) F(0) A(14)	Read Q=1 — ready on/off status word in CRATE 2
F(14) A(0-5) F(1) A(0-5)	Read Q=1 — test word CRATE 1, power supply module 1 to 6
F(14) A(6) F(1) A(6)	Read Q=1 — crate status word CRATE 1
F(14) A(8-13) F(1) A(8-13)	Read Q=1 — test word in CRATE 2 of power supply module 1 to 6
F(14) A(14) F(1) A(14)	Read Q=1 — crate status word CRATE 2
F(28) A(0-5) F(4) A(0-5)	Read Q=1 — status word in CRATE 1 of power supply module 1 to 6
F(28) A(8-13) F(4) A(8-13)	Read Q=1 — status word in CRATE 2 of power supply module 1 to 6
F(30) A(0-5) F(6) A(0-5)	Read Q=1 — memory in CRATE 1 of power supply module 1 to 6
F(30) A(0-5) F(6) A(0-5)	Read Q=1 — memory in CRATE 2 of power supply module 1 to 6

With HOLD option (switch ON) the following commands are needed for reading

F(0) A(0-5) Q = 1 Read identification word in CRATE 1 of power supply module 1 to 6

F(0) A(6) Q = 1 Read ready on/off status word in CRATE 1

F(0)	A(8-13)	Q = 1	Read identification word in CRATE 2 of power supply module 1 to 6
F(0)	A(14)	Q = 1	Read ready on/off status word in CRATE 2
F(1)	A(0-5)	Q = 1	Read test word in CRATE 1 of power supply module 1 to 6
F(1)	A(6)	Q = 1	Read crate status word CRATE 1
F(1)	A(8-13)	Q = 1	Read test word in CRATE 2 of power supply module 1 to 6
F(1)	A(14)	Q = 1	Read crate status word CRATE 2
F(4)	A(0-5)	Q = 1	Read status word in CRATE 1 of power supply module 1 to 6
F(4)	A(8-13)	Q = 1	Read status word in CRATE 2 of power supply module 1 to 6
F(6)	A(0-5)	Q = 1	Read memory in CRATE 1 of power supply module 1 to 6
F(6)	A(8-13)	Q = 1	Read memory in CRATE 2 of power supply module 1 to 6

The following commands are independent of HOLD option.

F(16)A(0-5)S1	Q = 1	Write memory in CRATE 1 of power supply module 1 to 6
F(16)A(6)S1	Q = 1	Reset power failure circuit in CRATE 1
F(16)A(8-13)S1	Q = 1	Write memory in CRATE 2 of power supply module 1 to 6
F(16)A(14)S1	Q = 1	Reset power failure circuit in CRATE 2
F(2)A(15)	Q = 1	Read TRANSCEIVER module states R1 on if connection to CRATE OK R2 on if connection to CRATE OK R3 on if HOLD option is ON.

INTERCONNECTION BUS FUNCTIONS

DATAWAY SIGNALS (pos. logic)						CAMAC function	Encoded function code			COMMENT
$\overline{N}$	$\overline{F1}$	$\overline{F2}$	$\overline{F4}$	$\overline{F8}$	$\overline{F16}$		CR1	CR2	CCW	
0	1	1	1	1	1	F(0)	1	0	0	Read IDENTIFICATION WORD
0	0	1	1	1	1	F(1)	0	0	0	Read DIGITAL TEST WORD
0	1	0	1	1	1	F(2)	-	-	-	Read TRANSCEIVER MODULE STATUS WORD
0	1	1	0	1	1	F(4)	0	1	0	Read REGULATOR STATUS WORD
0	1	0	0	1	1	F(6)	1	1	0	Read MEMORY CONTROL WORD
0	1	1	0	0	1	F(12)	1	0	0	Transfer IDENTIFICATION WORD
0	1	0	0	0	1	F(14)	0	0	0	Transfer DIGITAL TEST WORD
0	1	1	1	1	1	F(16)	X	X	1	Write MEMORY CONTROL WORD
0	1	0	1	0	0	F(28)	0	1	0	Transfer REGULATOR STATUS WORD
0	1	1	0	0	0	F(30)	1	1	0	Transfer MEMORY CONTROL WORD

```
1                       ;       **** MULTIPOLE MICROPROCESSOR VARILOG ****
 2                      ;
 3                      ;               BY DR. P J HORNE  (23/11/76)
 4                      ;
 5                      ;
 6                      ;       PROGRAMME TO MONITOR THE POWER SUPPLIES FOR THE MULTIPOLES
 7                      ;       COMPUTING THE AREA UNDER EACH OF THE CURVES DURING EACH
 8                      ;       BOOSTER CYCLE.
 9                      ;
10                      ;       FREQUENCY OF TWO PHASE CLOCK =2.2MHZ (460NS PERIOD)
11                      ;       EXECUTION TIME OF PROGRAMME = 700MS
12                      ;
13                      ;       30 16 BIT RESULTS ARE AVAILABLE AFTER THE PROGRAMME HAS
14                      ;       FINISHED AND A 31ST BYTE WHICH ACTS AS A STATUS REGISTER
15                      ;       SUCH THAT IF BIT 8 IS SET AN ERROR HAS OCCURED, EITHER
16                      ;       DUE TO  TOO MANY INTERRUPTS OR AN HARDWARE FAULT.
17                      ;       IF BIT ONE IS SET AN ERROR OCCURED DUE TO A HIGH USE OF
18                      ;       CAMAC BY THE MAIN COMPUTER DURING THE BOOSTER CYCLE, THUS
19                      ;       INTERRUPTING THE TASK TOO MANY TIMES FOR THE RESULTS TO BE
20                      ;       VALID.
21                      ; BEGIN (1)
22   C008                       ATOD    EQU     0C008H  ;NAF FOR A/D
23   00AF                       TOOBIG  EQU     0AFH    ;DELAY THRESHOLD
24   0473                       STATUS  EQU     473H    ;STATUS WORD
25   0472                       DC      EQU     472H    ;FOR DELAY COUNT
26   0478                       INCMPX  EQU     478H    ;TEMPORARY STORE
27   E004                       MPX1    EQU     0E004H  ;NAF FOR MULTIPLEXER
28   E005                       MPX2    EQU     0E005H  ;MULTIPLEXER 2
29   E006                       MPX3    EQU     0E006H  ;MULTIPLEXER 3
30   0500                       STACK   EQU     500H    ;TOP OF STACK
31   0000                       MCSR    EQU     0H      ;CONTROL AND STATUS REGISTER
32   0002                       HIGHBY  EQU     02H     ;CAMAC REGITER HIGH BYTE
33   0001                       LOWBYT  EQU     01H     ;CAMAC REGISTER LOW BYTE
34   0003                       CAMCOM  EQU     03H     ;'NAF' REGISTER (CAMAC COMMAND)
35   0400                       DATA    EQU     400H    ;START OF DATA BLOCK
36   0474                       EOB     EQU     474H    ;END OF DATA BLOCK
37   043C                       EOTB    EQU     43CH    ;END OF TRANSFER BLOCK FOR RESULTS
38   047A                       TEMP    EQU     47AH    ;TEMPORARY STORE FOR H-L PAIR
39                      ;
40                      ;
41                      ;
42   0000                       ORG 0
43                      ;
44                      ;       POWER UP THROUGH HERE AND INTERRUPT THROUGH ADD. 08H
45                      ;       (RST 1) FOR EITHER A CAMAC B OR THE BUSY SIGNAL & THROUGH
46                      ;       018H (RST 3) FOR STBI.
47                      ;
48   0000 C32000                JMP 20H             ;START PROGRAMME
49   0008                       ORG 8H
50   0008 C34400                JMP INTSUB          ;INTERRUPT SUBROUTINE
51   0018                       ORG 18H
52   0018 219F00                LXI H,START         ;STBI INTERRUPT
53   001B E3                    XTHL
54   001C C9                    RET
55                      ;
56                      ;       INITIALISATION SEQUENCE
57                      ;       TEST TO SEE IF BUSY SIGNAL IS ENABLED (MAY BE DUE TO CABLE
58                      ;       NOT BEING IN PLACE) AND LOOP UNTILL NOT SET, IF SET THE SET
59                      ;       ERROR BIT IN STATUS WORD
60                      ; BEGIN (2)
61   0020                       ORG 20H
62   0020 310005                LXI SP,STACK
63   0023 2104F2                LXI H,0F204H        ;INC MPX1 CAMAC COMMAND
64   0026 227804                SHLD INCMPX         ;SAVE AT TEMPORARY ADDRESS
65   0029 217304                LXI H,STATUS
66   002C 3603                  MVI M,03H           ;SET 'COMPUTING NOT FINISHED' &
67                      ;                           ERROR BITS
68   002E DB00          TESTB:  IN MCSR             ;READ MCSR
69   0030 E608                  ANI 8H              ;IS BUSY BIT SET
```

```
 70   0032 CA3A00           JZ NOTSET
 71   0035 3683             MVI M,83H       ;SET ERROR BIT IN STATUS WORD
 72   0037 C32E00           JMP TESTB       ;LOOP UNTILL NOT BUSY
 73   003A 7E       NOTSET: MOV A,M         ;GET STATUS
 74   003B E67F             ANI 7FH         ;CLEAR 'BUSY' BIT
 75   003D 77               MOV M,A         ;SAVE STATUS
 76   003E 3E00             MVI A,0H
 77   0040 D300             OUT 0H          ;MASK OFF INTERRUPT FROM BUSY & B(CAMAC)
 78   0042 FB               EI              ;ENABLE INTERRUPT
 79   0043 76               HLT             ;WAIT FOR INTERRUPT
 80                 ; END (2)
 81                 ;
 82                 ;       INTERRUPT SUBROUTINE
 83                 ;
 84                 ; BEGIN (3)
 85   0044 217204   INTSUB: LXI H,DC        ;POINTER TO DELAY COUNT
 86   0047 DB00             IN MCSR         ;READ MCSR
 87   0049 E608             ANI 8H          ;IS BUSY BIT SET
 88   004B CA5600           JZ TESTC        ;NO
 89   004E 34       LO7:    INR M           ;INCREMENT DELAY COUNT
 90   004F DB00             IN MCSR         ;READ MCSR
 91   0051 E608             ANI 08H
 92   0053 C24E00           JNZ LO7         ;LOOP UNTILL NOT SET
 93                 ;
 94                 ;       THIS LOOP TESTS THE VALUE OF REGISTER 'C', THE
 95                 ;       NEW MULTIPLEXER SETTING, AND RESETS THE MULTIPLEXERS TO
 96                 ;       THIS VALUE
 97                 ;       AS THERE ARE THREE MULTIPLEXERS ONE MUST FIRST FIND WHICH
 98                 ;       MULTIPLEXER IS IN USE (I.E ADDRESS (IN REG C) 0-15=MPX1,
 99                 ;       16-31=MPX2, 32-38=MPX3) AND THEN RESET THIS MULTIPLEXER TO
100                 ;       THE CORRECT VALUE WITH THE OTHER TWO AT ZERO AND DISABLED
101                 ;       (BY WRITING TO ONE MULTIPLEXER THE OTHER TWO ARE AUTOMATICALLY
102                 ;       RESET AND DISABLED). ONE MUST ALSO CHANGE THE INCMPX COMMAND,
103                 ;       IF NECESSARY, TO THE NEXT MULTIPLEXER.
104                 ;
105                 ;
106   0056 3E00     TESTC:  MVI A,0H
107   0058 D302             OUT HIGHBY      ;CLEAR W(2)
108   005A 79               MOV A,C         ;GET C
109   005B D610             SUI 10H         ;IS 0<C=<15
110   005D FA7100           JM L1           ;JMP IF C<16
111   0060 D610             SUI 10H         ;IS C=<31
112   0062 FA8400           JM L2           ;JUMP IF C<32
113   0065 21F2F2           LXI H,0F2F8H    ;N(5)A(0)F(25), @ MPX3
114   0068 227804           SHLD INCMPX     ;SAVE @ ADDRESS INCMPX
115   006B 2106E0           LXI H,MPX3
116   006E C37A00           JMP RESET
117                 ;
118                 ;       0<C<=15
119                 ;
120   0071 2104E0   L1:     LXI H,MPX1      ;MPX1:- CAMAC WRITE (N(4)A(0)F(16))
121   0074 79               MOV A,C
122   0075 FE0F             CPI 0FH         ;IS IT = 14
123   0077 CC9800           CZ SET16        ;CALL SET16 IF = 15
124   007A D301     RESET:  OUT LOWBYT      ;
125   007C 77               MOV M,A         ;LOAD N,A,F REGISTER
126   007D D303             OUT CAMCOM      ;DO CAMAC DATWAY CYCLE
127   007F 21D600           LXI H,CAMAC     ;RESET RETURN ADDRESS
128   0082 E3               XTHL            ;PUSH ON STACK
129   0083 C9               RET             ;RETURN FROM INTERRUPT
130                 ;
131                 ;       15<C<=31
132                 ;
133   0084 79       L2:     MOV A,C         ;GET C
134   0085 D610             SUI 10H         ;C=C-16
135   0087 FE0F             CPI 0FH
136   0089 CC9800           CZ SET16
137   008C 2105F2           LXI H,0F205H    ;N(5)A(0)F(25) @ MPX2
138   008F 227804           SHLD INCMPX     ;SAVE @ ADDRESS INCMPX
```

```
0092 2105E0           LXI H,MPX2      ;TO ADDRESS MPX2
0095 C37A00           JMP RESET       ;RESET MULTIPLEXERS
                ;
                ;       THIS ROUTINE IS TO SET EITHER MPX1 OR MPX2 TO ADDRESS 14
                ;       WITH THE ENABLE BIT SET (BIT 16). THIS SETTING IS DIFFERENT
                ;       TO ALL OTHER INTERRUPT RESET CASES DUE TO PECULIARITIES
                ;       IN THE MULTIPLEXER HARDWARE.
                ;
0098 3E80       SET16:  MVI A,80H       ;TO SET BIT 16 OF MPX'S
009A D302               OUT HIGHBY
009C 3E0E               MVI A,0EH       ;NEW MPX ADDRESS
009E C9                 RET
                ;       END(3)
                ;
                ;
                ;       MAIN SECTION OF PROGRAMME
                ;       MULTIPOLES ARE SAMPLED 128 TIMES DURING ONE BOOSTER CYCLE
                ;       AND THE AREA UNDER EACH CURVE (FEEDBACK FROM THE POWER SUPPLY)
                ;       CALCULATED AND STORED IN MEMORY LOCATIONS 400H -- 43BH (THERE
                ;       ARE 30 POWER SUPPLIES). EACH RESULT IS A SIXTEEN BIT WORD
                ;       AND LOCATION 43CH IS A STATUS WORD WITH BIT '0' SET IF THE
                ;       RESULTS ARE INVALID DUE TO TOO MANY INTERRUPTS DURING ONE CYCLE
                ;
                ; BEGIN (4)
009F 063A       START:  MVI B,3AH       ;CLEAR MEMORY LOCATION LOOP
00A1 317404             LXI SP,E0B
00A4 1600               MVI D,0H
00A6 1E00               MVI E,0H
00A8 D5         LO1:    PUSH D
00A9 05                 DCR B
00AA C2A800             JNZ LO1         ;END OF LOOP
00AD 3E03               MVI A,03H       ;FOR ERROR BITS IN STATUS BYTE
00AF 217304             LXI H,STATUS    ;POINT H-L AT STATUS BYTE
00B2 77                 MOV M,A         ;SET ERROR BITS IN STATUS BYTE
00B3 3E01               MVI A,1H
00B5 D300               OUT 0H          ;ENABLE INTERRUPT FROM BUSY AND B(CAMAC)
                ;
                ;
                ;       THIS BLOCK CONTAINS ALL THE CAMAC DATAWAY OPERATIONS
                ;       THUS THE INTERRUPT SYSTEM IS ENABLED AND DISABLES BEFORE
                ;       AND AFTER DATAWAY OPERATIONS
                ;
00B7 310005             LXI SP,STACK    ;RESET STACK
00BA 0640               MVI B,40H       ;NUMBER OF SAMPLES
00BC 3E00       CAMA:   MVI A,0H        ;CLEAR ACCUMULATOR
00BE D301               OUT LOWBYT      ;CLEAR P(1)
00C0 D302               OUT HIGHBY
00C2 2104F2             LXI H,0F204H    ;RESET TO MPX1
00C5 227804             SHLD INCMPX     ;SAVE
00C8 2104E0             LXI H,MPX1
00CB 77                 MOV M,A         ;LOAD 'NAF' REGISTER
00CC D303               OUT CAMCOM      ;DO CAMAC DATAWAY COMMAND
00CE 0E00               MVI C,0H        ;FOR POWER SUPPLY NUMBER
                ;
                ;       THIS FOLLOWING SUBLOCK IS REPEATED 36 TIMES, AND SCANS ALL
                ;       THE POWER SUPPLIES TO OBTAIN THE SAMPLES.  ADDRESS VALUES
                ;       6,7,14 AND 15 FOR THE FIRST TWO MULTIPLEXERS ARE INVALID, BUT
                ;       ARE SCANNED FOR EASE OF PROGRAMMING.  HOWEVER ADDRESS 6 SHOULD
                ;       GIVE A ZERO (+/- 1BIT) RESULT AND CAN THEREFORE BE USED TO
                ;       TEST THE EQUIPMENT STATUS.
                ;
00D0 210004             LXI H,DATA      ;DATA POINTER
00D3 227A04             SHLD TEMP       ;SAVE H-L
00D6 FB         CAMAC:  EI
00D7 2A7804             LHLD INCMPX     ;GET CAMAC COMMAND
00DA 77                 MOV M,A         ;LOAD INTO 'NAF' REGISTER
00DB D303               OUT CAMCOM      ;START DATAWAY OPERATION
00DD 2108C0             LXI H,ATOD      ;GET CAMAC A/D READ COMMAND
00E0 77                 MOV M,A         ;LOAD 'NAF'
```

```
00E1 D303               OUT CAMCOM      ;DO OPERATION
00E3 F3                 DI
00E4 DB01               IN LOWBYT       ;READ W(1)
00E6 5F                 MOV E,A         ;SAVE IN REGISTER E
00E7 DB02               IN HIGHBY       ;READ W(2)
00E9 57                 MOV D,A         ;SAVE IN REGISTER D
                ;
                ;       TRIPLE ADD LOOP
                ;
00EA 2A7A04             LHLD TEMP       ;GET H-L
00ED 7B                 MOV A,E
00EE 86                 ADD M           ;GET PREVIOUS RESULT
00EF 77                 MOV M,A         ;SAVE NEW RESULT
00F0 23                 INX H           ;NEXT LOCATION
00F1 7A                 MOV A,D         ;NEW DATA IN A
00F2 8E                 ADC M           ;ADD PREVIOUS RESULT WITH CARRY
00F3 77                 MOV M,A         ;STORE RESULT
00F4 23                 INX H           ;NEXT ADDRESS
00F5 D2F900             JNC L04         ;IS CARRY SET
00F8 34                 INR M           ;YES THEN INCREMENT MEMORY
00F9 23         L04:    INX H           ;
00FA 227A04             SHLD TEMP       ;SAVE H-L
                ;       TEST LOOP COUNTS C AND B
                ;
00FD 0C                 INR C           ;POWER SUPPLY COUNT
00FE 79                 MOV A,C         ;SAVE
00FF FE26               CPI 26H         ;IS IT = 38
0101 C2D600             JNZ CAMAC
0104 05                 DCR B           ;SAMPLE COUNT
0105 CA0B01             JZ L8
0108 C34101             JMP DELAY       ;TIMING FOR CORRECT SAMPLE RATE
010B 217204     L8:     LXI H,DC        ;DELAY COUNT (DUE TO INTERRUPTS)
010E 7E                 MOV A,M
010F 3E00               MVI A,0H
0111 D300               OUT 0H          ;MASK OFF INTERRUPT FROM BUSY AND B (CAMAC)
0113 D6AF               SUI TOOBIG      ;
0115 FA1F01             JM NEXT
0118 217304             LXI H,STATUS    ;STATUS WORD
011B 7E                 MOV A,M         ;GET STATUS
011C C604               ADI 04H         ;SET 'DELAY ERROR' BIT
011E 77                 MOV M,A         ;SAVE STATUS
011F CD5001     NEXT:   CALL REARR      ;SUBROUTINE TO REARRANGE DATA
0122 3E00               MVI A,0H
0124 D300               OUT 0H          ;MASK OFF INTERRUPT FROM BUSY & B(CAMAC)
0126 217304             LXI H,STATUS
0129 7E                 MOV A,M         ;GET STATUS
012A E6FC               ANI 0FCH        ;ARE THERE ANY ERROR BITS SET
012C C23401             JNZ L11         ;JUMP IF YES
012F 3E00               MVI A,0H        ;CLEAR STATUS ERROR BITS
0131 C33701             JMP L12
0134 7E         L11:    MOV A,M
0135 E6FD               ANI 0FDH        ;CLEAR END OF COMPUTATION BIT
0137 323C04     L12:    STA EOTB        ;SAVE STATUS AT NEW ADDRESS
013A 3E00               MVI A,0
013C 323D04             STA EOTB+1      ;CLEAR  HIGH BYTE
013F FB                 EI
0140 76                 HLT             ;WAIT FOR NEXT BOOSTER CYCLE
                ; END (4)
                ;       DELAY TIMING FOR SAMPLE RATE
                ;
                ; BEGIN (5)
0141 1601       DELAY:  MVI D,01H       ;CORSE ADJUST
0143 0E01       L9:     MVI C,01H       ;FINE ADJUST
0145 0D         L10:    DCR C
0146 C24501             JNZ L10
0149 15                 DCR D
014A C24301             JNZ L9
014D C3BC00             JMP CAMA
                ; END (5)
```

```
277                     ; END (1)
278                     ;
279                     ;       SUBROUTINE TO REARRANGE DATA INTO ONE BLOCK OF
280                     ;       30 (2 BYTE) WORDS WITH A 1 BYTE STATUS WORD AT THE END
281                     ;       OF THE BLOCK.  THE START OF DATA IS ADDRESS 400 (HEX)
282                     ;       OR FBFFH WHEN ADDRESSED FROM CAMAC.
283                     ;
284   0150 0605         REARR:  MVI B,05H       ;BLOCK COUNT
285   0152 210004               LXI H,DATA      ;MEM ADD. OF 24BIT DATA
286   0155 110004               LXI D,DATA      ;MEM ADD OF 16 BIT DATA(NEW RESULTS)
287   0158 0E06         LOOP2:  MVI C,6H
288   015A 23           LOOP1:  INX H           ;MISS LOW BYTE OF 3 BYTE WORD
289   015B 7E                   MOV A,M         ;GET A BYTE
290   015C 23                   INX H           ;INCREMENT ADDRESS
291   015D 12                   STAX D          ;STORE BYTE IN NEW ADDRESS
292   015E 13                   INX D           ;INCREMENT NEW ADDRESS
293   015F 7E                   MOV A,M         ;GET MSB
294   0160 12                   STAX D          ;SAVE MSB
295   0161 23                   INX H           ;INCREMENT ADDRESS
296   0162 13                   INX D           ;INC NEW ADDRESS
297   0163 0D                   DCR C
298   0164 C25A01               JNZ LOOP1
299   0167 78                   MOV A,B
300   0168 E601                 ANI 01H         ;ODD OR EVEN LOOP ?
301   016A CA7301               JZ LOOP4        ;ODD LOOP THEN JUMP
302   016D 7D                   MOV A,L         ;GET OLD MEMORY  ADDRESS
303   016E C603                 ADI 03H         ;ADD 3
304   0170 C37601               JMP LOOP5
305   0173 7D           LOOP4:  MOV A,L
306   0174 C606                 ADI 06H         ;INCREMENT ADDRESS PAST 6 USELESS BYTES
307   0176 6F           LOOP5:  MOV L,A         ;NEW ADD IN H,L
308   0177 05                   DCR B
309   0178 C25801               JNZ LOOP2       ;LOOP UNTILL DONE
310                     ;
311   017B 061D                 MVI B,01DH      ;THIS SECTION WILL SHIFT THE 16 BIT WORD
312   017D 210004               LXI H,DATA      ;RIGHT ONE LOCATION TO FORM A 15 BIT WORD
313   0180 23           LOOP3:  INX H           ;POINT TO HIGH BYTE
314   0181 37                   STC             ;SET CARRY
315   0182 3F                   CMC             ;COMPLEMENT CARRY
316   0183 7E                   MOV A,M         ;GET HIGH BYTE
317   0184 1F                   RAR             ;ROTATE BYTE THROUGH CARRY
318   0185 77                   MOV M,A         ;PUT BACK IN MEMORY
319   0186 2B                   DCX H           ;DECREMENT H-L POINTER
320   0187 7E                   MOV A,M
321   0188 1F                   RAR             ;ROTATE HIGH BYTE
322   0189 77                   MOV M,A         ;PUT BACK IN MEMORY
323   018A 23                   INX H
324   018B 23                   INX H           ;POINT TO NEXT WORD
325
326   018C 05                   DCR B
327   018D C28001               JNZ LOOP3       ;LOOP UNTILL DONE
328   0190 C9                   RET
329   0000                      END
```