

The ALICE Inner Tracker System Upgrade

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Abstract. The phase II upgrade of the Large Hadron Collider (LHC) at CERN is planned under the assumption that the LHC will progressively increase the luminosity of heavy ion beams, eventually reaching an interaction rate of about 50 kHz in Pb-Pb collisions, i.e. instantaneous luminosities of $L = 6 \times 10^{27} \text{ cm}^{-2}\text{s}^{-1}$. In this perspective, the two main ALICE tracking devices, the TPC and the Inner Tracking system (ITS) will be both upgraded to cope with the foreseen interaction rates. In particular, the various ALICE silicon detectors will be fully replaced with a new, high-resolution, multi-layered, low-material, 12500 megapixel system allowing for very high data rates, and enhancing the vertexing and tracking capabilities at low transverse momenta (p_T).

The challenge and the uniqueness of the new ALICE ITS is the very small material budget of the silicon tracker, which will be a factor 4 to 5 smaller than existing similar systems at CERN. The present article describes the design and implementation of complex and reliable assembly procedures (focusing on the detector Outer Layers) which was crucial to push the new ITS technology into production.

1. Introduction

In order to fulfill the ALICE RUN3 (2021-23) physics program, a large area silicon pixel detector with high resolution and fast readout pixel sensors was developed under the following operating conditions:

- **Material Budget:** the improvement of the tracking and vertexing performance and the impact parameter resolution at low p_T can be achieved by a significant reduction of the material budget in order to minimize multiple Coulomb scattering. Specifically, the use of extremely thin Monolithic Active Pixel Sensors (MAPS) chips [1] of $50 \mu\text{m}$ thickness at maximum for the Inner tracking Layers, closest to the interaction point, will allow a $\times 7$ reduction of the thickness in comparison to the present ALICE ITS. In addition, low power consumption and a highly optimised signal and power distribution allow for the material budget of the electrical power and signal cables to be reduced by a factor of 5. Combining these new solutions it is possible to build a detector for which the material budget per detection layer is decreased down to about 0.3% radiation lengths (X_0).
- **Intrinsic Spatial Resolution:** the tracking performance, in particular the capability to separate secondary vertices of heavy flavour decays, is determined by the impact parameter resolution. This is a convolution of the primary vertex resolution and the track pointing resolution. Specifically, the challenging intrinsic spatial resolution of $5 \mu\text{m}$ is required to reach this performance thus requiring a pixel pitch of about $30 \mu\text{m} \times 30 \mu\text{m}$ for the new ITS while the present pixel size is $50 \mu\text{m} \times 425 \mu\text{m}$.



- **Chip Dimensions:** after several years of R&D, the Tower Jazz 0.18 μm CMOS technology has been selected for the implementation of the pixel chip of the new ALICE ITS Muon Forward Tracker detectors. This allows for a maximum chip length of 30 mm in z -direction. The limitation of the chip width to 15 mm was motivated by geometrical considerations, thus a chip size of 15 mm \times 30 mm has consequently been chosen as baseline dimension for the performance studies.
- **Power Density:** the maximum tolerable material budget puts severe limitations on the amount of material that can be used for detector cooling system. The power density on the sensor has thus to be brought to a minimum and does not exceed 300 mW/cm² in order to be compatible with the cooling capability of the support structure. This in turn requires a careful design of the power distribution as well as of the read-out architecture on the chip.
- **Integration Time:** in order to cope with interaction rates of up to 50 kHz for Pb-Pb collisions and 1 MHz for p-p collisions, the maximum acceptable sensor integration time is about 30 μs in order to limit pile-up effects and the consequent loss of tracking efficiency.
- **Dead Time at 50 kHz Interaction Rate:** a maximum dead time (equivalent to data being discarded) of 10% at 50 kHz Pb-Pb interaction rate can be tolerated. Chip buffer memories and bandwidths must be dimensioned such that they can cope with the expected occupancy level.
- **Radiation Hardness:** to ensure full functionality especially for the ITS Inner Layers (IL), the pixel sensors have to be tolerant against radiation levels (expected for the innermost layer) of 2700 krad. This value includes a safety factor of 4 for a collected data set corresponding to 10 nb⁻¹ Pb-Pb and 6 nb⁻¹ p-p collisions.
- **Assembly Procedure:** the highest criticality in the assembly procedure is the manipulation of very fragile low thickness silicon detectors: 50 μm for the IL and 100 μm for the Outer and Middle Layers (OL and ML, respectively). In addition, the tracking target resolution puts stringent limits on the accuracy of the positioning of each single detecting element. The goal is to reach a geometrical placement accuracy of the individual chip in the horizontal plane of the order of 50 μm or better.

This proceeding will describe many of the technical solutions that have been developed for the new ALICE ITS [2] detector. Such a practical know-how as well as the related physics analysis, will open new perspectives in view of the new generation of many different high performance silicon detectors as well as in frontier precision for high energy experiments. In addition, this project will open a range of new opportunities for applications that benefit from a high resolution tracking system, able to operate in vacuum and within a magnetic field and in many environments, including the use of hadrons (mainly protons and carbon ions) for cancer radiation treatment.

2. Outer Layers ITS Production

The efforts to establish the ITS OL and ML detector element production increased dramatically starting from mid 2016. The infrastructures at the production sites were reorganized to cope with the requirements for the assembly and the manipulation of very fragile and low-thickness (100 μm) silicon sensors with open wire bonds.

Each so-called ITS “stave” is composed by two Half-Staves (HS) where an HS is in turn composed by 7 base modules (Hybrid Integrated Circuit, HIC) containing 2 rows of 7 ALPIDE sensors.

The ALPIDE sensors are aligned and glued to the HIC printed circuit using a custom assembly machine in the HIC production centers (Bari, Strasbourg, Liverpool, Wuhan, and Pusan) and are then bonded with three Al wire per pad to ensure redundancy against wire breaking. The wire bonds are not protected: this avoids the introduction in the detector of materials that can



Figure 1. *An OB HIC at the reception test. Center: the HIC is contained in a carrier plate which allows transport, storage, powering, testing, and vacuum gripper placement for handling. The left side of the HIC shows the so-called “tab” used to connect the sensors to the readout system. Once the HIC is qualified for alignment and gluing, the tab has to be cut as shown in the leftmost photo. Right: the two HS assembled in a stave: the sensors are glued directly on the carbon fiber strips. The blue pipes are the embedded water cooling lines (input and output). The HS are read-out by soldering an extension tab which is the interface with the outside world of the 98 ALPIDE chips. It can be clearly seen that the two HS come in different flavors (upper and lower) which have a partial longitudinal overlap requiring a definite sequence of installation.*

degrade with time but on the other hand introduces a “zero tolerance” also in case of minor mishandlings. In total an HS features 98 ALPIDE sensors (7 HICs and 7×2 chips per HIC) for a total of 51 megapixels.

The two rows of sensors are readout independently using a Master-Slave scheme: the first sensor of the row acts as a master collecting the hits from the remaining 6 slaves in addition to its own. Such a setup is suitable for the ITS OL and ML as the expected occupancies are much less than those of the inner barrel which is as close as 22 mm to the interaction point. In this case the ALPIDE sensors which make up an IL stave are readout individually to cope with much higher rates.

Before usage, the HICs have to be electronically tested for integrity using the “tab” interface shown in the left and central photos of figure 1. The high density “firefly” connectors are soldered directly on the HIC printed circuit and once the HIC is tested must be cut at the level of the pad contacts in order to make the HIC alignable.

The cut is performed using a custom high-precision cutting system which rail can run the blades only $50 \mu\text{m}$ away from the silicon sensor edges as shown in the left part of figure 1. The cut HICs possess contact pads for the CLK, CTRL, and DATA lines at both ends. At this point 7 of them can be aligned and glued (chip side facing down) on water-cooled carbon fiber strips to make the HS. The HICs have reference markers which can be aligned (using the Coordinate Measuring Machine, CMM) along the longitudinal and transverse directions with an accuracy of the order of $10 \mu\text{m}/1.5 \text{ m}$. After the alignment the HICs making up an HS must have the module-to-module interconnections soldered and the termination resistors removed (except the HIC in position 7) to enable the readout lines along the HS. Each HIC position along the HS is bit encoded by 3 resistors which are removed using soldering tweezers to program the module address.

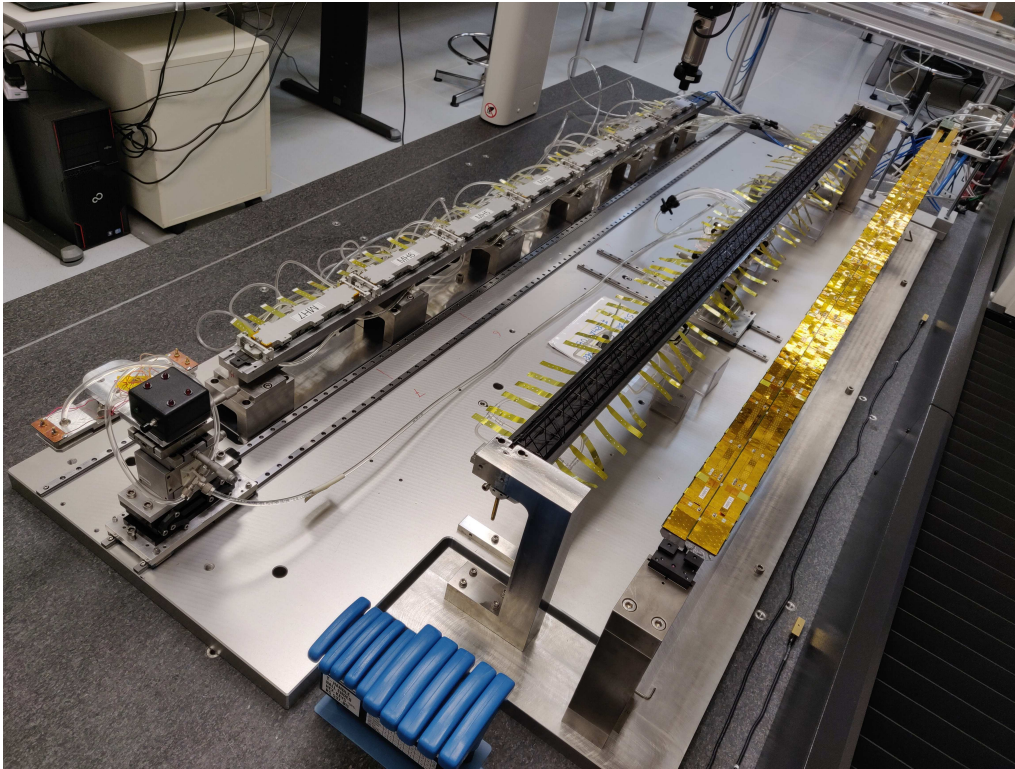


Figure 2. *Three tasks going on in parallel on the CMM jig. Station 1 on the left contains 7 HICs aligned and glued to make an HS. The vacuum grippers used to bring the HICs from the carrier plates to the gluing position can be seen as they are removed only when the Araldite 2011 glue has cured. Station 2 (in the middle) contains an already finished stave ready to be moved in the “gray area” for the installation of the PB and BB, and their folding. Station 3 on the right contains a finished stave, with the PB and BB already folded, for the final metrology.*

As mentioned above, two HS are needed to make a stave. The HS come also in two flavors: upper and lower and they must be glued to the carbon fiber support frame (Space Frame, SF) in the sequence (upper, lower) as there is a small overlap between them as shown in the right part of figure 1. The produced stave is then moved out from the CMM jig to the soldering station of the power distribution lines (Power Bus - PB - and Bias Bus - BB) and for additional electronic testing.

The CMM jig has three stations: station 1 is used to perform the HIC alignment and gluing for an HS of given flavor, while the second station is used to align and glue an already soldered HS to the support structure (SF). The third station is used to validate the finished stave metrologically before and after the installation and folding of the power and bias distribution lines as shown in figure 2.

Once the stave is assembled it is moved into the station for the installation of the power distribution system and the final tests. The two HS have separate powering called PB(BB)-U and PB(BB)-L and their relative filter boards, where L stands for lower and U stands for upper. The assembly of PB, BB, and filter board is soldered on a custom jig where the required ceramic capacitors (Murata GRM 220 μF) are first soldered to the PB. The position of soldering defines if the PB is of U or L type. The amount of tin that has to be used to solder the capacitors must be carefully controlled in order to avoid the introduction of extra thickness which can cause

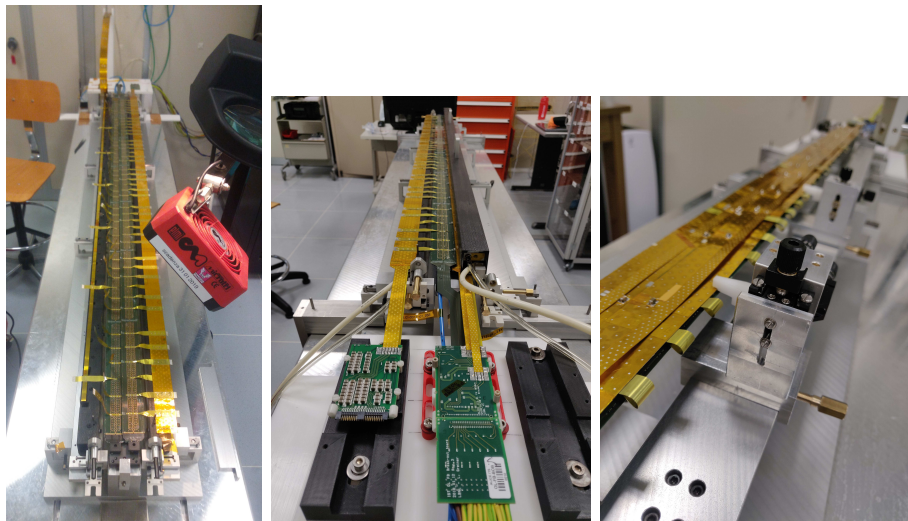


Figure 3. *The left photo shows a stave on the folding jig with the power and bias bus distributions ships ready for soldering on the handling bars. The upper PB is rolled out to allow the soldering of the BB to the corresponding HIC cross cables. Once the BB is soldered, the PB is lowered to be soldered to the remaining cross cables. The center figure shows a PB+BB assembly rotated and inserted into the U-arms of the upper half stave (keep in mind that the HS is upside-down in this position) with the filter board connected to the break-out board from the power board. In this position the HS is tested to make sure no bonds were damaged by the folding procedure. The carbon fiber handling bar is removed if the test is successful. The right photo shows the two PB+BB systems folded and the insertion of the remaining (smaller) U-arms to lock the busses into position.*

mechanical interferences once the stave is inserted into the half barrel support. The folding jig has two handling bars which can hold the PB and BB stripes in place using suction cups. These bars are fixed to the jig by means of special pivots screws which can first rotate, then step down and slide. The upper PB+BB assembly has to be inserted between the HS-U and HS-L inside special holders glued on the HS called U-arms. More U-arms are put after the folding to ensure the PB+BB system cannot move and is kept at an appropriate distance from the bonds underneath.

The stave is finally inserted into an aluminum box which is in turn closed with an envelope to keep the relative humidity under control. The Al box is inserted in a wooden box which has a suspension system to minimize mechanical shocks during the transport. The temperature must be also controlled and it shall never drop below 15° during the transport.

The production started early in 2018 and reached a sustained rate of 0.7 stave/week. The present production yield is 91% (fraction of detector grade HS).

In conclusion, the ITS Outer Layers and Middle Layers production has successfully started and ramped up in all OL (Daresbury, Frascati, Nikhef, and Torino) and ML (Berkeley) sites and is proceeding at a good rate and 95% yield. The present production rate will ensure that all the needed staves will be at CERN on time for the ITS surface commissioning (the ITS Inner Barrel construction is already finished) and for installation in the ALICE cavern during the summer of 2020.

3. References

- [1] M. Šuljić, ALPIDE: the Monolithic Active Pixel Sensor for the ALICE ITS upgrade, 2018 *Nuovo Cimento C* **41** 91
- [2] Technical Design Report for the Upgrade of the ALICE Inner Tracking System, 2014 *J. Phys. G: Nucl. Part. Phys.* **41** 087002