EUROPEAN ORGANISATION FOR NUCLEAR RESEARCH

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Project : LPI
Domain : CONTROLS
Category: LAYOUT
Status : FINAL

LEP PREINJECTOR (LPI)

19 MHZ FAST TIMING SYSTEM

TECHNICAL REFERENCE MANUAL

PAUL SCHENKELS

Abstract

Description of the Fast Timing System for the LEP PreInjector.(LPI). The LPI Fast Timing System is responsible for the pulsing of the LEP Injector Linacs (LIL) and the injection and ejection system of EPA .
This paper is a detailed technical description of the system.

Geneva Switzerland

TABLE OF CONTENTS

Section Page

Section Page

1 INTRODUCTION

This paper is a more detailed description of the LPI 19 MHz Fast Timing System. The main issues are the hardware layout and the interconnections, description of the individual used modules and the functional description of the hardware and software of the LPI timing sequencer (IKBOX).

This reference manual is used as the blueprint for the installation of the LPI 19 MHz Fast Timing System.

It is also intended as a technical reference manual of the system. The main users of this manual will be the PS/CO exploitation specialists.

More information on the functionality of the timing system can be found in 3 other notes : 1) Options for an LPI Timing layout PS/CO/WP 85-014, 2) Le Timing Central PS/CO/Note 86-5 and 3) LPI Fast Timing Sequencer and datatable Editor PS/CO/Note 86-009.

To keep this reference up to date, this manual has to be updated for every modification made to the system. The source of this manual can be found under <PRDEV>(LPI-DOC)FAST-TIMING-DOC:TEXT

CHAPTER 2

GENERAL LAYOUT

2 GENERAL LAYOUT

2.1 DESCRIPTION

The LPI Fast Timing system can be divided into 3 parts : Injection Timing, Ejection Timing and Instrumentation Timing.

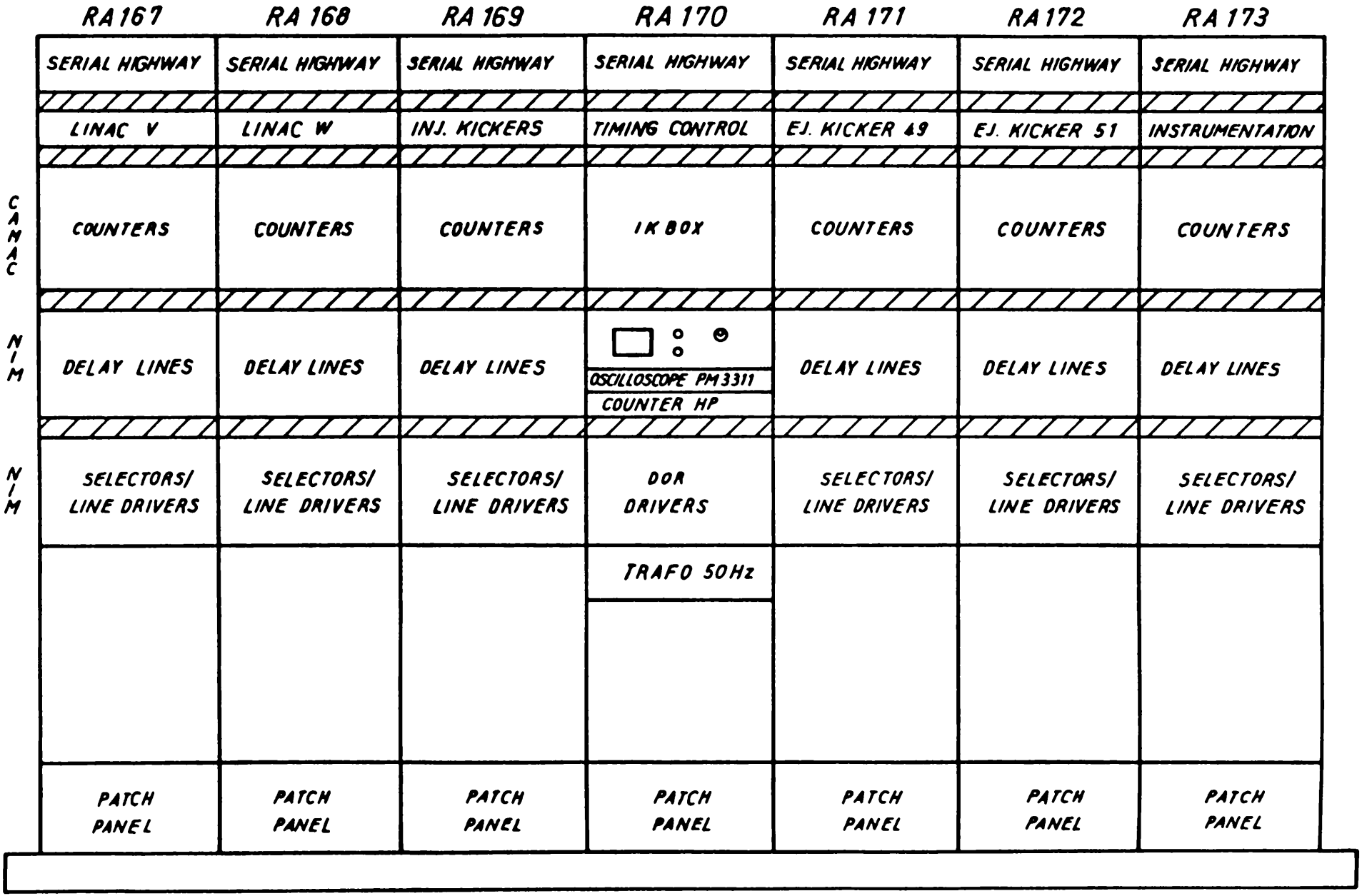
These 3 subsystems are controlled by the Timing Control system (Clock Generators and IKBOX).

The Injection Timing is the susbsystem which provides timings every 10 ms for the 2 Linacs and the 4 injection kickers.

The Ejection Timing generates timings for the ejection kickers and the ejection septum once for every ejection started by HX.WEJ.

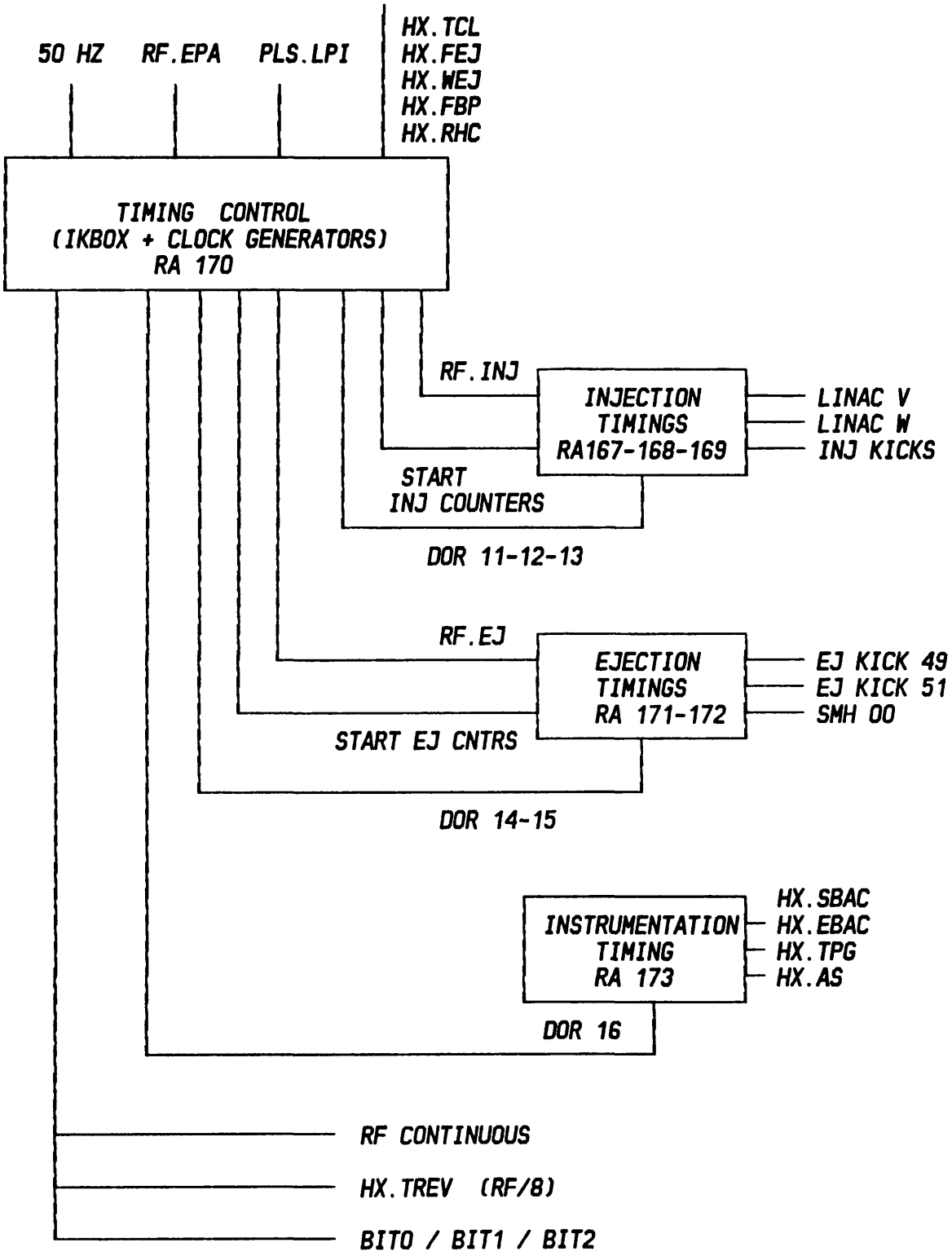
The general layouts of the different subsystems are shown in the following paragraphs and the more detailed layouts and cabling schemes are described in the following chapters (one chapter per subsystem).

Chapter 10 gives general descriptions of the different modules used to implement the system.

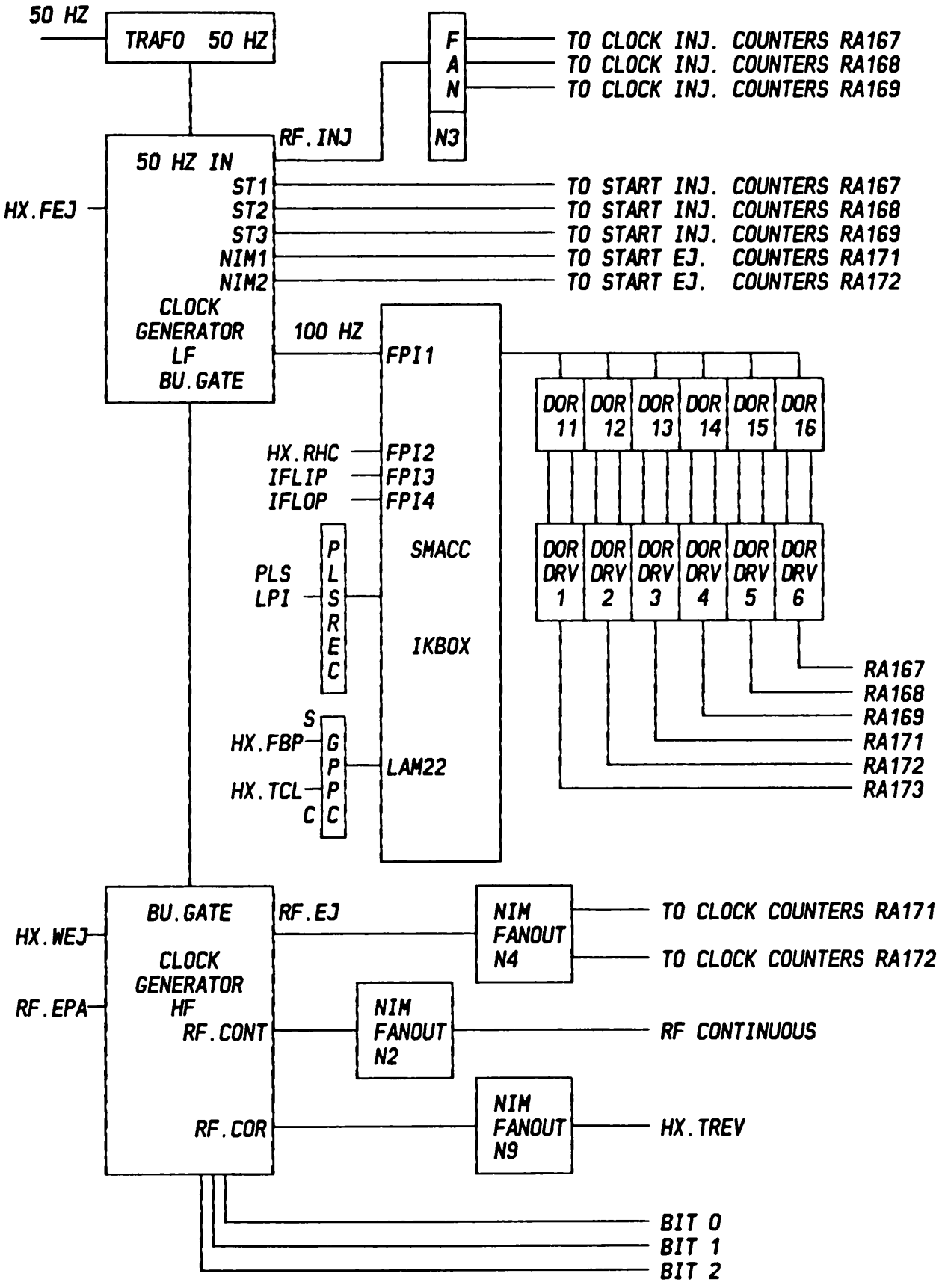


GENERAL RACK LAYOUT

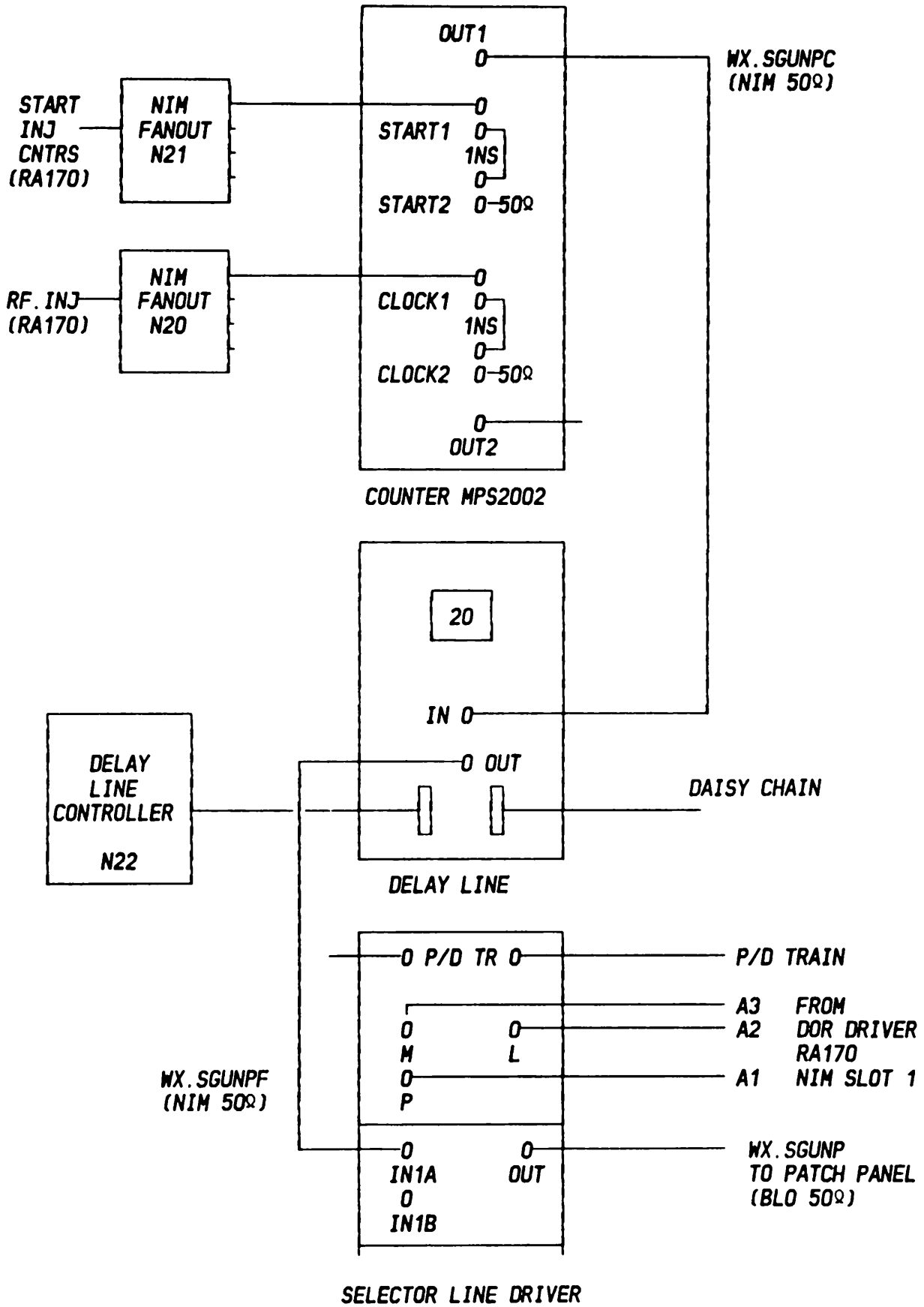
2.1.2 LPI FAST TIMING : GENERAL OVERVIEW



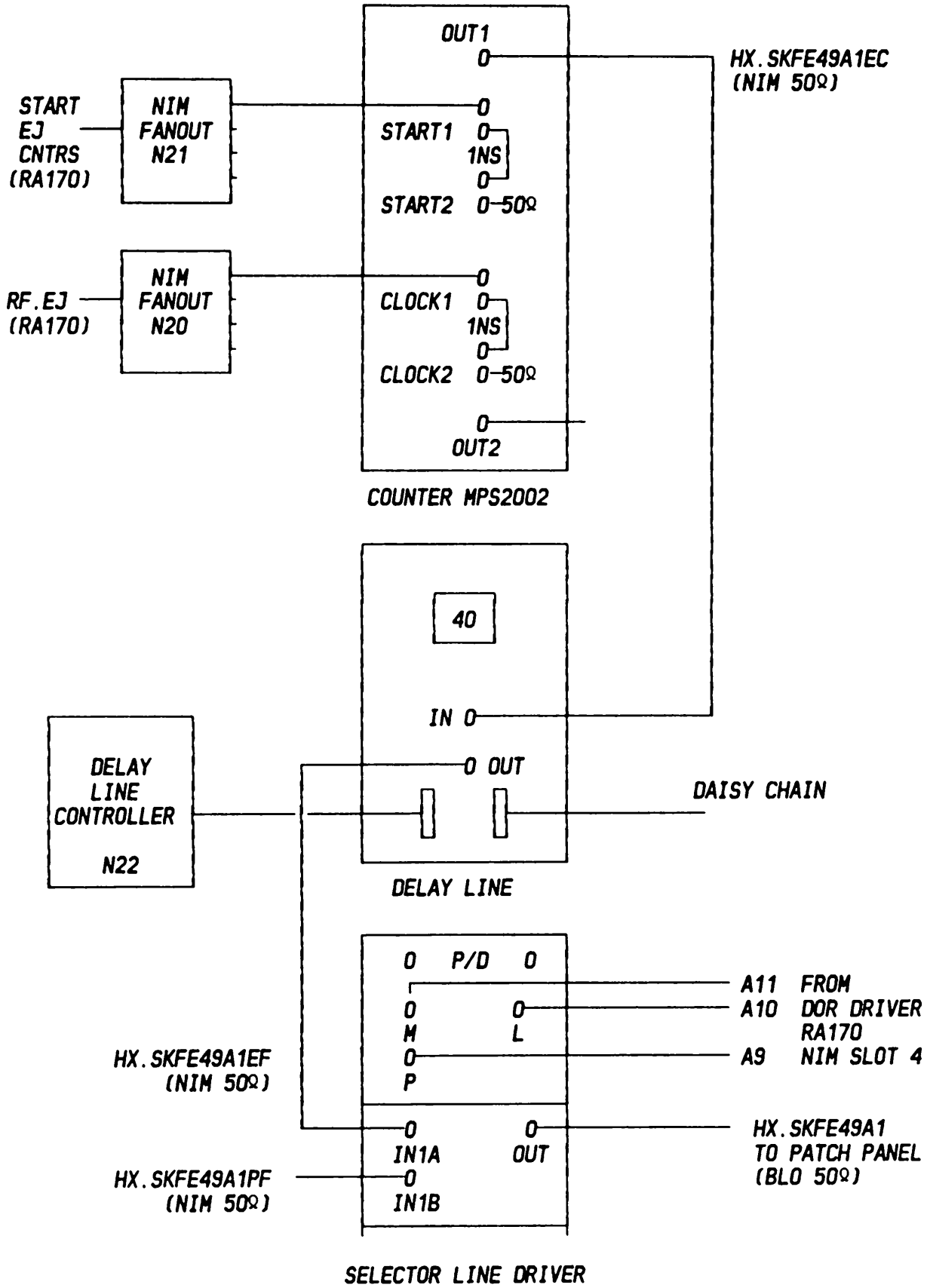
2.1.3 TIMING CONTROL RA 170



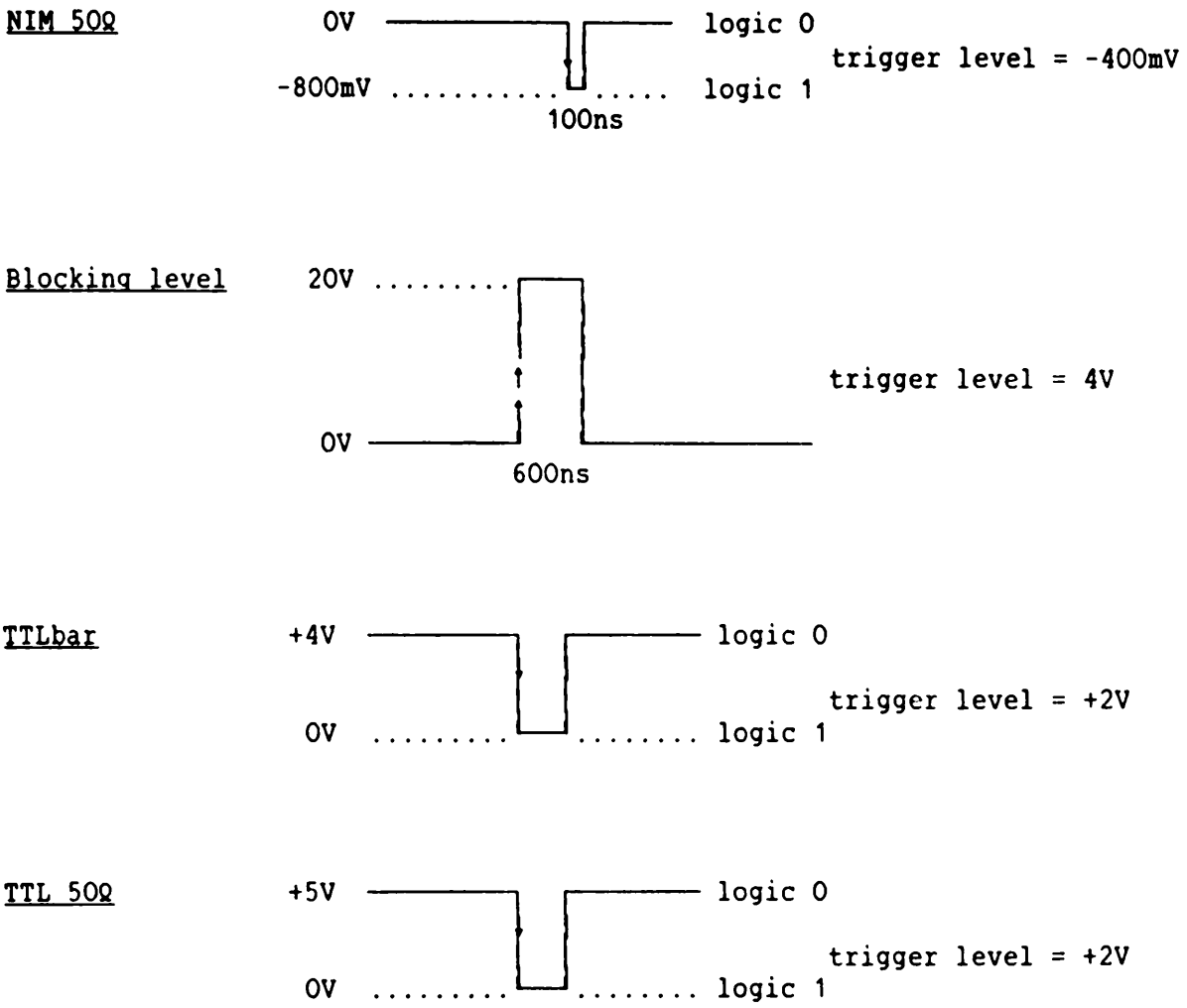
2.1.4 INJECTION TIMING (EXAMPLE WX.SGUNP)



2.1.5 EJECTION TIMING (EXAMPLE HX.SKFE49A1)



2.1.6 SIGNAL LEVELS



WARNING

If a 50Ω signal is not appropriately terminated with 50Ω, the voltage will be doubled in most cases. This may damage the input circuits if these are not well protected.

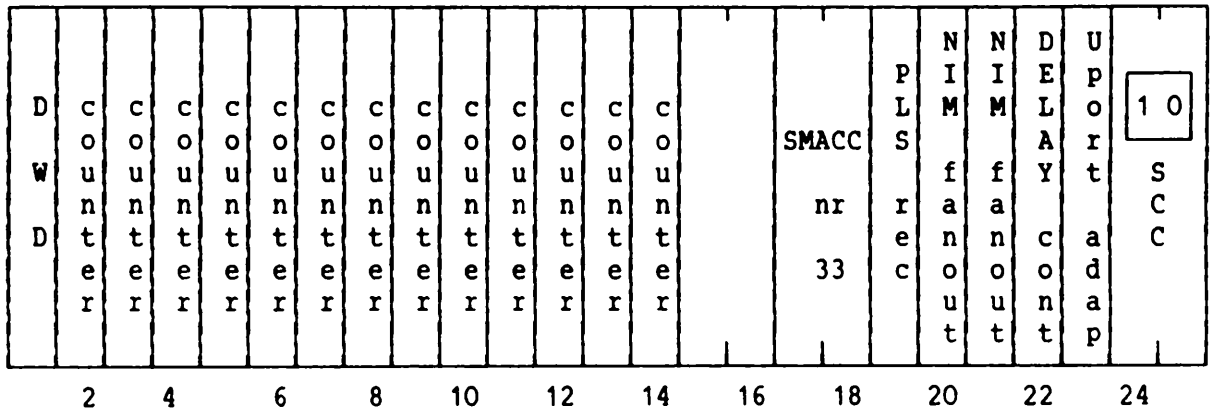
CHAPTER 3

LINAC V

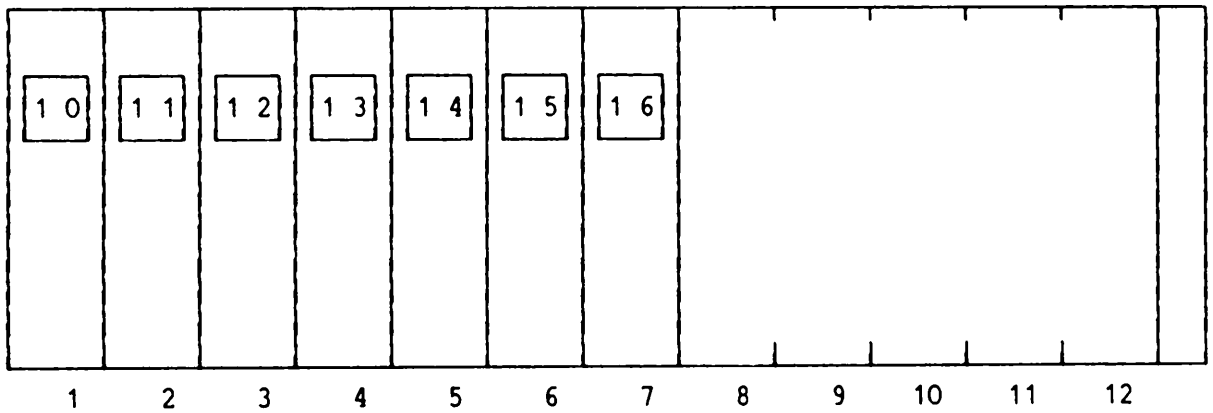
3 L I N A C V

LIL LOOP 2 CRATE 10 *RACK NR: RA167*

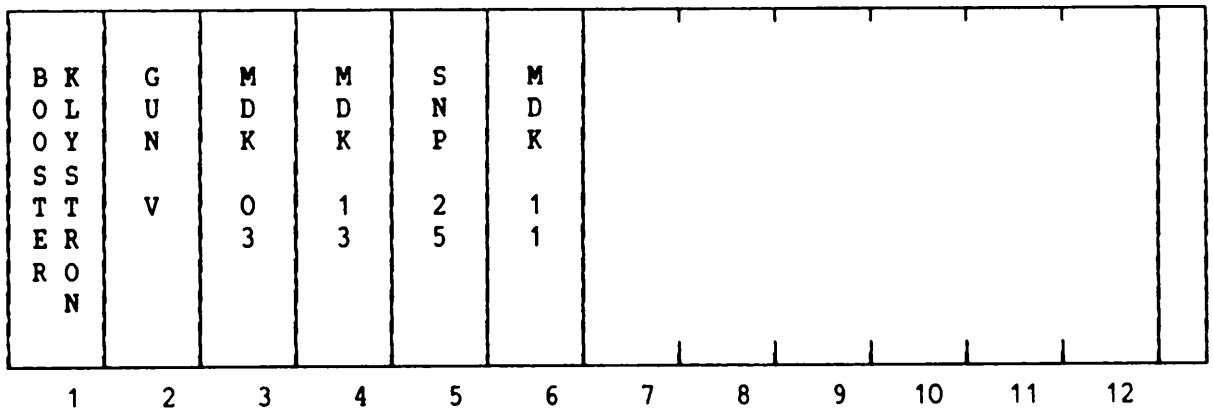
CAMAC CRATE



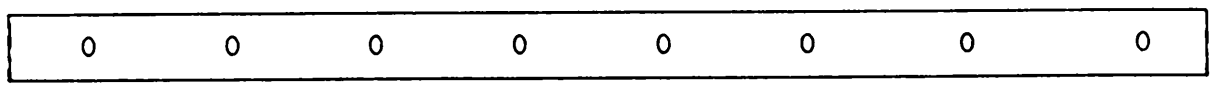
DELAY LINES



SELECTORS / LINE DRIVERS



PATCH PANEL



3.1 COUNTERS

P T I M						
Eq. nr.	Equipment name	CAMAC				Description
		L	C	N	A	
1	VX.SBKLY	2	10	2	0	Booster klystron start
2	spare			2	1	not used
3	VX.WGUNP			3	0	Production Gun V (-2 us)
4	VX.TAS			3	1	Train Acquisition Supplies(-1ms)
5	VX.SGUNPC			4	0	Start Gun V Production
6	VX.SGUND			4	1	Start Gun V Dummy (+1 ms)
7	VX.SKLY03			5	0	MDK03 firing
8	VX.SRFP03			5	1	MDK03 Pin diode switch on
9	VX.ERFP03			6	0	MDK03 Pin diode switch off
10	spare			6	1	not used
11	VX.SKLY13			7	0	MDK13 firing
12	VX.SRFP13			7	1	MDK13 Pin diode switch on
13	VX.ERFP13			8	0	MDK13 Pin diode switch off
14	VX.SRFI13C			8	1	MDK13 Phase shifter on
15	WX.FSNP25			9	0	SNP 25 forewarning
16	WX.ASNP25C			9	1	SNP 25 measurement
17	WX.WSNP25P			10	0	SNP 25 warning Production
18	WX.WSNP25D			10	1	SNP 25 warning Dummy
19	WX.SSNP25PC			11	0	SNP 25 firing Production
20	WX.SSNP25DC			11	1	SNP 25 firing Dummy
21	spare					not used
22	spare					not used
23	spare					not used
24	spare					not used
35	VX.SKLY11			12	0	MDK11 firing (spare klystron)
36	VX.SRFP11			12	1	MDK11 Pin diode switch on
37	VX.ERFP11			13	0	MDK11 Pin diode switch off
38	VX.SRFI11EC			13	1	MDK11 Phase shifter on e-
39	VX.SRFI11PC			14	0	MDK11 Phase shifter on e+
40	spare					not used

3.2 DELAY LINES

P T I M						
Eq. nr.	Equipment name	CAMAC				Description
		L	C	N	nr	
25	VX.SGUNPF	2	10	22	10	fine delay VX.SGUNP
26	VX.SRFI13F				11	fine delay VX.SRFI13
27	WX.ASNP25F				12	fine delay WX.ASNP25
28	WX.SSNP25PF				13	fine delay WX.SSNP25P
29	WX.SSNP25DF				14	fine delay WX.SSNP25D
30	VX.SRFI11EF				15	fine delay VX.SRFI11E
31	VX.SRFI11PF				16	fine delay VX.SRFI11P
32	spare					
33	spare					
34	spare					

3.3 CABLING

LIL LOOP 2 CRATE 10 RACK NR: RA167

CAMAC crate external connections
---

1) N20 IN : NIM fanout 9050 : RF.INJ

   source: Rack RA17O CAMAC crate N3 out1 (NIM fanout 9050)

2) N21 IN : NIM fanout 9050 : start INJ. counters

   source: Rack RA17O CAMAC crate N8 Start INJ counters out 1

3) SMACC FPI1 : not used

   source:

4) SMACC FPI2 : not used

   source:

5) SMACC FPI3 : not used

   source:

6) SMACC FPI4 : not used

   source:

7) N19 PLS-RECEIVER : PLS-LPI

   source: Timing distributor

8) M / L / P - connections on the selector/line drivers

   source: RA17O NIM crate DOR-driver NIM slot 1

Internal connections

- N20 NIM fanout for RF.INJ . Every output is connected with the CLOCK of the counter in the respective slot e.g.: out2 is connected with the clock of N2

- N21 NIM fanout for Start INJ. counters. Every output is connected with the START of the counter in the respective slot.

- N22 DELAY LINE controller. The controller is connected in daisy chain with all the delay lines in the rack

3.4 PATCH PANEL

WX. FSNP25	WX. WSNP25	WX. SSNP25	HX.AS	WX. ASNP25			
0	0	0	0	0	0	0	0

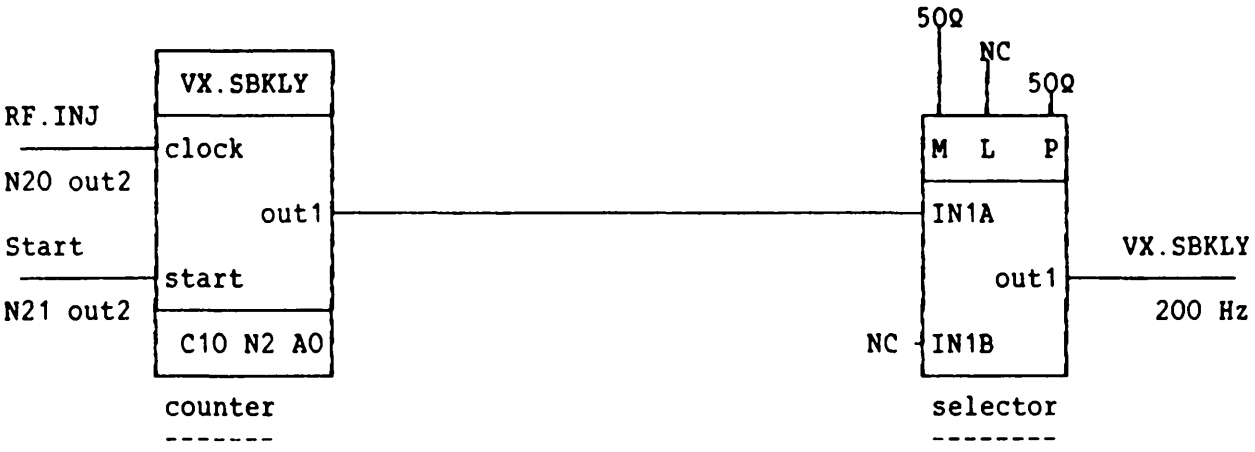
		VX. ERFP03					
0	0	0	0	0	0	0	0

VX. WGUNP	VX. TAS	VX. SRFP03					
0	0	0	0	0	0	0	0

VX. SBKLY	VX. SGUN	VX. SKLY03	VX. SKLY13	VX. SRFP13	VX. ERFP13	VX. SRFI13	
0	0	0	0	0	0	0	0

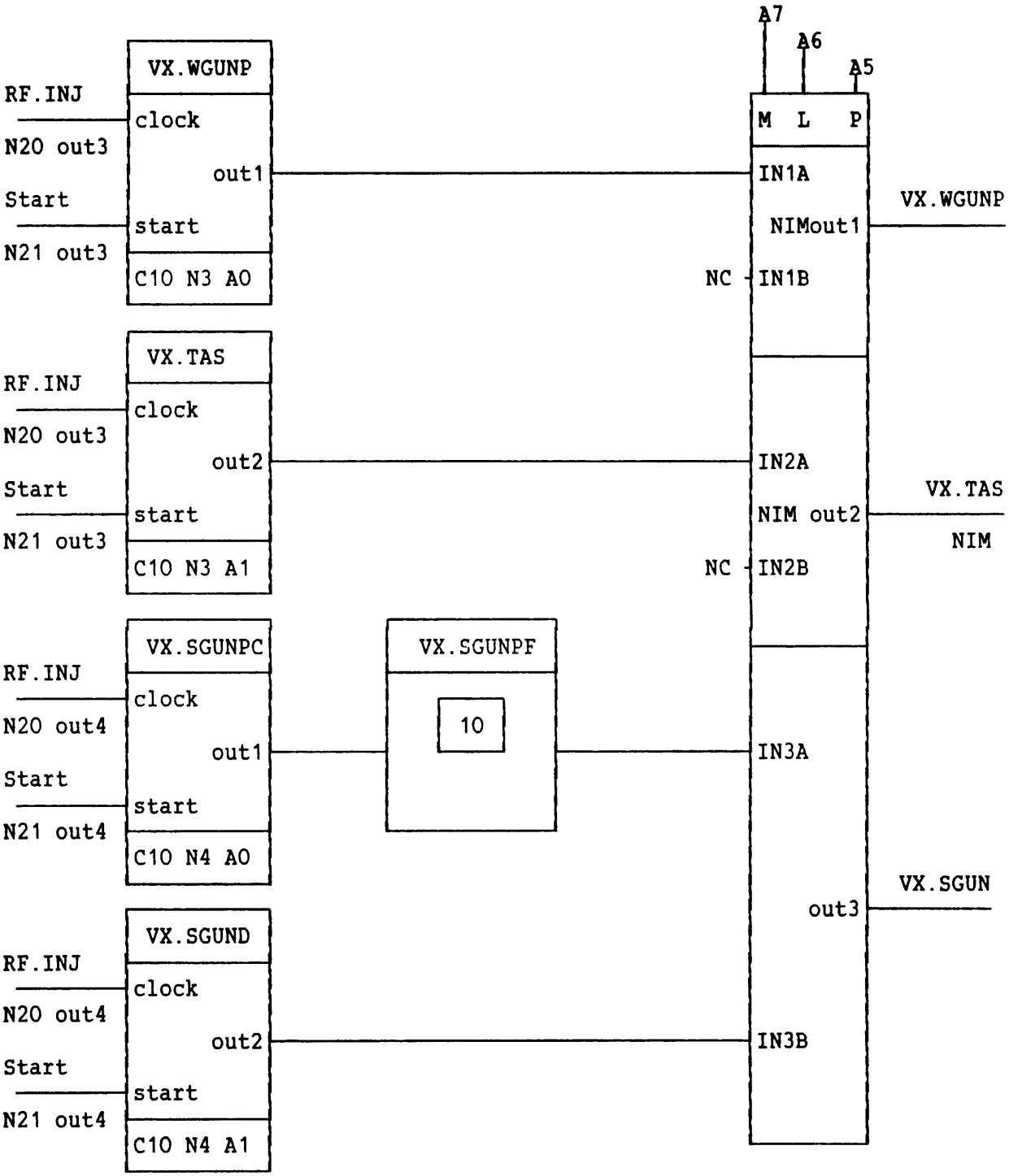
3.5 TIMINGS

3.5.1 BOOSTER KLYSTRON



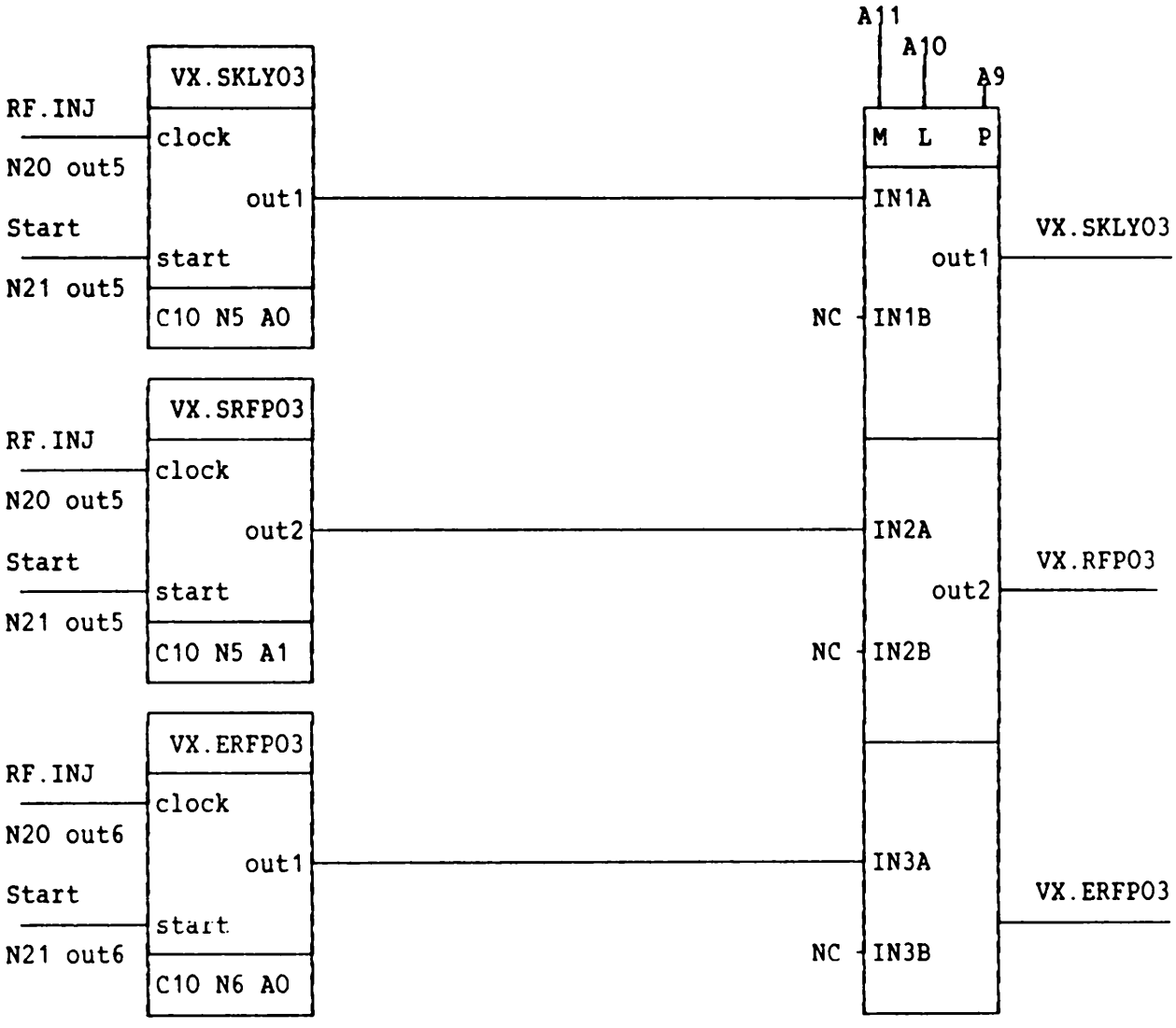
selector straps connections			
11-out 12-in 13-out	21-out 22-in 23-out	31-out 32-in 33-out	41-out 42-in 43-out

3.5.2 GUN V



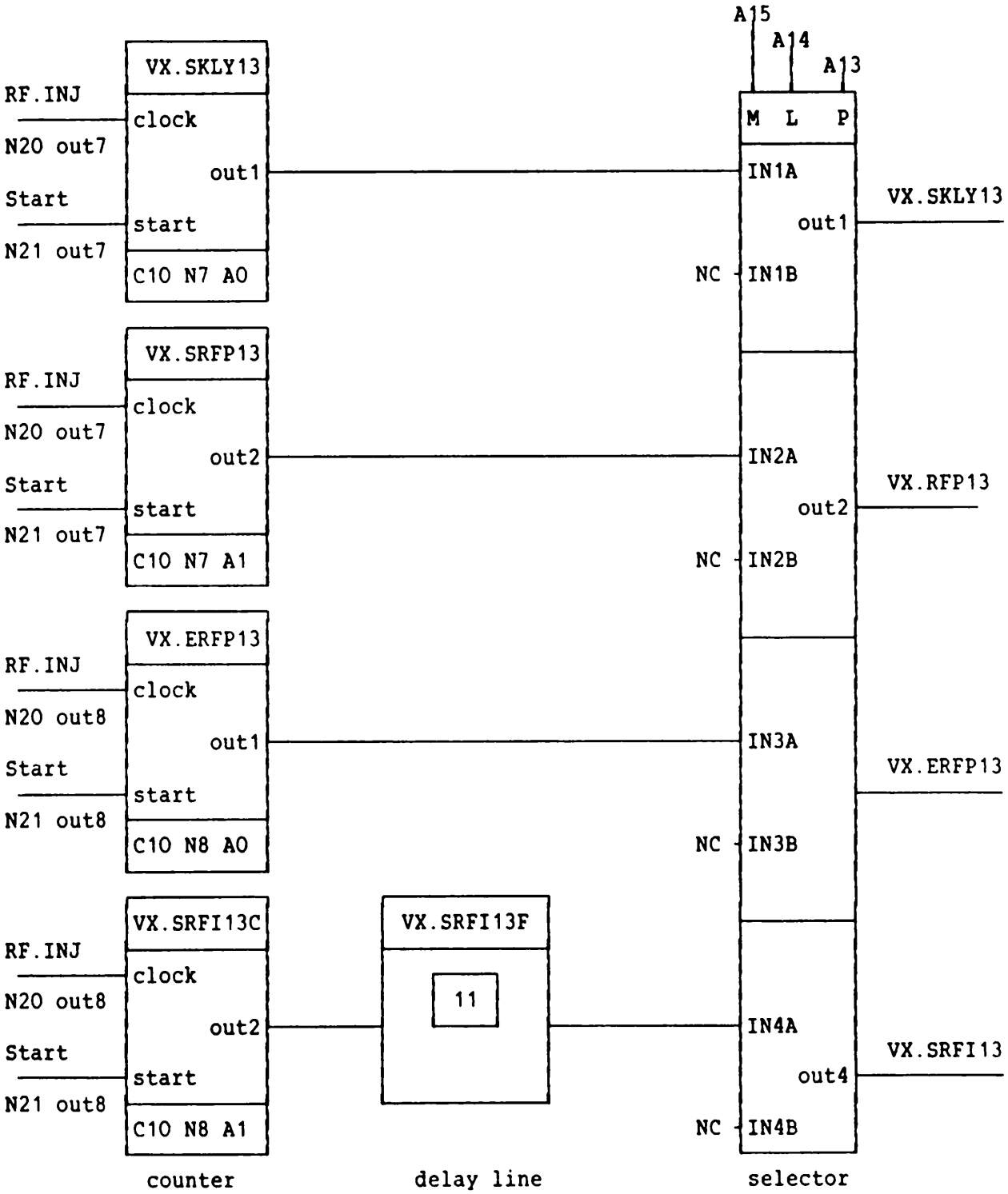
selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

3.5.3 MDK 03



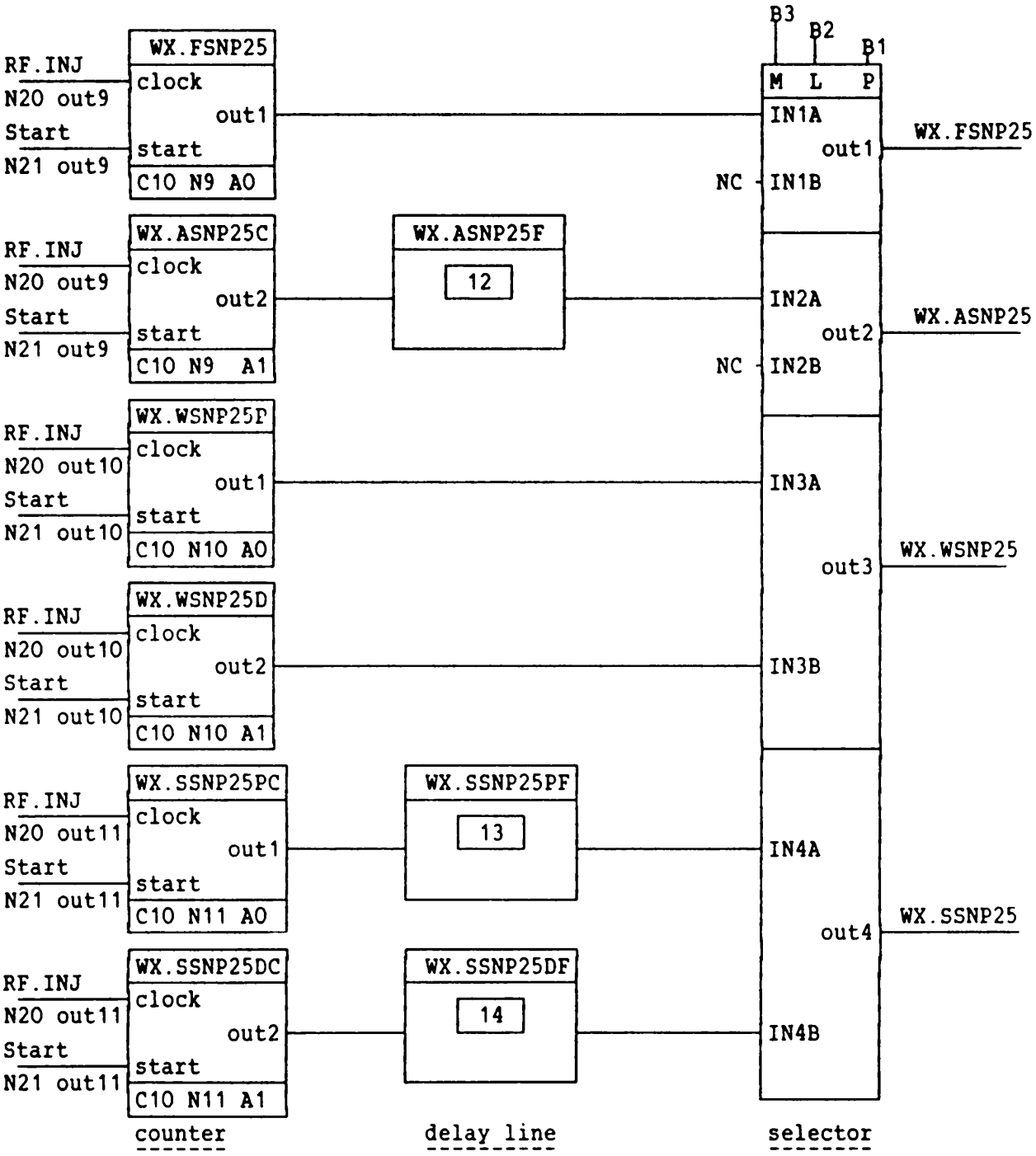
selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

3.5.4 MDK 13



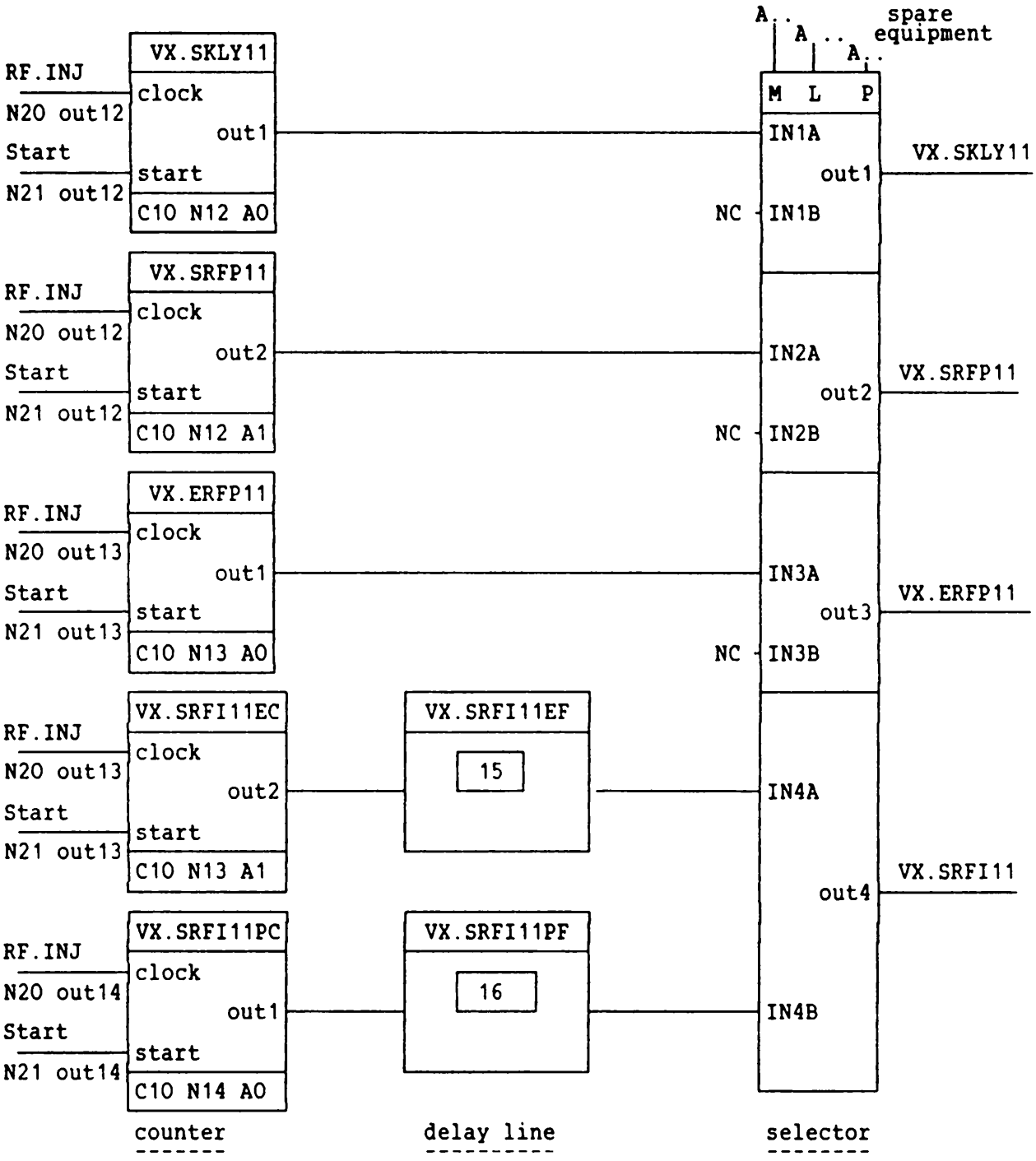
selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

3.5.5 SNP 25



selector straps connections			
11-in 12-out 13-in	21-in 22-out 23-in	31-out 32-in 33-in	41-out 42-in 43-in

3.5.6 MDK 11



selector straps connections			
11-in 12-out 13-in	21-in 22-out 23-in	31-in 32-out 33-in	41-out 42-in 43-in

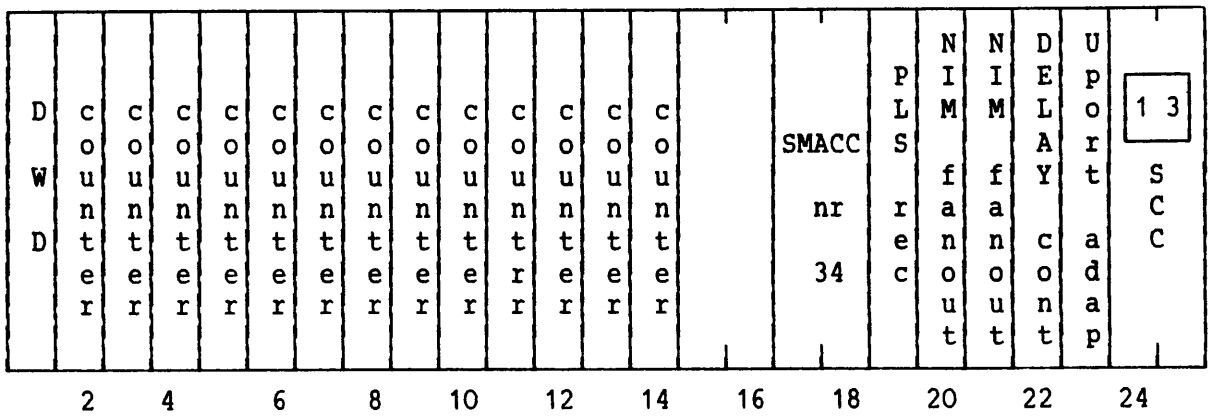
CHAPTER 4

LINAC W

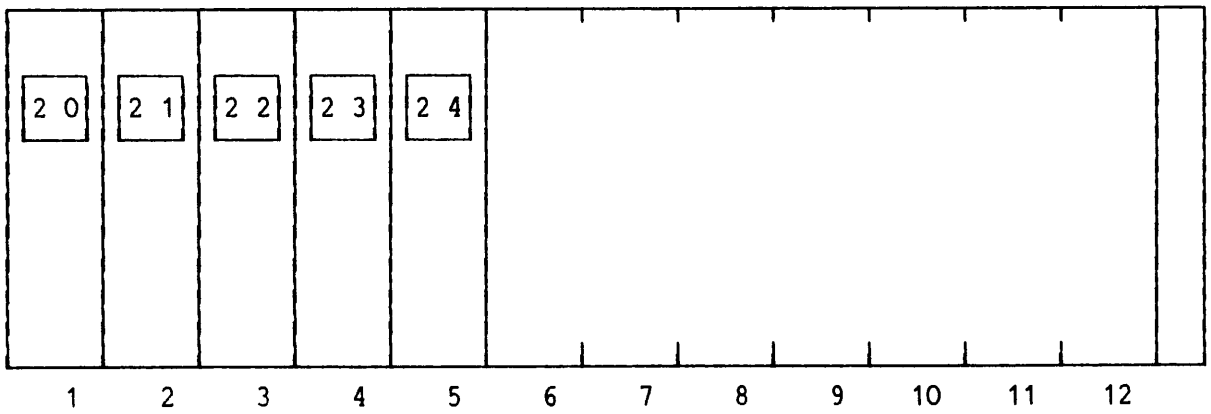
4 L_I_N_A_C___W

LIL LOOP 2 CRATE 13 *RACK NR: RA168*

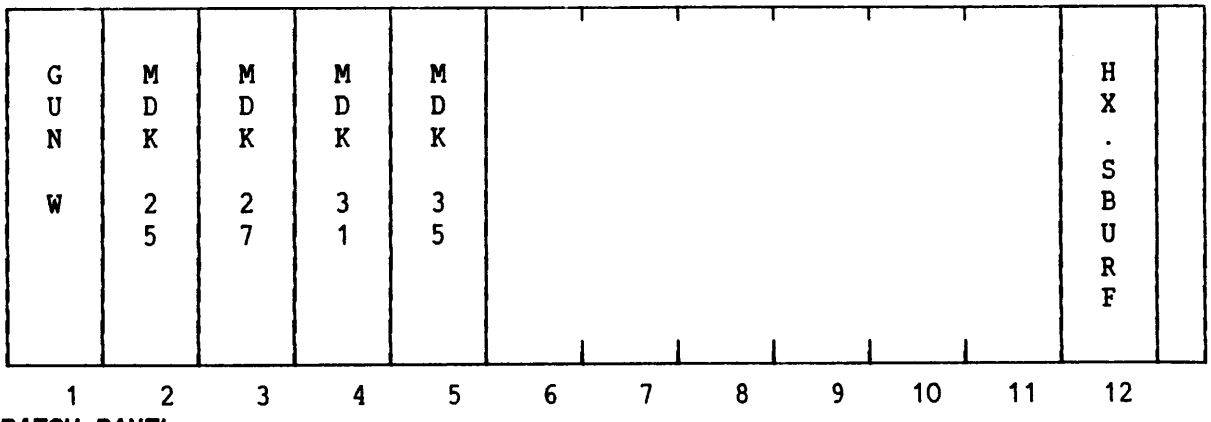
CAMAC CRATE



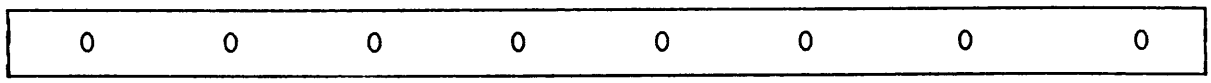
DELAY LINES



SELECTORS / LINE DRIVERS



PATCH PANEL



4.1 COUNTERS

P T I M						
Eq. nr.	Equipment name	CAMAC				Description
		L	C	N	A	
51	WX.SGUNPC	2	13	2	0	Start Gun W Production
52	WX.SGUND			2	1	Start Gun W Dummy
53	WX.WGUNP			3	0	Production Gun W (-2μs)
54	HX.TZC			3	1	Basic Train /Train Zero Crossing
55	WX.TAS			4	0	Train Acquisition Supplies(-1ms)
56	HX.SBURF			4	1	Start Burst RF(timing reference) (value is fixed 1)
57	WX.SKLY25			5	0	MDK25 firing
58	WX.SRFP25			5	1	MDK25 Pin diode switch on
59	WX.ERFP25			6	0	MDK25 Pin diode switch off
60	spare			6	1	not used
61	WX.SKLY27			7	0	MDK27 firing
62	WX.SRFP27			7	1	MDK27 Pin diode switch on
63	WX.ERFP27			8	0	MDK27 Pin diodes off
64	WX.SRFI27EC			8	1	MDK27 Phase shifter on e^-
65	WX.SRFI27PC			9	0	MDK27 Phase shifter on e^+
66	spare			9	1	not used
67	WX.SKLY31			10	0	MDK31 firing
68	WX.SRFP31			10	1	MDK31 Pin diode switch on
69	WX.ERFP31			11	0	MDK31 Pin diodes off
70	WX.SRFI31EC			11	1	MDK31 Phase shifter on e^-
71	WX.SRFI31PC			12	0	MDK31 Phase shifter on e^+
72	spare			12	1	not used
73	WX.SKLY35			13	0	MDK35 firing
74	WX.SRFP35			13	1	MDK35 Pin diode switch on
75	WX.ERFP35			14	0	MDK35 Pin diode switch off
76	spare			14	1	not used
77	spare					not used
78	spare					not used
79	spare					not used
80	spare					not used

4.2 DELAY LINES

P T I M						
Eq. nr.	Equipment name	CAMAC				Description
		L	C	N	nr	
81	WX.SGUNPF	2	13	22	20	fine delay WX.SGUNP
82	WX.SRFI27EF				21	fine delay WX.SRFI27E
83	WX.SRFI27PF				22	fine delay WX.SRFI27P
84	WX.SRFI31EF				23	fine delay WX.SRFI31E
85	WX.SRFI31PF				24	fine delay WX.SRFI31P
86	spare					not used
87	spare					not used
88	spare					not used
89	spare					not used

4.3 CABLING

LIL LOOP 2 CRATE 13 RACK NR: 168

CAMAC crate external connections
---

1) N20 IN : NIM fanout 9050 : RF.INJ

   source: Rack RA170 CAMAC crate N3 out2 (NIM fanout 9050)

2) N21 IN : NIM fanout 9050 : start INJ. counters

   source: Rack RA170 CAMAC crate N8 Start INJ counters out 2

3) SMACC FPI1 : not used

   source:

4) SMACC FPI2 : not used

   source:

5) SMACC FPI3 : not used

   source:

6) SMACC FPI4 : not used

   source:

7) N19 PLS-RECEIVER : PLS-LPI

   source: Timing distributor

8) M / L / P - connections on the selector/line drivers

   source: RA170 NIM crate DOR-driver NIM slot 2

Internal connections

- N20 NIM fanout for RF.INJ . Every output is connected with the CLOCK of the counter in the respective slot
  e.g.: out2 is connected with the clock of N2

- N21 NIM fanout for Start INJ. counters. Every output is connected with the START of the counter in the respective slot.

- N22 DELAY LINE controller. The controller is connected in daisy chain with all the delay lines in the rack

4.4 PATCH PANEL

HX.TZC	WX. ERFP25	WX. ERFP27		WX. ERFP31		WX. ERFP35	
0	0	0	0	0	0	0	0

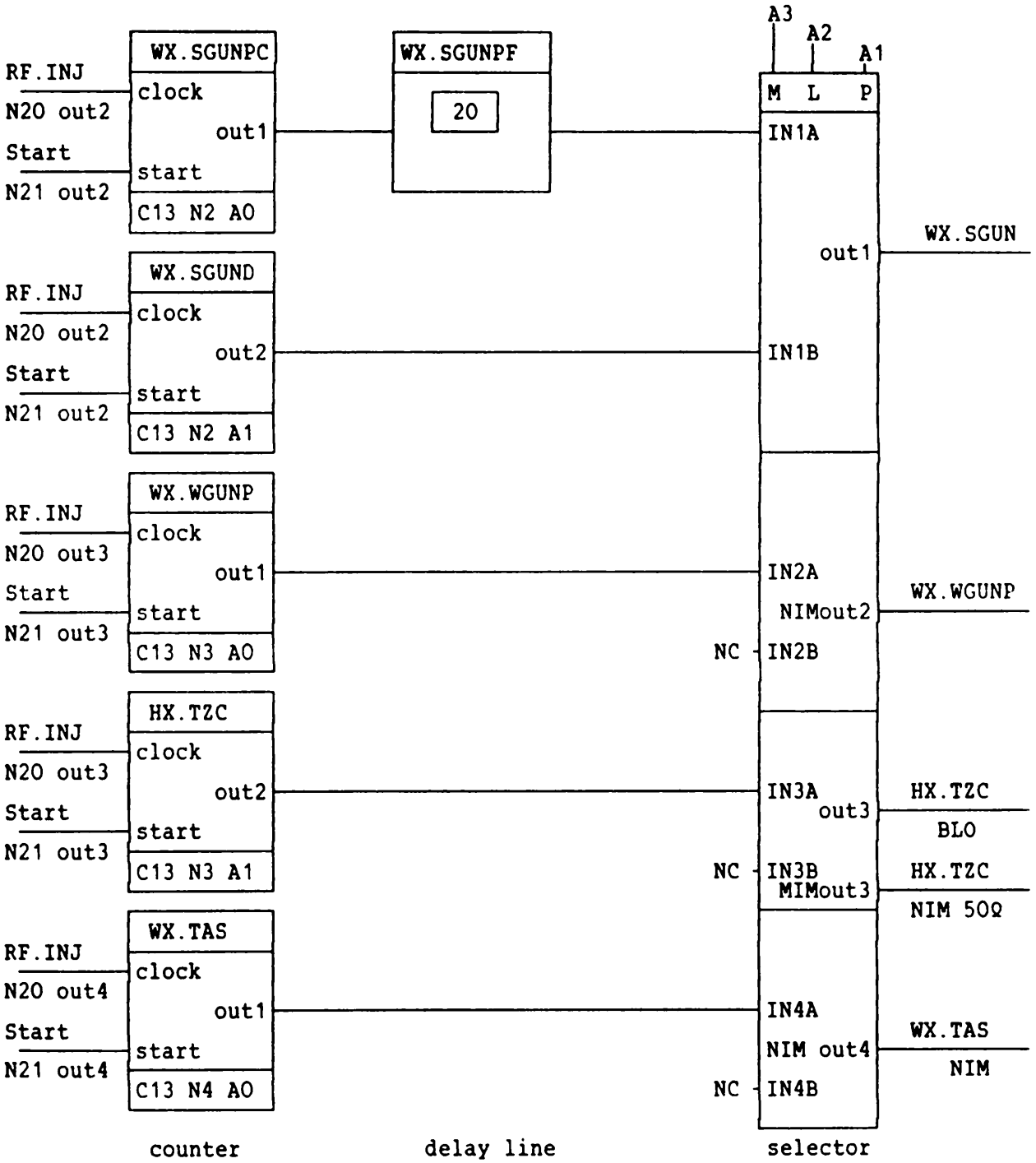
	WX. SRFP25	WX. SRFP27		WX. SRFP31		WX. SRFP35	
0	0	0	0	0	0	0	0

	WX. SKLY25	WX. SKLY27	WX. SRFI27	WX. SKLY31	WX. SRFI31	WX. SKLY35	
0	0	0	0	0	0	0	0

WX. SGUN							
0	0	0	0	0	0	0	0

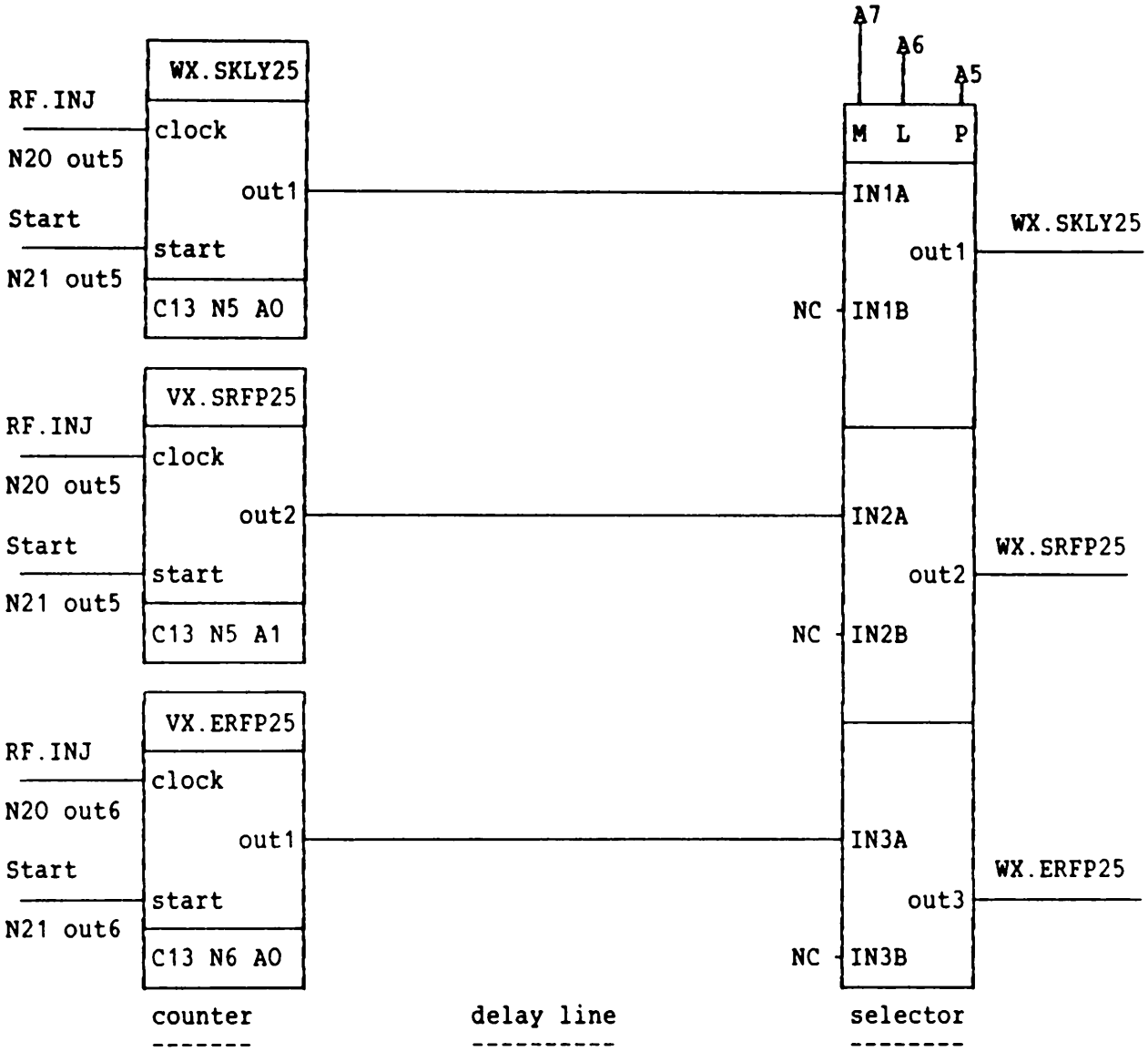
4.5 TIMINGS

4.5.1 GUN W



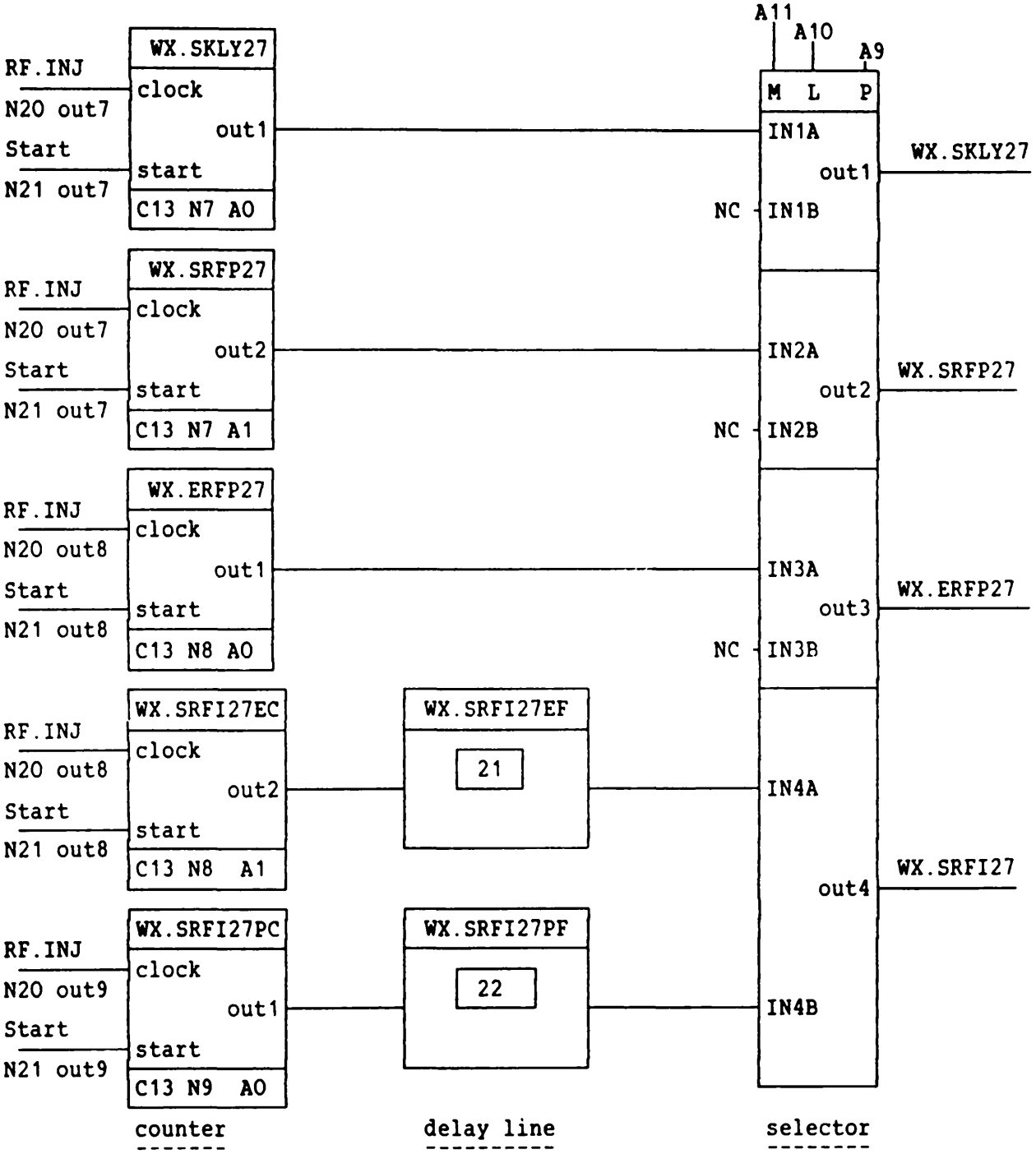
selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-in 32-out 33-in	41-out 42-in 43-in

4.5.2 MDK 25



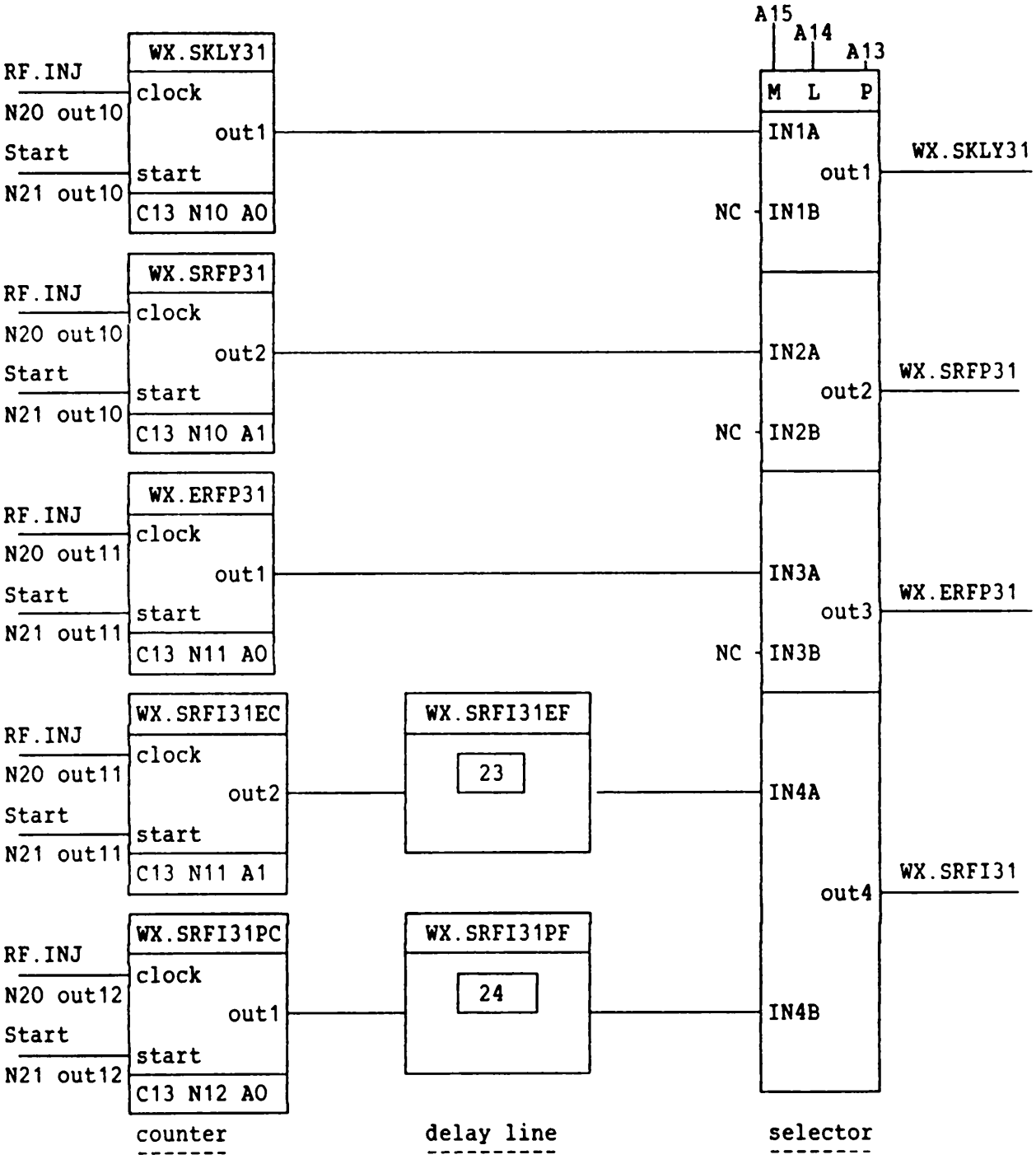
selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

4.5.3 MOK 27



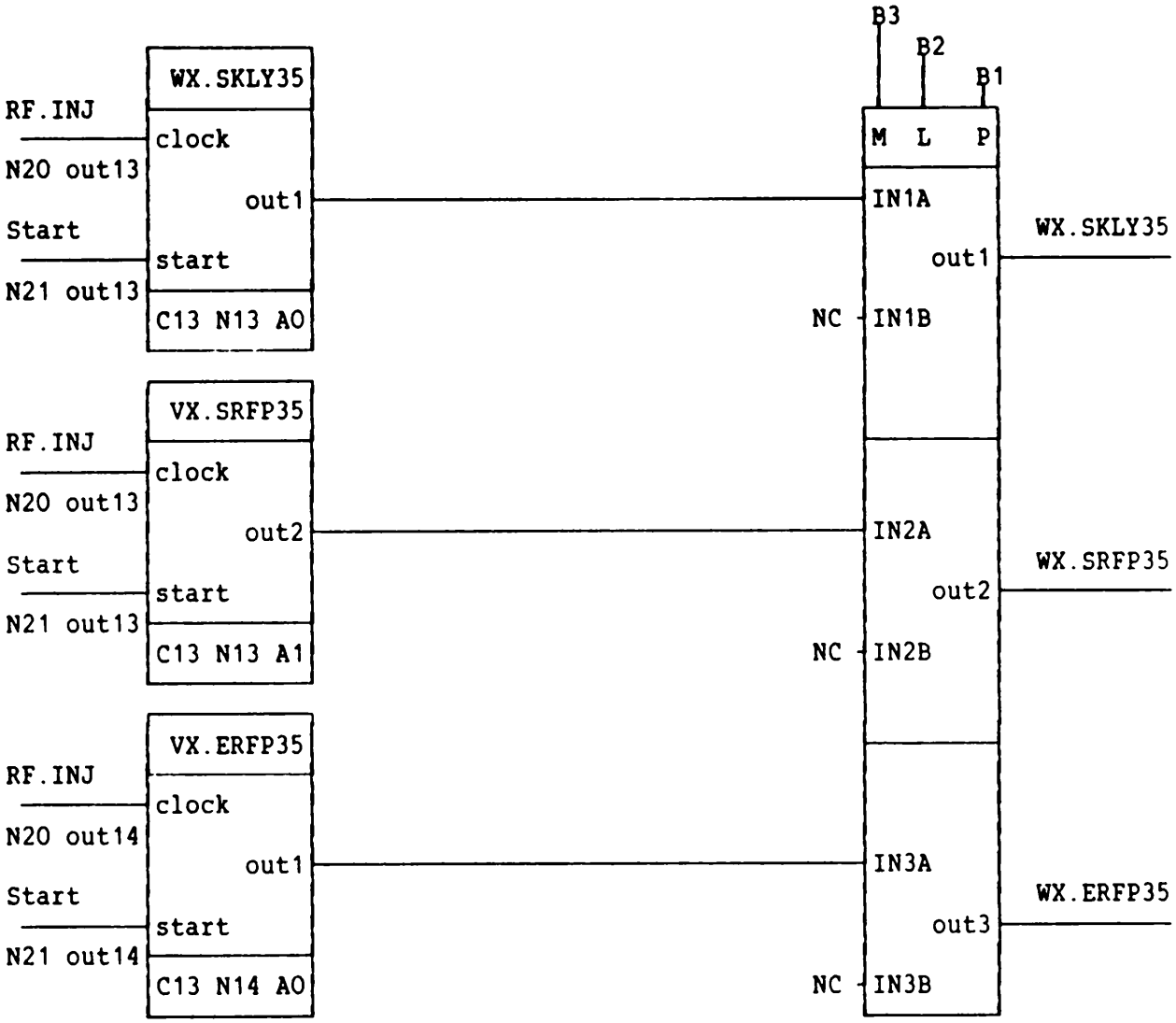
selector straps connections			
11-in 12-out 13-in	21-in 22-out 23-in	31-in 32-out 33-in	41-out 42-in 43-in

4.5.4 MDK 31



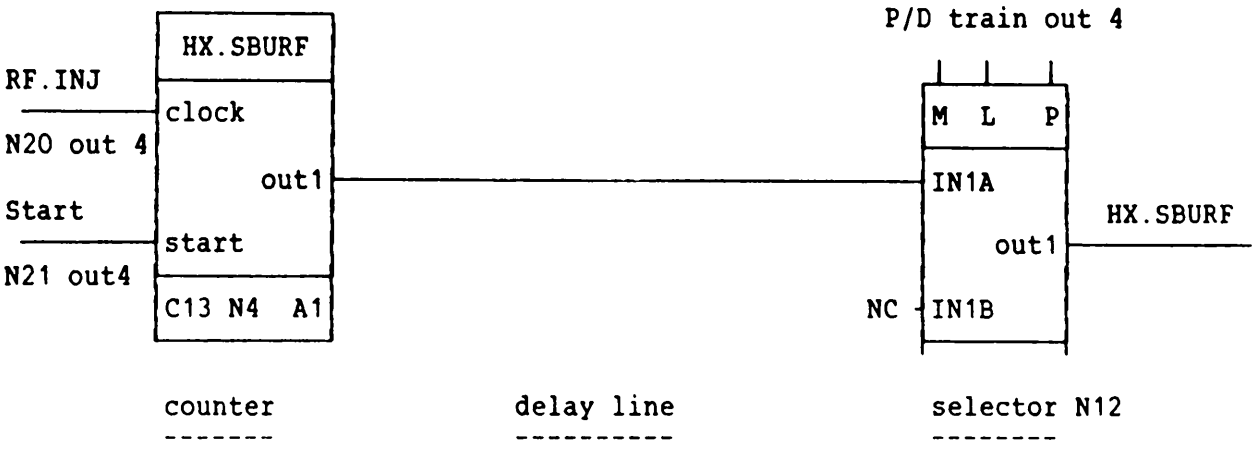
selector straps connections			
11-in 12-out 13-in	21-in 22-out 23-in	31-in 32-out 33-in	41-out 42-in 43-in

4.5.5 MOK 35



selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

4.5.6 HX.SBURF



selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

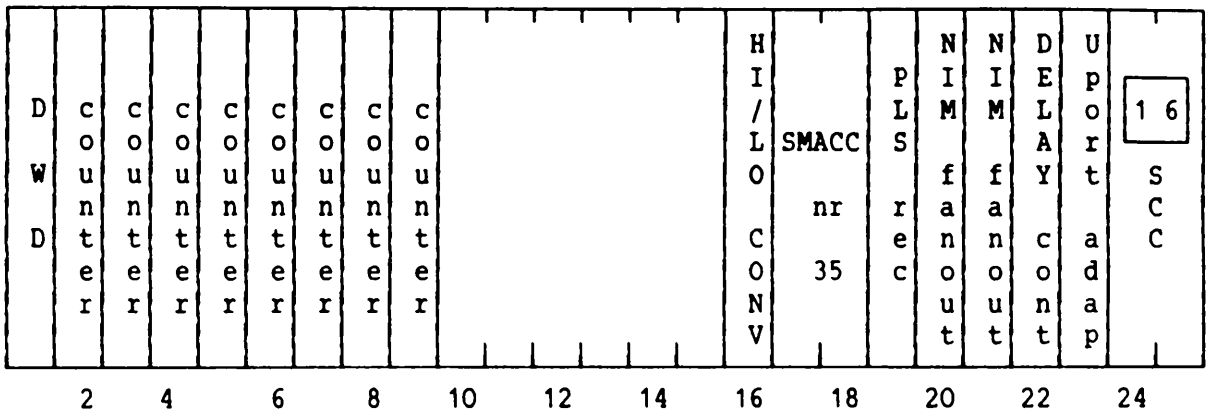
CHAPTER 5

INJECTION KICKERS

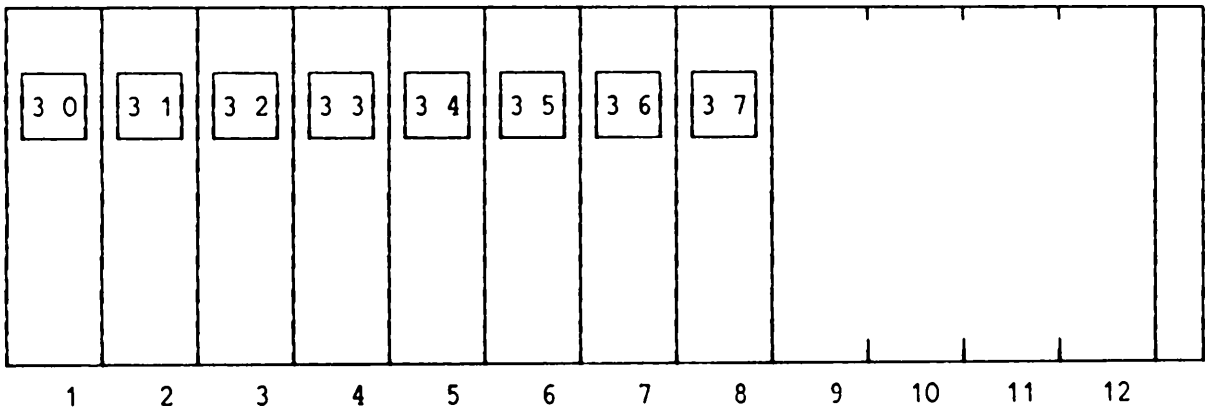
5 INJECTION KICKERS

LIL LOOP 2 CRATE 16 *RACK NR: RA169*

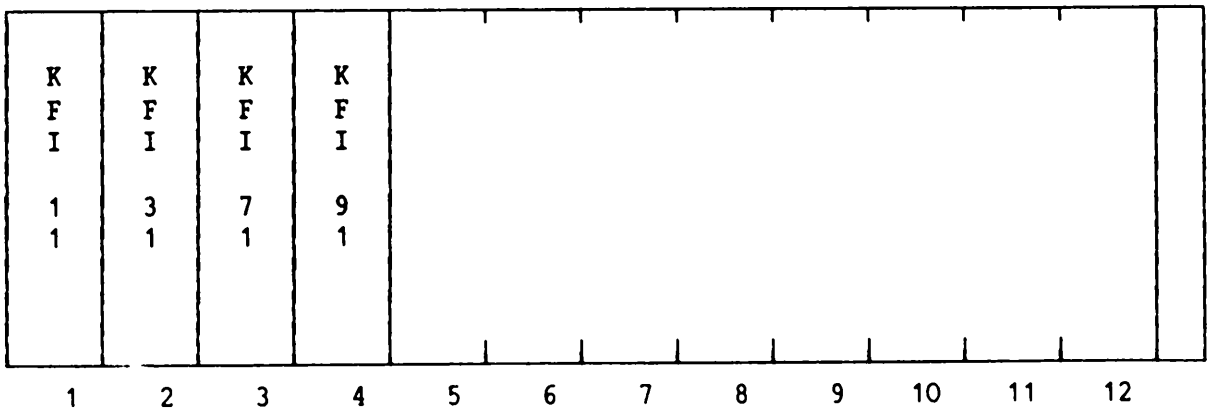
CAMAC CRATE



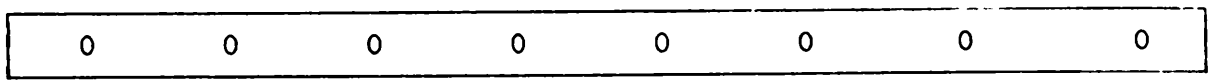
DELAY LINES



SELECTORS / LINE DRIVERS



PATCH PANEL



5_1_COUNTERS

P T I M						
Eq. nr.	Equipment name	CAMAC				Description
		L	C	N	A	
101	HX.WKFI11	2	16	2	0	KFI11 charging
102	HX.SKFI11C			2	1	KFI11 firing main
103	HX.EKFI11C			3	0	KFI11 firing dump
104	spare			3	1	not used
105	HX.WKFI31			4	0	KFI31 charging
106	HX.SKFI31C			4	1	KFI31 firing main
107	HX.EKFI31C			5	0	KFI31 firing dump
108	spare			5	1	not used
109	HX.WKFI71			6	0	KFI71 charging
110	HX.SKFI71C			6	1	KFI71 firing main
111	HX.EKFI71C			7	0	KFI71 firing dump
112	spare			7	1	not used
113	HX.WKFI91			8	0	KFI91 charging
114	HX.SKFI91C			8	1	KFI91 firing main
115	HX.EKFI91C			9	0	KFI91 firing dump
116	spare			9	1	not used
117	spare					not used
118	spare					not used
119	spare					not used
120	spare					not used

5.2 DELAY LINES

P T I M						
Eq. nr.	Equipment name	CAMAC				Description
		L	C	N	nr	
121	HX.SKFI11F	2	16	22	30	fine delay HX.SKFI11
122	HX.EKFI11F				31	fine delay HX.EKFI11
123	HX.SKFI31F				32	fine delay HX.SKFI31
124	HX.EKFI31F				33	fine delay HX.EKFI31
125	HX.SKFI71F				34	fine delay HX.SKFI71
126	HX.EKFI71F				35	fine delay HX.EKFI71
127	HX.SKFI91F				36	fine delay HX.SKFI91
128	HX.EKFI91F				37	fine delay HX.EKFI91
129	spare					not used
130	spare					not used

5.3 CABLING

LIL LOOP 2 CRATE 16 *RACK NR: RA169*

CAMAC crate external connections
---

1) N20 IN : NIM fanout 9050 : RF.INJ

   source: Rack RA170 CAMAC crate N3 out3 (NIM fanout 9050)

2) N21 IN : NIM fanout 9050 : start INJ. counters

   source: Rack RA170 CAMAC crate N8 Start INJ counters out 3

3) SMACC FPI1 : not used

   source:

4) SMACC FPI2 : not used

   source:

5) SMACC FPI3 : not used

   source:

6) SMACC FPI4 : not used

   source:

7) N19 PLS-RECEIVER : PLS-LPI

   source: Timing distributor

8) M / L / P - connections on the selector/line drivers

   source: RA170 NIM crate DOR-driver NIM slot 3

Internal connections

- N20 NIM fanout for RF.INJ . Every output is connected with the CLOCK of the counter in the respective slot
  e.g.: out2 is connected with the clock of N2

- N21 NIM fanout for Start INJ. counters. Every output is connected with the START of the counter in the respective slot.

- N22 DELAY LINE controller. The controller is connected in daisy chain with all the delay lines in the rack

5.4 PATCH PANEL

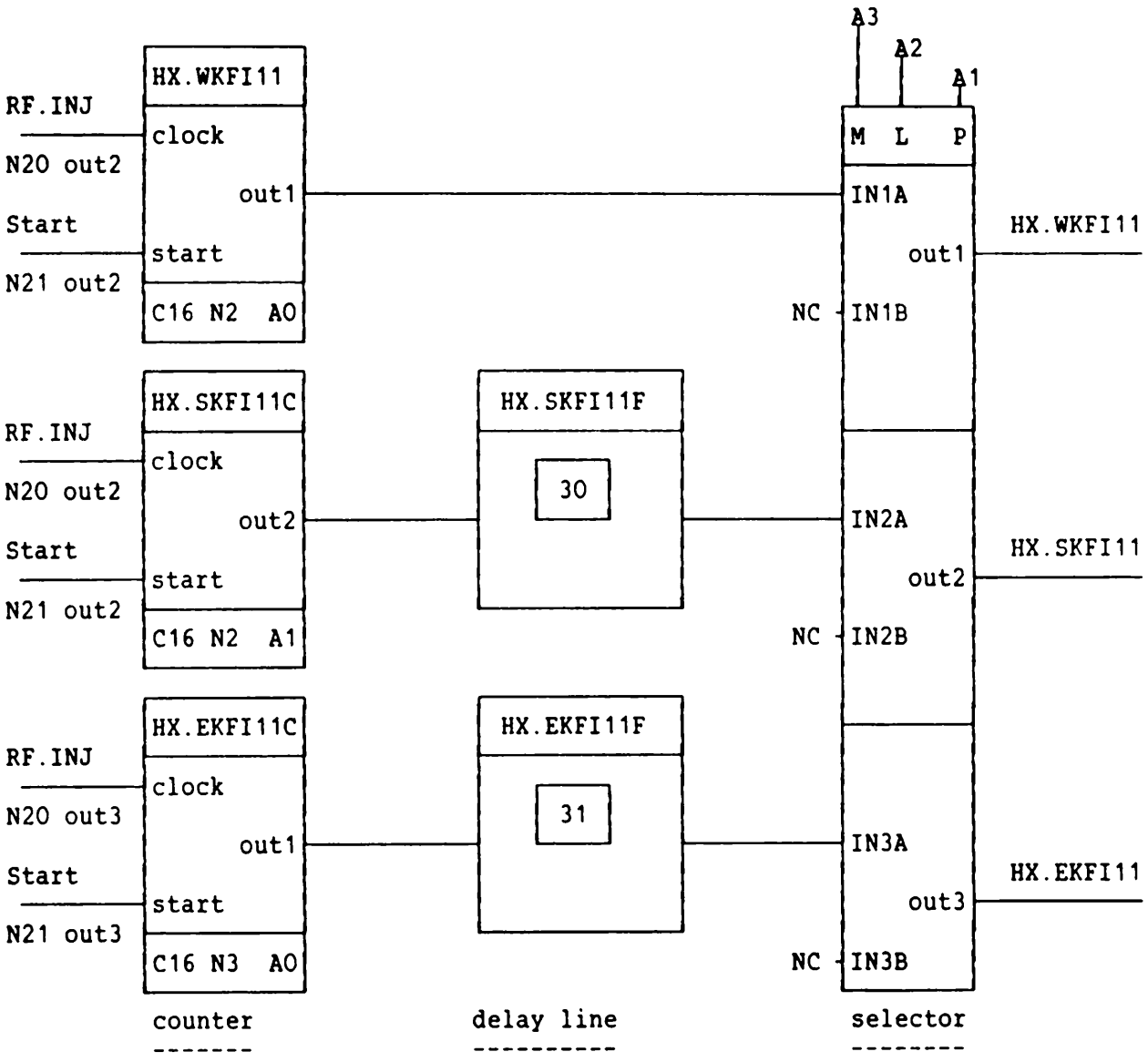
HX. EKFI11	HX. EKFI31	HX. EKFI71	HX. EKFI91				
0	0	0	0	0	0	0	0

HX. SKFI11	HX. SKFI31	HX. SKFI71	HX. SKFI91				
0	0	0	0	0	0	0	0

HX. WKFI11	HX. WKFI31	HX. WKFI71	HX. WKFI91				
0	0	0	0	0	0	0	0

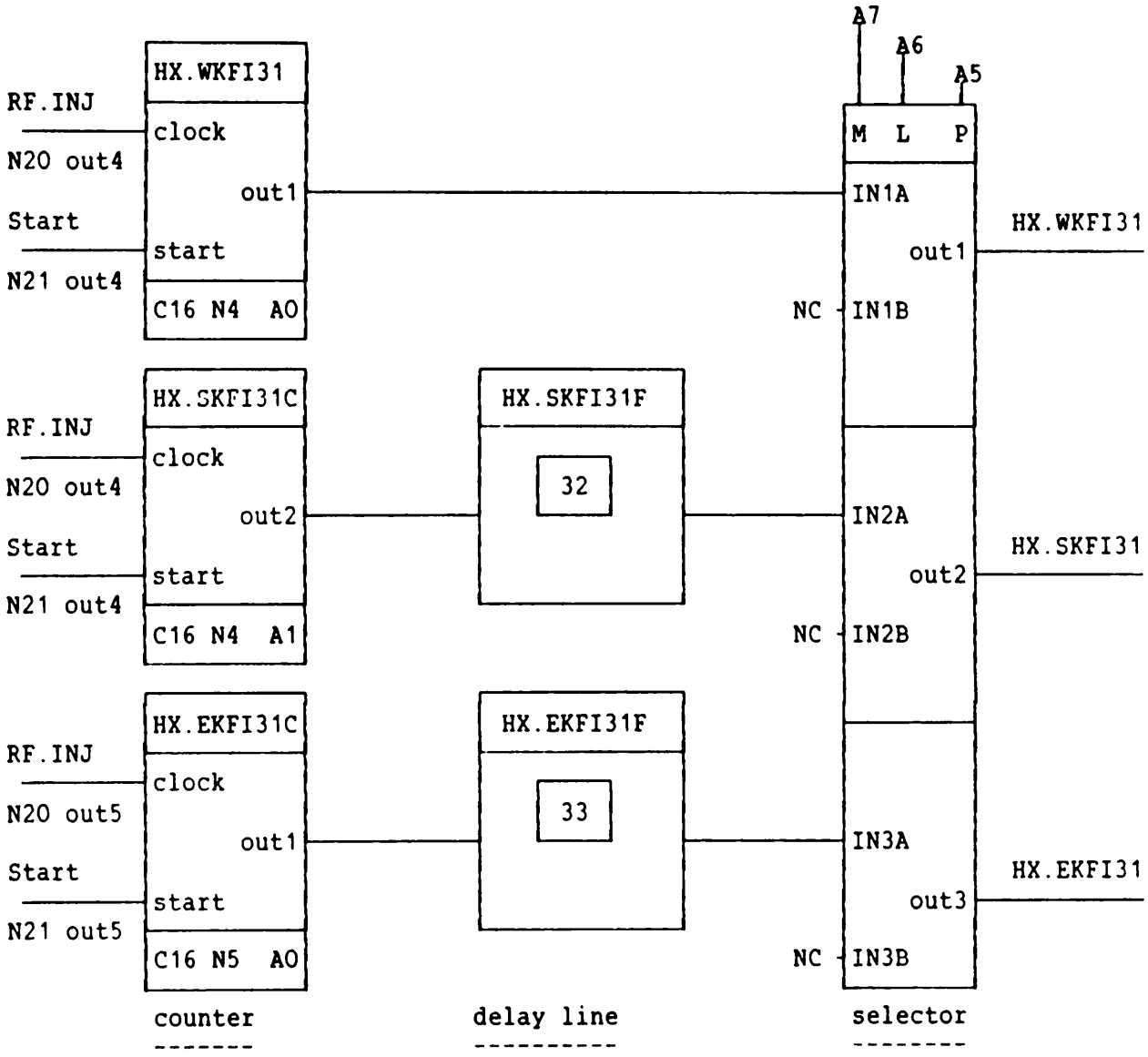
5.5 TIMINGS

5.5.1 KFI 11



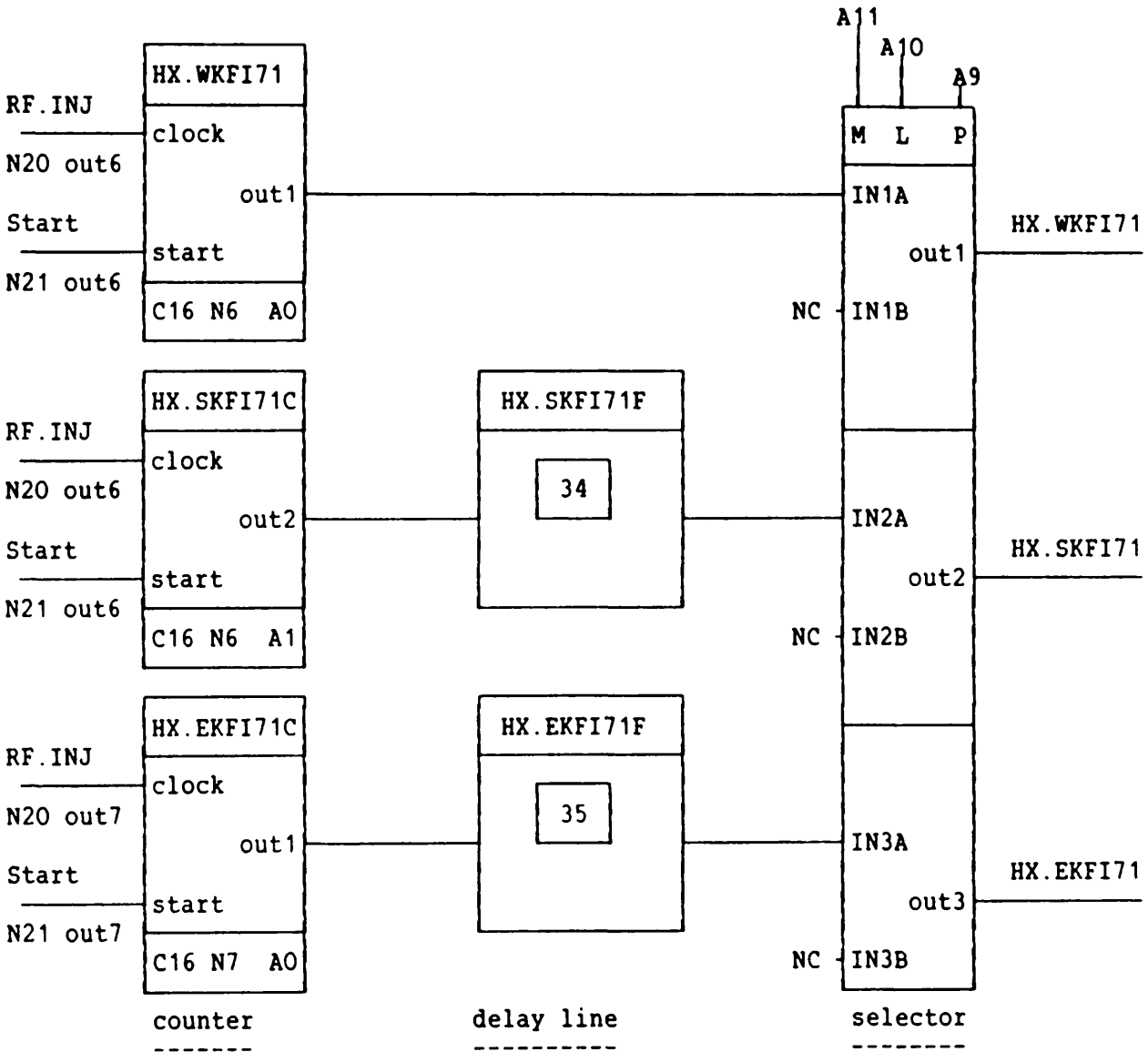
selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

5.5.2 KFI 31



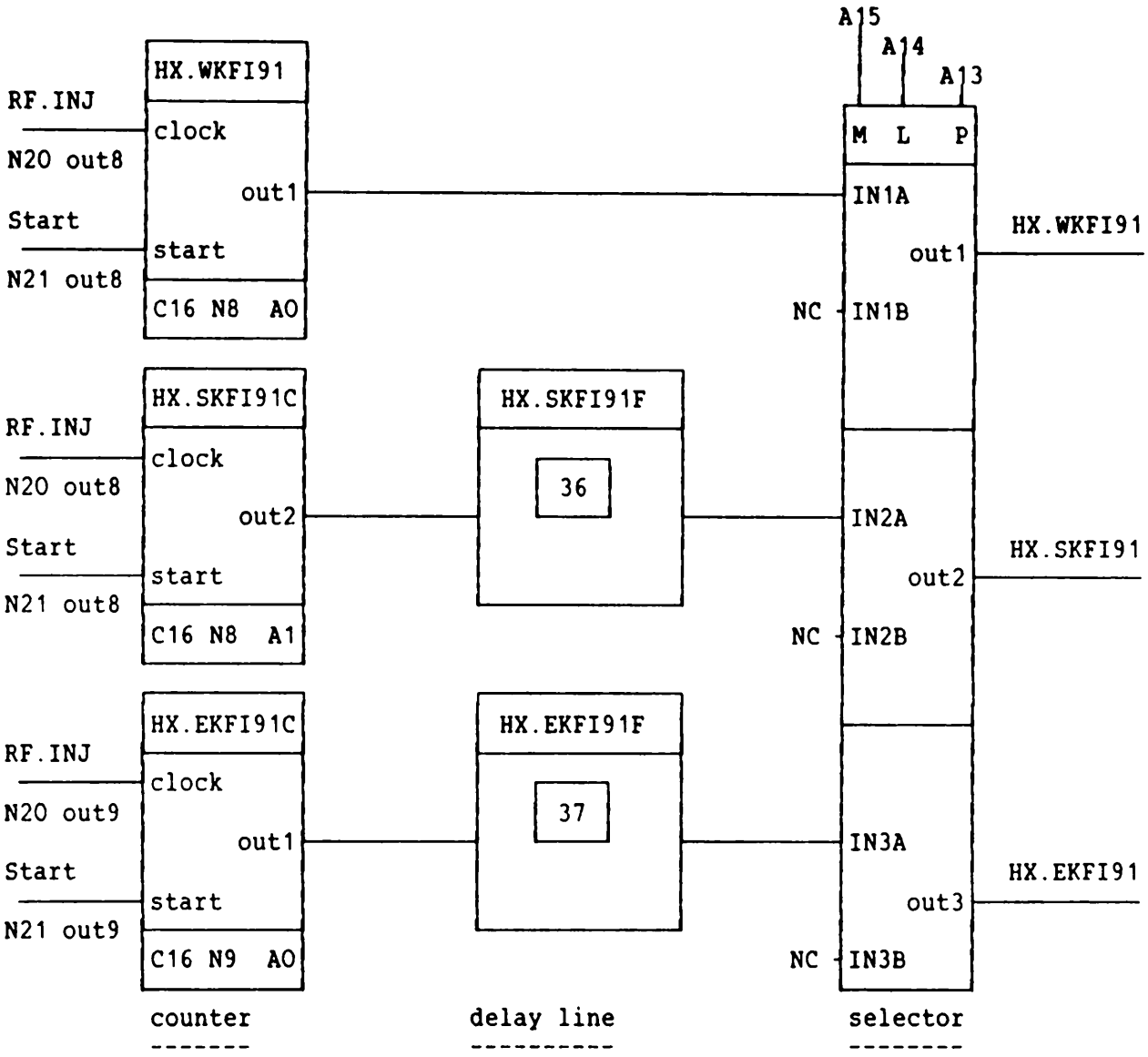
selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

5.5.3 KFI 71



selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

5.5.4 KFI 91



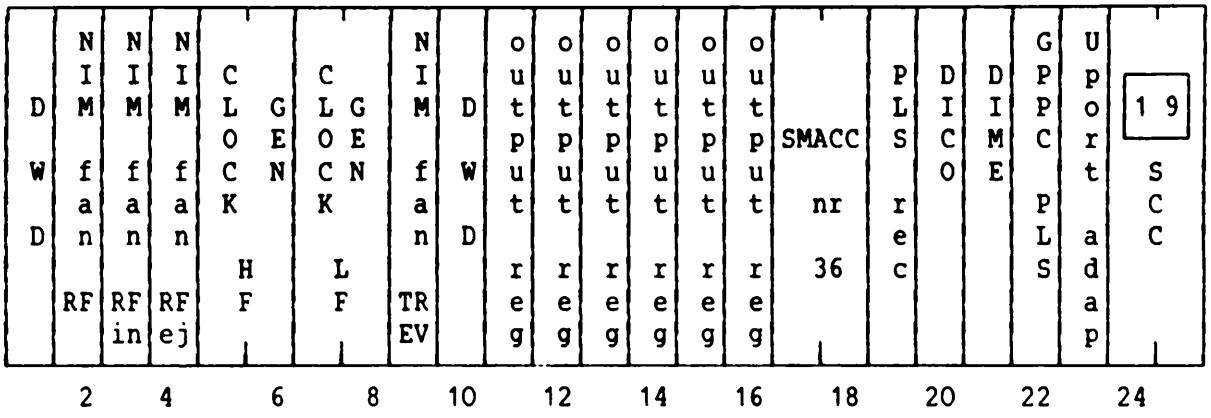
selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

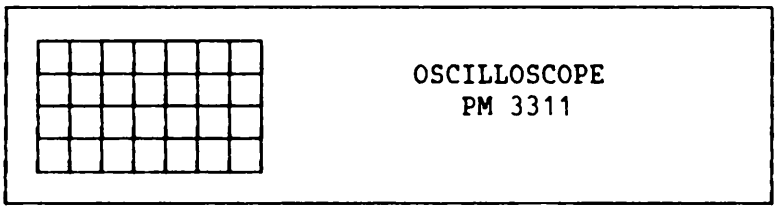
CHAPTER 6

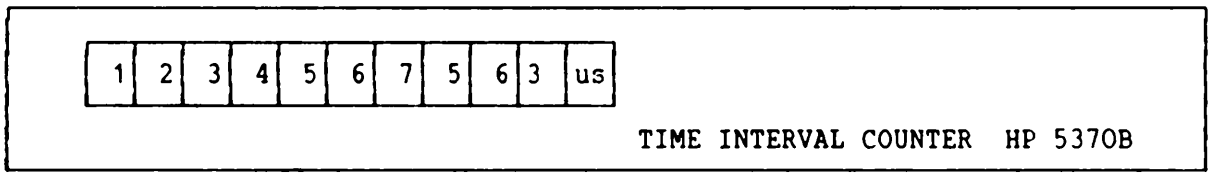
TIMING CONTROL

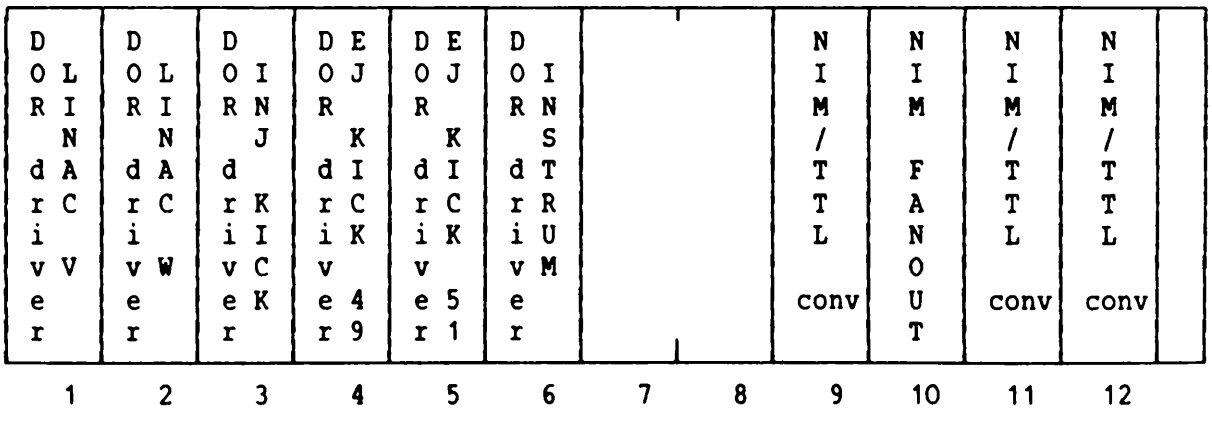
6 TIMING CONTROL

LIL LOOP 2 CRATE 19 **RACK NR: RA170**

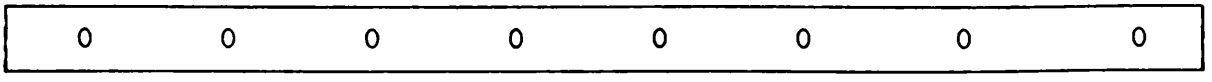








PATCH PANEL



6.1 CABLING

LIL LOOP 2 CRATE 19 RACK NR RA170

CAMAC connections
---

1) N2 : NIM fanout 9050 : RF.CONT continuous 19 MHz RF train NIM/50Ω

IN : from N6 RF.CONT

OUT1 : to Instrum EB1
OUT2 : to RA 170 NIM slot 11 / in 2
OUT3 : to Instrum in LOPI Control Room via patch in RA173
OUT7 : to EB2 R006 Synchrotron Radiation

2) N3 : NIM fanout 9050 : RF.INJ RF burst for injection counters NIM/50Ω

IN : from N6 RF.INJ

OUT1 : to RA167 N20 / IN
OUT2 : to RA168 N20 / IN
OUT3 : to RA169 N20 / IN

3) N4 : NIM fanout 9050 : RF.EJ RF burst for ejection counters NIM/50Ω

IN : from N6 RF.EJ

OUT5 : to RA171 N20 / IN
OUT6 : to RA172 N20 / IN

4) N5-N6 : 19 MHz Clock Generator HF

RF.IN : from patch panel RF 19 MHz (TTL/50Ω)
BU.GATE : from N8 BU.GATE (TTLbar)
RF.CONT : to N2 NIM fanout IN
continuous 19 MHz train (NIM/50Ω)
RF.INJ : to N3 NIM fanout IN
19 MHz bursts for injection counters (NIM/50Ω)
RF.EJ : to N4 NIM fanout IN
19 MHz bursts for ejection counters (NIM/50Ω)
WEJ : from RA169 CAMAC N16 out 1
Warning EJection (=ej-2ms) (TTLbar)
SWEJ : Simulated Warning EJection
currently not used
RF.COR : (= HX.TREV) to same crate N9 IN
19/8 MHz sync with first ejected bucket (NIM/50Ω)

BIT0 : 19/2 MHz train to NIM Fanout IN1
BIT1 : 19/4 MHz train in NIM crate IN2

BIT2 : 19/8 MHz train in RA170 slot 10 IN3

5) N7-N8 : 19 MHz Clock Generator LF

50 Hz In : from 100V/2V transformer in rack RA170 rear panel
BU.GATE : to N6 BU.GATE (TTLbar)

Start Inj cntrs :
1) to RA167 Crate 10 N21 / IN (NIM/50Ω)
2) to RA168 Crate 13 N21 / IN (NIM/50Ω)
3) to RA169 Crate 16 N21 / IN (NIM/50Ω)
4) not used

P/D train :
1) to RA167 NIM crate selectors/linedrivers (TTL/50Ω)
2) to RA168 NIM crate selectors/linedrivers (TTL/50Ω)
3) to RA169 NIM crate selectors/linedrivers (TTL/50Ω)
4) not used

100 HZ μP Int : to SMACC (IKBOX) FPI1 (TTLbar)

TTL / NIM converters :

IN1 : from HX.FEJ (= -10ms) from Timing Central RA174
OUT1 : to RA171 CAMAC N21 in (NIM 50 Ω)
= Start ejection kicker 49

IN2 : from IN1
OUT1 : to RA172 CAMAC N21 in (NIM 50 Ω)
= Start ejection kicker 51

6) N9 : NIM fanout 9050 RF.CONT = HX.TREV (NIM 50 Ω)
RF EPA / 8 synchronised on 1st ejected bucket

IN : from N6 RF.CONT

OUT0 : to Timing Central RA174 (via RA173 NIM slot 2)
OUT4 : to RA170 NIM slot 11 IN 1
OUT6 : to RA170 NIM slot 11 IN 2
OUT9 : to RA170 NIM slot 9 IN 4

7) N10 : Dataway Display to show routines active in the IKBOX

Write 1 : FPI1 100 Hz
Write 2 : FPI2 HX.RHC
Write 3 : FPI3 IFLIP
Write 4 : FPI4 IFLOP
Write 5 : PLS routine started on LAM from GPPC in N22

8) N11 : Dual Outputregister

2 * 25-pair cable to DOR driver LINAC V
in RA170 NIM crate slot 1 (A + B)

9) N12 : Dual Outputregister

2 * 25-pair cable to DOR driver LINAC W
in RA170 NIM crate slot 2 (A + B)

10) N13 : Dual Outputregister

2 * 25-pair cable to DOR driver INJECTION KICKERS
in RA170 NIM crate slot 3 (A + B)

11) N14 : Dual Outputregister

2 * 25-pair cable to DOR driver EJECTION KICKER 49
in RA170 NIM crate slot 4 (A + B)

12) N15 : Dual Outputregister

2 * 25-pair cable to DOR driver EJECTION KICKER 51
in RA170 NIM crate slot 5 (A + B)

13) N16 : Dual Outputregister

2 * 25-pair cable to DOR driver INSTRUMENTATION
in RA170 NIM crate slot 6 (A + B)

14) N17-N18 : SMACC (IKBOX)

FPI1	: from 100 HZ µP Int in N8	(TTLbar)
FPI2	: from timing ditributor HX.RHC	(TTLbar)
FPI3	: IFLIP special purpose	(TTLbar)
FPI4	: IFLOP special purpose	(TTLbar)

15) N19 : PLS Receiver PLS-LPI

source : timing distributor

16) N22 : GPPC used to generate LAM after delay to start user PLS routine

Start IN : HX.FBP (TTLbar) from Timing Central
Clock IN : HX.TCL (BLO) from Timing Central

NIM Connections

1) Slot 1 : DOR Driver LINAC V

connected to selectors in RA167

2) Slot 2 : DOR Driver LINAC W

connected to selectors in RA168

3) Slot 3 : DOR Driver INJECTION KICKERS

connected to selectors in RA169

4) Slot 4 : DOR Driver EJECTION KICKER 49

connected to selectors in RA171

5) Slot 5 : DOR Driver EJECTION KICKER 51

connected to selectors in RA172

6) Slot 6 : DOR Driver INSTRUMENTATION and e+ / e- lines

output A out 2/5 generates HX.SBAC & HX.EBAC
output B out 1/2 gives complementary e+/e- line

7) Slot 9 : NIM / TTL 50 Ω converter

IN1 : BIT0 from NIM slot 10 out 1
IN2 : BIT1 from NIM slot 10 out 2
IN3 : BIT2 from NIM slot 10 out 3
IN4 : HX.TREV from CAMAC N9 out 9

OUT1 : BIT0 (TTL/50Ω) to Beam Scope in LPI control Room
OUT2 : BIT1 (TTL/50Ω) to Beam Scope in LPI control Room
OUT3 : BIT2 (TTL/50Ω) to Beam Scope in LPI control Room
OUT4 : HX.TREV to console LPI via patch in RA173 (273107)

8) Slot 10 : NIM fanout

IN1 : BIT 0 from RA170 CAMAC N6
IN2 : BIT 1 from RA170 CAMAC N6
IN3 : BIT 2 from RA170 CAMAC N6

OUT1-2-3 : to NIM slot 9 and slot 13

9) Slot 11 : NIM/TTL 50Ω converter

IN1 : HX.TREV form RA170 CAMAC N9 out4
OUT1 : HX.TREV to LPI Control Room

IN2 : HX.TREV form RA170 CAMAC N9 out6
OUT2 : HX.TREV to Beam Scope in LPI Control Room

10) Slot 12 : NIM / TTL 50 Ω converter

IN1 : BIT0 from NIM slot 10 out 1 (right)
IN2 : BIT1 from NIM slot 10 out 2 (right)
IN3 : BIT2 from NIM slot 10 out 3 (right)

OUT1 : BIT0 (TTL/50Ω) to Instrumentation in EB1
OUT2 : BIT1 (TTL/50Ω)
OUT3 : BIT2 (TTL/50Ω)

IN4 : RF from RA170 CAMAC N2 OUT 2
OUT4 : to Instrumentation in EB1

6.2 PATCH PANEL

0	0	0	0	0	0	0	0

RF Instrum	RF from EPA	HX.TREV to EPA	HX.TPG Instrum	BIT 0	BIT 1	BIT 2	
0	0	0	0	0	0	0	0

HX.TPG to RA047	RF to sync rad						
0	0	0	0	0	0	0	0

6.3 LPI FAST TIMING SEQUENCER (IKBOX) CONTROL PROGRAM DESCRIPTION

6.3.1 General

The LPI Fast Timing Sequencer (IKBOX) is build up from a standard SMACC configuration : SMACC CAMAC module + RMS68K operating system. There are no equipment modules resident in this SMACC. The software in the IKBOX consists of an initialisation part and 4 ISR's (Interrupt Service Routines) linked to the 4 Frontpanel Interrupts and the standard PLS handler. Because RMS68K is a multitasking system, it is possible to add if necessary real-time embedded diagnostic programs, but this is not foreseen in the initial stage. More general information about the working of the IKBOX and the way how to fill the datatables can be found in a separate note PS/CO/NOTE 86-009 : LPI Fast Timing Sequencer (IKBOX) and Datatable Editor.

6.3.2 Initialisation

The initialisation is run in principle only once at cold startup. It is responsible for a) setting all the variables in a predetermined initial state, b) connecting the 4 ISR's to the correct Frontpanel interrupts, c) initialising the PLS routines, loading the GPPC in N22 with the correct values and connecting the PLS routines to LAM 22 (GPPC) and d) putting the IKBOX in a WAIT state. During normal operation of the IKBOX this WAIT state is only interrupted by the 4 Frontpanel Interrupts and the PLS-LAM. Other events external to the IKBOX could also interrupt the WAIT state at a lower priority e.g. : NODAL interpreter, serial communication links, etc. The 4 ISR's linked to the Frontpanel Interrupts are the Real-Time routines in the IKBOX. Except for the Power-Fail feature they run at the highest possible priority, so that all other software running in the SMACC will always be interrupted by an FPI-ISR. All 4 FPI-ISR's have the same priority so that once an FPI-ISR is running , it cannot be interrupted by another FPI-ISR. The 2nd FPI-ISR will queue up until the 1st FPI-ISR has finished execution.

6.3.3 FPI1 : 100 Hz µP Int

This FPI-ISR is the most frequently used and also the most important. It comes every 10 ms at about 2 ms after every zerocrossing of the 50 Hz mains. This routine will set the state of the machine for every LIL Period. This routine first checks whether the IKBOX is in the DUMMY state or not. There are 2 possible ways to put the IKBOX in the DUMMY state RSDUM and NRDUM. RSDUM (ReSettable DUMmy) is used by the ISR itself if some anomaly is detected e.g. : corrupted or out of bound parameters. Whem for example a Basic Period Nr of 68 is read (max = 63), the IKBOX will put the LPI by means of the Timing System in a predetermined DUMMY state and report the error to the operator. However in order not to block the whole system for a temporary or spurious fault, the RSDUM state is reset on every Start Cycle (FPI2). The RSDUM feature can be regarded as a dynamic internal security system. The NRDUM (Non Resettable DUMmy) on the contrary is a facility offered to the user to force the LPI by means of the Timing system in the DUMMY state for an undetermined period of time. The user can put the IKBOX in the NRDUM state only by actually overwriting the NRDUM variable. The only way to reset the IKBOX to the normal state is to overwrite the NRDUM variable again or to do a general

initialisation of the IKBOX. This NRDUM option is incorporated in the IKBOX software to create a possibility to stop all beam production in the LPI by pushing only one button. The IKBOX will be put in the DUMMY state immediately (max 2 ms) after the NRDUM variable has been overwritten. Then the correct CST line is fetched from memory. The nr of the CST line to be fetched depends on a) Basic Period nr, b) LIL Period offset in the chosen Basic Period. The value at this memory location gives the nr of CST line to fetch. Every used variable is checked for out of bound errors. Then the injection and ejection scheme is fetched and depending of the offsets in these schemes the correct bucket numbers are fetched and output to the 19 MHz Clock Generator in the same CAMAC crate. If up to now no errors are detected, the data in the selected CST line is also output to the Dual Output Registers. If during one of the out-of-boundery checks an anomaly is detected, the IKBOX will be put in the RSDUM state for the rest of the cycle. To be able to monitor the errors, a diagnostic tool is provided. A special purpose array DIAGN is reserved. Every error check has a sequence nr. If during for example error check nr 22 an inconsistency is detected, the 22nd place in the array will be incremented by 1. This allows to see how many times a specific error occured. Also a general error counter (place 0) is incremented by 1. This allows a quick check to see if an error has been detected at all or not. This array DIAGN is reset to 0 only at initialistion of the IKBOX. As a consequence can this array be used as a permanent error log for the IKBOX. After all the data has been output, a last check is performed to see whether the Basic Period is self-terminating or not. A Basic Period that is not self-terminating will expect a Start Cycle Interrupt (FPI2) to switch over to the next Basic Period. If the LIL Period counter exceeds the max nr of programmed LIL Periods in the programmed Basic Period, this will result in an error and the IKBOX will go in the DUMMY state. A Basic Period that is self-terminating does not wait for FPI2 to switch over to the next Basic Period. As soon as the LIL Period counter reaches the max nr of programmed LIL Periods in the Basic Period, the IKBOX will read immediately the contents of the last LPI-PLS and update the Basic Period numbers and the injection and ejection scheme. The status whether the IKBOX is in the Normal (IFLIP) or Spare (IFLOP) state is maintained during the switchover, the injection scheme counter is also not reset to allow for a smooth changeover from one Basic Period to the next one. The self-termination option is used during long accumulations (i.e. normally Basic Periods that do not include an ejection).

6.3.4 FPI2 : Start Cycle

This ISR copies the new Normal (FLIP) Basic Period nr, the Spare (FLOP) Basic Period nr, the injection scheme nr and the ejection scheme nr from the Temporary values to the Operational values. The internal counters and RSDUM are all reset. The current Basic Period nr is set equal to the Spare Basic Period nr.

6.3.5 FPI3 : IFLOP (ISPARE HX.RST0)

The current Basic Period nr is overwritten by the Spare (FLOP) Basic Period nr. The use of the FLIP-FLOP mechanism is described more detailed in PS/CO/NOTE 86-009 The LPI Fast Timing Sequencer and Datatable Editor.

6.3.6 FPI4 : IFLIP (INORMAL HX.RAC)

The current Basic Period nr is overwritten by the NORMAL (FLIP) Basic Period nr.

6.3.7 PLS Handler

This task is reponsible to get the information out of the PLS and store the Normal Basic Period nr, Spare Basic Period nr, injection and ejection scheme nr into the Temporary values T_NBP , T_SBP , T_INS and T_EJS .

6.3.8 Software maintenance

This Control Program is written in M68mil assembler and runs under RMS68K in the version which is used in the PS Control System. In the following paragraph a list is given of the steps to follow if a modification has to be made to this program. The source file of this program can be found under <PRDEV>(RT-LPI)M68-IKBOX:SYMB.

1) Editing can be done by PED.
2) As a backup file one can use (RT-LPI)M68-BACKUP-IKBOX:SYMB
3) Assembling is done on the PRDEV under RT-LPI

   @XCOM (M68)/MODE M68-IKBOX L <CR> or new routine by J. Lewis

4) Construct SMACC IMAGE

   @XCOM (M68)/MODE IMA-IKBOX L <CR> or new routine by J. Lewis

   The resulting binary file is placed in <PRDEV>(VOL)IKBOX:BIN
   The cross-reference listing is produced on the Lineprinter if requested.

5) This binary file has to be transferred to the destination FEC (LIL) with the RT-NODAL program <PRDEV>TRANS
   The destination file on the FEC is <LIL>(A-A)ACC36:BIN

6) From the destination FEC the binary file can be loaded in the SMACC with the RT-NODAL Program (A-A)INIT-IKBOX:NOD
   This program also reloads the tables. .

7) The IKBOX is located in LIL Loop 2 crate 19
   The SMACC nr is 36

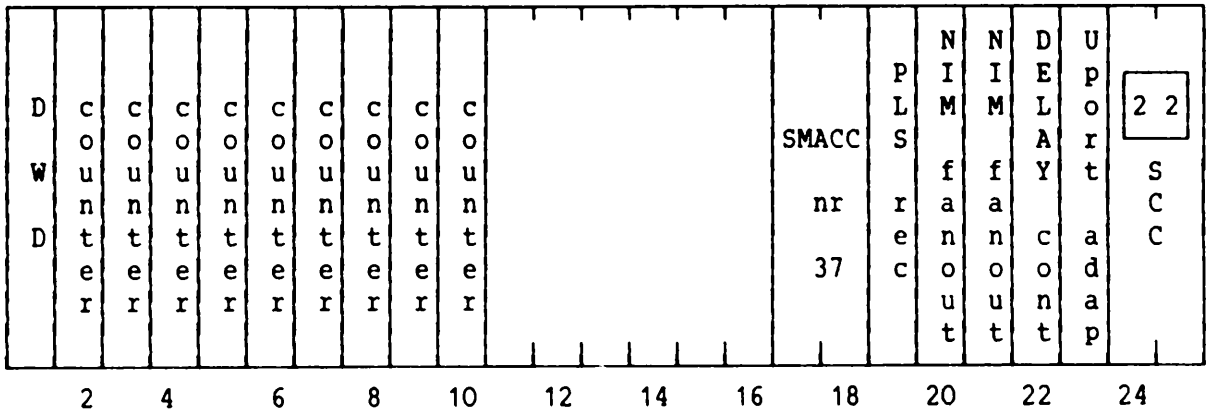
CHAPTER 7

EJECTION KICKER 49

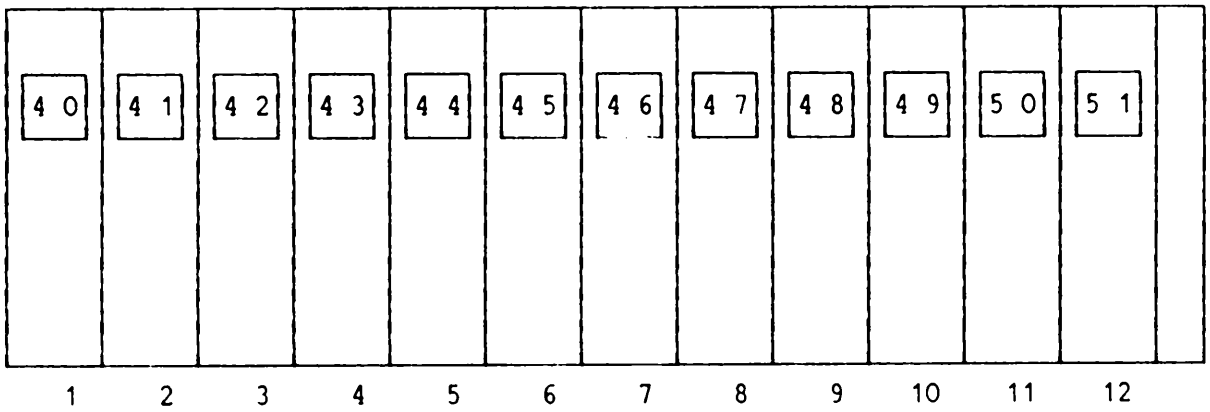
7 EJECTION KICKER 49

LIL LOOP 2 CRATE 22 RACK NR: RA171

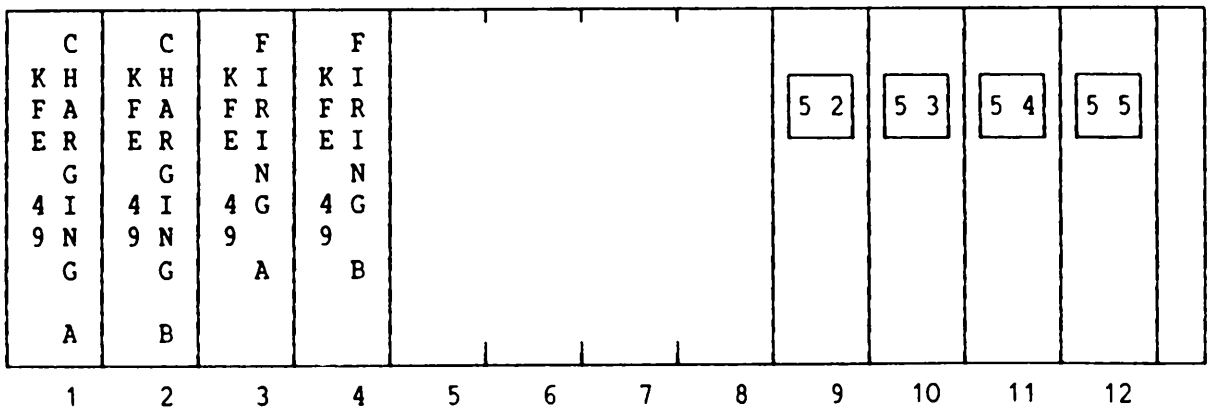
CAMAC CRATE



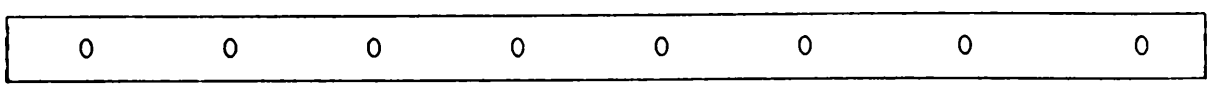
DELAY LINES



SELECTORS / LINE DRIVERS



PATCH PANEL



7.1 COUNTERS

PTIM						
Eq. nr.	Equipment name	CAMAC				Description
		L	C	N	A	
151	HX.WKFE49A	2	22	2	0	KFE49 charging line A
152	HX.WKFE49B			2	1	KFE49 charging line B
153	HX.SKFE49A1EC			3	0	KFE49 firing A1 e^-
154	HX.SKFE49A1PC			3	1	KFE49 firing A1 e^+
155	HX.SKFE49A2EC			4	0	KFE49 firing A2 e^-
156	HX.SKFE49A2PC			4	1	KFE49 firing A2 e^+
157	HX.SKFE49A3EC			5	0	KFE49 firing A3 e^-
158	HX.SKFE49A3PC			5	1	KFE49 firing A3 e^+
159	HX.SKFE49A4EC			6	0	KFE49 firing A4 e^-
160	HX.SKFE49A4PC			6	1	KFE49 firing A4 e^+
161	HX.SKFE49B1EC			7	0	KFE49 firing B1 e^-
162	HX.SKFE49B1PC			7	1	KFE49 firing B1 e^+
163	HX.SKFE49B2EC			8	0	KFE49 firing B2 e^-
164	HX.SKFE49B2PC			8	1	KFE49 firing B2 e^+
165	HX.SKFE49B3EC			9	0	KFE49 firing B3 e^-
166	HX.SKFE49B3PC			9	1	KFE49 firing B3 e^+
167	HX.SKFE49B4EC			10	0	KFE49 firing B4 e^-
168	HX.SKFE49B4PC			10	1	KFE49 firing B4 e^+
169	spare					not used
170	spare					not used

E J E C T I O N K I C K E R 4 9

7.2 DELAY LINES

P T I M						
Eq. nr.	Equipment name	CAMAC				Description
		L	C	N	nr	
171	HX.SKFE49A1EF	2	22	22	40	fine delay HX.SKFE49A1E
172	HX.SKFE49A1PF				41	fine delay HX.SKFE49A1P
173	HX.SKFE49A2EF				42	fine delay HX.SKFE49A2E
174	HX.SKFE49A2PF				43	fine delay HX.SKFE49A2P
175	HX.SKFE49A3EF				44	fine delay HX.SKFE49A3E
176	HX.SKFE49A3PF				45	fine delay HX.SKFE49A3P
177	HX.SKFE49A4EF				46	fine delay HX.SKFE49A4E
178	HX.SKFE49A4PF				47	fine delay HX.SKFE49A4P
179	HX.SKFE49B1EF				48	fine delay HX.SKFE49B1E
180	HX.SKFE49B1PF				49	fine delay HX.SKFE49B1P
181	HX.SKFE49B2EF				50	fine delay HX.SKFE49B2E
182	HX.SKFE49B2PF				51	fine delay HX.SKFE49B2P
183	HX.SKFE49B3EF				52	fine delay HX.SKFE49B3E
184	HX.SKFE49B3PF				53	fine delay HX.SKFE49B3P
185	HX.SKFE49B4EF				54	fine delay HX.SKFE49B4E
186	HX.SKFE49B4PF				55	fine delay HX.SKFE49B4P
187	spare					not used
188	spare					not used
189	spare					not used
190	spare					not used

7.3 CABLING

LIL LOOP 2 CRATE 22 ***RACK NR: RA171***

CAMAC crate external connections
---

1) N20 IN : NIM fanout 9050 : RF.EJ

   source: Rack RA170 CAMAC crate N4 out5 (NIM fanout 9050)

2) N21 IN : NIM fanout 9050 : HX.FEJ (= start EJ. counters)

   source: Rack RA170 CAMAC crate N8 TTL / NIM out 1

3) SMACC FPI1 : not used

   source:

4) SMACC FPI2 : not used

   source:

5) SMACC FPI3 : not used

   source:

6) SMACC FPI4 : not used

   source:

7) N19 PLS-RECEIVER : PLS-LPI

   source: Timing distributor

8) M / L / P - connections on the selector/line drivers

   source: RA170 NIM crate DOR-driver NIM slot 4

Internal connections

- N20 NIM fanout for RF.EJ . Every output is connected with the CLOCK of the counter in the respective slot
  e.g.: out2 is connected with the clock of N2

- N21 NIM fanout for Start EJ. counters. Every output is connected with the START of the counter in the respective slot.

- N22 DELAY LINE controller. The controller is connected in daisy chain with all the delay lines in the rack

E J E C T I O N K I C K E R 4 9

7.4 PATCH PANEL

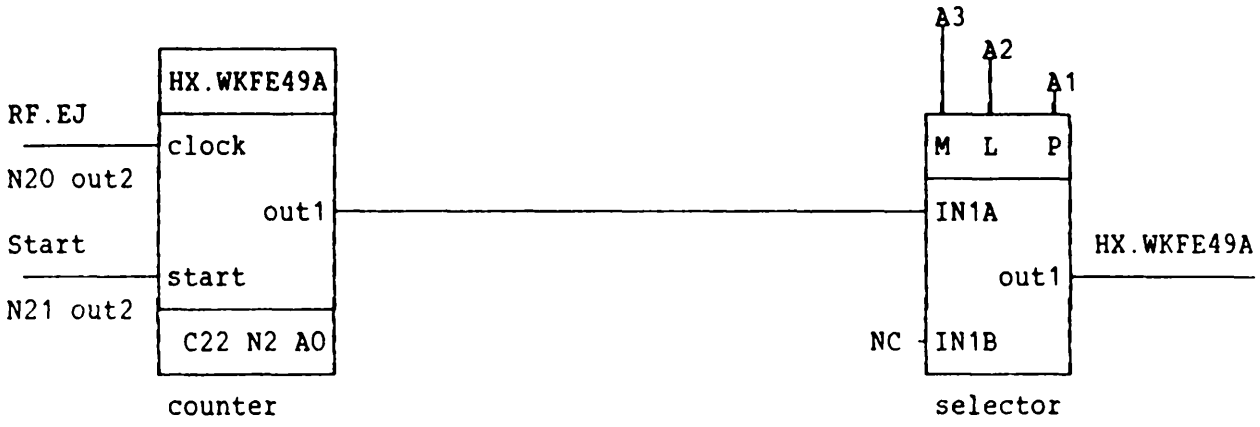
	HX. SKFE49A3		HX. SKFE49B3				
0	0	0	0	0	0	0	0

HX. WKFE49B	HX. SKFE49A2		HX. SKFE49B2				
0	0	0	0	0	0	0	0

HX. WKFE49A	HX. SKFE49A1	HX. SKFE49A4	HX. SKFE49B1	HX. SKFE49B4			
0	0	0	0	0	0	0	0

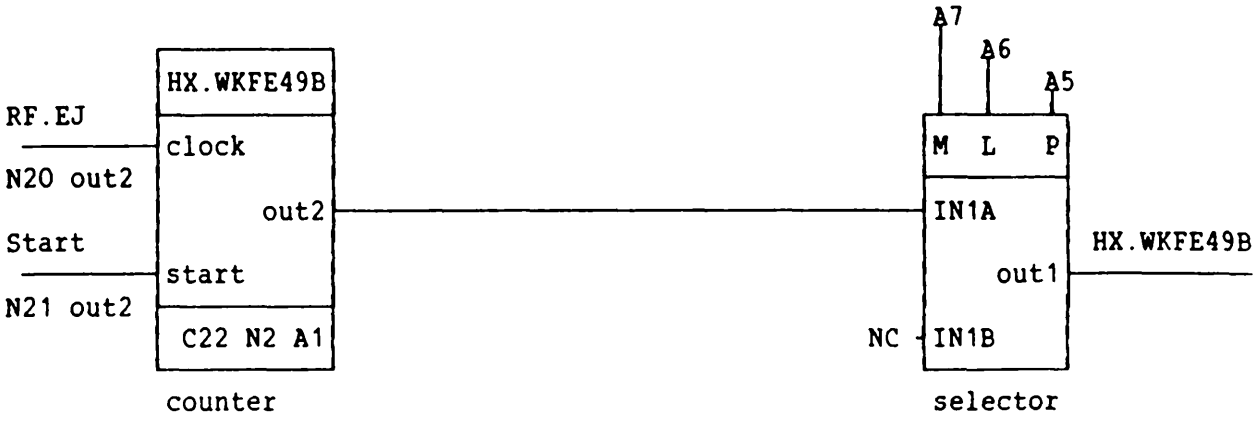
7.5 TIMINGS

7.5.1 KFE 49 CHARGING A



selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

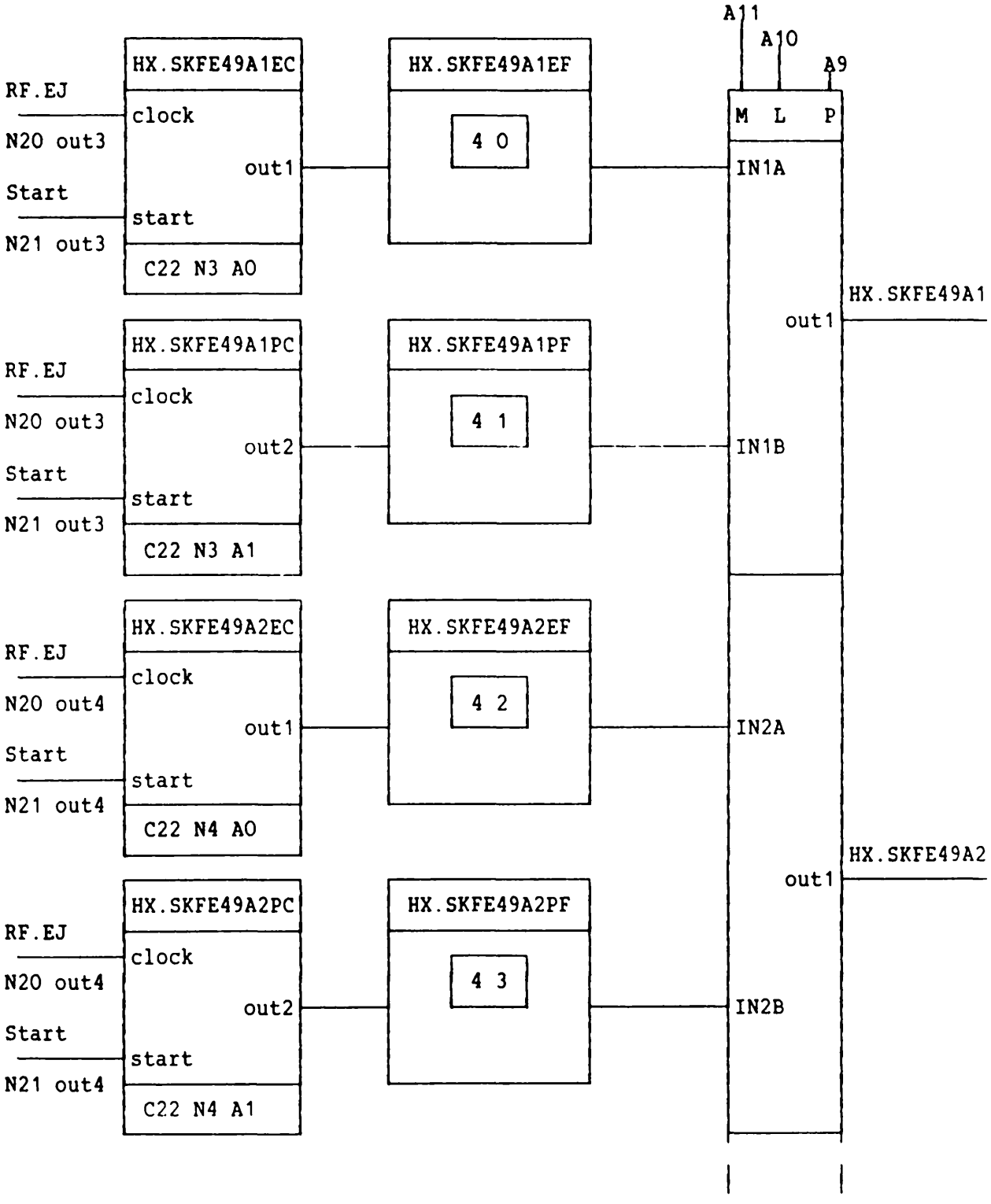
7.5.2 KFE 49 CHARGING B



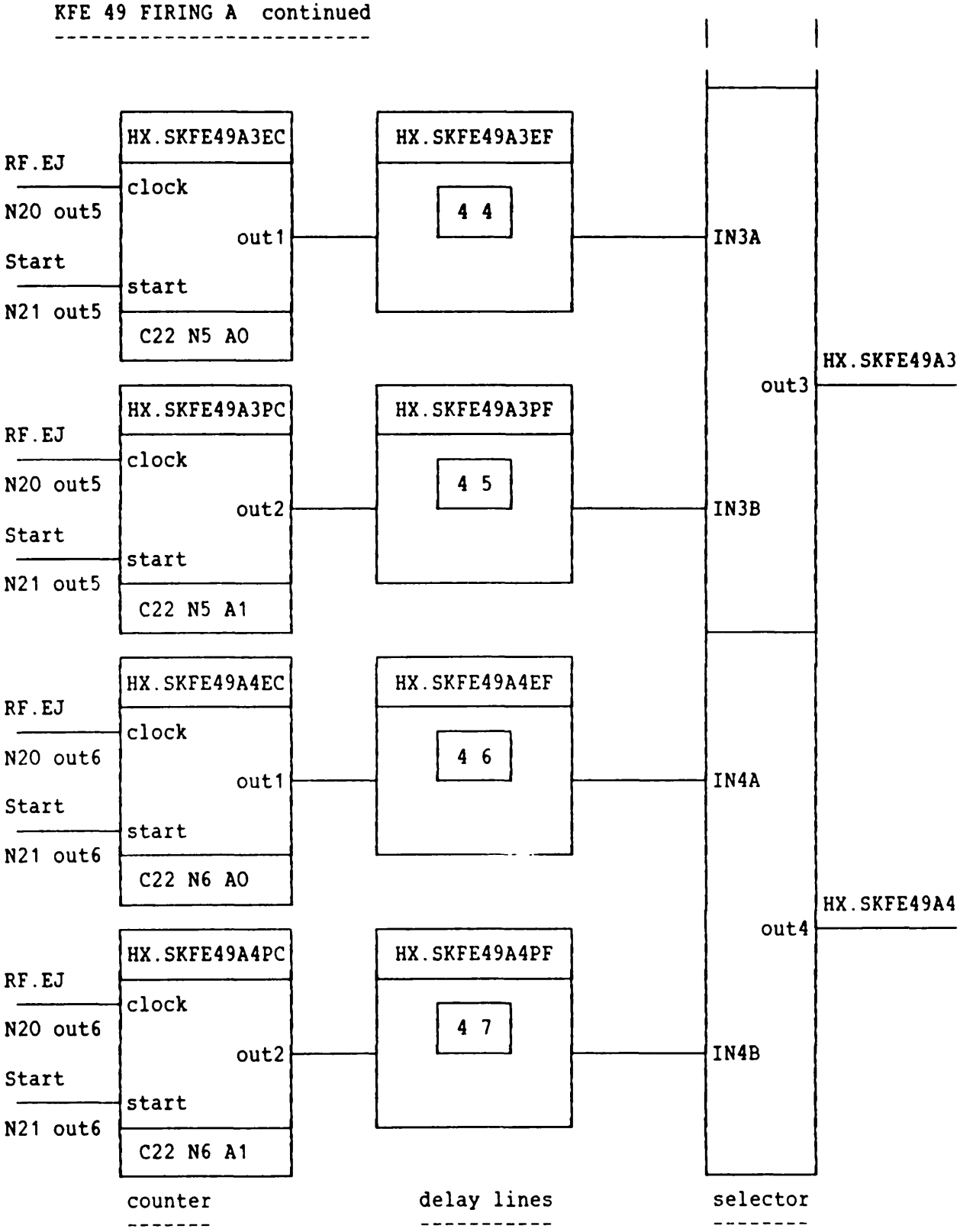
selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

E J E C T I O N K I C K E R 4 9

7.5.3 KFE 49 FIRING A

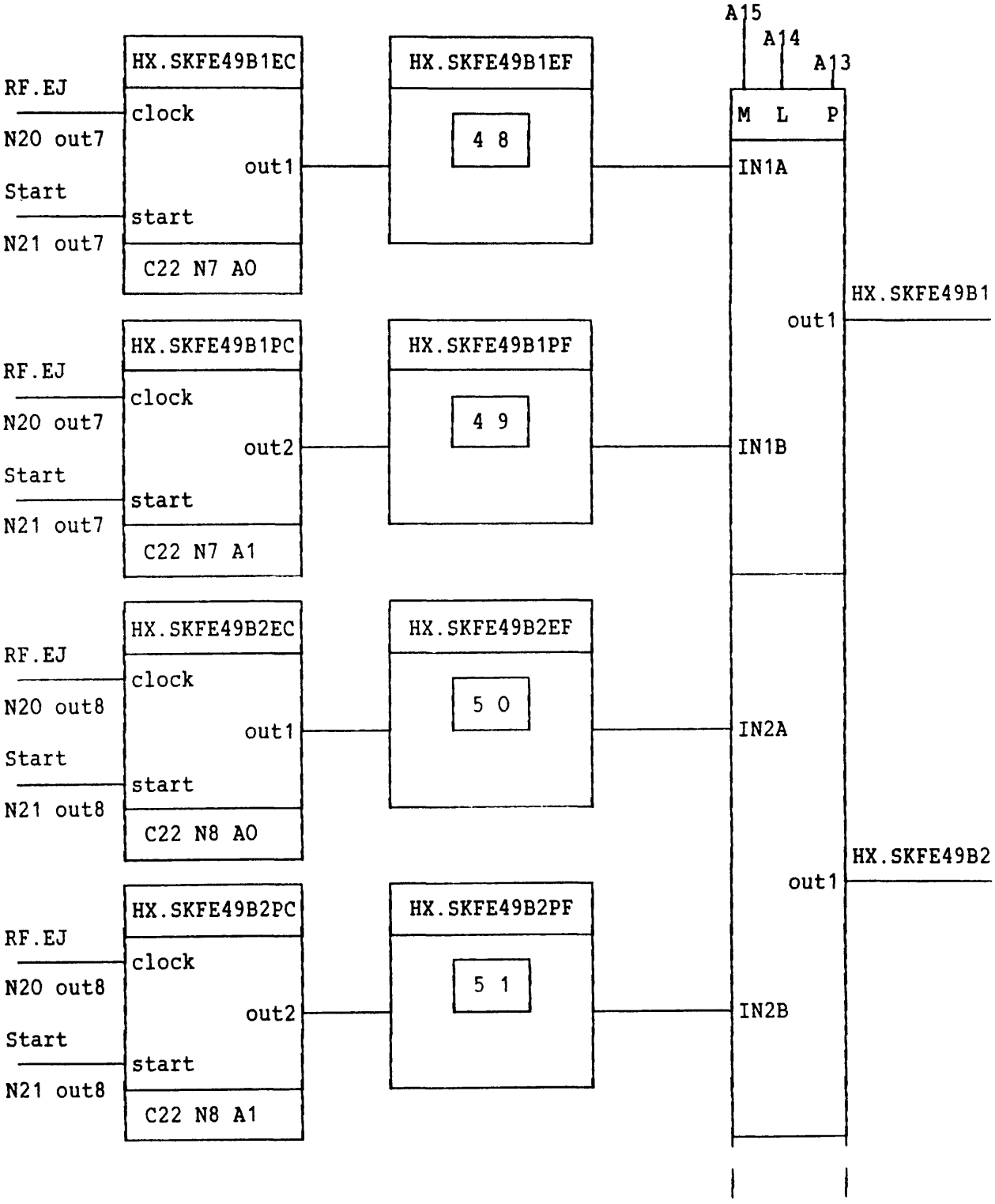


KFE 49 FIRING A continued

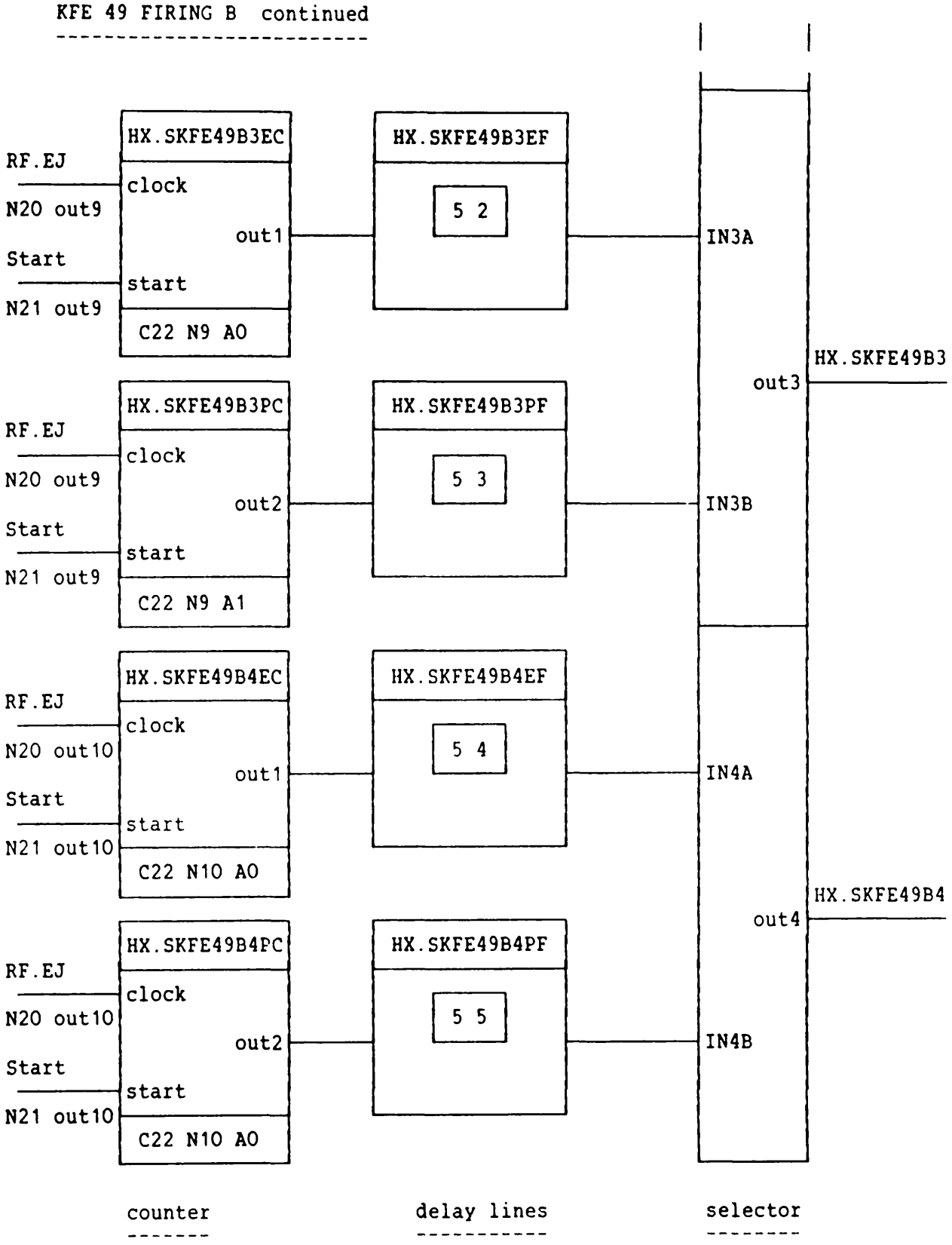


selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

7.5.4 KFE 49 FIRING B



KFE 49 FIRING B continued



selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

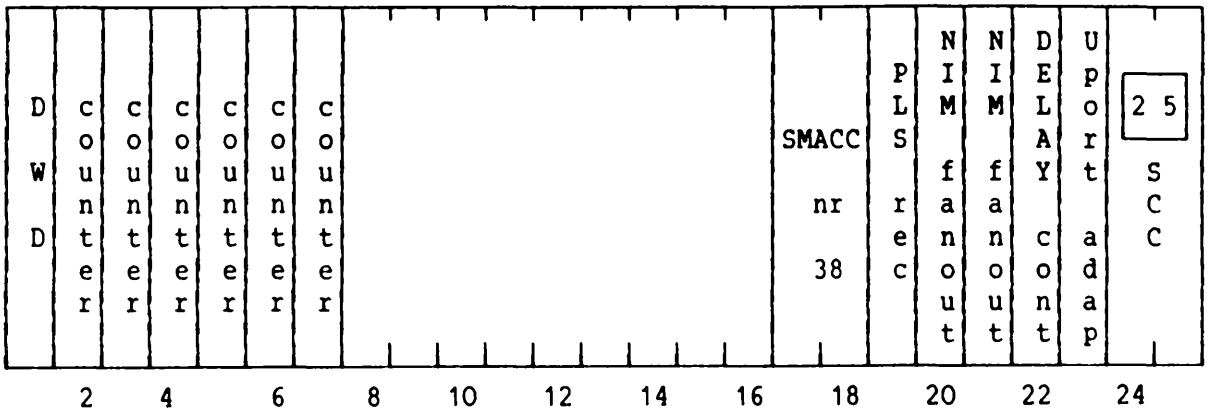
CHAPTER 8

EJECTION KICKER 5.1

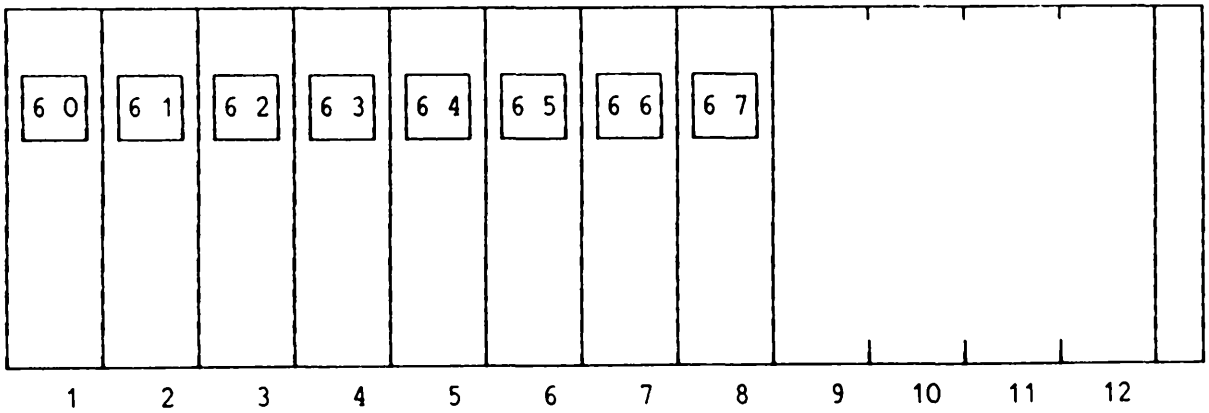
8 EJECTION KICKER 51

LIL LOOP 2 CRATE 25 *RACK NR: RA172*

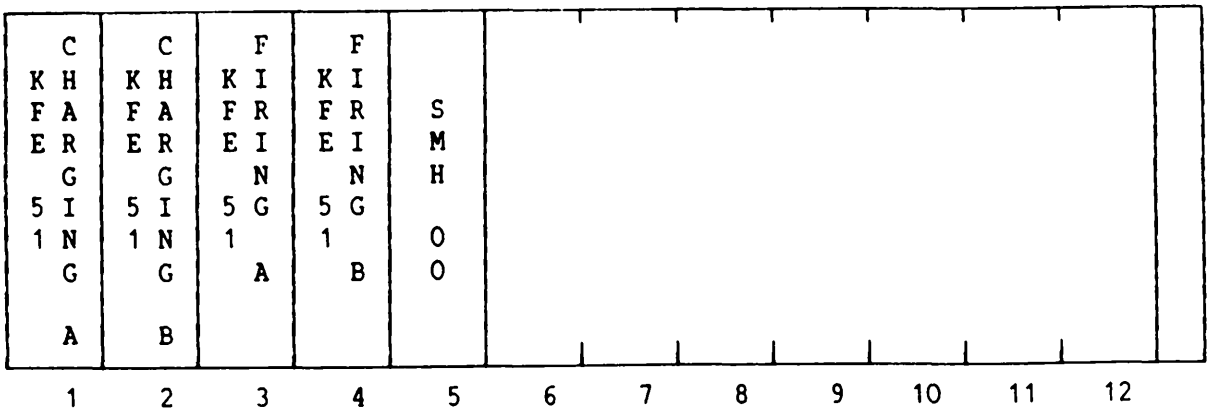
CAMAC CRATE



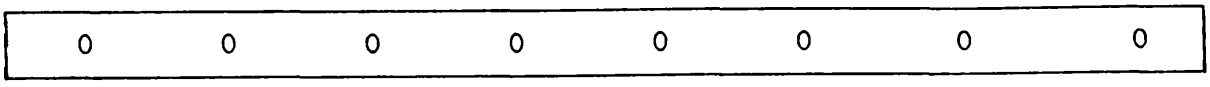
DELAY LINES



SELECTORS / LINE DRIVERS



PATCH PANEL



8.1 COUNTERS

P T I M						
Eq. nr.	Equipment name	CAMAC				Description
		L	C	N	A	
201	HX.WKFE51A	2	25	2	0	KFE51 charging line A
202	HX.WKFE51B			2	1	KFE51 charging line B
203	HX.SKFE51A1C			3	0	KFE51 firing A1
204	HX.SKFE51A2C			3	1	KFE51 firing A2
205	HX.SKFE51A3C			4	0	KFE51 firing A3
206	HX.SKFE51A4C			4	1	KFE51 firing A4
207	HX.SKFE51B1C			5	0	KFE51 firing B1
208	HX.SKFE51B2C			5	1	KFE51 firing B2
209	HX.SKFE51B3C			6	0	KFE51 firing B3
210	HX.SKFE51B4C			6	1	KFE51 firing B4
211	HX.SSMH00C			7	0	Start SMH00
212	HX.SKFE			7	1	Measure SMH00
213	spare					not used
214	spare					not used
215	spare					not used
216	spare					not used
217	spare					not used
218	spare					not used
219	spare					not used
220	spare					not used

8.2 DELAY LINES

P T I M						
Eq. nr.	Equipment name	CAMAC				Description
		L	C	N	nr	
221	HX.SKFE51A1F	2	22	25	60	fine delay HX.SKFE51A1
222	HX.SKFE51A2F				61	fine delay HX.SKFE51A2
223	HX.SKFE51A3F				62	fine delay HX.SKFE51A3
224	HX.SKFE51A4F				63	fine delay HX.SKFE51A4
225	HX.SKFE51B1F				64	fine delay HX.SKFE51B1
226	HX.SKFE51B2F				65	fine delay HX.SKFE51B2
227	HX.SKFE51B3F				66	fine delay HX.SKFE51B3
228	HX.SKFE51B4F				67	fine delay HX.SKFE51B4
229	spare					not used
230	spare					not used
231	spare					not used

8_3_CABLING

LIL LOOP 2 CRATE 25 *RACK NR: RA172*

CAMAC crate external connections
---

1) N20 IN : NIM fanout 9050 : RF.EJ

   source: Rack RA170 CAMAC crate N4 out6 (NIM fanout 9050)

2) N21 IN : NIM fanout 9050 : HX.FEJ (= start EJ. counters)

   source: Rack RA170 CAMAC crate N8 TTL/NIM out 2

3) SMACC FPI1 : not used

   source:

4) SMACC FPI2 : not used

   source:

5) SMACC FPI3 : not used

   source:

6) SMACC FPI4 : not used

   source:

7) N19 PLS-RECEIVER : PLS-LPI

   source: Timing distributor

8) M / L / P - connections on the selector/line drivers

   source: RA170 NIM crate DOR-driver NIM slot 5

Internal connections

- N20 NIM fanout for RF.EJ . Every output is connected with the CLOCK of the counter in the respective slot
  e.g.: out2 is connected with the clock of N2

- N21 NIM fanout for Start EJ. counters. Every output is connected with the START of the counter in the respective slot.

- N22 DELAY LINE controller. The controller is connected in daisy chain with all the delay lines in the rack

E J E C T I O N K I C K E R 5 1

8.4 PATCH PANEL

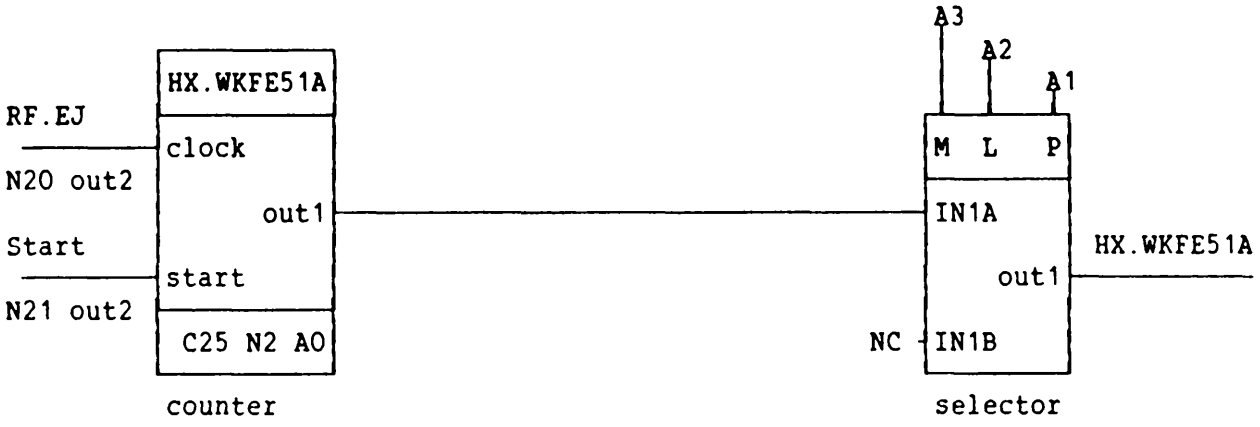
	HX. SKFE51A3		HX. SKFE51B3				
0	0	0	0	0	0	0	0

HX. WKFE51B	HX. SKFE51A2		HX. SKFE51B2		HX. SSMH00		
0	0	0	0	0	0	0	0

HX. WKFE51A	HX. SKFE51A1	HX. SKFE51A4	HX. SKFE51B1	HX. SKFE51B4	HX.SKFE		
0	0	0	0	0	0	0	0

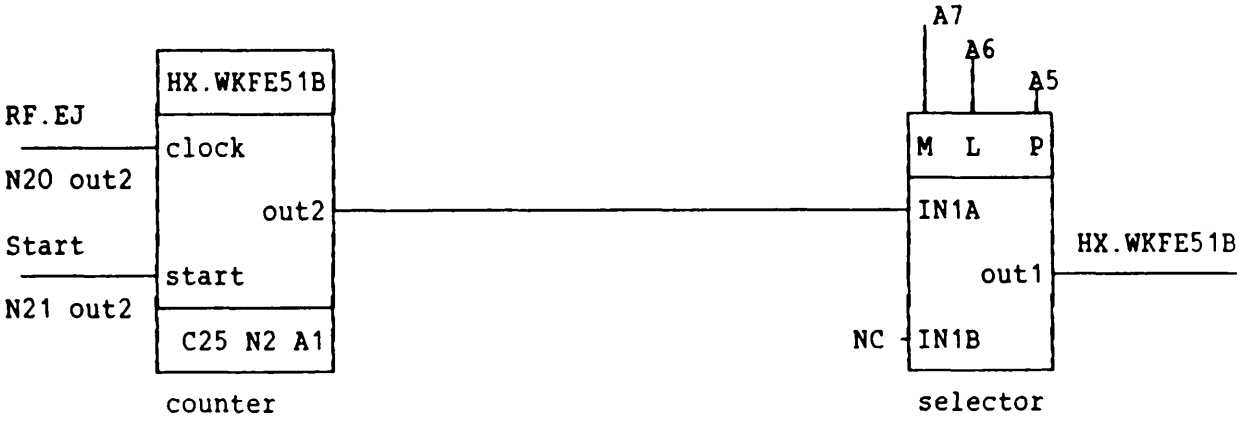
8.5 TIMINGS

8.5.1 KFE 51 CHARGING A



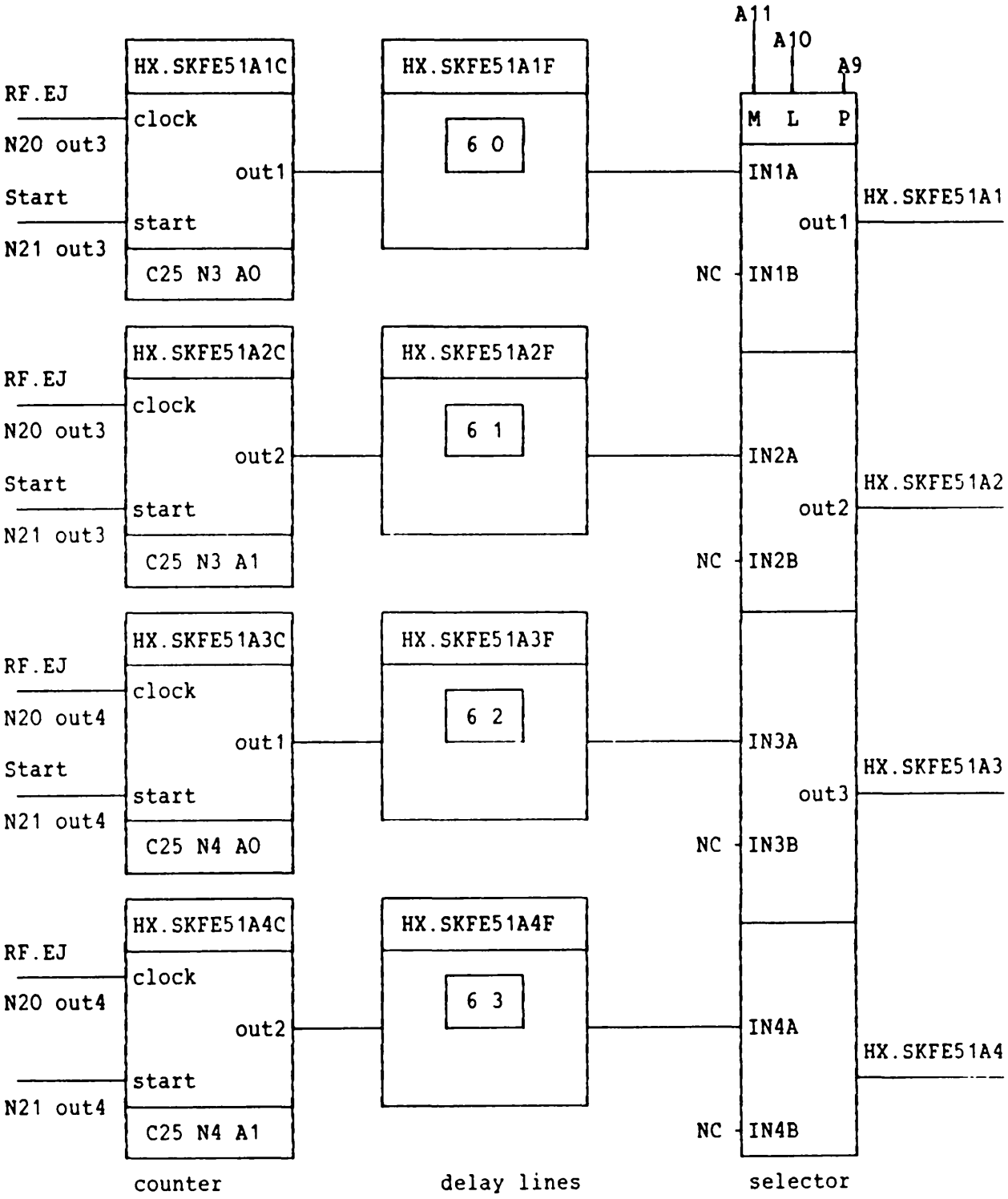
selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

8.5.2 KFE 51 CHARGING B



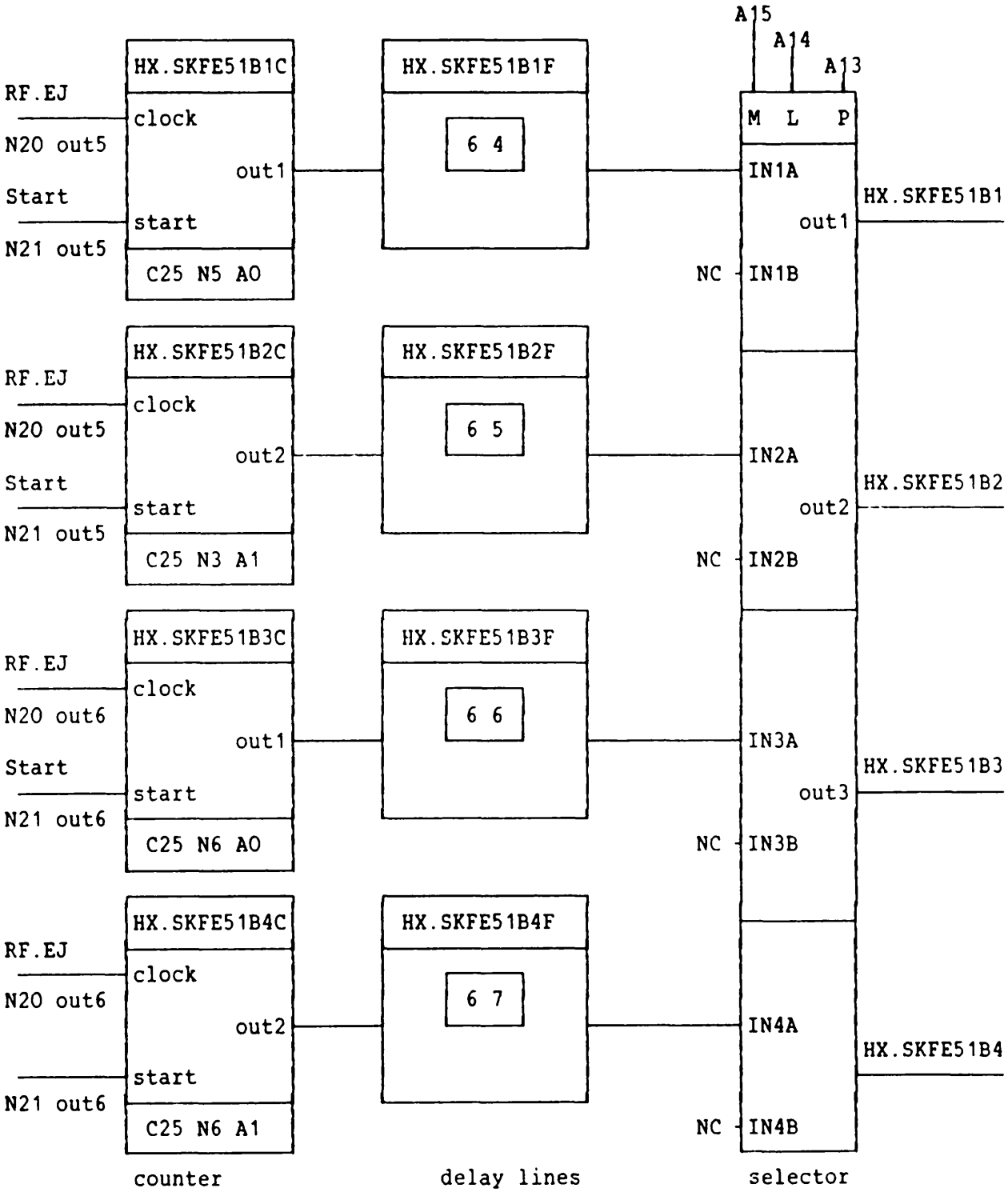
selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

8.5.3 KFE 51 FIRING A



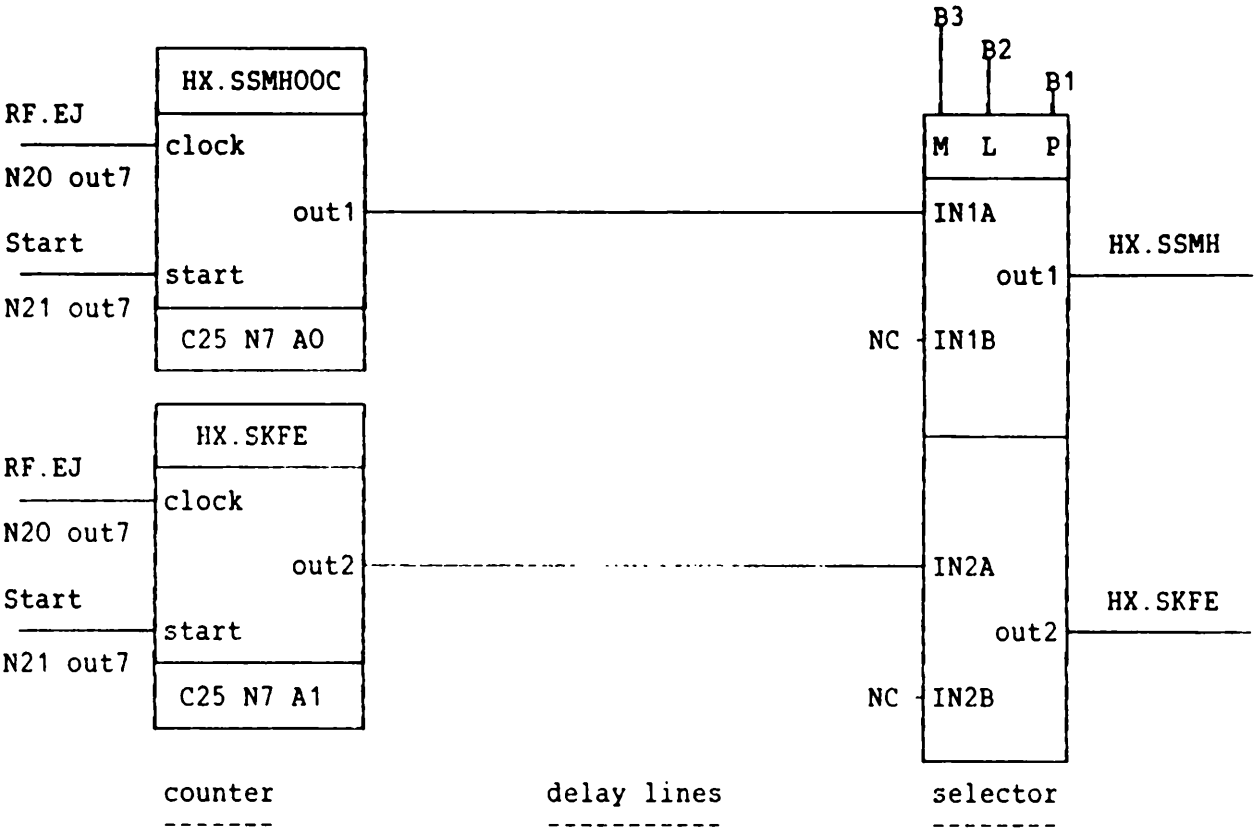
selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

8.5.4 KFE 51 FIRING B



selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

8.5.5 SMH 00



selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

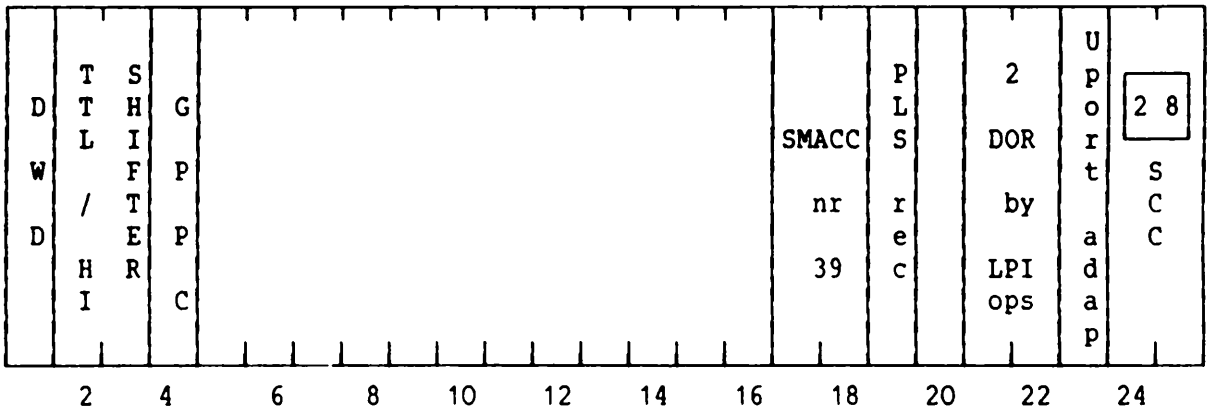
CHAPTER 9

INSTRUMENTATION

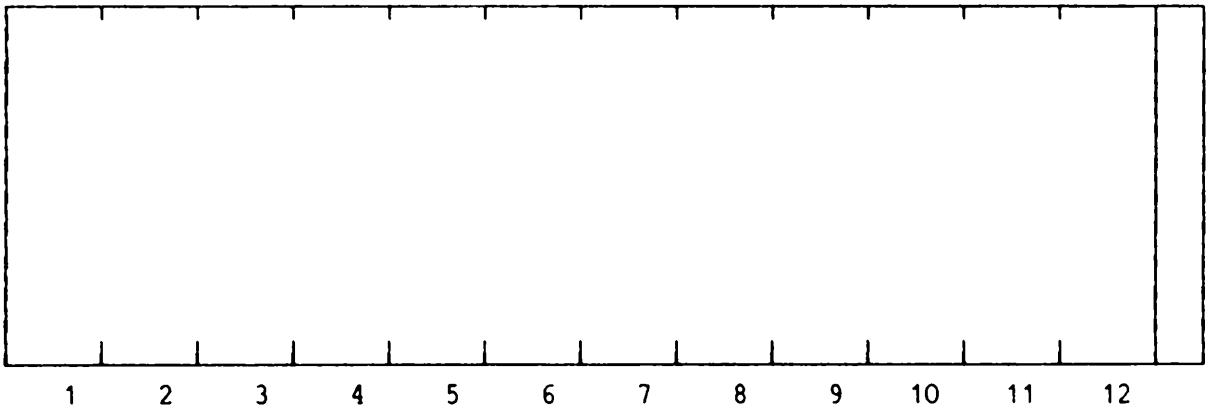
9 INSTRUMENTATION

LIL LOOP 2 CRATE 28 *RACK NR: RA173*

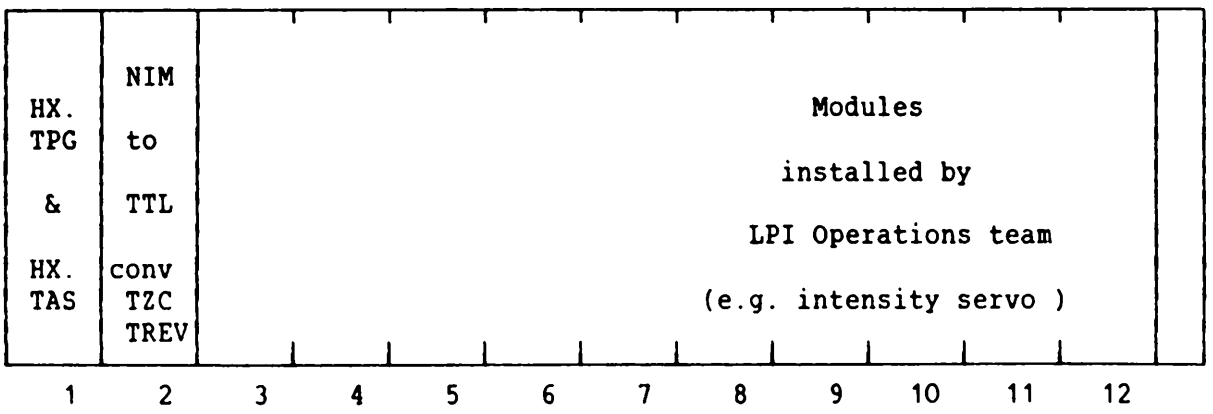
CAMAC CRATE



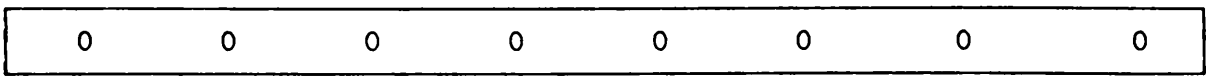
DELAY LINES



SELECTORS / LINE DRIVERS



PATCH PANEL



9.1 COUNTERS

P T I M						
Eq. nr.	Equipment name	CAMAC				Description
		L	C	N	A	
251	HX.AS (GPPC)	2	28	4	0	Pulse Acquisition Supplies -1ms
252	spare			4	1	not used
253	spare					not used
254	spare					not used
255	spare					not used
256	spare					not used
257	spare					not used
258	spare					not used
259	spare					not used
260	spare					not used

9.2 DELAY LINES

P T I M						
Eq. nr.	Equipment name	CAMAC				Description
		L	C	N	nr	
261	spare	2	28	22	80	not used
262	spare				81	not used

9.3 CABLING

LIL LOOP 2 CRATE 28 ***RACK NR: RA173***

CAMAC crate external connections
---

3) SMACC FPI1 : not used

source:

4) SMACC FPI2 : not used

source:

5) SMACC FPI3 : not used

source:

6) SMACC FPI4 : not used

source:

7) N19 PLS-RECEIVER : PLS-LPI

source: Timing distributor

8) M / L / P - connections on the selector/line drivers

source: RA170 NIM crate DOR-driver NIM slot 6

Internal connections

9.4 PATCH PANEL

BACK OF THE RACK

0	0	0	0	0	0	0	0

HX.TPG							
0	0	0	0	0	0	0	0

HX.AS (SNP25)	HX.AS (KFI's)						
0	0	0	0	0	0	0	0

9.5 TIMINGS

9.5.1 ON-OFF BUMPERS (HX.EBAC & HX.SBAC)

The purpose of HX.EBAC and HX.SBAC can be found in "Specifications du timing pour les bumpers de EPA/ P. Burla PS/CO/WP 85-060". The 2 timing pulses are generated by using 2 output lines of the Dual Output Register Drivers as input for 2 channels of a TTL/HI level shifter. A 0 to 1 transition in TTLbar will generate a blocking output pulse. By means of the IKBOX one can program for the equipment names SBAC and EBAC 2 possible states : Production and Dummy. The Production state will output the value 0 or binary 0000 and the Dummy state outputs the value 1 or binary 0001 on the lines A4-A1 for SBAC (lines A8-A5 for EBAC) of the Dual Output Register Drivers for the Instrumentation via the DOR in RA170 slot 16. A programmed changeover from Dummy to Production will generate a 0 to 1 transition on line A1 for SBAC and A5 for EBAC, which is used after level shifting as HX.SBAC and HX.EBAC. (see fig : On/Off Bumpers Timing). These 2 timings are generated in the window of 8-6 ms before the next beam production, before which the bumpers have to be in the new state.

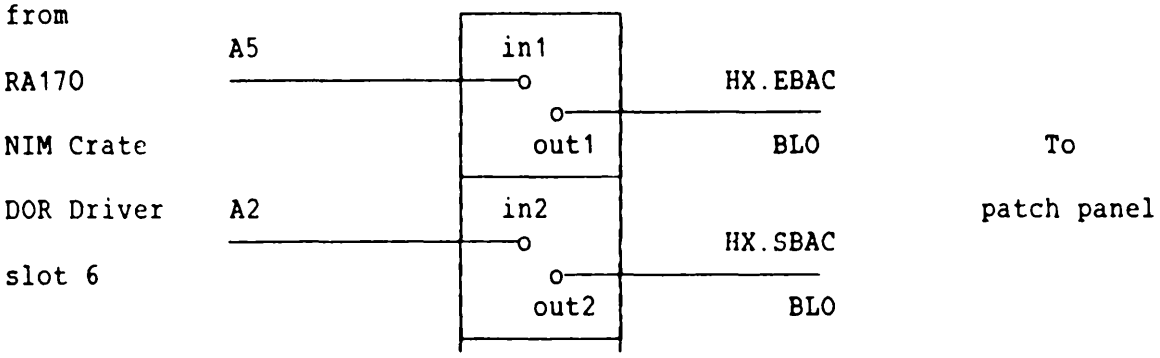
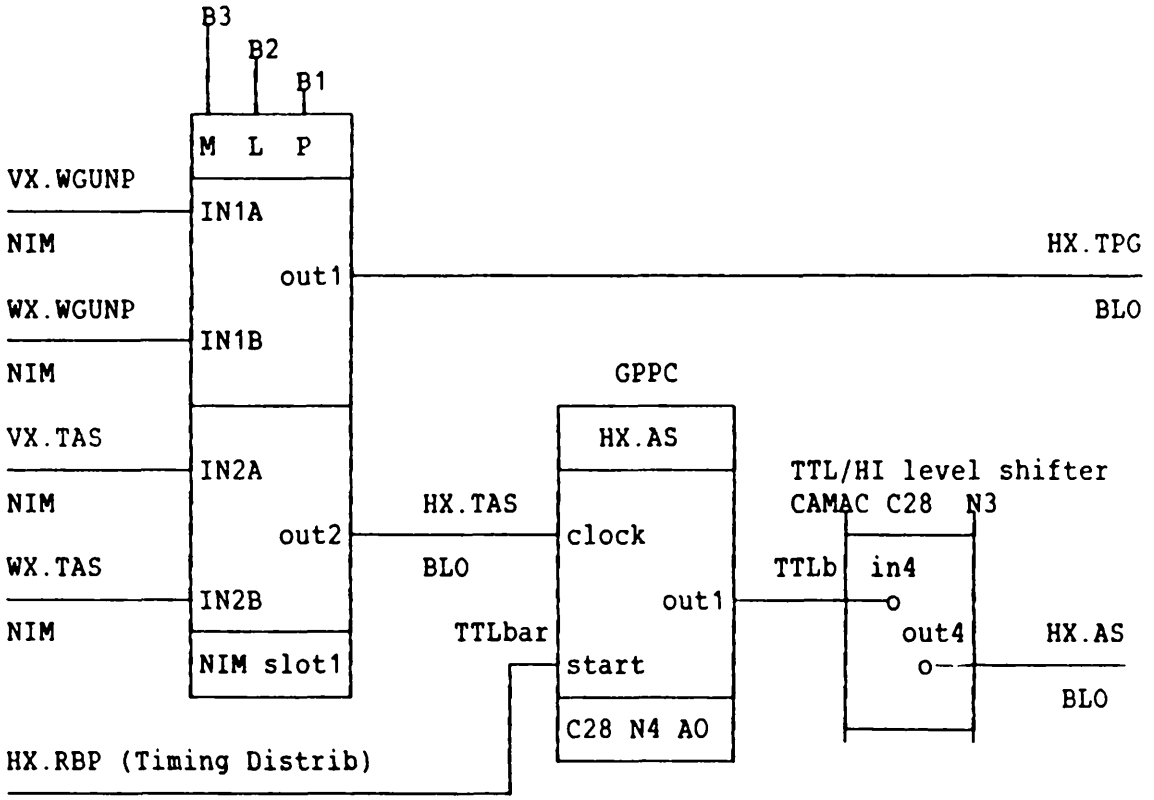


FIG : ON/OFF BUMPERS TIMING

9.5.2 TRAIN GUN PRODUCTION (HX.TPG) & TIMING ACQUISITION SUPPLIES (HX.AS)

The train HX.TPG, Production Gun Train, is a train which is synchronous with the real beam in the Linacs. This train gives only pulses out when the active Gun is pulsed in Production. Each Gun, Gun V and Gun W, generates a train synchronous with the Start Gun pulse if pulsed in Production. The 2 trains, VX.WGUNP and WX.WGUNP, are produced by the Selector/linedrivers of the specific Gun. In a second Selector/linedriver, in rack RA173 (NIM slot 1), the choice is made between VX.WGUNP and WX.WGUNP, depending of the value programmed in the IKBOX (fig: HX.TPG & HX.AS)



selector straps connections			
11-out 12-in 13-in	21-out 22-in 23-in	31-out 32-in 33-in	41-out 42-in 43-in

FIG : HX.TPG & HX.AS

In order to produce HX.AS, first a train HX.TAS is generated in a identical way as HX.TPG. The train HX.TPG is derived from the 2 local trains VX.TAS and WX.TAS .The only difference between these 2 trains is that they are shifted in time : HX.TPG = -2μs and HX.TAS = -1ms relative to the beam. This train HX.TAS is used as the clock for a GPPC, which has as the start pulse HX.RBP.

Depending of the value N in the counter, one does a measurement/acquisition on the Nth Production pulse in every Basic Period. In this way only one measurement/acquisition is done in every Basic Period.

9.5.3 HX.TZC & HX.TREV TO TIMING CENTRAL

HX.TZC is used in the Central Timing to generate a C-train in phase with the 50 Hz mains and also to synchronize C-timings on the accumulation timing. HX.TREV is used in the Central Timing to generate timings more precise than 1 ms prior to ejection towards CPS.

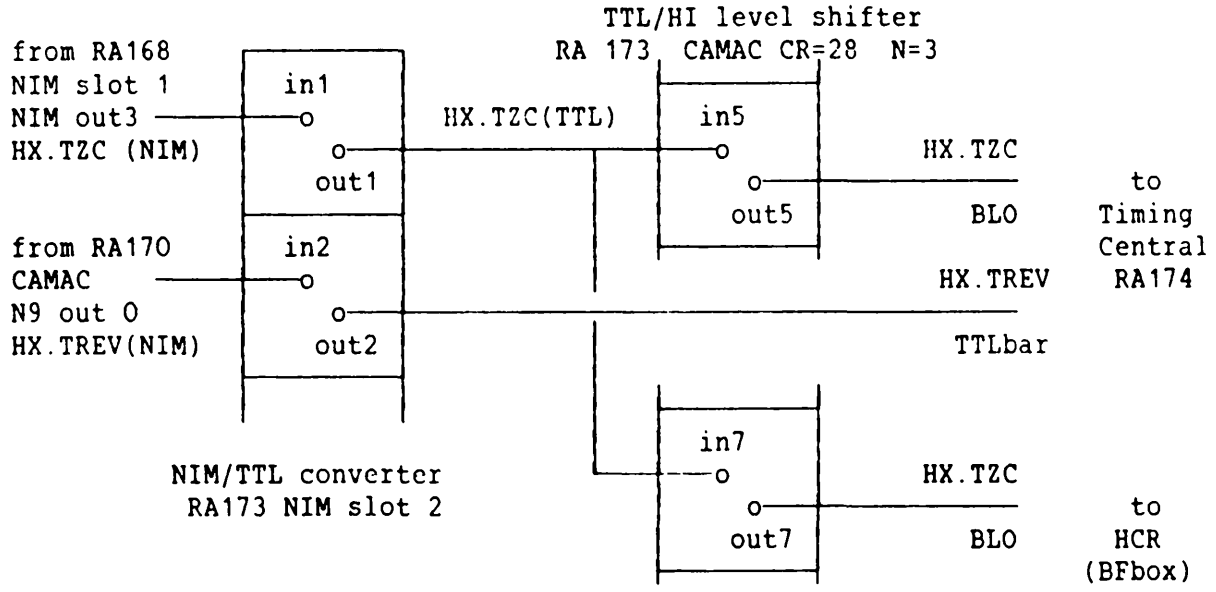


FIG : HX.TZC & HX.TREV

I N S T R U M E N T A T I O N

CHAPTER 10

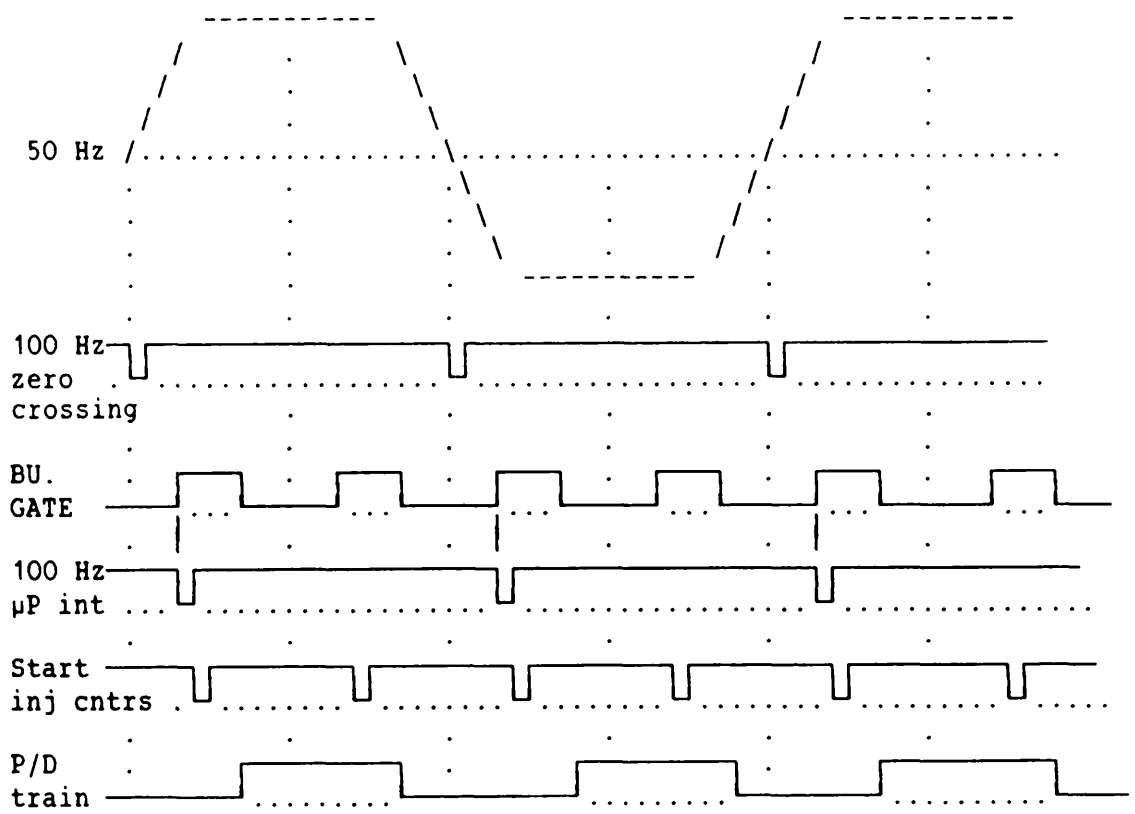
DESCRIPTION OF HARDWARE MODULES

10 DESCRIPTION OF HARDWARE MODULES

10.1.19 MHZ CLOCK GENERATOR LF 80142C0

The purpose of this specially designed CAMAC module (P. Perriraz) is to synchronise the accumulation timing on the zerocrossings of the 50 HZ mains. The only input in this mode is the 50 HZ coming from a transformer that transforms the 220V/phase S (green) to a 2V level. This transformer is situated just under the NIM crate in rack nr RA170. The outputs are: 1) BU.GATE to gate the 19 MHZ RF in the 19 MHZ Clock Generator HF 2) Start injection Counters (4) 3) 100HZ µP Int serves as FPI1 for the IKBOX 4) P/D train to synchronise the selector/linedrivers with the 50Hz mains (4). (fig: Timing Diagram)

TIMING DIAGRAM



Two additional TTL/NIM converters are foreseen. They are used for the start ejection counters and have no connection with the 50 Hz.

The two LED's 50 Hz R and S indicate wether the used 50 Hz is the real 50 Hz from the mains or an internally simulated 50 Hz. If the internal simulation is used all phase relation with the mains is lost of course.

INPUT

50 HZ : 2V / 50 Hz Hz internally terminated with 1KΩ to +5V
TTL/NIM : TTLbar

OUTPUT

50 Hz : TTLbar 100 HZ zerocrossings of the mains
BU.GATE : TTLbar to clockgenerator HF
100 HZ µP Int : TTLbar to FPI1 of IKBOX
Start inj cntr(4): NIM/50Ω
P/D train (4) : TTL / 50
TTL / NIM (2) : NIM/50Ω to ejection counters

CAMAC ACCESS

none

ref : 19 MHz Clock Generator LF. Description fonctionelle.
P. Perriraz PS/CO/Note 86-033

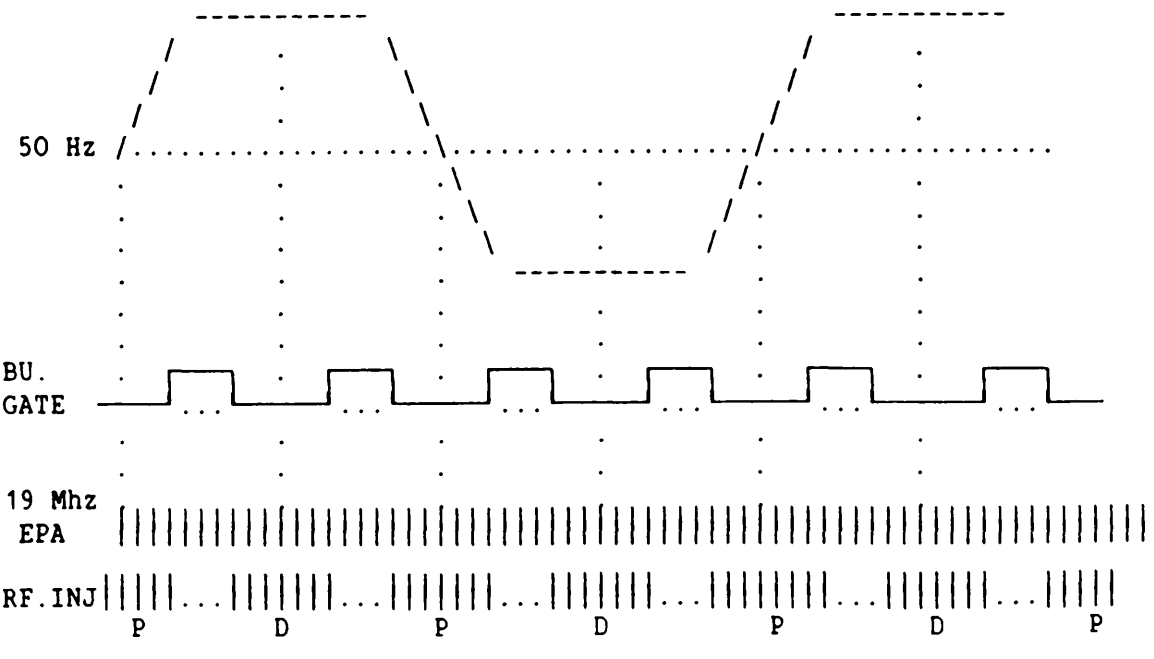
10.2 19 MHZ CLOCK GENERATOR HF 80373C0

The purpose of this specially designed CAMAC module is to provide the clock trains for the counters of the LPI 19 MHz Fast Timing system. The whole 19 MHz Fast Timing system can be divided in 2 parts: the accumulation timing (LIL + injection kickers) and the ejection timing (ejection kickers + ejection septum). These 2 parts are asynchronous. They only link between these 2 parts is the bucket wheel counter i.e. the 3-bit counter that labels the 8 buckets in EPA with a number (0-7). The common input for the 2 parts is the 19 MHz RF from the EPA-RF system. This frequency is used as the basic clock because the EPA-RF system determines the exact location of the 8 buckets circulating in the EPA. All the timings generated are relative to the phase of the EPA-RF. The 2 parts will now be desribed in more detail.

ACCUMULATION

This part will generate the clock for the counters used for Linac V, Linac W and the injection kickers. The main inputs are the EPA-RF, the BU.GATE from the 19 MHz Clock Generator LF and the bucket nr coming via the CAMAC dataway and send by the SMACC (IKBOX). The BU.GATE comes at a frequency of 200 Hz and gates the EPA.RF. The fine gating is accomplished by the injection bucket nr which is send by the IKBOX synchronous with the 50 Hz mains. This will synchronise the start of the RF.INJ burst with the bucket nr in which one wants to inject in the next LIL period. This bucket nr can change every 10 ms. A burst of 3 ms is produced every 5 ms. The bursts synchronized with the zerocrossings of the mains 50 Hz are used to produce the Production timings, the bursts synchronous with the tops are used to generate the Dummy timings.(fig: Timing diagram)

TIMING DIAGRAM



EJECTION

The ejection is only a single shot event and is not synchronised with the mains 50 Hz. The output of the 19 Mhz Clock Generator HF is a single burst of 19 MHz (RF.EJ) triggered by the warning ejection (WEJ) input. This signal is coming from the PS timing and is called HX.WEJ. The output burst is fine synchronised on the ejection bucket nr coming from the SMACC (IKBOX).

A second signal generated by the ejection part is the RF.COR . This is a train of continuous RF/8 synchronised with the first bucket to be ejected. This train is called HX.TREV . Tis train is used in the PS to synchronise the PS-RF on the EPA-RF and on the first bucket from EPA to be accepted.

Besides all these clocks a few other general trains are produced:

1) RF.CONT : 19 MHz continuous RF

2) BIT 0,1,2 : output of the 3 bit bucket counter to be used in the instrumentation

3) Start.ej : the OR-ed signal of WEJ and SWEJ

also 2 extra control signal are foreseen:

1) RESET : reset bucket nr. gives the possibility to synchronise the 3 bit bucket counter on an external event

2) SWEJ : simulated warning ejection . idem as WEJ

On the frontpanel in the bottom 2 LEDs display the state of thc 19 MHz RF input:

1) R : real 19 MHz is OK

2) S : real 19 MHz is not OK but is simulated by an internal oscillator of the same frequency. If the 19 MHz is internally simulated , the timings are changed not very much, but of course every phase relation with the EPA-RF is lost. The main use of the simulation is to operate the 2 Linacs in standalone mode without EPA.

INPUT

```
RF        : TTLbar 19 MHz EPA-RF internally terminated with 50Ω
            to ground
RESET     : TTLbar stops the 3 bit bucket counter term intern
            1KΩ to +5V
WEJ       : TTLbar terminated internally with 1KΩ to +5V
SWEJ      : TTLbar terminated internally with 1KΩ to +5V
```

OUTPUT

```
RF.CONT   : NIM/50Ω   19 MHz continuous
RF.INJ    : NIM/50Ω   19 MHz injection counters clock
RF.EJ     : NIM/50Ω   19 MHz ejection counters clock
RF.COR    : NIM/50Ω   19/8 MHz train continuous sync ejection bucket nr

BIT 0
BIT 1
BIT 2     : NIM/50Ω   3 bit bucket counter

Start Ejection : NIM/50 Ω    WEJ OR SWEJ
```

CAMAC ACCESS

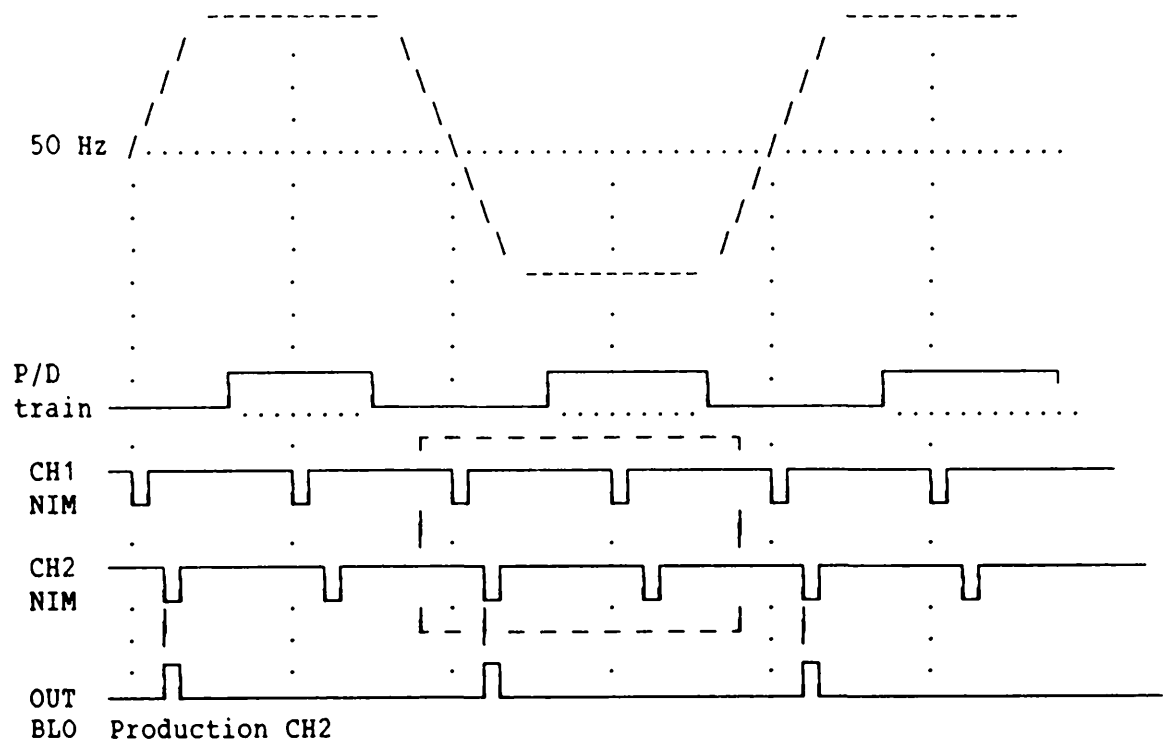
```
F16 A0 :  W1 - W3  : injection bucket nr
          W5 - W7  : ejection bucket nr


F0  A0 :  R1 - R3  : injection bucket nr readback
          R5 - R7  : ejection bucket nr readback
```

10.3 SELECTOR / LINE DRIVER (80299.C01)

The purpose of this special purpose developed module (by M. Sleptsov) is to choose for each channel (4 channels) 1 out of 4 possible NIM timing pulses and convert them to an isolated blocking level.

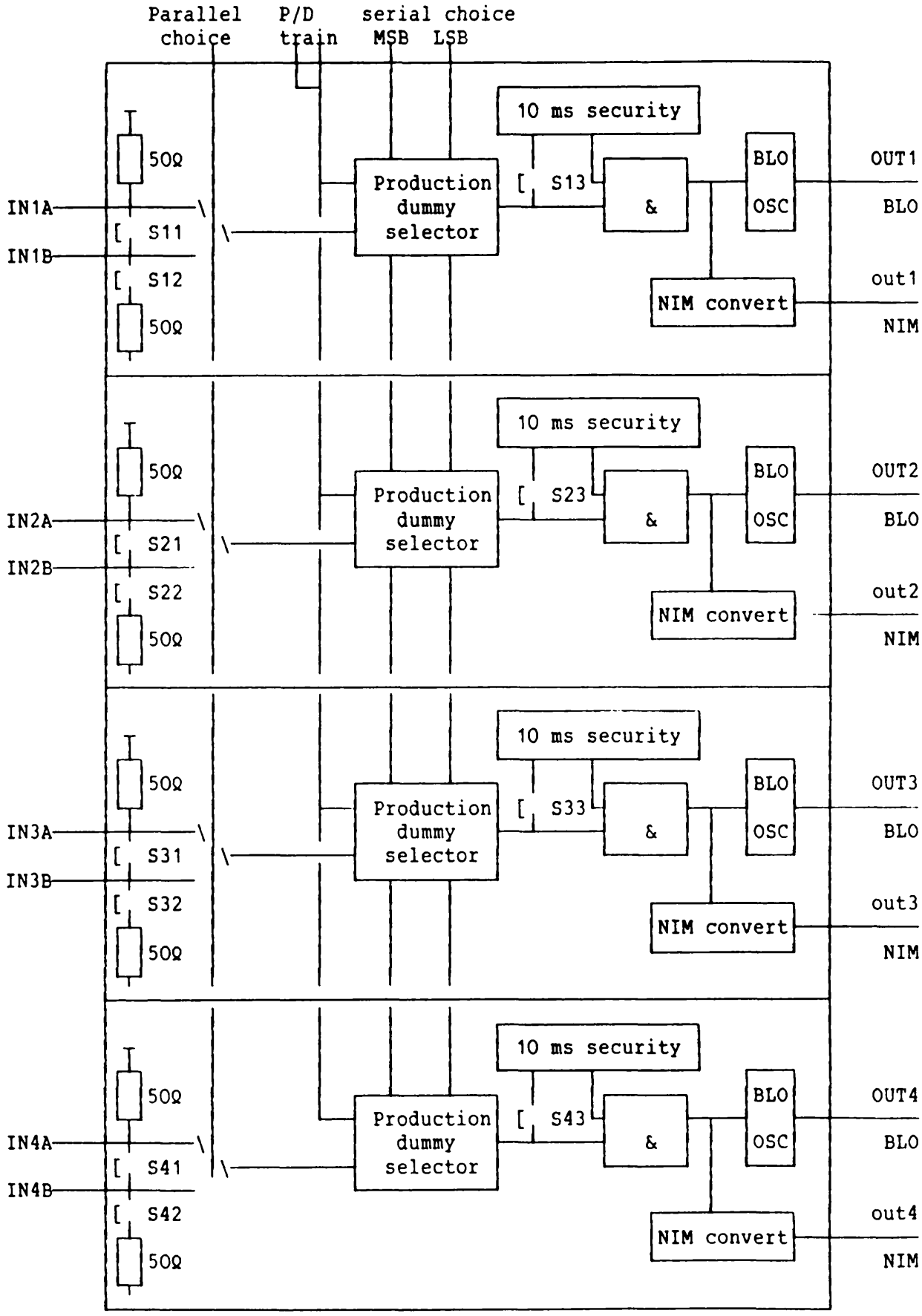
The linacs V an W of the LPI pulse at a frequency of 100 HZ (10 ms). Because this timeinterval is to small for the standard PLS a special purpose timing system is developed. One of the caracteristics of this timing system is that even when the real timings acting on the machines change of mode, the values in the counters and delay lines are not reloaded. Therefore all the possible timings are generated in parallel and depending of the modes of operation the machines are in , the correct timing is selected and transmitted to the equipment. For every equipment a choice can be made out of maximum 4 timings. The 4 timings enter on 2 lines and on every line 2 timing pulses are generated in series separated by 5 ms. The timing pulses that come on the same line have thus a frequency of 200 Hz and one is synchronized with the zerocrossings of the 50 Hz mains while the other is synchronized with the tops of the 50 Hz mains (fig : Timing diagram selector / line driver)

TIMING DIAGRAM SELECTOR/LINE DRIVER



The selector can choose 1 out of 4 timing pulses depending on the information on the 2 serial choice and 1 parallel choise inputs (fig : selector/line driver functional diagram).

SELECTOR / LINE DRIVER FUNCTIONAL DIAGRAM



```
Parallel choice  TTLbar
---------------
A +5V or open or logic 0       will select input A
A  0V or  50Ω or logic 1       will select input B


Serial choice    TTLbar
-------------
MSB =  0V =  50Ω = logic 1
LSB = +5V = open = logic 0       will select DUMMY output


MSB = +5V = open = logic 0
LSB =  0V =  50Ω = logic 1       will select PRODUCTION output
```

All other combinations will inhibit the output pulse.

DUMMY means the timing pulse on the selected input during the time the P/D train was logic 0 or +5V (on the tops of the mains 50Hz phase S)

PRODUCTION means the timing pulse on the selected input during the time the P/D train was logic 1 or 0V (on the zerocrossings of the mains 50 HZ phase S)

The use of straps in this module offered a greater flexibility and avoided the fabrication of different versions of the same module. It also avoided the use of the LEMO Y's which have appeared as unreliable. For every channel 3 straps are foreseen. Sx1 permits to connect INxA and INxB internally. Sx2 permits to terminate INxB with 50Ω. The purpose of Sx1 and Sx2 is to be able to have the same input on A and B without external cable and LEMO Y. This is especially usefull when only one channel out of 4 has a different timing for A and B (e.g. e^+ and e^-) and the 3 other channels have the same timing for A and B. In this case the 3 channels have Sx1 in and Sx2 out. The 4th channel has Sx1 out and Sx2 in. Because the parallel choice input will choose for the 4 channels the same input (A or B), for the 3 channels there is no difference, but the 4th channel is switched from A to B (e.g. e^+ to e^-). In the module a security is foreseen so that no 2 output pulses can come out that are separated by less than 8 ms. This is the normal case. There is nevertheless one exception namely the Booster Klystron which pulses continuously at a fixed frequency of 200 HZ (5ms), so in this case the security is not used and Sx3 is removed.(fig: layout of straps)

INPUTS

IN1A to IN4B : NIM internally terminated with 50Ω to ground

Serial choice (2)
Parallel choice : TTLbar internally terminated with 1KΩ to +5V

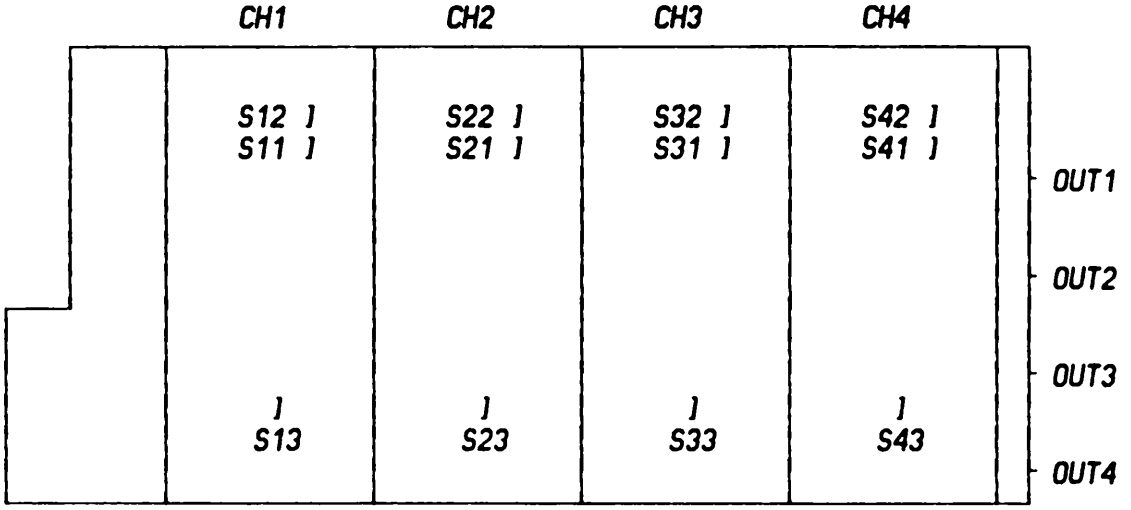
P/D train : TTLbar not internally terminated but has to be terminated with 50Ω at the end of the daisy chain

OUTPUTS

OUT1 to OUT4 BLO : Blocking level 16V/600ns to be terminated by 50Ω

DIAGN1 to DIAGN4 : NIM level to be terminated by 50Ω at the end

LAYOUT OF THE STRAPS



10.4 BOUCHERON PRESET COUNTER (MPS2002)