CPS94-RF #2
Réunion du 1/02/94

Présents : M. Arruat, G.P. Benincasa, R. Cappi, G. Cyvoct, G. Daems, Y. Deloose, R. Garoby, F. Giudici, W. Heinze, J. Lewis, P. Maesen, F. Di Maio, F. Pedersen, F. Perriollat, J.P. Riunaud, C. Serre, L. Sermeus, J.P. Terrier, J.L. Vallet

cc: J. Boucheron, S. Hancock

Ordre du jour :

- Le P.L.S.: évolution au cours des 12 derniers mois, et prévisions pour l'avenir (G. Daems)
- Le M.T.G. et le module TG8: principe et caractéristiques essentielles (J. Lewis)

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1. Sujets préliminaires

C. Serre communique les corrections suivantes au compte-rendu #1 (je cite textuellement):

- p.2 - Responsabilités du groupe CO:
  Le groupe CO est chargé:
  - du logiciel système et réseau, du logiciel de base (EM et RT), du protocole, de l'ensemble d'interaction au niveau workstation, des programmes génériques workstation, de la liaison et du contenu de la data base ORACLE, ainsi que de l'infrastructure DSC.
  - de l'infrastructure de réalisation des logiciels, et du support à donner aux utilisateurs (cas des programmes génériques ou de certains cadres)
  - les programmes d'application opérationnels sont en général à la charge du groupe OP, le logiciel spécifique à un équipement est à la charge du groupe responsable de l'équipement (groupes BD, RF, PO par exemple au niveau DSC ou G64),

- ANNEXE 1 - & 1.4 PERSONNEL
  ... Groupe CO: ...
  Y. Deloose (lay-out, interconnections, démarrage)
  M. Arruat (mise en exploitation et suivi RF)

fin de citation.

2. Le PLS ... (cf. transparents en annexe 1) par G. Daems

- Architecture des équipements du PLS avant 1993, structure du train PLS distribué.

- Première phase de rénovation du PLS (opérationnel en 1993): disparition du Nord 100 et du crate CAMAC attaquant les PLS encoders, mise en service de 2 PCs sous LynxOS (MTG1 et MTG2), apparition du train MTG ...

- Deuxième phase de rénovation du PLS (pour le démarrage 1994): hiérarchisation des PCs MTG1 et 2, génération du timing central PS par des modules TG8 ... L'ancien train PLS reste entièrement fonctionnel, mais le train MTG est désormais capable de prendre progressivement la relève. Un seul PC MTG suffit pour contrôler le PLS. Le second peut à tout moment le remplacer, ce qui garantit un niveau de disponibilité maximum pour ce système clé.

- Principes de sélection automatique des programmes NORMAL / SPARE / DUMP par décision à partir des conditions extérieures. Notion de user ZERO.

- Introduction aux messages MTG (5 bytes toutes les 125 µs), principe de distribution. Noter la transmission systématique d'un train machine (D au PSB, C au PS, ...) pour permettre la re-synchronisation des impulsions générées par les TG8 (sinon jitter de 500 ns du à la conception même du module).

3. MTG (suite) et module TG8 (cf. transparents en annexe 2) par J. Lewis

- Présentation succincte des grands principes à la base du PLS. BCD et cheminement le long du supercycle avec sélection des cycles NORMAL / SPARE / DUMP en fonction des conditions extérieures, User matrix. Caractéristiques essentielles du MTG.

- Origine du projet TG8. Développement commun avec la division SL, sur la base de leur expérience (hardware : SL, software: PS/CO).

- Architecture, génération du télégramme MTG (présence de 2 tables à usage alterné pour une modulation sans à-coups du super-cycle).

- Caractéristiques du TG8 (A2-9) et hardware (A2-10).

- Description fonctionnelle du TG8. Notion d' "actions" (A2-13). Driver existant (A2-14). Récapitulation des capacités (A2-16).

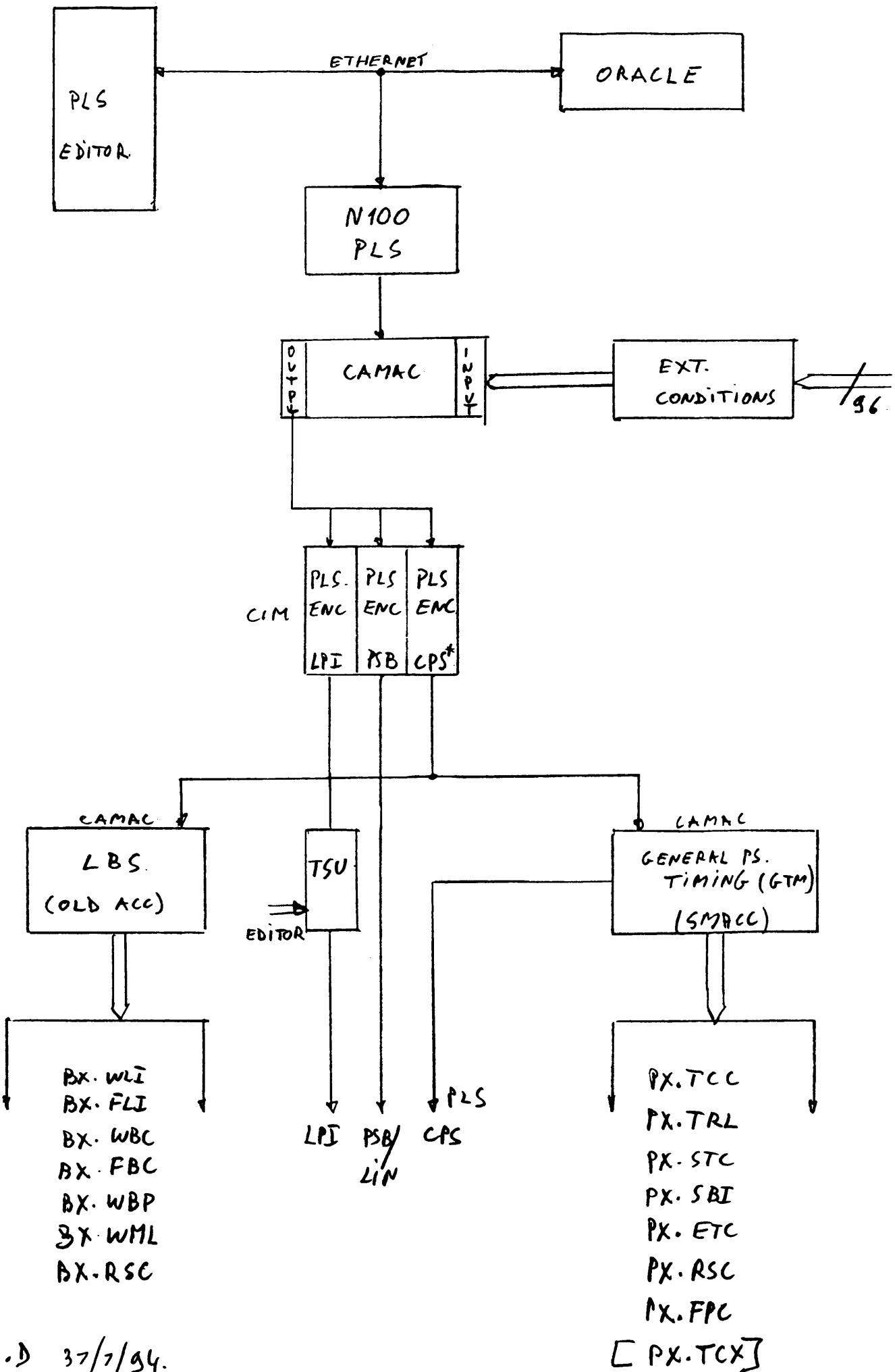
- Possibilités de diagnostic assez étendues, basées sur la capacité de dater et mémoriser les 100 dernières impulsions. Exemples d'utilisation dans ce domaine (A2-17 et A2-18).

Prochain rendez-vous : Mardi 8 février 1994
14 h
Salle d'exploitation MCR

Ordre du jour:

- Le PLS à 24 users (G. Daems)
- "Mode d'emploi" du nouveau PLS (B. Frammery)

ANNEXE 1 — PLS - OLD (before 1993) (G.DAENS/CO)



PLS G.D 37/7/94.

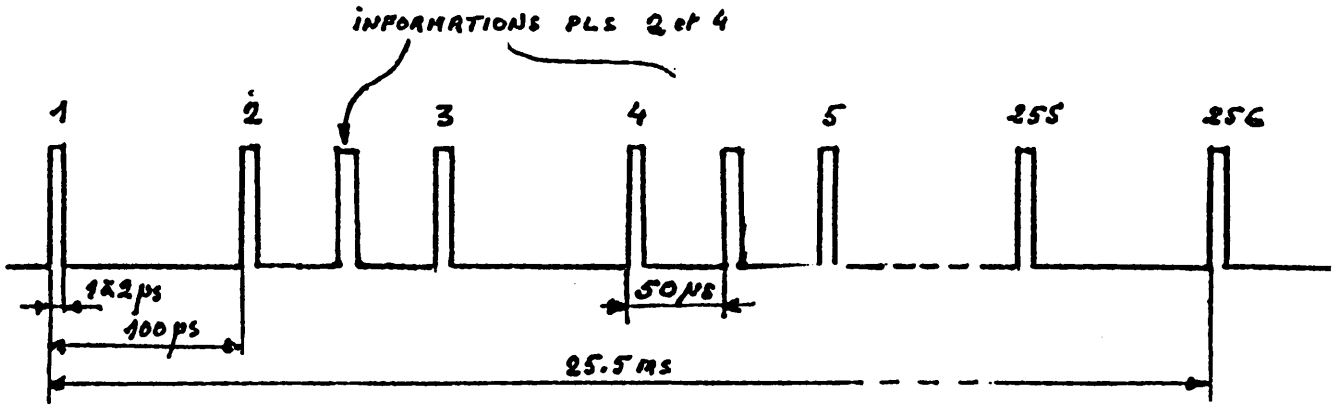
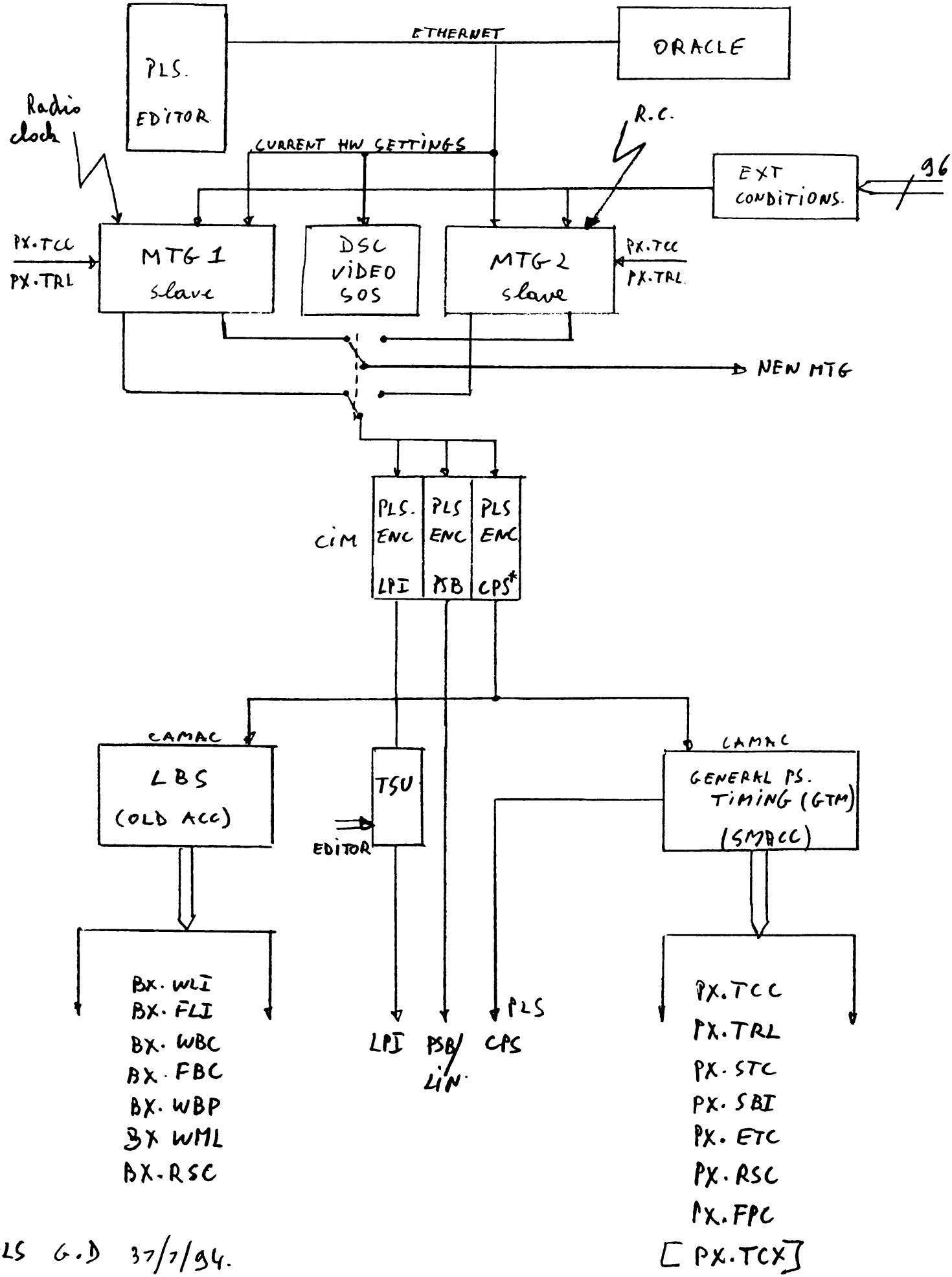


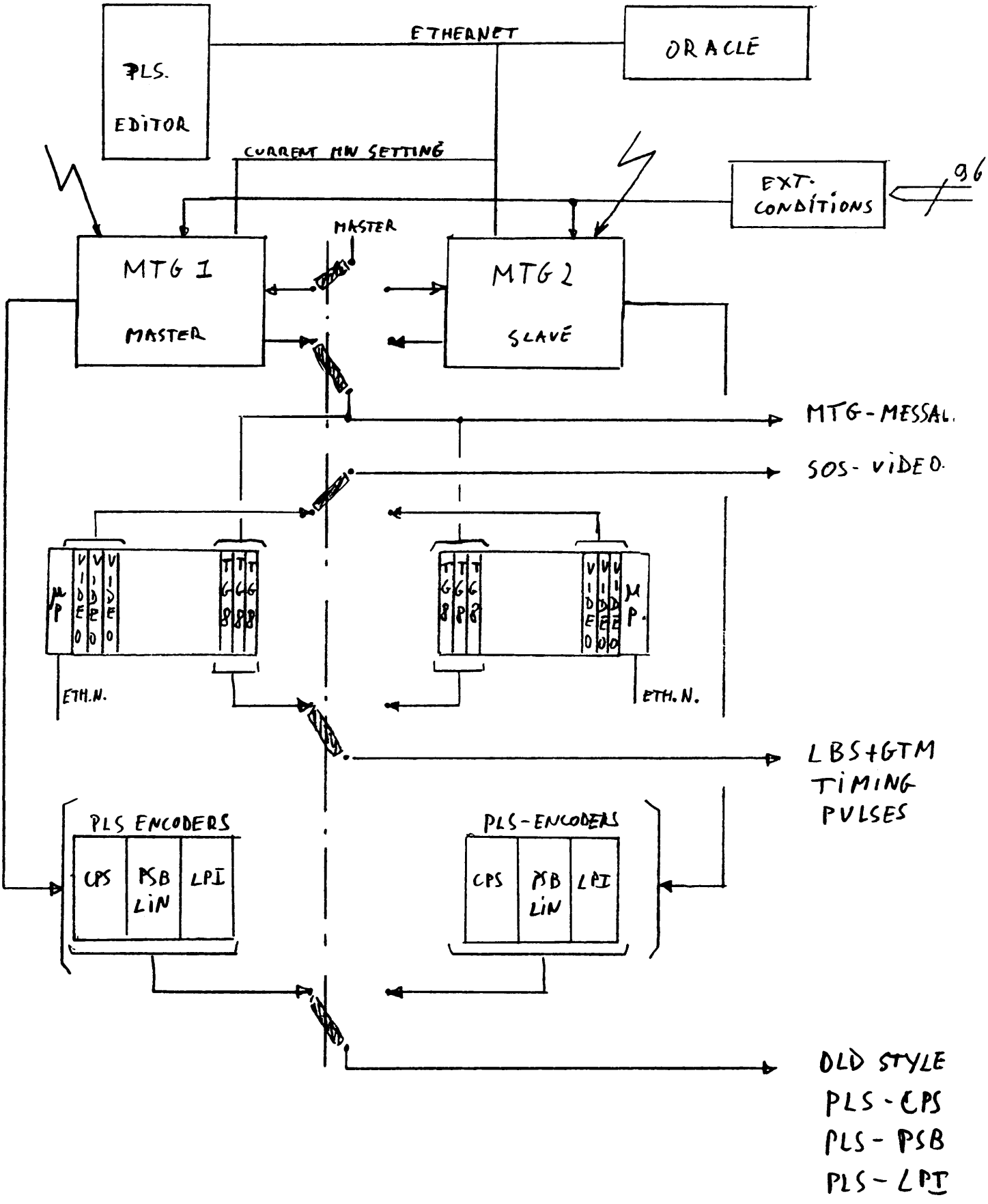
FIG. 4 - STRUCTURE DU TRAIN PLS

NEW PLS Phase 1 (All 1993)



PLS G.D 37/7/94.

NEW PLS Phase 2 (1994)



PLS G.D 31/1/94

MTG - Particularities

1 MTG = Master timing generator

consist of 1 industrial PC (33MHz, 486)
running LYNXOS real time UNIX
Standard PC-based ISC
Some additionnal I/O cards
for telegrams and timing

MTG-System = 2 PC's
1 Master
1 slave as hot backup.
Switching from one to an other
without effect on the operation

A new BCD (= new supercycle definition)
will be copied in both MTG, by the flash
copy technique, at the end of the supercycle

MTG = central timing for CPS
key pulses for PSB, LI and LPI

MTG Timings hierarchy (Initial setting)

- **PX.TCC** The 1KHz master clock train, distributed CERN wide.
- **PX.TRL** The 1.2 second clock train derived from dividing PX.TCC by 1200.
  - — **PX.MST** The CPS pulse family master.
    - * **PX.SBI** Start (B flux density) Increasing the magnetic field.
    - * **PX.STC** Start of Cycle.
    - * **PX.ETC** End of Cycle.
    - * **PX.FPC** Forewarning PS Cycle.
    - * **PX.FPD** Forewarning PS Cycle Delayed.
    - * **PX.RSC** Ready to start a new CPS Super-Cycle.
  - — **BX.MST** The PSB pulse family master.
    - * **BX.WLI** Warning Linac.
    - * **BX.FLI** Forewarning Linac.
    - * **BX.WBC** Warning Booster Cycle.
    - * **BX.FBC** Forewarning Booster Cycle.
    - * **BX.WBP** Warning Booster to PS.
    - * **BX.WBM** Warning Booster to ML.
    - * **BX.RSC** Ready to start a new PSB Super-Cycle.
  - — **HX.MST** The LPI pulse family master.
    - * **HX.FEJ** Forewarning EJection.
    - * **HX.FBP** Forewarning Basic Period.
    - * **HX.FHC** Forewarning LPI Cycle.
    - * **HX.FES** Forewarning Ejection power Supplies.
    - * **HX.FH** Forewarning LPI.
  - — **PX.WPLS** Warning CPS PLS telegram, and strobe PLS encoder.
  - — **BX.WPLS** Warning PSB PLS telegram, and strobe PLS encoder.
  - — **HX.WPLS** Warning LPI PLS telegram, and strobe PLS encoder.
  - — **PX.RPLS** CPS PLS telegram is Ready for use. TG8 activates new telegram.
  - — **BX.RPLS** PSB PLS telegram is Ready for use. TG8 activates new telegram.
  - — **HX.RPLS** LPI PLS telegram is Ready for use. TG8 activates new telegram.
  - — **PX.TASK** Start the MTG main and output tasks.

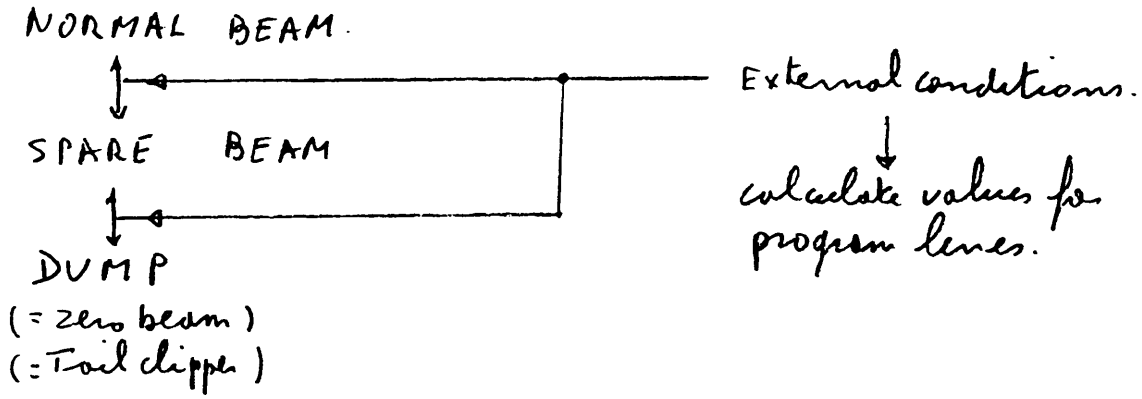
MTG - Diagnostics.

Different displays to follow the MTG behaviours

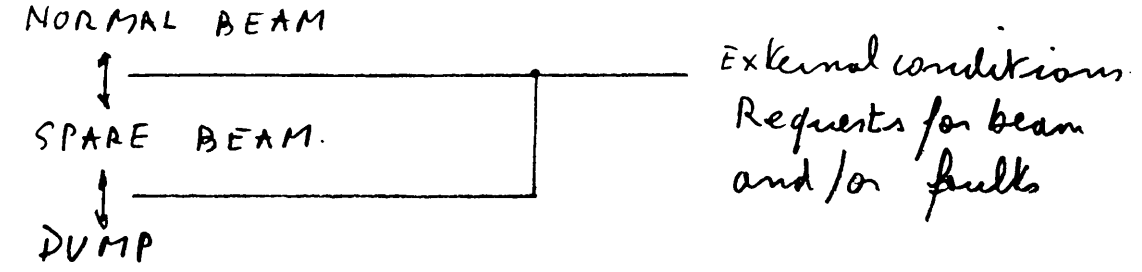
- video displays for 3 old style PLS telegrams
- X-window displays from the MTG:
  - PLS vistas ON-LINE for the 3 telegrams
  - External conditions ON-LINE display
- X-window display in the DSC
  - PLS vistas of the received telegram
  - User-matrix
  - acces routines to PLS informations (Program line names, etc)
- TGP: surveillance of the distributed MTG-messages

Normal and Spare

1) up to mid 1993

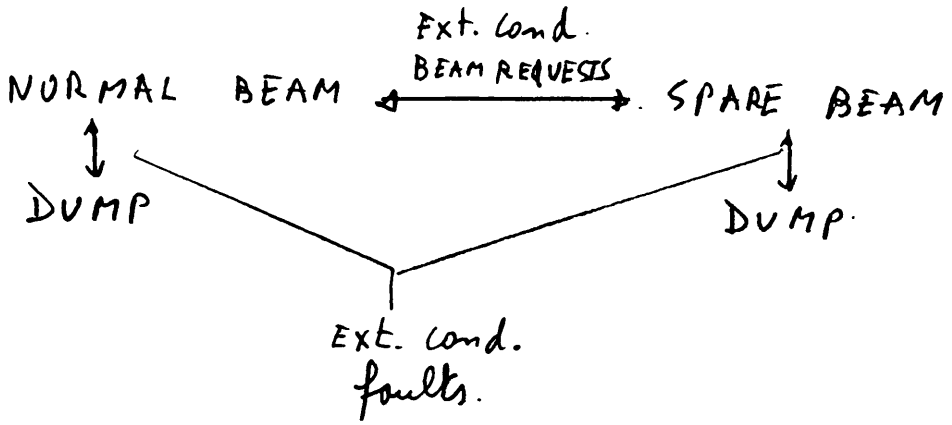


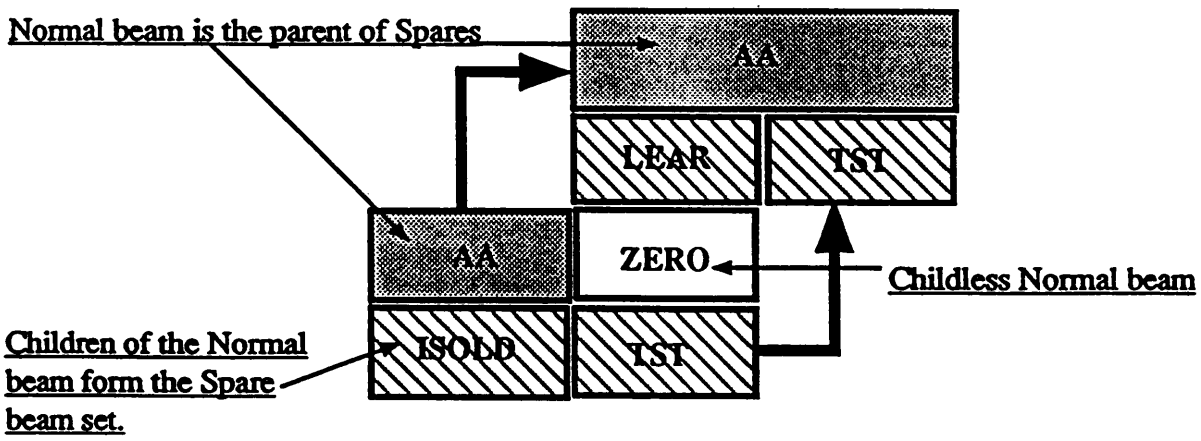
2) mid 1993 → end 1993



change from $\bar{p}$ production (= AA uses) to $\bar{p}$ transfert (= LEAR + TST) immediately on "transfert request"

3) New (probably startup 1994)




Normal beam is the parent of Spares
AA
LEAR
TST
AA
ZERO
Childless Normal beam
Children of the Normal beam form the Spare beam set.
ISOLD
TST

ZERO - BEAMS.

* up to now not well defined.

1] - "zero line" in the telegram when dump or other line

+ Tail clipper activated in the linac

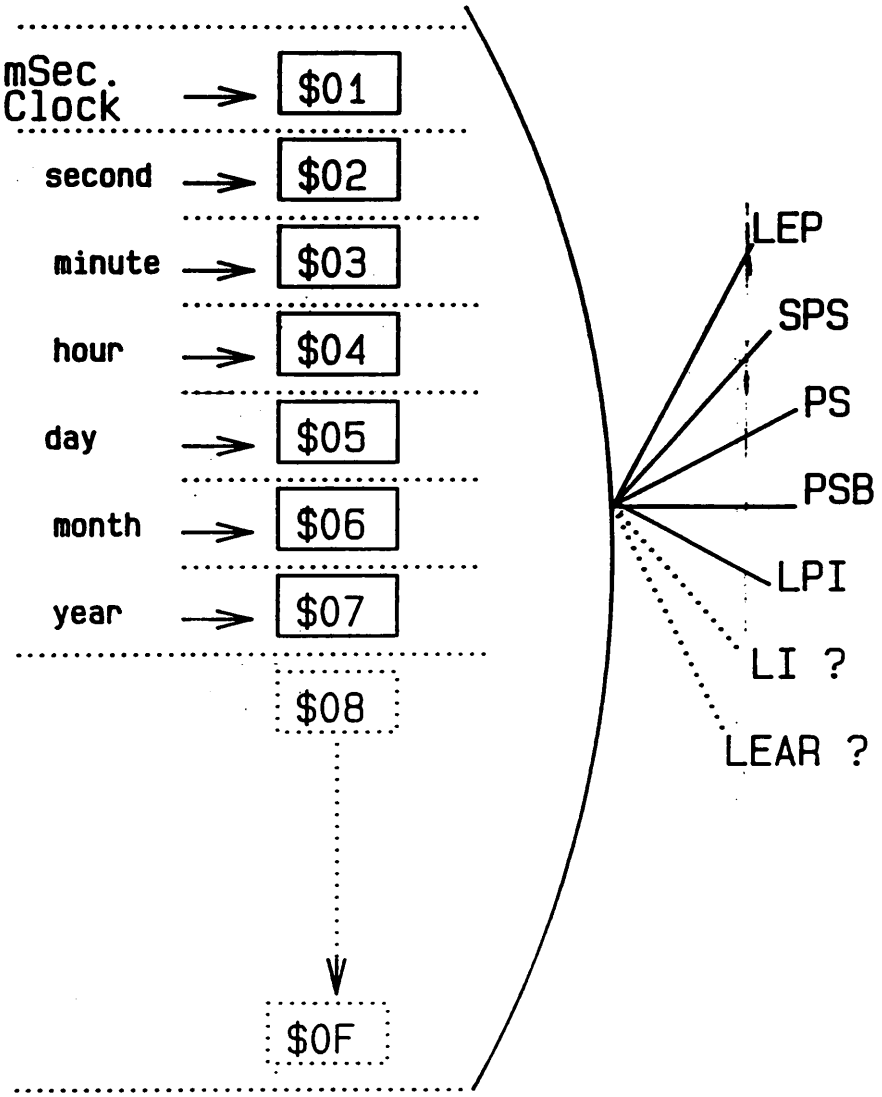
2] beam to fill in holes in the super cycle editor. Confusing with existing beam

* NEW: beam "ZERO" expressed by a user "ZERO" to be defined as any other user.

CERN-wide TIMING :
Proposal for new headers:

(part 1 of 3)

A set of Headers are common to all CERN machines



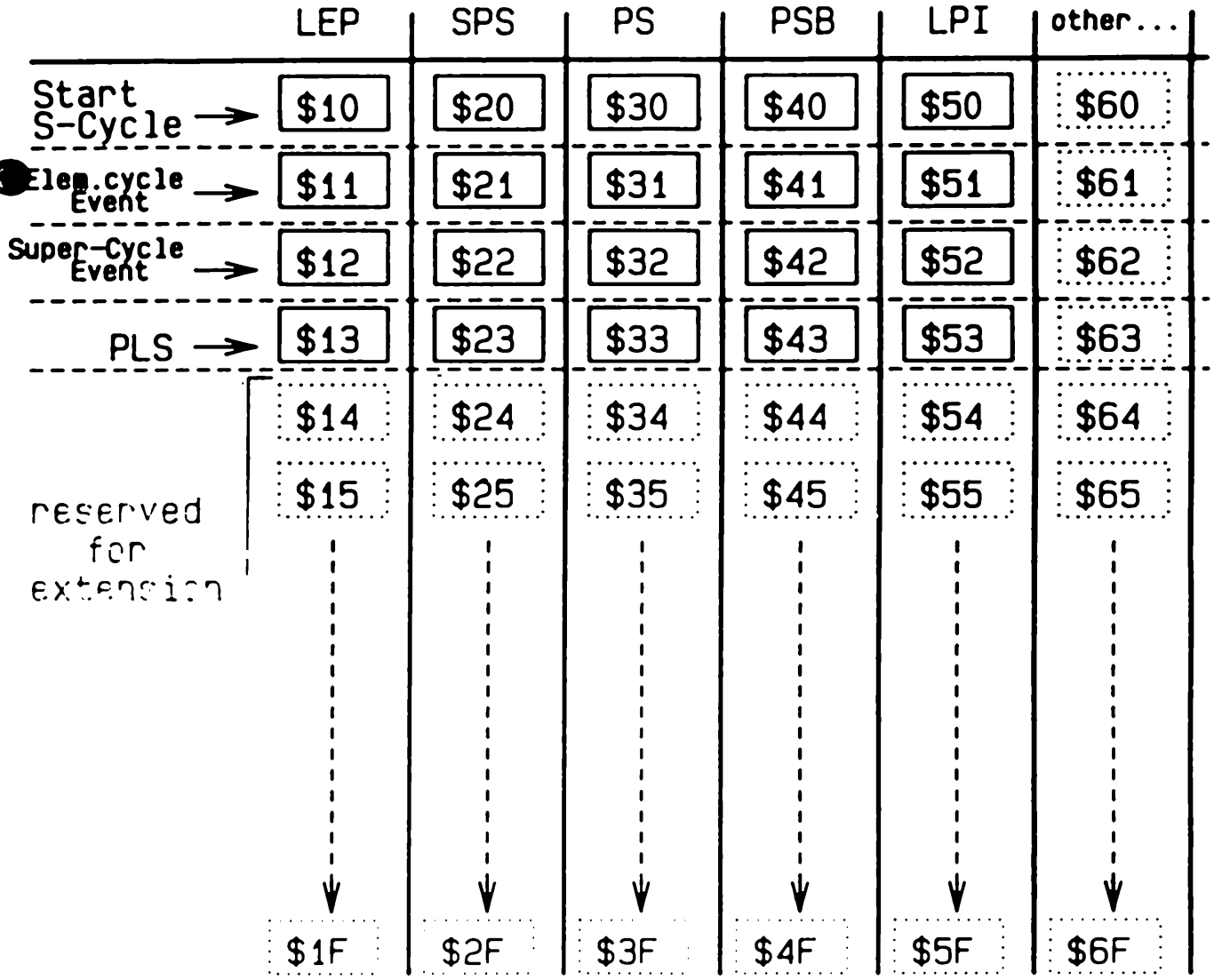
$xx = Hex Format

B.P. 05 Nov.90

CERN-wide TIMING :
Proposal for new headers:

(part 2 of 3)

Reserve a group of 16 Headers for each machine

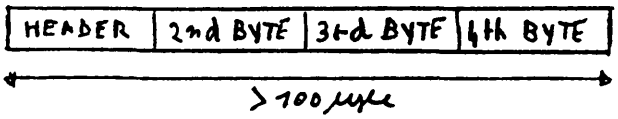


$xx = Hex Format

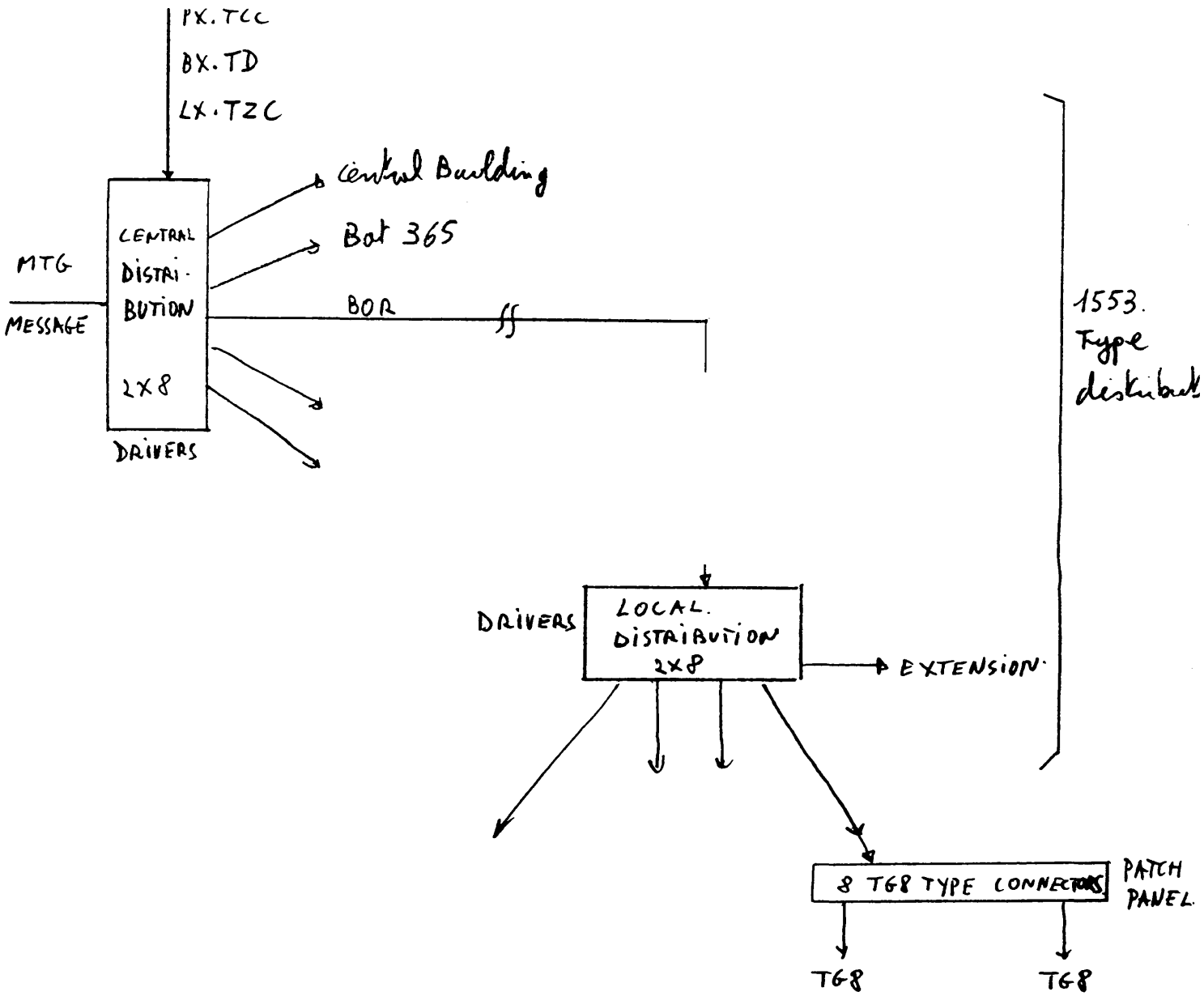
B.P. 05 Nov.90

MTG - Messages information.

- Coding of MTG - messages

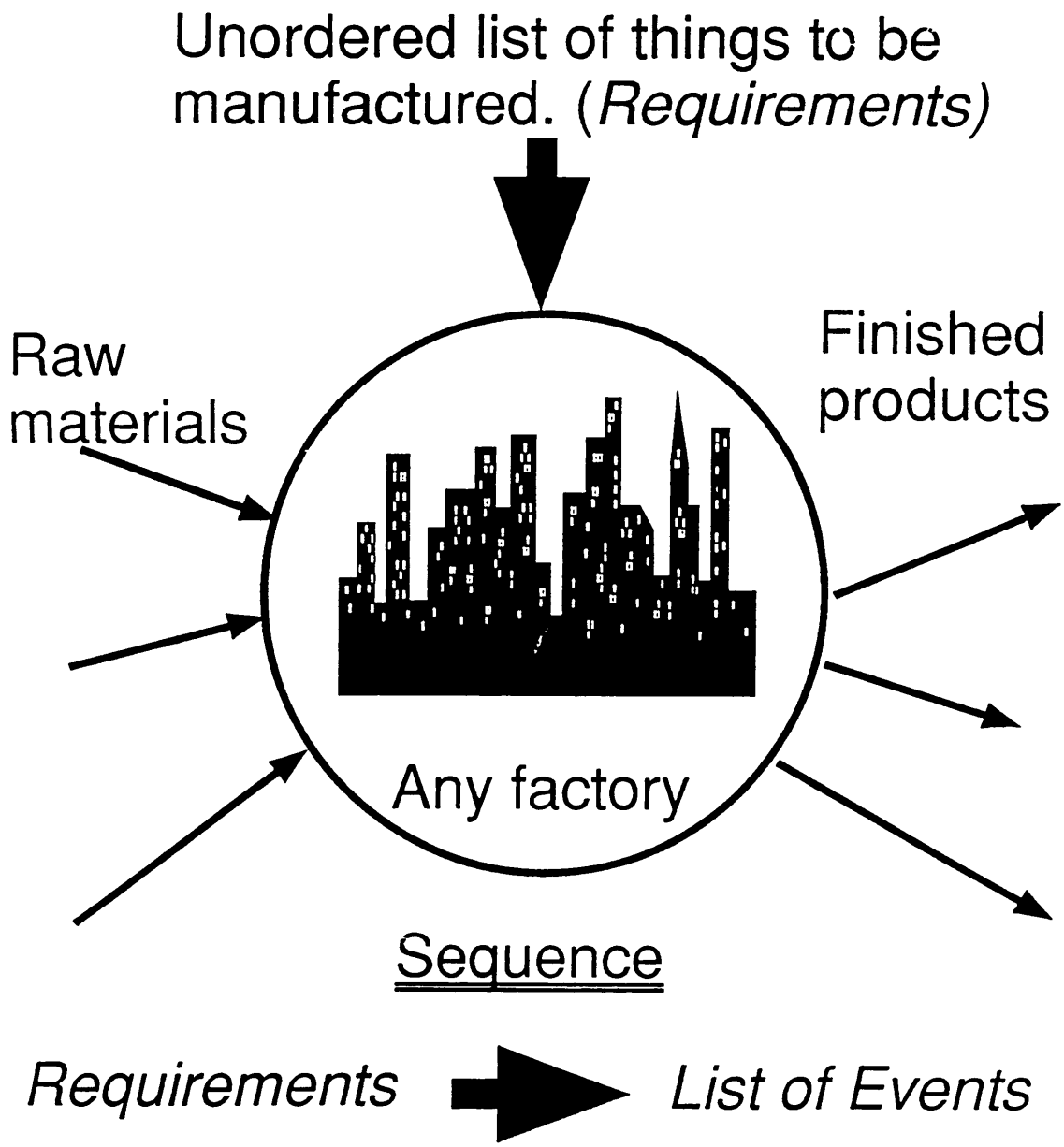


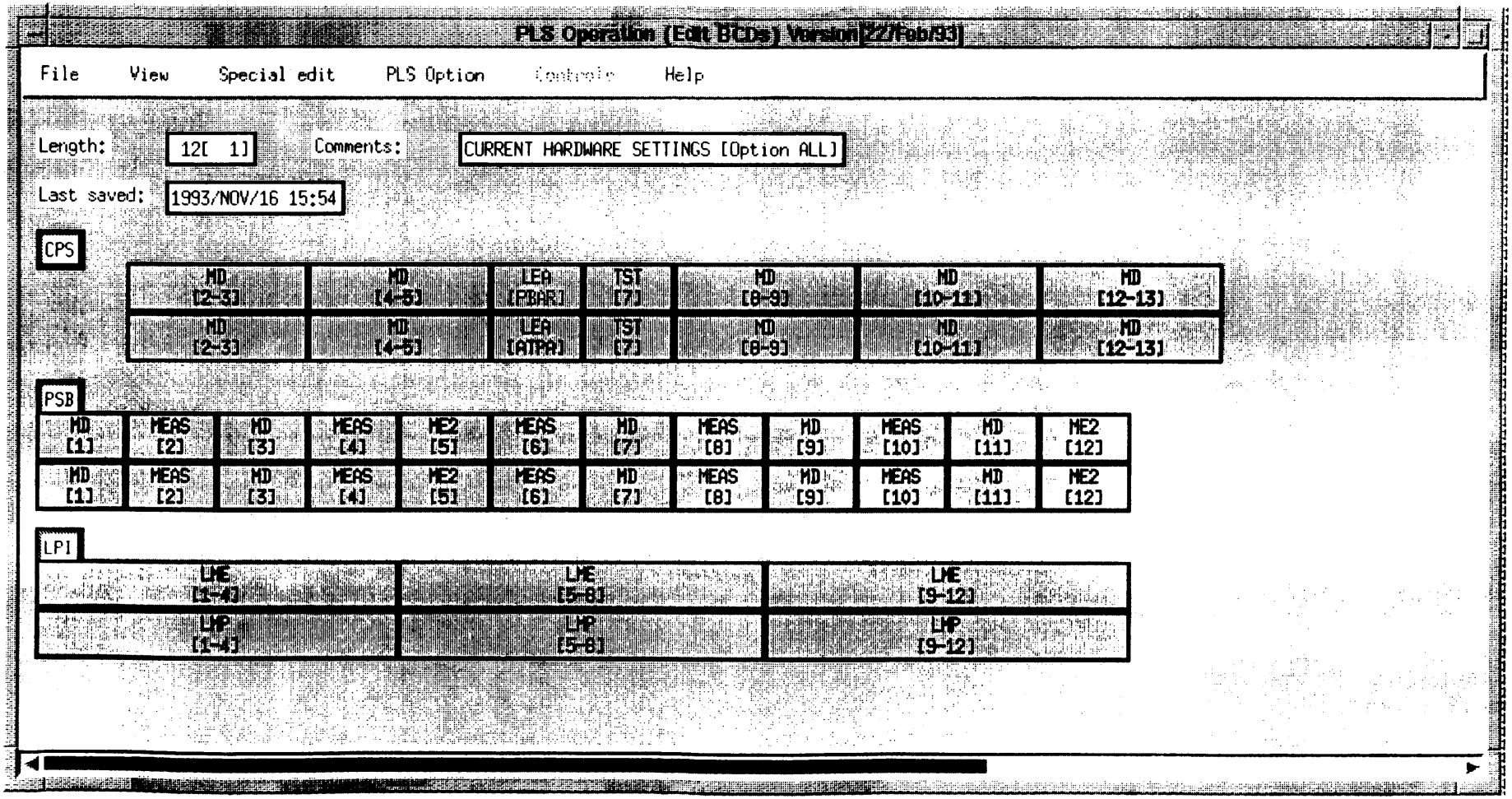
- Distribution.



ANNEXE 2 (J LEWIS / CO)

The problem

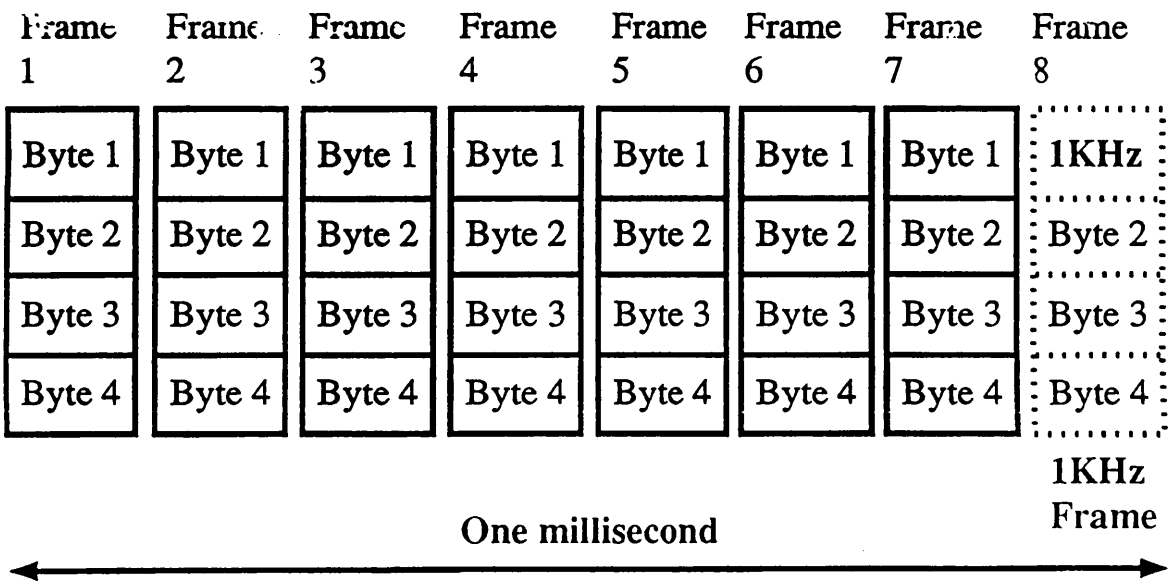



PLS Operation (Edit BCDs) Version 22/Feb/93
File
View
Special edit
PLS Option
Controls
Help
Length:
12[1]
Comments:
CURRENT HARDWARE SETTINGS [Option ALL]
Last saved:
1993/NOV/16 15:54
CPS
MD [2-3]
MD [4-5]
LEA [PBAR]
TST [7]
MD [8-9]
MD [10-11]
MD [12-13]
MD [2-3]
MD [4-5]
LEA [ATPA]
TST [7]
MD [8-9]
MD [10-11]
MD [12-13]
PSB
MD [1]
MEAS [2]
MD [3]
MEAS [4]
ME2 [5]
MEAS [6]
MD [7]
MEAS [8]
MD [9]
MEAS [10]
MD [11]
ME2 [12]
MD [1]
MEAS [2]
MD [3]
MEAS [4]
ME2 [5]
MEAS [6]
MD [7]
MEAS [8]
MD [9]
MEAS [10]
MD [11]
ME2 [12]
LPI
LME [1-4]
LME [5-8]
LME [9-12]
LMP [1-4]
LMP [5-8]
LMP [9-12]

HOP16
HOPEN
MISC
DEST
POWER
HARMN
LWPNT
HWPNT
PARTY
ZRO_BIT
CT
FE16S
FE16D
FE16A
FE16A
FE16L
FE16I
FE58L
FE58S
FE58D
---12
SE61
FE26
---15
---16
FBAR
DBL_EJ
---19
B05
D48
D47
TT70
D7
D2
D3
---27
FTS
FTA
ATPA
ATPP
---32
A
B
C
D
E
F
G
H
H420
H20
H20LI
H5WP
H10
H6H12
H240
HB
LELOW
LELEC
LEHIG
LEDEC
LEMD1
LEMD2
LEINT
NOLE
HEA
HEB
HEC
HEMD
HEE
NOHE
---71
---72
PROTON
ANTIPROT
DEUTERON
OXYGEN
ELECTRON
POSITRON
ALPHA
SULPHUR
Duration (BPs)
2
CANCEL
HELP

A2-3

Synchronization



AL-4

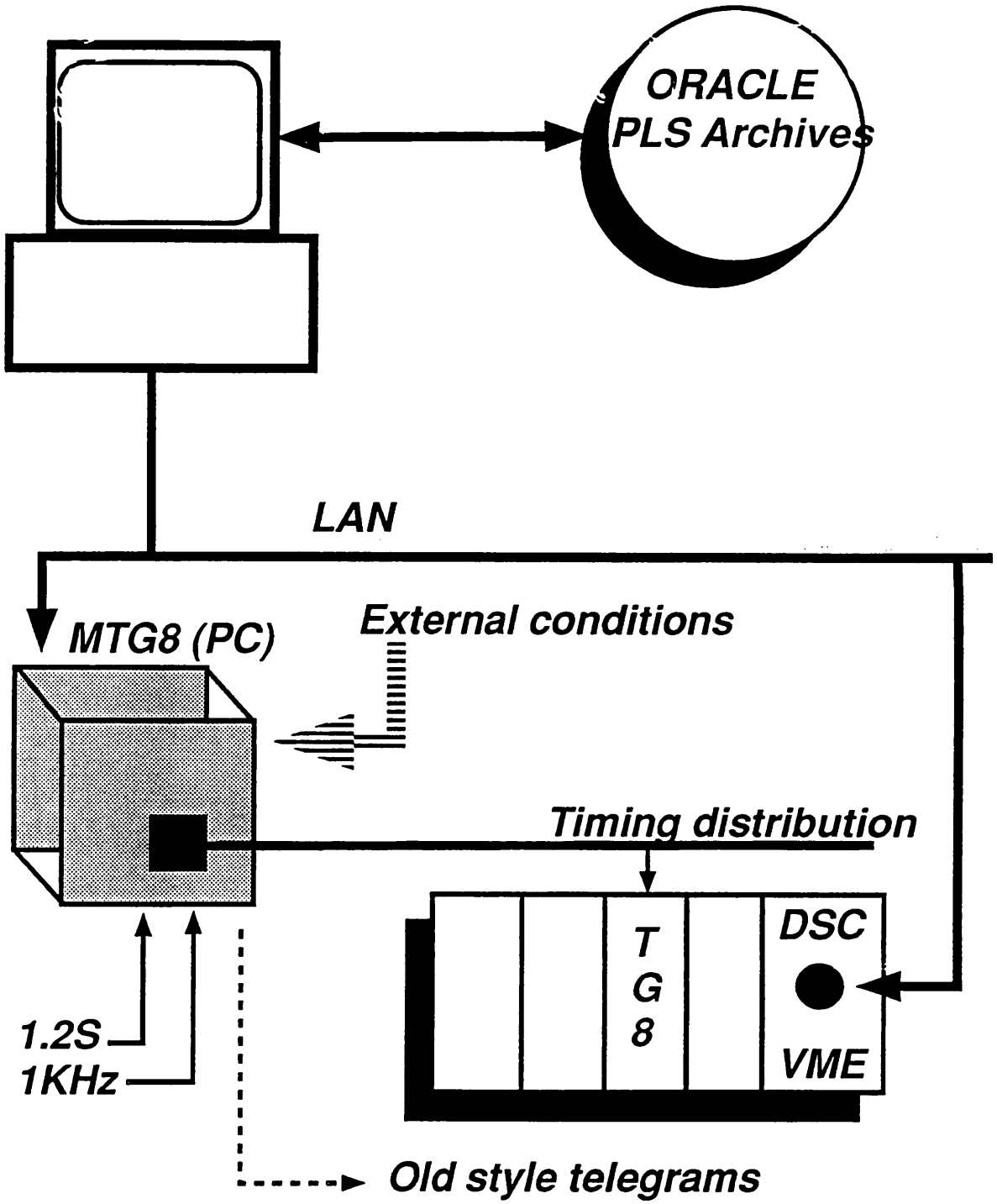
The MTG summary:

- Seemless intellegent automated super cycle changes base on the BEAM concept.
- Easy modification of MTG logical behaviour in real time.
- Unlimited place for future telegram expansion.
- One cable contains all telegrams and coarse timings for the PS complex machines.
- External events and software events.
- Date/Time correct to the nearest ms.
- 1ms resolution 500 ns precision.
- Maximum of 6 events per ms.

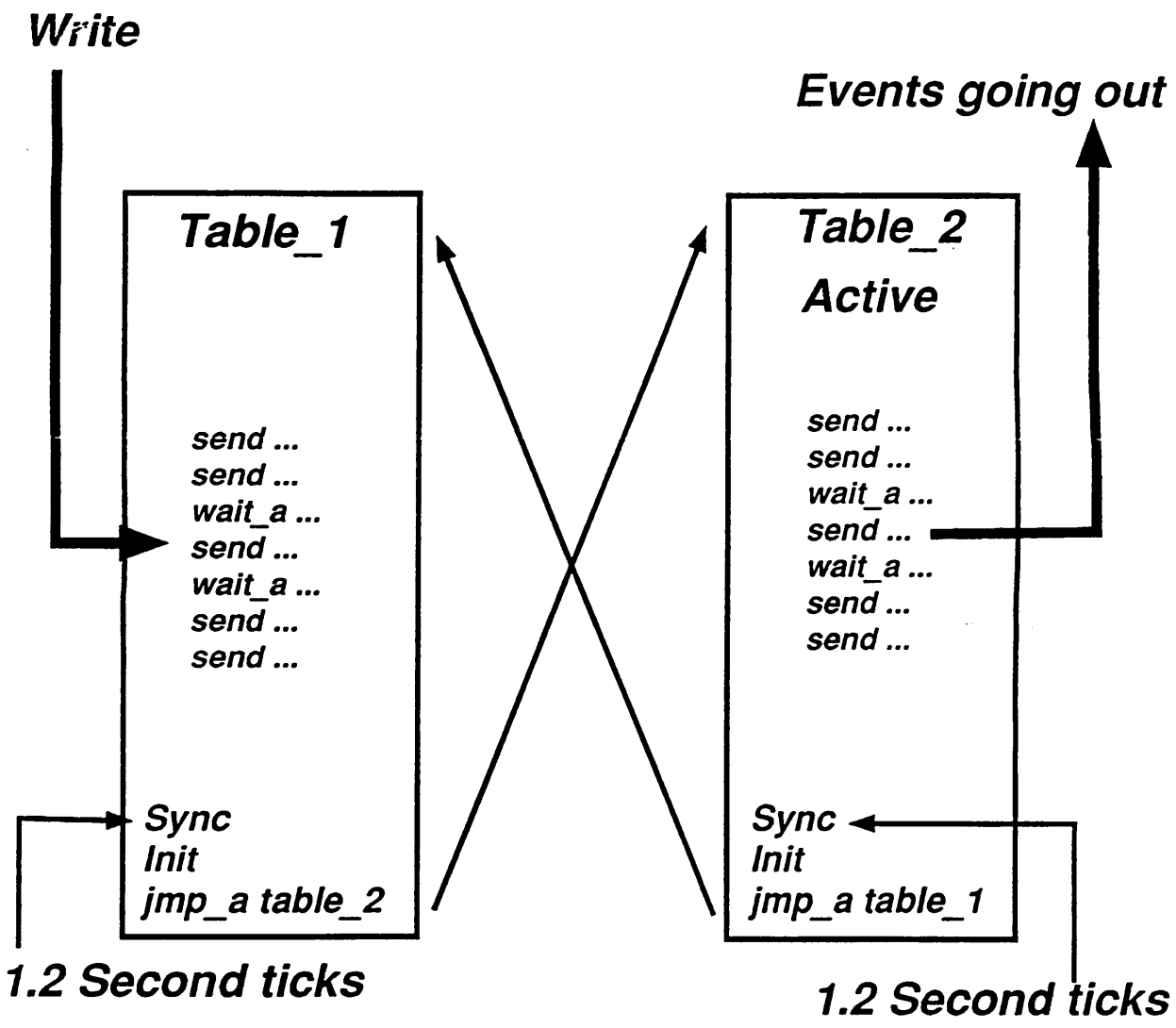
The Tg8 project:

- Born at CUF
- A common PS/SL standard compatible with the Tg3 and PPM
- VME based module
- Mtg hardware -> Philippe Nouchi (SL)
- Tg8 hardware -> Bruno Puccio (SL)
- Software -> PS/CO

Architecture

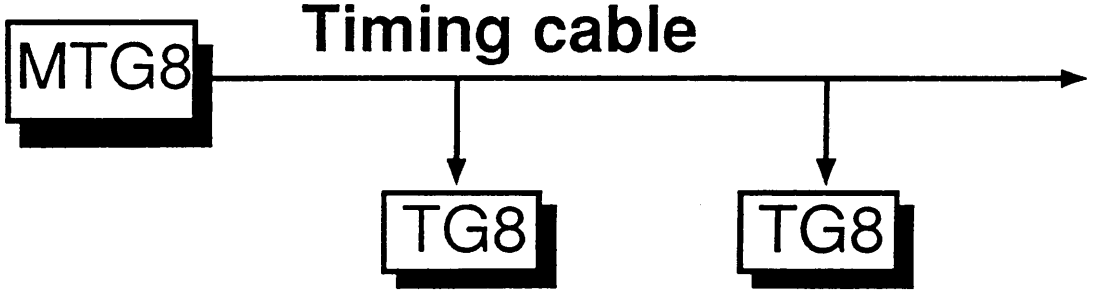


Event and telegram generation by the MTG



Timing distribution via TG8

- Common PS/SL => MTG8 and TG8
- Single cable distributes
  - — 1 KHz clock
  - — Simple events
  - — Time of day
  - — Telegrams
- 3 External clocks (20 MHz)
- 2 External starts
- 8 Outputs
- VME Bus interrupts
- PLS Conditioning
- Up to 256 programmable actions



The Tg8 Hardware :

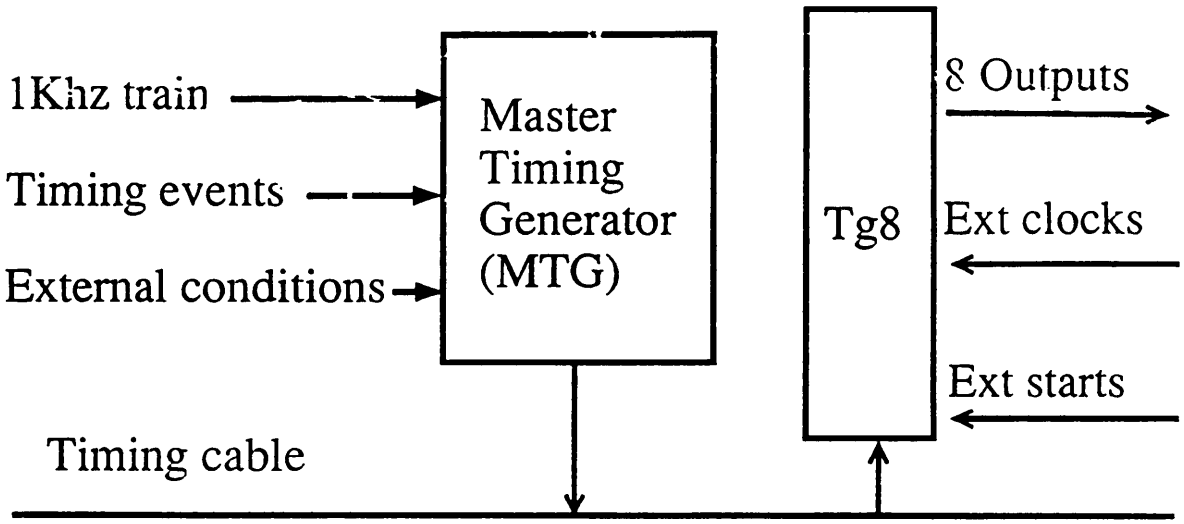
- The timing drop net and cable clock reception logic
- A Content Addressed Memory (CAM) fo fast event lookup
- An MC68332 16MHz processor with 64K RAM and 128K EPROM
- A 4K Dual Port Ram (DPRAM) mail box for communicating with the VME host.
- 8 Programmable counters implemented in 2 large XILINX gate arrays

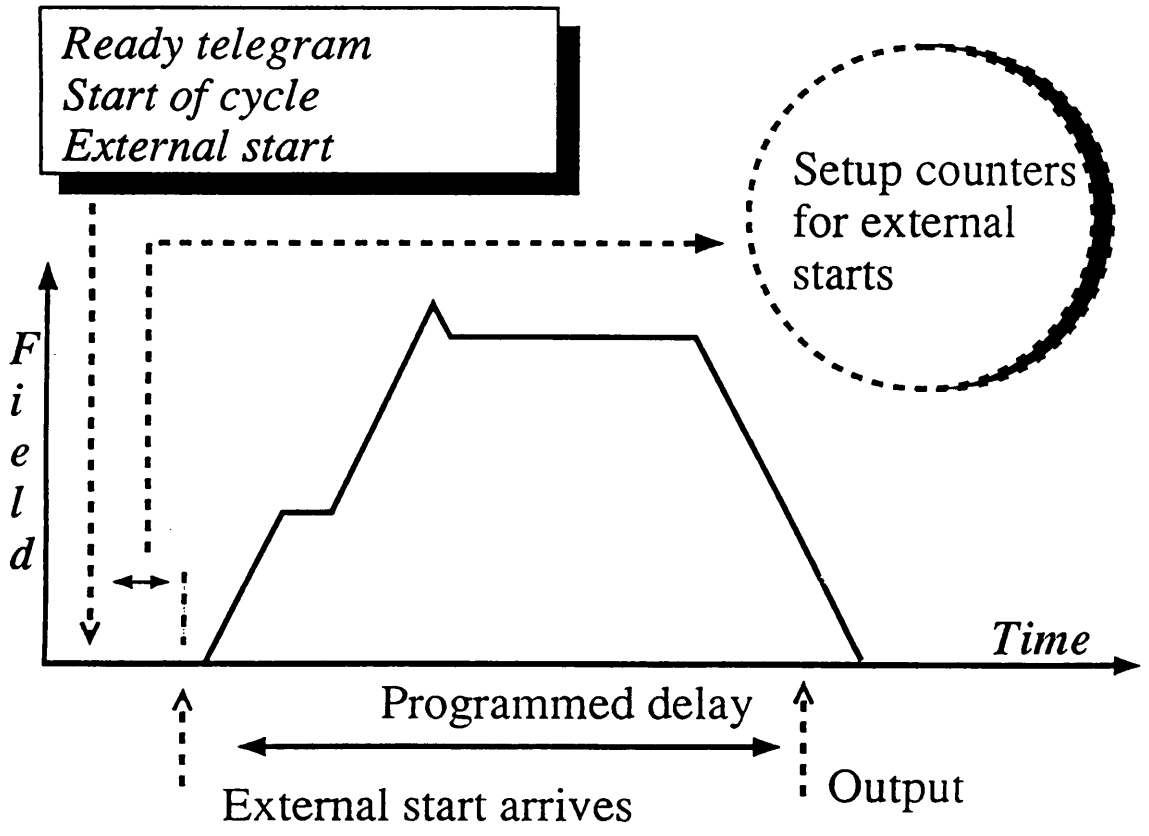
  (Counter 8 is special as it is an Up/Down counter, the other 7 are Down counters)

The MTG cable carries:

- **Simple events which mark interesting moments in machine cycles (up to 5 per ms)**
- **The PLS telegrams which describe these cycles**
- **The central 1KHz timing clock train**
- **A machine dependent cable clock (CPS = C-Train, PSB = D-Train, LPI = 100Hz)**
- **The date and time events (Received by a long wave radio clock in the Mtg)**
- **15 External events input via the Mtg front panel.**
- **Software triggered events.**

Synchronization





A2-12

TG8 Actions

- An action is a unit of TG8 work
- Actions are the means by which applications instruct the TG8 what to do
- Action = Start + Duration + Result
  - — Start = Event + PLS
  - — Duration = Clock + Count
  - — Result = Bus interrupt + Output
- Event = RtClk | External | Accelerator
- PLS = Group name + Value
- Clock = 1Khz | External | Internal 10Mhz

```
Action = Start(Ext1,PLS(DEST,D3) +
         Duration(1KHz,500) +
         Result(Output(1));
```

```
Action = Start(Ext1,PLS(DEST,D2) +
         Duration(Internal,1000) +
         Result(Output(1),Interrupt);
```

```
#include "/dsc/data/tg8/mtg_bindings"        % Include central timing definitions

% Member 1048 is an example of zero group timeout substitution

CMember.Member{ 1048 }                       % Px... equipment number
CMember.Module{ 1 }                          % First module in hardware description
CMember.Channel{ 1 }                         % Top most output
CMember.TriggerMember{PxSTC}                % Mtg event which triggers these actions
CMember.Clock{INTERNAL}                      % Internal 10 MHz clock
CMember.CheckMode{EQUALITY}                  % Trigger if telegram EQUALS line
CMember.Machine{CPS}                         % Which telegram to look at
CMember.CounterStart{EXTERNAL_START_1}       % The start will come later
CMember.CounterMode{SINGLE}                  % One output
CMember.Dimension{ 9 }                       % Number of actions to reserve
CMember.GroupNumber{ HOP16 :  0..8 }         % Group range is 0..8, it can be any Eg 3..7
CMember.Delays{ 100, 93, 68, 68, 72 : DISABLE, 93, 72, 72 : DISABLE, 72 }

% Member 1049 is an example of gaited parallel timing generation

Define.COMHW{12}  % Group number for COmbined-line-HardWare-specialists
Define.WBP{0x08}  % Warning-Booster-injection-cPs bit in COMHW
Define.WML{0x10}  % Warning-booster-Measurement-Line bit in COMHW

CMember.Member{ 1385 }                       % Bx... equipment number
CMember.Module{ 1 }
CMember.Channel{ 2 }
CMember.TriggerMember{PxTRL}
CMember.Clock{ONE_KHZ}                       % Event based Mtg clock train 500ns jitter
CMember.CheckMode{LOGICAL_AND}               % If telegram AND bits not zero
CMember.Machine{PSB}
CMember.CounterStart{NORMAL}                 % Next 1Khz clock tick starts counter
CMember.CounterMode{SINGLE}                  % One single direct output
CMember.Dimension{ 2 }                       % Number of actions to reserve
CMember.GroupNumber{COMHW}                   % Bit pattern type group
CMember.BitMasks{WBP, WML}                   % Which bits to check for each action
CMember.Delays{ 72, 49 }                     % Delay for each bit pattern

% Hardware addresses

ModuleAddress.VMEAddress{0xfe800000}
ModuleAddress.InterruptVector{0x61}
ModuleAddress.InterruptLevel{2}
ModuleAddress.SwitchSetting{1}

% Firmware object

FirmwareObject.FileName{/dsc/bin/drivers/tg8/tg8.exe}
```

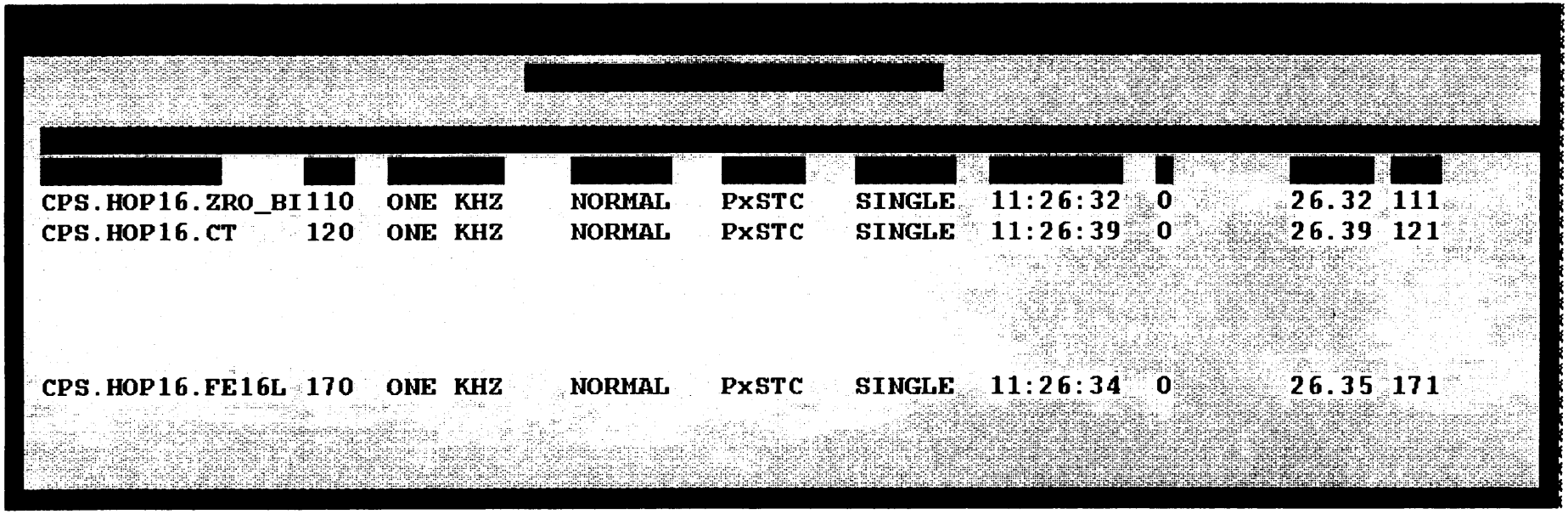
Tg8 and Tg3 Events layout and headers table

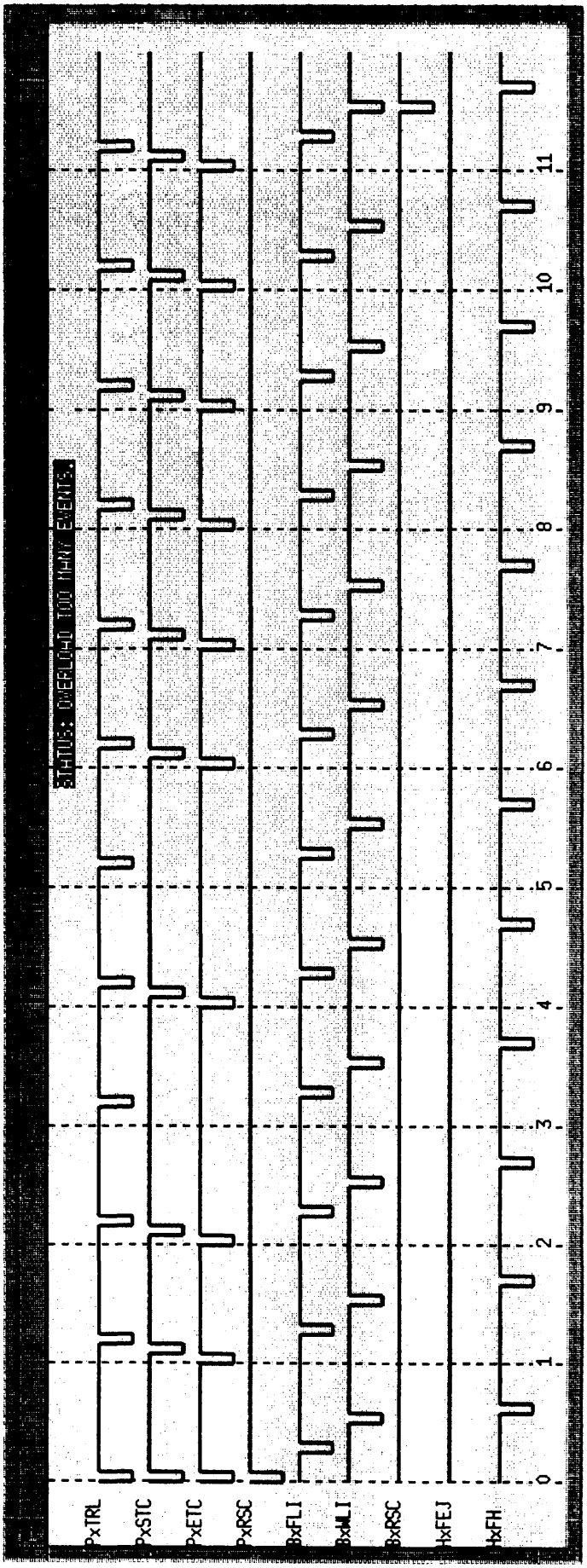
Header and code	** m = machine	*Byte 2*	*Byte 3*	*Byte 4*
1KHz	*01*	*1ms ticks*	*100ms ticks*	*Don't care*
Tg3 Second	*02*	*BCD value*	*Don't care*	*Don't care*
Tg3 Minute	*03*	*BCD value*	*Don't care*	*Don't care*
Tg3 Hour	*04*	*BCD value*	*Don't care*	*Don't care*
Tg3 Day	*05*	*BCD value*	*Don't care*	*Don't care*
Tg3 Month	*06*	*BCD value*	*Don't care*	*Don't care*
Tg3 Year	*07*	*BCD value*	*Don't care*	*Don't care*
Tg8 Time	*08*	*Hour*	*Minute*	*Second*
Tg8 Date	*09*	*Year*	*Month*	*Day*
Tg8 Simple	m4	*Code*	*Cycle type*	*Cycle number*
Tg3 Simple	m1	*Code*	*Cycle type*	*Cycle number*
Tg3 Start S-Cycle	m0	*Cycle number byte 0*	*Cycle number byte 1*	*Cycle number byte 2*
Tg3 Super cycle event	m2	*Code*	*$01*	*$01*
Tg8 Telegram	m3	*Group number*	*Group value byte 0*	*Group value byte 1*

** m = machine 1=LEP 2=SPS 3=CPS 4=PSB 5=LPI 6=LHC

Tg8 Summary:

- Diagnostics
  - — Lookat a member
  - — Scope
- Configurable timing layout via software
- Autonomous device needs no RT task in the host DSC
- 32 Programmable actions (Quasi para-lell timing engines) per counter.
- Driver based on the concept of member number.


CPS.HOP16.ZRO_BI 110 ONE KHZ NORMAL PxSTC SINGLE 11:26:32 0 26.32 111
CPS.HOP16.CT 120 ONE KHZ NORMAL PxSTC SINGLE 11:26:39 0 26.39 121
CPS.HOP16.FE16L 170 ONE KHZ NORMAL PxSTC SINGLE 11:26:34 0 26.35 171


STATUS: OVERFLOWED TOO MANY EVENTS.
PxTRL
PxSTC
PxETC
PxRSC
BxFLI
BxMLI
BxRSC
HxFEJ
HxFH
0
1
2
3
4
5
6
7
8
9
10
11