MPS/BR Note/75-20
30.10.1975

The TRANSCEIVER and the CONTROL UNIT

for the control of the new PSB multipoles using CAMAC

B.I. Hallgren

1. Introduction

The control system for the power supplies of the new PSB multipoles uses the CAMAC technology for data transmission. For various reasons (not an efficient way using CAMAC, earth loop currents problem, etc.) it was decided not to place the control electronics for the power supplies directly, in a CAMAC crate. Instead the control part of the 56 power supplies is placed in 12 CIM-crates with the same mechanical dimensions as CAMAC. For the connection with CAMAC two modules have been developed: one single unit CAMAC-module called the TRANSCEIVER and one single unit CIM-module called the MULTIPOLE CONTROL UNIT. This report describes these two modules in detail. For a full description of the PSB new multipoles, see Ref. 1.

2. General description

The control electornics of a power supply is placed in a 4-unit CIM-module. A CIM-crate accommodates 6 of these modules. The remaining single unit place is used for the MULTIPOLE CONTROL UNIT. The interconnection between the control electronics of a power supply and the CONTROL UNIT is made via connectors on the rear of the crate. The interconnection consists of a 16-bit bidirectional databus (tristate), 3 bit function code bus, a strobe bus line for writing to a power supply module and one individual line to each of the 6 power supply modules.

The CONTROL UNIT and the TRANSCEIVER are connected via a 52 lines cable. This connection is made via optocouplers in both directions (sending and receiving of data) so that the CONTROL UNIT and the TRANSCEIVER is galvanically isolated. The TRANSCEIVER can communicate with two CONTROL UNITS separately. The communication distance between the TRANSCEIVER and the CONTROL UNIT is intended to be less than 10 m.

For each power supply there are 4 words of 16 bits to be read by CAMAC and 1 word of 16 bits to be written. These words are named: IDENTIFICATION WORD, DIGITAL TEST WORD, REGULATOR STATUS WORD and MEMORY CONTROL WORD. This latter word can both be read and written. There is also one 16 bit word per CIM-crate called the READY/ON/OFF STATUS WORD and one 1 bit word

to be written for. In total there are 25 words to be read and 7 to be written to in each CIM-crate. These words are identified by means of a 3 bit function code. Each power supply module is accessed via one CAMAC subaddress. One TRANSCEIVER thus reads 50 words and writes to 14 words. In the appendix a specification of the TRANSCEIVER CAMAC functions is shown.

2.1 TRANSCEIVER

In the TRANSCEIVER it has been implemented a total of 145 different combinations of CAMAC subaddresses and functions. This relatively large number is due to :

a) the subaddresses A(0) to A(15) are not decoded so that a maximum of 8 subaddresses can be addressed in a CIM-crate.

b) two modes of operation because Data to be read must be available at the CAMAC-dataway before the strobe S1.

This is not possible to achieve directly, therefore two different sets of functions are used for two modes of reading data from the power supply modules. One method uses the HOLD option P2-line[2]. The other method uses two CAMAC functions for a read operation: one to transfer data from the power supply module to a buffer register in the TRANSCEIVER and a second CAMAC function to read from the buffer register.

Fig. 1 shows a block diagram of the TRANSCEIVER. The main parts are: decoder of the CAMAC functions F(0), F(1), F(4), F(6), F(12), F(14), F(16), F(28), F(30), F(2) which are sent to the CONTROL UNIT as encoded subfunctions; CCR1, CCR2, CCW, transfer status flip-flop for hand-state circuits; manual p.c. board switch and HOLD option flip-flop, command address register and comparator used in the transfer mode. Below a detailed description of the main parts of the TRANSCEIVER is given.

Decoding and encoding of functions

Fig. 2 shows a circuit diagram of decoding and encoding circuits, which are using standard TTL-circuits. Table 1 gives a summary of how the different CAMAC functions are implemented.

X-response

X response is given according to the equation (1)

$$X = R + TR + W + F(2)\cdot A(15)\cdot N \qquad (1)$$

where $R = \{F(0) + F(1) + F(4) + F(6)\}\cdot N$
$TR = \{F(12) + F(14) + F(28) + F(30)\}\cdot N$
$W = F(16)\cdot N.$

Q-response

Q response is given according to equation (2)

$$Q = TS*(H*R + W*FS1 + H*TR) + H*R*K + F(2)*A(15)*N \qquad (2)$$

where TS = transfer status
H = hold option is on
FS1 = status bit, which is set by S1 and reset when CAMAC dataway operation is completed
K = true when memorized command to the CONTROL UNIT consisting of CCR1, CCR2, CCW, CN1, CN2, CA1, CA2, CA3, is equal to given CAMAC function and subaddresses.

R, TR, W } see under X-response.

Handshake circuits

After decoding of the CAMAC function (when R + TR + W = 1) the handshake circuit sends a positive (+ 3.5 V) signal to the CONTROL UNIT, where it is immediately returned via optocoupler and gate to the set input of the TRANSFER STATUS flip-flop (see Fig. 3). The purpose of this circuit is to prevent the TRANSCEIVER from sending or receiving data from the CONTROL UNIT when fault conditions exist: cable between TRANSCEIVER and CONTROL UNIT not connected or failure of + 5V power supply in CIM crate. If TS = 0 no Q response is given. The delay of the circuits used in the handshake especially in the optocouplers should

be as low as possible so that TS can change state well before the strobe S1.

Hold circuits

A strap on the printed circuit card can be placed in two positions: HOLD = ON or HOLD = OFF. A R-S flip-flop is used for the HOLD. The HOLD flip-flop is set if equation (3) is true:

$$H = R \cdot H \cdot TS. \qquad (3)$$

The set signal is differentiated so that the HOLD flip-flop can be reset by the end-of-operation (EOP) pulse from the CONTROL UNIT. The HOLD option on the P2-line stops the dataway cycle in such a way that the set in other case is always true. The HOLD option flip-flop can also be reset by the CAMAC Z.

Transfer mode

When the HOLD option is off (H = 0), reading from a power supply module must be accomplished by means of two commands, i.e. to read the memory control word, the following CAMAC commands must be given:

a) to transfer data from power supply module to transceiver buffer register: CNA(2)F(30),

b) to read from TRANSCEIVER buffer register to the computer: CNA(2)F(6).

It is not possible to ensure that these commands are following directly each other in time. It may happen that another command will try to read the buffer register between command a) and b). Therefore a memory and a comparator are incorportated in the TRANSCEIVER (see Fig. 5). The memory is loaded on a transfer command (F(12), F(14), F(21) or F(30)) according to condition (4):

$$TR * \overline{H} * S2. \qquad (4)$$

Upon a read command (F(0), F(1), F(4) or F(6)) Q response is given only if K = 1, i.e. when a stored transfer command is equal to the corresponding read command.

Timing of signals between the TRANSCEIVER and the MULTIPOLE CONTROL UNIT

Fig. 6 shows the timing diagram for writing. From signal N it can be seen that the CAMAC dataway cycle in this case takes 1.7 µs. This is due to the distance (∿ 20 m) between the CAMAC crate and the computer interface ICP11B.

The handshake signal HO is returned so that the TRANSFER STATUS bit TS is set after 270 ns. The crate select signal CN is sent at 480 ns. The CONTROL UNIT sends the END of OPERATION EOP signal after 2.3 µs.

Fig. 7 shows a diagram for the transfer commands (HOLD off). The cycle is in this case 180 ns shorter than write because the crate select signal CN is sent at 300 ns. The EOP arrives 2.1 µs after the start of the CAMAC dataway cycle.

Fig. 8 shows a diagram for reading with HOLD. The CAMAC DATAWAY cycle is in this case 3.5 µs. After the status bit TS is set the P2-line (HOLD) goes to OV. and the CAMAC DATAWAY cycle is stopped until the EOP from the CONTROL UNIT arrives. Thereafter the CAMAC dataway cycle resumes at the timing point it was stopped.

In all above cases the transmission distance between the TRANSCEIVER and the MULTIPOLE CONTROL UNIT was 3 m.

2.2 MULTIPOLE CONTROL UNIT

Fig. 9 shows a block diagram of the CONTROL UNIT. The main parts are the handshake circuit, subfunction and subaddress register, address decoder, READ register, WRITE register, timing circuit and master reset circuit.

Upon the arriving of the crate select signal CN the CONTROL UNIT cycle begins. CN loads the subaddress and subfunction register and starts the timing circuit. This circuit provides 7 different timing pulses T1 to T7 each 200 ns long. The cycle takes approximately 1.7 µs.

The 3 bit subaddress is decoded to give 6 individual station lines. A seventh line is used as a subaddress for two 16 bit status words which are entered directly to the CONTROL UNIT via the back edge connector. The seventh line of the decodes is also used for the reset bit of the POWER FAILURE CIRCUIT.

Fig. 10 shows a timing diagram of signals between the CONTROL UNIT and the power supply modules. During a write operation T1 loads the WRITE Register. T2 sets the bus enable flip-flop and this enables the address decoder and function gates. During T4 the write strobe is active and loads the data from the WRITE register to the memory of the power supply module. The "bus enable flip flop" is reset by T6, and during T7 the "End of operation signal" EOP 13 sent to the TRANSCEIVER.

A read cycle starts by T2, which sets the bus enable flip-flop. The data from a power supply module is loaded into the READ register by T4. T5 sends a load signal LOD to the TRANSCEIVER. T6 resets the bus enable flip-flop and the end of operation EOP is sent by T7.

The master reset circuit is used to clear (set = 0) the memory data register in all power supply modules upon the switch on of the + 5 V power supply of the CIM crate,by writing 0 to all modules. This is necessary because these registers do not have separate clear inputs.

3. Computer test program

A test program has been written in ESAU[3)] with the RSX 11-D operating system on a PDP 11/45. With this program it is possible to make a complete functional test of the TRANSCEIVER and the CONTROL UNIT. The CONTROL UNIT is placed in a special test CIM-crate and is connected to a test module, which simulates a power supply module. This module contains one 16 bit buffer register which can be written and read and also 3 x 16 bit hardwired test words, which can only be read. These test words can be read either normal or complemented. The mode is determined by help of a front panel switch.

The program is called TRATST-ESU. Below an example using the program is shown.

```
MCR>RUN E'.AU

*** ESAU 11'45 RSX11D ***

MCR>
<LOAD TRATST ESU
<
 RUN
CRATE NUMBER C=?

 2
IN WHAT STATION NUMBER IS THE TRANSCEIVER

 8
HOLD OPTION IS ON   (SEE PC-BOARD SWITCH)
CIM CRATE 1 IS CONNECTED'
CIM CRATE 2 IS NOT CONNECTED'
SCANNING TEST                => DO 4
READ TEST                    => DO 6
WRITE AND READ BACK TEST => DO 10
 AFTER CHANGE OF CABEL OR PC-BOARD SWITCH = DO 1
```

There are 3 different tests which can be performed:

3.1 Scanning test

The test is called by the command DO4. In this program a scanning is done consisting of all possible combinations of subaddresses and functions to detect all X-responses of the TRANSCEIVER. The test can be done with or without test protocoll. This saves 146 lines of printout text.

```
<DO 4
SCANNING TEST OF X-RESPONSE
FULL PROTOCOLL NEEDED YES = 1 NO = 0

 1

THE FOLLOWING FUNC AND SUBADDRS GIVE X-RESPONSE
   X    Q    N    A    F  COMMENTS
   1    1    6    0    0       OK
   1    1    8    0    1       OK
   1    1    8    0    4       OK
   1    1    8    0    6       OK
```

1	0	8	0	12	OK
1	0	8	0	14	OK
1	1	8	0	16	OK
1	0	8	0	28	OK
1	0	8	0	30	OK
1	1	8	1	0	OK
1	1	8	1	1	OK
1	1	8	1	4	OK
1	1	8	1	6	OK
1	0	8	1	12	OK
1	0	8	1	14	OK
1	1	8	1	16	OK
1	0	8	1	28	OK
1	0	8	1	30	OK
1	1	8	2	0	OK
1	1	8	2	1	OK
1	1	8	2	4	OK
1	1	8	2	6	OK
1	0	8	2	12	OK
1	0	8	2	14	OK
1	1	8	2	16	OK
1	0	8	2	28	OK
1	0	8	2	30	OK
1	1	8	3	0	OK
1	1	8	3	1	OK
1	1	8	3	4	OK
1	1	8	3	6	OK
1	0	8	3	12	OK
1	0	8	3	14	OK
1	1	8	3	16	OK
1	0	8	3	28	OK
1	0	8	3	30	OK
1	1	8	4	0	OK
1	1	8	4	1	OK
1	1	8	4	4	OK
1	1	8	4	6	OK
1	0	8	4	12	OK
1	0	8	4	14	OK
1	1	8	4	16	OK
1	0	8	4	28	OK
1	0	8	4	30	OK

1	1	8	5	0	OK
1	1	8	5	1	OK
1	1	8	5	4	OK
1	1	8	5	6	OK
1	0	8	5	12	OK
1	0	8	5	14	OK
1	1	8	5	16	OK
1	0	8	5	28	OK
1	0	8	5	30	OK
1	1	8	6	0	OK
1	1	8	6	1	OK
1	1	8	6	4	OK
1	1	8	6	6	OK
1	0	8	6	12	OK
1	0	8	6	14	OK
1	1	8	6	16	OK
1	0	8	6	28	OK
1	0	8	6	30	OK
1	1	8	7	0	OK
1	1	8	7	1	OK
1	1	8	7	4	OK
1	1	8	7	6	OK
1	0	8	7	12	OK
1	0	8	7	14	OK
1	1	8	7	16	OK
1	0	8	7	28	OK
1	0	8	7	30	OK
1	0	8	8	0	OK
1	0	8	8	1	OK
1	0	8	8	4	OK
1	0	8	8	6	OK
1	0	8	8	12	OK
1	0	8	8	14	OK
1	0	8	8	16	OK
1	0	8	8	28	OK
1	0	8	8	30	OK
1	0	8	9	0	OK
1	0	8	9	1	OK
1	0	8	9	4	OK
1	0	8	9	6	OK
1	0	8	9	12	OK
1	0	8	9	14	OK
1	0	8	9	16	OK
1	0	8	9	28	OK
1	0	8	9	30	OK

```
1   0   8   10   0      OK
1   0   8   10   1      OK
1   0   8   10   4      OK
1   0   8   10   6      OK
1   0   8   10   12     OK
1   0   8   10   14     OK
1   0   8   10   16     OK
1   0   8   10   28     OK
1   0   8   10   30     OK
1   0   8   11   0      OK
1   0   8   11   1      OK
1   0   8   11   4      OK
1   0   8   11   6      OK
1   0   8   11   12     OK
1   0   8   11   14     OK
1   0   8   11   16     OK
1   0   8   11   28     OK
1   0   8   11   30     OK
1   0   8   12   0      OK
1   0   8   12   1      OK
1   0   8   12   4      OK
1   0   8   12   6      OK
1   0   8   12   12     OK
1   0   8   12   14     OK
1   0   8   12   16     OK
1   0   8   12   28     OK
1   0   8   12   30     OK
1   0   8   13   0      OK
1   0   8   13   1      OK
1   0   8   13   4      OK
1   0   8   13   6      OK
1   0   8   13   12     OK
1   0   8   13   14     OK
1   0   8   13   16     OK
1   0   8   13   28     OK
1   0   8   13   30     OK
1   0   8   14   0      OK
1   0   8   14   1      OK
1   0   8   14   4      OK
1   0   8   14   6      OK
1   0   8   14   12     OK
1   0   8   14   14     OK
1   0   8   14   16     OK
1   0   8   14   28     OK
1   0   8   14   30     OK
1   0   8   15   0      OK
1   0   8   15   1      OK
1   1   8   15   2      OK
1   0   8   15   4      OK
1   0   8   15   6      OK
1   0   8   15   12     OK
1   0   8   15   14     OK
1   0   8   15   16     OK
1   0   8   15   28     OK
1   0   8   15   30     OK
END OF TEST NO ERRORS
```

3.2 READ test

This test is called by command DO-6. The 3 hardwired test words in the test module are read both in normal and complemented mode. The test should be done both with and without the HOLD option. In the HOLD off mode a scanning of functions is made to check the memory and comparator in the TRANSCEIVER. Only two subaddresses are valid. For CIM-crate 1, A = 2 and for CIM-crate 2, A = 10. Two examples of a READ test are shown below:

1)

```
<DO 6
READ TEST
A=2 OR A= 10?
 10
SET SIMULATOR MODULE SWITCH TO POS "N" AND TYPE "1"
 1
SET SIMULATOR MODULE SWITCH TO POS "I" AND TYPE "0"
 0
END OF TEST
```

2)

```
 DO 6
READ TEST
A=2 OR A= 10?
 2
SET SIMULATOR MODULE SWITCH TO POS "N" AND TYPE "1"
 1
*ERROR* F= 0 DATA=-6487
*ERROR* F= 1 DATA=-6487
*ERROR* F= 4 DATA=-6487
SET SIMULATOR MODULE SWITCH TO POS "I" AND TYPE "0"
 0
*ERROR* F= 0 DATA=-6487
*ERROR* F= 1 DATA=-6487
*ERROR* F= 4 DATA=-6487
END OF TEST
```

Example of READ test with improper reading.

3.3 WRITE and READ BACK TEST

This test is called by the command DO 1Ø. The test writes the 16 bit memory register in the test-module and reads it back. This is done for a sequence of numbers covering all bit positions. The test should be done with and without HOLD option. Only two subaddresses is valid: for CIM-crate 1, A = 2 and for CIM-crate 2, A = 10.

Example of a WRITE AND READ BACK test.

```
 DO 1Ø
A=?
:
 1Ø
WRITE - READ  TEST  IS OK!
<
```

Example of a WRITE AND READ BACK test with TRANSCEIVER error.

```
<DO 1Ø
A=?
:
 2
*ERROR* 1/=-6487
*ERROR* 2/=-6487
*ERROR* 4/=-6487
*ERROR* 8/=-6487
*ERROR* 16/=-6487
*ERROR* 32/=-6487
*ERROR* 64/=-6487
*ERROR* 128/=-6487
*ERROR* 256/=-6487
TOO MANY ERRORS - TEST STOPS
<
```

Distribution : MPS Scientific Staff

REFERENCES

1. G. Baribaud et al., The new PSB multipoles, MPS/BR Note to be published.

2. F. Bel et al., CAMAC TIMING with special reference to crate controllers, CERN NP CAMAC Note 38-00, Dec. 1971.

3. J. Gamble, J. Stark, ESAU Version I, MPS/CCI/Note 75-15.

DATAWAY SIGNALS (pos. logic)						CAMAC Function	Encoded Function Code			COMMENT
$\overline{N}$	$\overline{F1}$	$\overline{F2}$	$\overline{F4}$	$\overline{F8}$	$\overline{F16}$		CR1	CR2	CCW	
0	1	1	1	1	1	F(0)	1	0	0	Read IDENTIFICATION WORD
0	0	1	1	1	1	F(1)	0	0	0	Read DIGITAL TEST WORD
0	1	0	1	1	1	F(2)	–	–	–	Read TRANSCEIVER MODULE STATUS WORD
0	1	1	0	1	1	F(4)	0	1	0	Read REGULATOR STATUS WORD
0	1	0	0	1	1	F(6)	1	1	0	Read MEMORY CONTROL WORD
0	1	1	0	0	1	F(12)	1	0	0	Transfer IDENTIFICATION WORD
0	1	0	0	0	1	F(14)	0	0	0	Transfer DIGITAL TEST WORD
0	1	1	1	1	1	F(16)	X	X	1	Write MEMORY CONTROL WORD
0	1	0	1	0	0	F(28)	0	1	0	Transfer REGULATOR STATUS WORD
0	1	1	0	0	0	F(30)	1	1	0	Transfer MEMORY CONTROL WORD

TABLE 1

CAMAC DEVICE DATA SHEET

DATE:

1 CLASSIFICATION	2 CODE

3 DESIGNATION	4 MANUFACTURER	5 TYPE/VERSION	6 PRICE
TRANSCEIVER	MPS-CERN	MPS/BR 861-12	

7 WORDS/BITS	8 RANGE/RESOLUTION/ACCURACY	9 SUPPLY	10 WIDTH
16 bits	Writes and reads data in modules in 2 separate CIM-crates	+ 6V	1/25

11 I/O/SIGNAL/NAME		TYPE/POLARITY	CONNECTOR
IN/OUT	connection crate 1	Optocouplers bidirectional TTL	Cannon 2D52
IN/OUT	connection crate 2	Optocouplers bidirectional TTL	Cannon 2D52
IN	external N	TTL open collector	LEMO

12 MANUAL CONTROLS

Printed circuit board switch for HOLD option ON/OFF

13 INDICATORS

Crate 1 ON if crate 1 is addressed

Crate 2 ON if crate 2 is addressed

14 DATAWAY FUNCTIONS

F(0), F(1), F(2), F(4), F(6), F(12), F(14), F(16), F(28), F(30)

15 DATAWAY STATUS/CONTROLS

P2 HOLD

☒ X ☒ Z
☒ Q ☐ C
☐ L ☐ I
☐ B ☐ P1
☒ P2

16 DATAWAY COMMANDS WITH Q-RESPONSE AND SIGNIFICANCE

Without HOLD option (switch OFF) the following pair of commands are needed:

F(12) A(0-5) F(0) A(0-5)	Read Q=1	identification word CRATE 1, Power supply module 1 to 6.
F(12) A(6) F(0) A(6)	Read Q=1	ready on/off status word in CRATE 1
F(12) A(8-13) F(0) A(8-13)	Read Q=1	identification word CRATE 2, Power supply module 1 to 6
F(12) A(14) F(0) A(14)	Read Q=1	ready on/off status word in CRATE 2
F(14) A(0-5) F(1) A(0-5)	Read Q=1	test word CRATE 1, Power supply module 1 to 6
F(14) A(6) F(1) A(6)	Read Q=1	crate status word CRATE 1
F(14) A(8-13) F(1) A(8-13)	Read Q=1	test word in CRATE 2 of Power supply module 1 to 6

cont'd

17 COMMENTS

MPS/BR Note/75-20 describes the module in detail.

☒ NON-STANDARD FUNCTIONS USED
☐ F ☒ A-LINES NOT FULLY DECODED

☒ DATAWAY NOT USED ACCORDING TO 4100 SPECS
☐ RIGHT- ☐ LEFT-MOST STATION ADDRESS

(cont'd)

F(14) A(14) } Read Q=1 crate status word CRATE 2
F(1) A(14) }

F(28) A(0-5) } Read Q=1 status word in CRATE 1 of Power supply module 1 to 6
F(4) A(0-5) }

F(28) A(8-13) } Read Q=1 status word in CRATE 2 of Power supply module 1 to 6
F(4) A(8-13) }

F(30) A(0-5) } Read Q=1 memory in CRATE 1 of Power supply module 1 to 6
F(6) A(0-5) }

F(30) A(0-5) } Read Q=1 memory in CRATE 2 of Power supply module 1 to 6
F(6) A(0-5) }

With HOLD option (Switch ON) the following commands are needed for reading

F(0) A(0-5) Q = 1 Read identification word in CRATE 1 of Power supply module 1 to 6

F(0) A(6) Q = 1 Read ready on/off status word in CRATE 1

F(0) A(8-13) Q = 1 Read identification word in CRATE 2 of Power supply module 1 to 6

F(0) A(14) Q = 1 Read ready on/off status word in CRATE 2

F(1) A(0-5) Q = 1 Read test word in CRATE 1 of Power supply module 1 to 6

F(1) A(6) Q = 1 Read crate status word CRATE 1

F(1) A(8-13) Q = 1 Read test word in CRATE 2 of Power supply module 1 to 6

F(1) A(14) Q = 1 Read crate status word CRATE 2

F(4) A(0-5) Q = 1 Read status word in CRATE 1 of Power supply module 1 to 6

F(4) A(8-13) Q = 1 Read status word in CRATE 2 of Power supply module 1 to 6

F(6) A(0-5) Q = 1 Read memory in CRATE 1 of Power supply module 1 to 6

F(6) A(8-13) Q = 1 Read memory in CRATE 2 of Power supply module 1 to 6

The following command is independent of HOLD option.

F(16)A(0-5)S1 Q = 1 Write memory in CRATE 1 of power supply module 1 to 6

F(16)A(6)S1 Q = 1 Reset power failure circuit in CRATE 1

F(16)A(8-13)S1 Q = 1 Write memory in CRATE 2 of power supply module 1 to 6

F(16)A(14)S1 Q = 1 Reset power failure circuit in CRATE 2

F(2)A(15) Q = 1 Read TRANSCEIVER module states R1 on if connection to CRATE OK
R2 on if connection to CRATE OK
R3 on if HOLD option is ON.

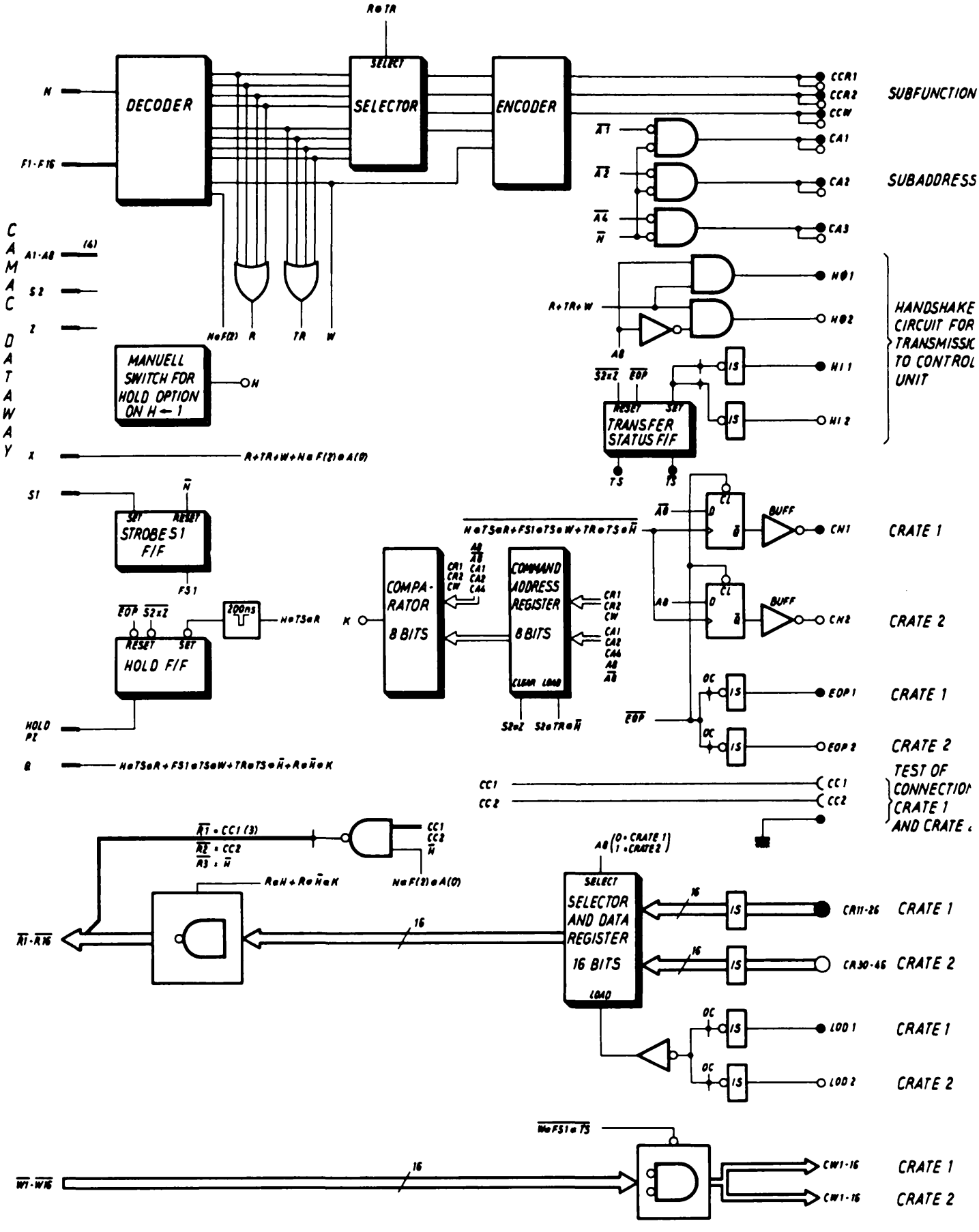

Fig. 1

BLOCK DIAGRAM TRANSCEIVER

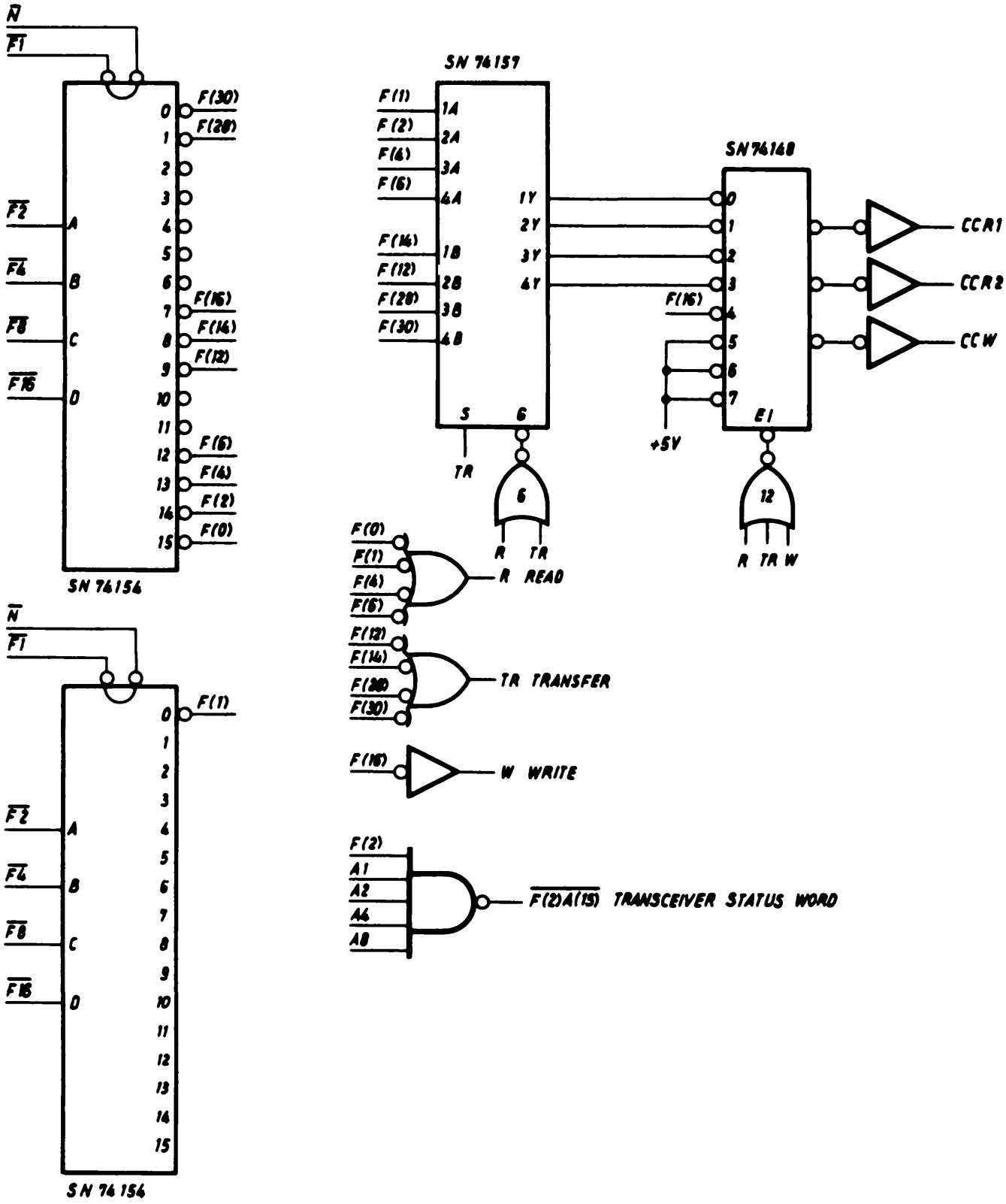

Fig. 2

DECODING AND ENCODING OF FUNCTIONS

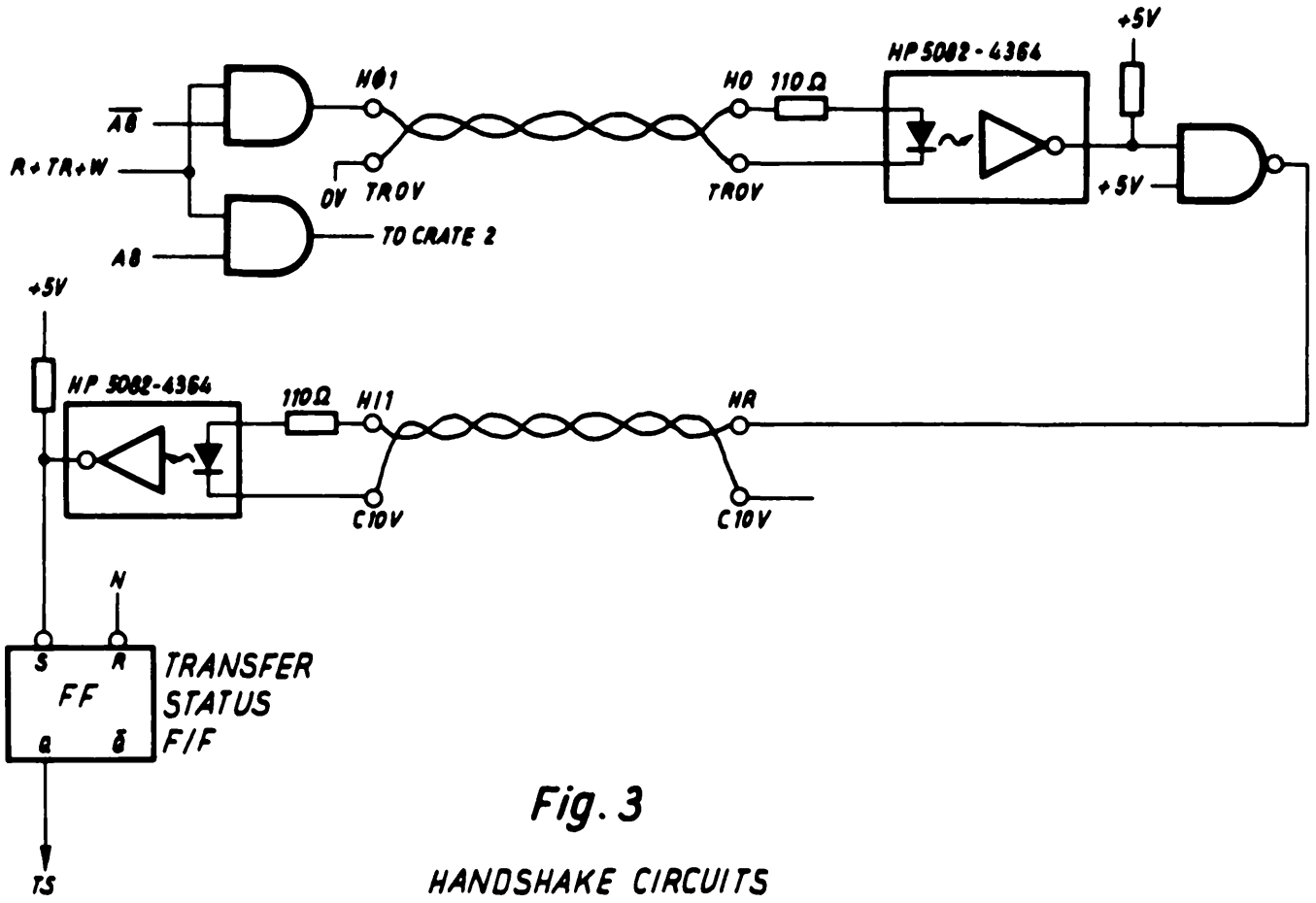

Fig. 3

HANDSHAKE CIRCUITS

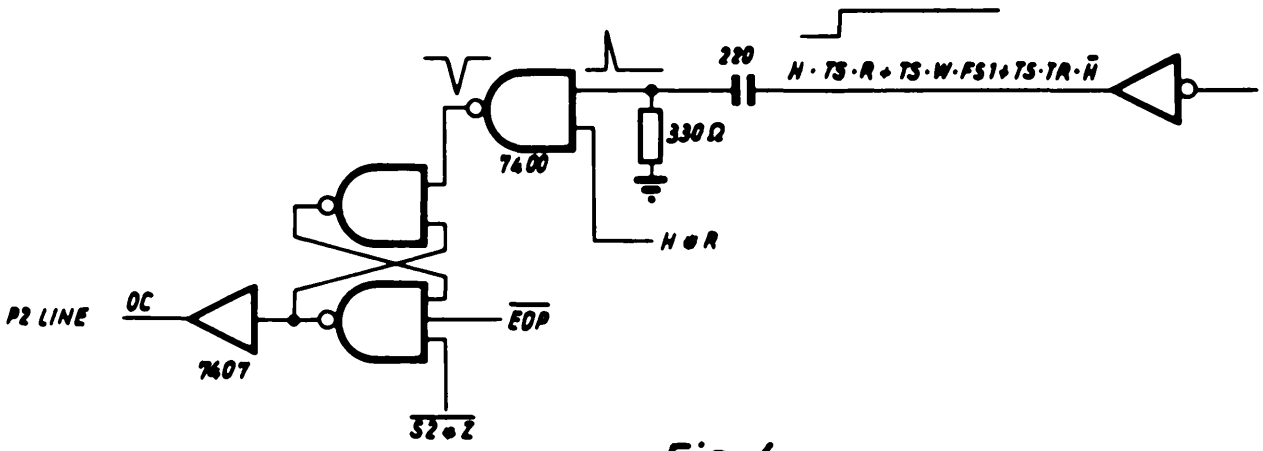

Fig. 4

HOLD CIRCUITS

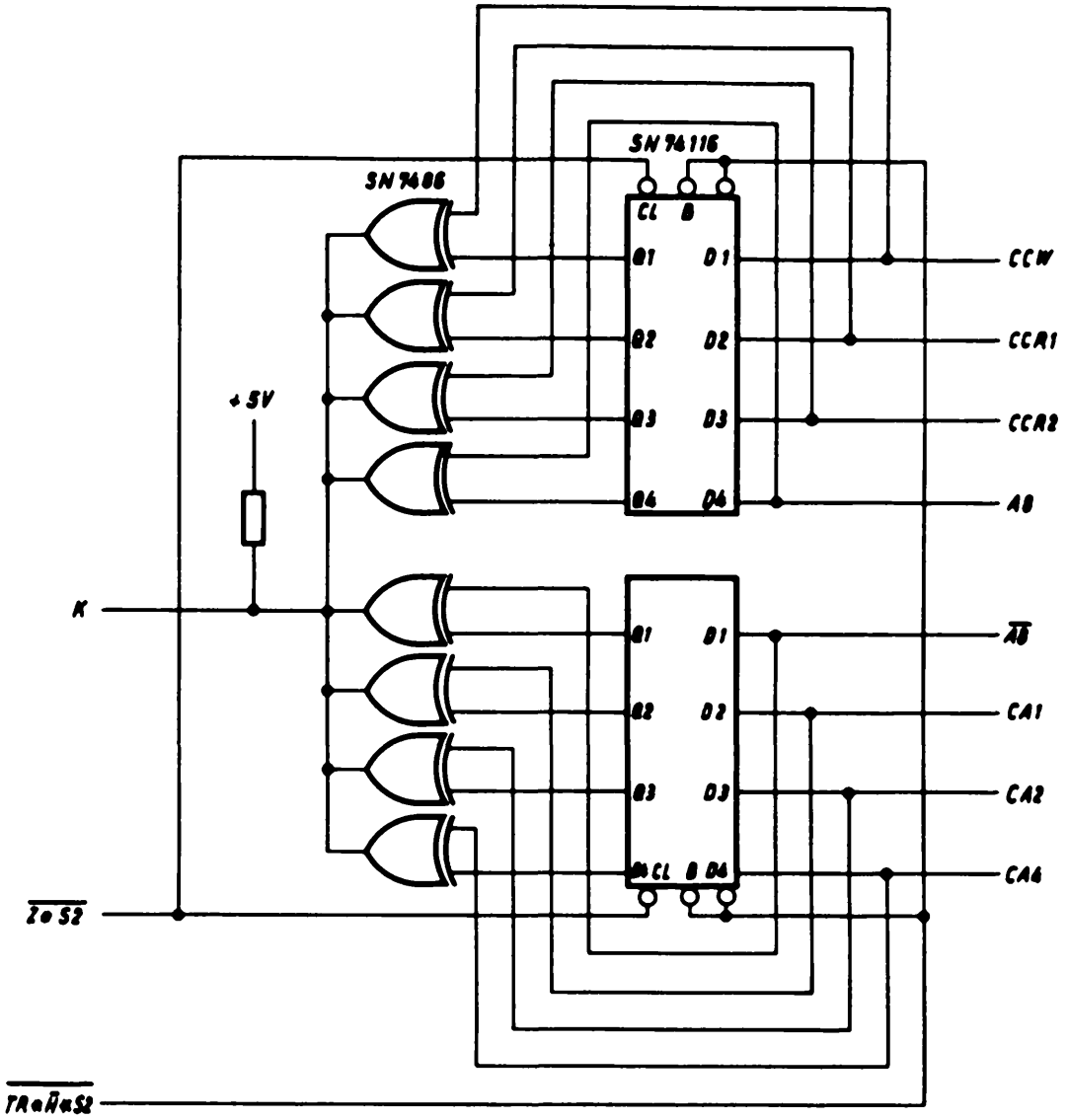

Fig. 5

COMMAND AND ADDRESS REGISTER AND COMPARATOR

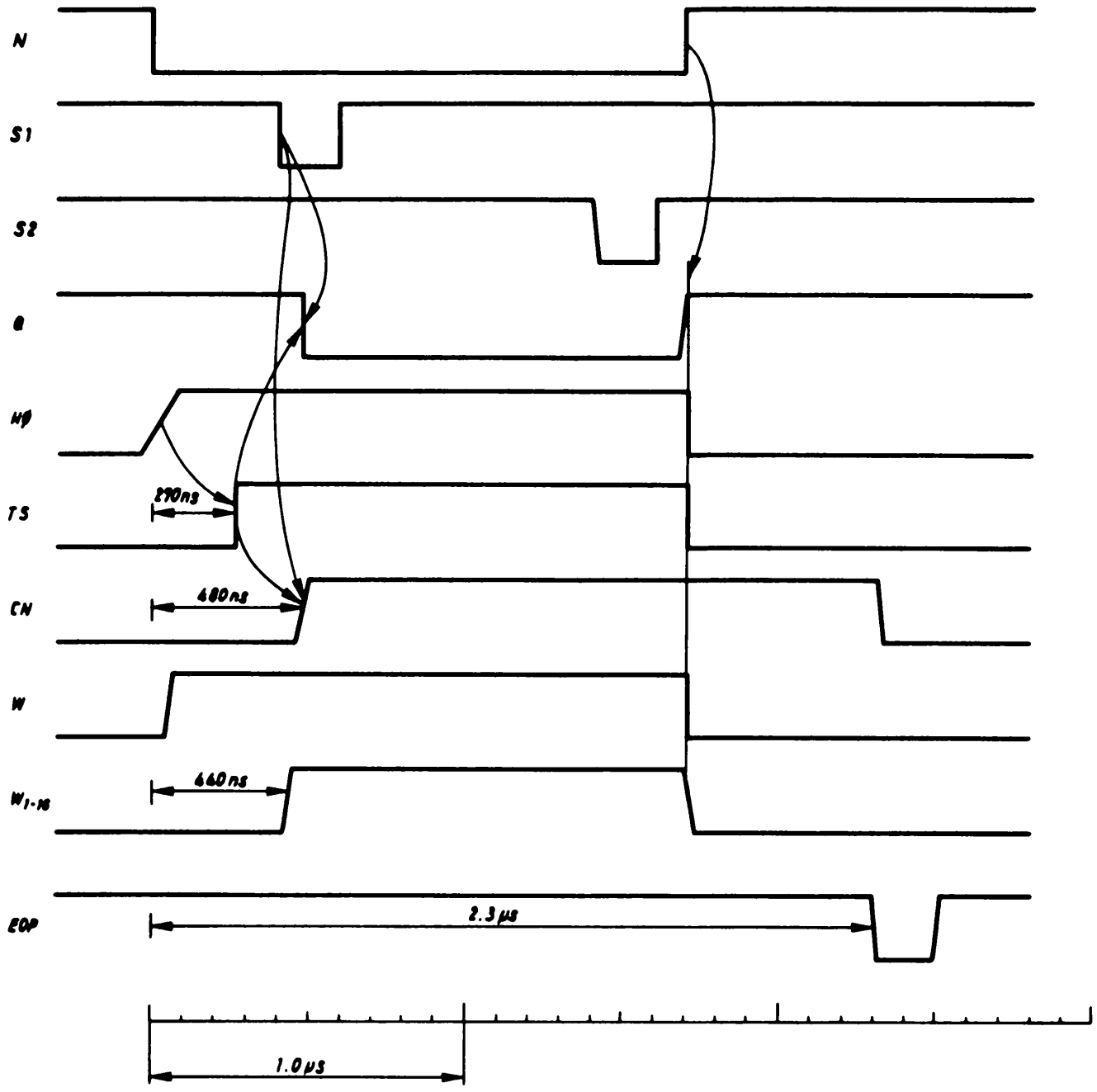

Fig. 6

TIMING DIAGRAM FOR WRITE TIMING TRANSCEIVER MULTIPOLE CONTROL UNIT

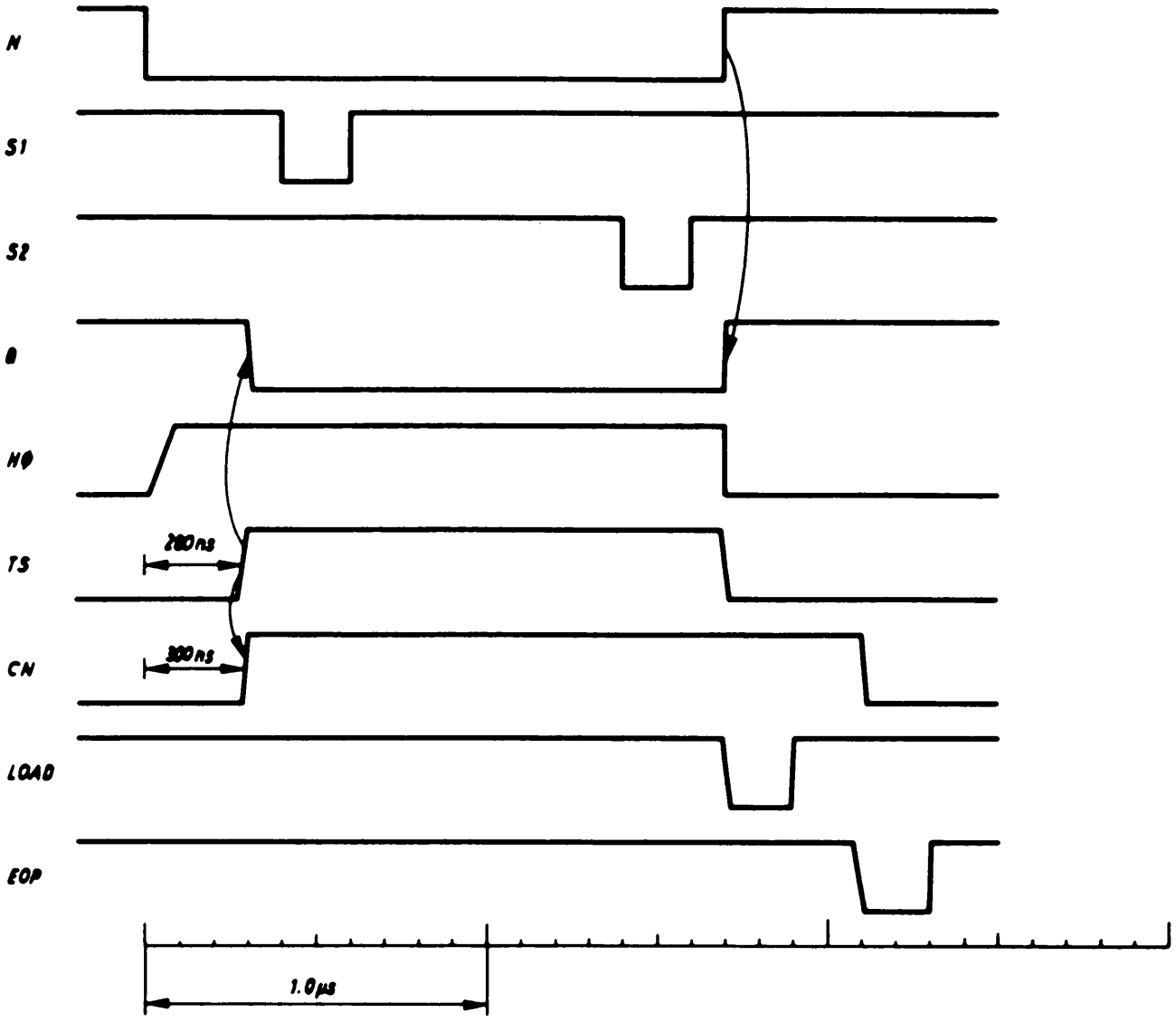

Fig. 7

TIMING DIAGRAM FOR TRANSFER COMMAND TIMING WITH HOLD OFF TRANSCEIVER MULTIPOLE CONTROL UNIT

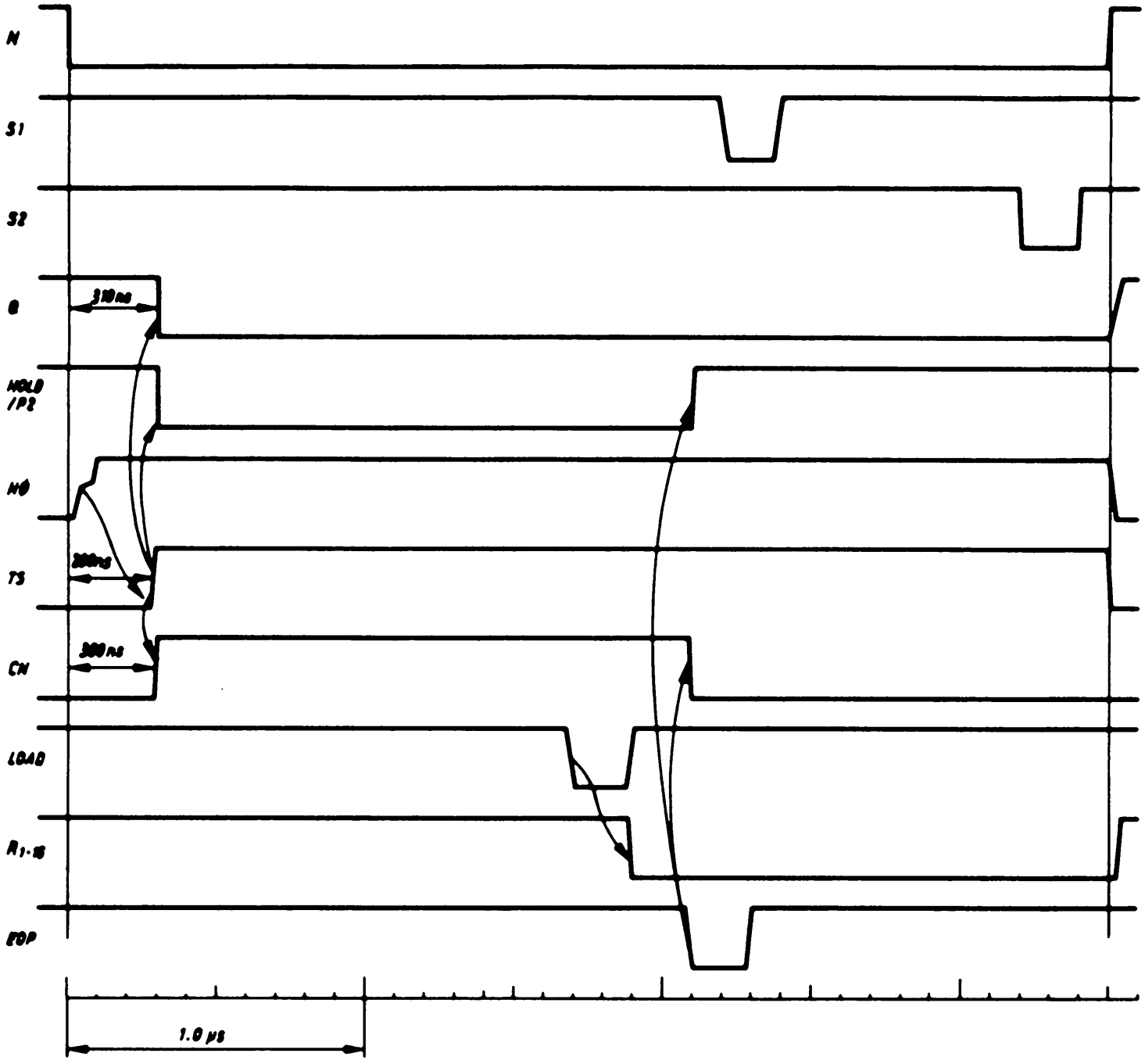

Fig. 8

TIMING DIAGRAM FOR READ TIMING WITH HOLD TRANSCEIVER - MULTIPOLE CONTROL UNIT

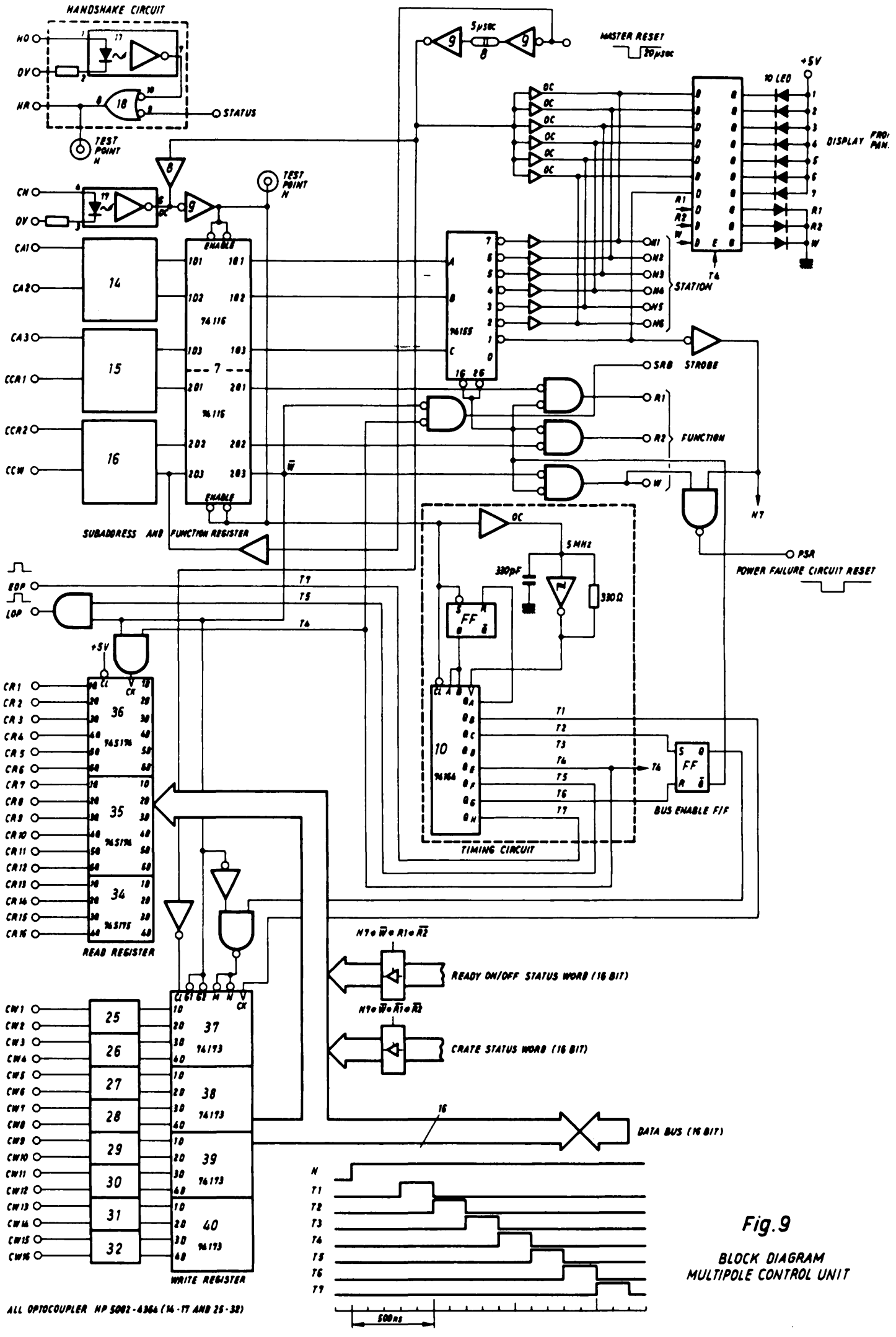

Fig.9

BLOCK DIAGRAM
MULTIPOLE CONTROL UNIT

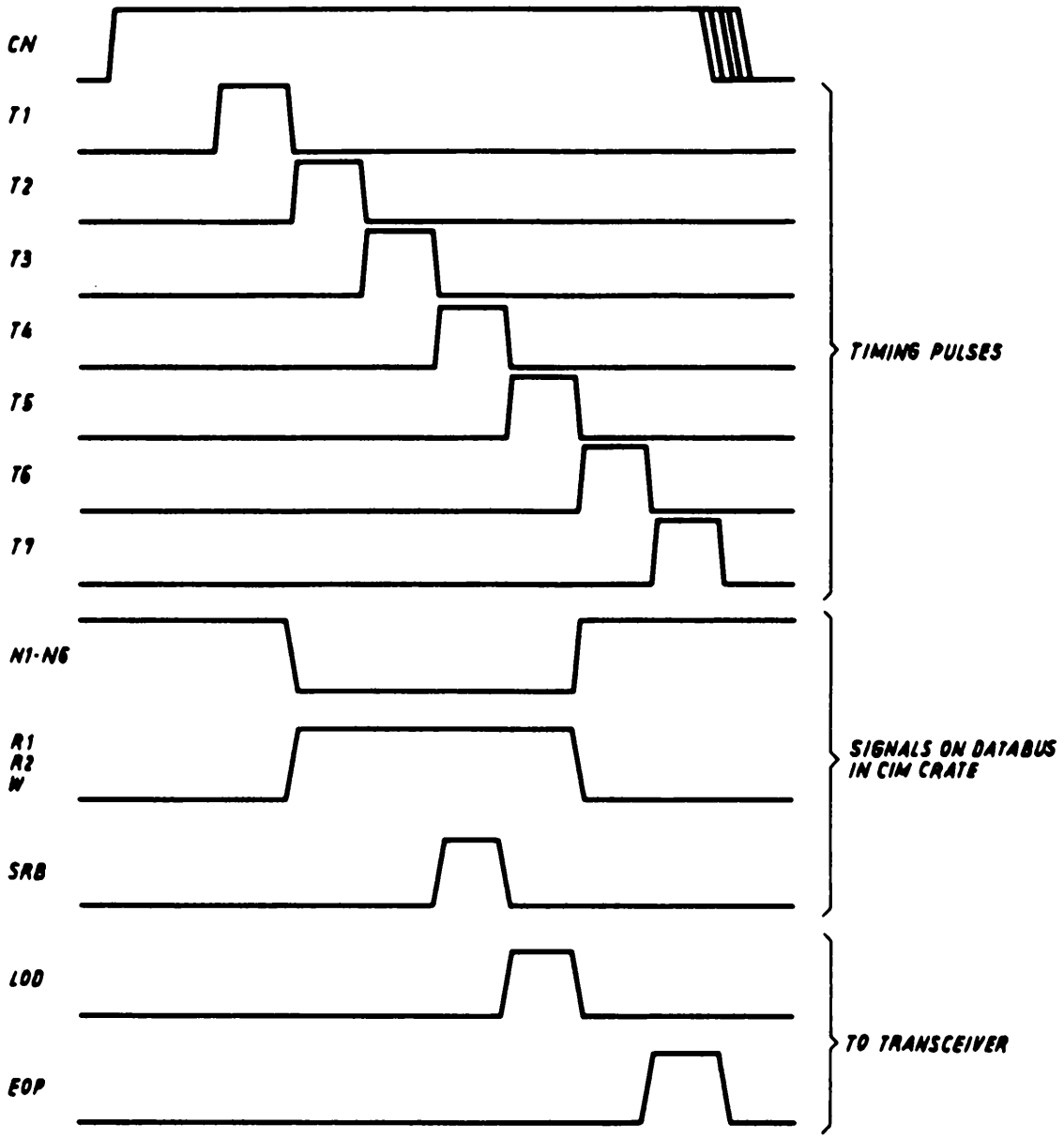

Fig. 10

TIMING DIAGRAM MULTIPOLE CONTROL UNIT