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GENERAL DESCRIPTION OF THE PS HADRON INJECTION KICKER CONTROL AND ACQUISITION SYSTEM (KSU-KICK STRENGTH UNIT)

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Geneva, Switzerland
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B. Bleus, H. Gaudillet, J. Schipper

Abstract

The CERN PS control system is being completely rejuvenated. The former system, whose design options were frozen in 1978, used 16 bit minicomputers for process computers and for conventional consoles and services.

These are being replaced by the agreed CERN Standard Architecture, using UNIX workstations as operator interface and VME based processors, under RT-UNIX.

This note describes the hardware and software implementations of the KSU interface for the KFA 45 hadron injection system.

1. INTRODUCTION

This note describes the conversion of the KFA 45 control and acquisition system, for the PS hadron injection kickers, to allow adaptation to the control system changes mentioned in the abstract. The kicker system allows multi-user operations i.e., independently controllable parameters for the various injection processes.
A 'user' being a label for a set of parameters for a specific cycle.

2. OVERVIEW OF THE CPS CONTROL SYSTEM

The standard model used in the CPS complex is the image of the common architecture of the CERN accelerator control system (Figure1); it consists mainly of three different layers;

- Control room (MCR) layer with workstations and central servers; the connection to this layer is done only through Ethernet cable
- Front end computing layer distributed around the machines, based on Device Stub Controllers, DSC-KSU for the kicker system.
- Equipment control layer, the kicker hardware controlled by the DSC-KSU.

Information on the first mentioned layer can be found in the various reports written by the PS controls group (Refs. 1, 2, 3, 4, 5.)

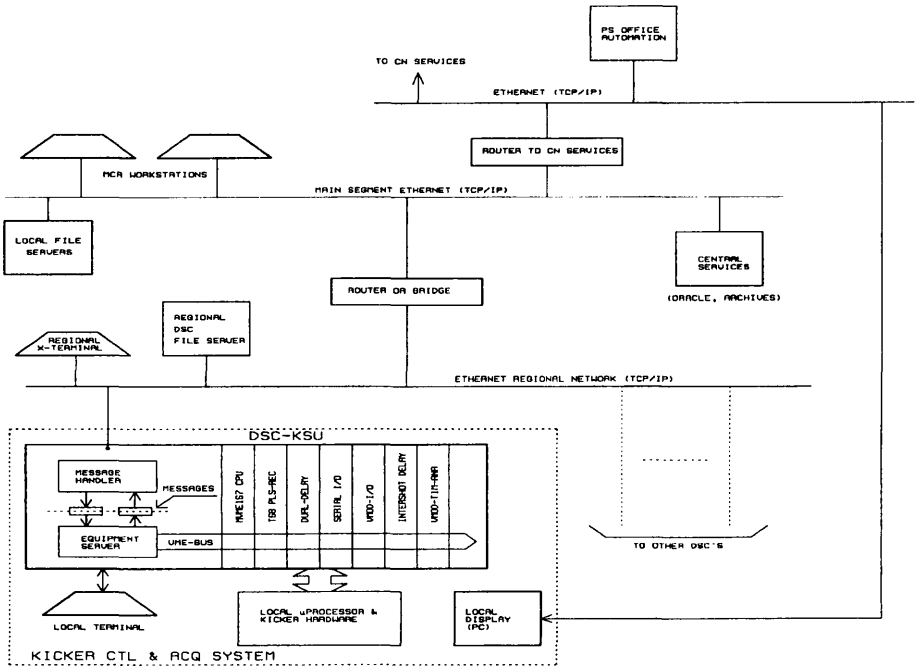


Figure1

3. THE FRONT-END COMPUTING LAYER (DSC-KSU)

The DSC-KSU interface represents the front end computing layer in the new control system. It can be found in the local area, i.e. near the kicker hardware, connected to the MCR workstations via a LAN, and to the kicker hardware via VME hardware modules.
The main functions of the DSC are:

- To provide a uniform interface to the equipment as seen from the MCR workstations.
- To provide direct control and acquisition of the kicker hardware, interfaced directly to the DSC.
- To act as a master and data concentrator for all the Local Processor Units (LPU, installed on every kicker module), interfaced via RS232 serial I/O links.

The DSC comprises a real-time UNIX compatible Operating System, LynxOS, it allows to run several tasks concurrently. The DSC is diskless meaning that a DSC file server is required to provide storage space for the operating system, system startup files, application programs, the real-time task and their data files.
The DSC provides a fast and deterministic response to external events which is necessary when operating in PPM mode (pulse to pulse modulation.)

PPM - operations whereby a system performs a function upon the arrival of a particular event sent by the PLS and performs the same function upon every subsequent similar event without re-programming.

PLS - program line sequencer, timing system consisting of a bit stream, containing information such as user, cycle and particle type.

4. COMMUNICATION BETWEEN FRONT-END AND CONTROL ROOM

Someone wishing to change the control parameters for the KFA kicker system would access it by means of an application program running on a workstation (or PC) in the MCR. This program allows the user to enter commands and view the results.

The application program does not communicate with the real-time task directly however, but via a message handler and equipment server (fig1), the so called equipment module, which is running on the same DSC as the real-time task. It is the duty of the equipment module to verify the validity of the request from the user before sending it to the real-time task, as well as receiving resultant messages.

5. LOCAL ACCESS FACILITIES

- Local display, showing all relevant data of the kicker complex for synoptic use.
  Application program running on local PC.
- Local terminal, (PC) connected to the DSC's tty1 socket, for local control of the KSU.
- Regional workstation, not for specific applications, can be seen as duplication of some services in the MCR.

6. BASIC PRINCIPLES OF THE KFA 45 SYSTEM

The KFA45 system consists of 4 kicker modules each one having its own Local Processor Unit (LPU - G64 bus standard).
To allow multi-users operations, the different 'kicks' for the different 'users' have to be modulated in pulse amplitude and width, to obtain the desired beam deflection.

The functionality of the KFA system is based on the standard PFN (Pulse Forming Network) principle (Figure2).

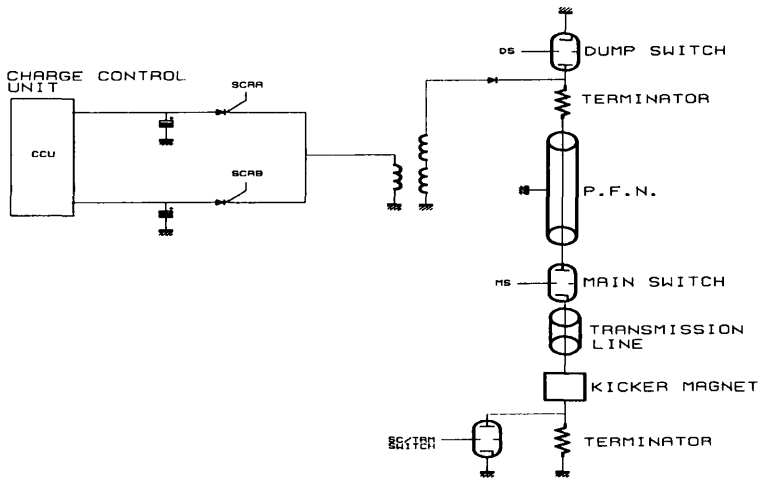


Figure 2

The charge control unit (CCU) can charge the PFN to the desired value from cycle to cycle.
To allow double batch operations two capacitor banks are required, one for batch A and one for batch B.
The use of the charge control unit makes the KFA45 a fully PPM compatible machine.

In addition the four kicker modules have the possibility to pulse either in a magnet with a terminating resistor (TRM) or in a short circuited magnet (SC).
When the magnet is in short circuit mode the current will double giving twice the kick strength compared to a terminated magnet, however the rise time of the pulse will increase significantly when in short circuit mode.

This process is fully PPM controllable and it is the KSU which decides the termination of the magnet.

The KSU will, if possible, select the kickers to pulse in a terminated magnet, this process of selecting the termination of the magnet is however completely transparent to the user.

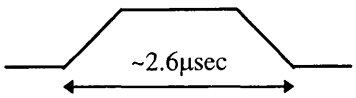
It is nevertheless possible to force a module to pulse in a SC or TRM, by means of the control parameters in the KSU equipment module (ANNEX1).

The CCU's obtain their reference voltage defining the pulse amplitudes from DAC's in the Local Processor Unit, and the pulse width is controlled by the MS & DS timing signals (START & END signals.)
By combining the different kicker modules the required beam deflection will be obtained.

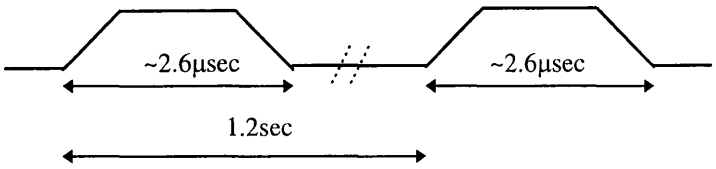
7. FORESEEN INJECTION OPERATION FOR THE KFA45

The following operations have to be covered by the KFA45 :

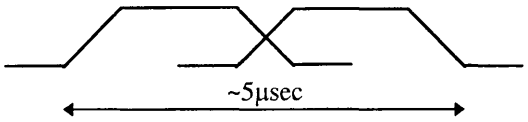
- Proton injection (SD42)
  1 Batch - 1 kick
  Pulse width ~ 2.6μsec



- Proton injection (double batch) - SPS/LHC
  2 Batches each with 1 kick, distance between batches ~1.2sec.
  Pulse width each ~ 2.6μsec



- Ion injection (long kick)
  1 Batch - 2 kicks
  Total pulse width ~ 5μsec



7.1 Particularities of the heavy ion injection scheme

The ion injection creates a few problems since the maximum pulse width that can be formed with the existing PFN is ~ 2.7μsec.
The required pulse width however is ~ 5μsec.

The solution applied to overcome this problem is to generate two overlapping pulses, augmenting the total pulse width up to the desired width, by changing the width of each individual pulse.

This however introduces some side effects.
To obtain the desired 'kick' amplitude all four kicker modules are required to pulse in a short circuited magnet.

Every pulse delivered by a kicker module produces a set of undesired reflection components due to thyratron switching effects.
(main switch and dump switch.)

Three of these (first order) reflection components will be discussed.

The principal reflection components caused by the main switch occur after a rising edge and falling edge of the kicker pulse and have a propagation delay of 2x transmission cable length.

The principal reflection component caused by the dump switch (refusal to switch on negative current) occurs after the falling edge of the kicker pulse, and has a propagation delay of 2x transmission cable length + 2x PFN length from the rising edge of the kicker pulse.

The reflection components caused by the main switches result in four reflection components near the middle of the sum signal, forming a 'hole' (or 'holes', depending on the propagation constants.)

The aim is to either create one large 'hole' in between two bunches, or two (maybe several) smaller 'holes' with a minor effect on the beam.

In order to be able to move the reflection components caused by the main switch in relation to each other, the following gymnastics are performed :

One of the two modules used to generate the first pulse will be delayed by δt at the end of the pulse (the start time of the pulses remain the same).
Furthermore one of the two modules used to generate the second pulse will be delayed with the same δt at the start of the pulse (the end time of the pulses remain the same).

The above mentioned process has been named reflection compensation for heavy ions.

8. DSC-KSU CONTROL AND ACQUISITION

8.1 Block diagram KFA45 control and acquisition system

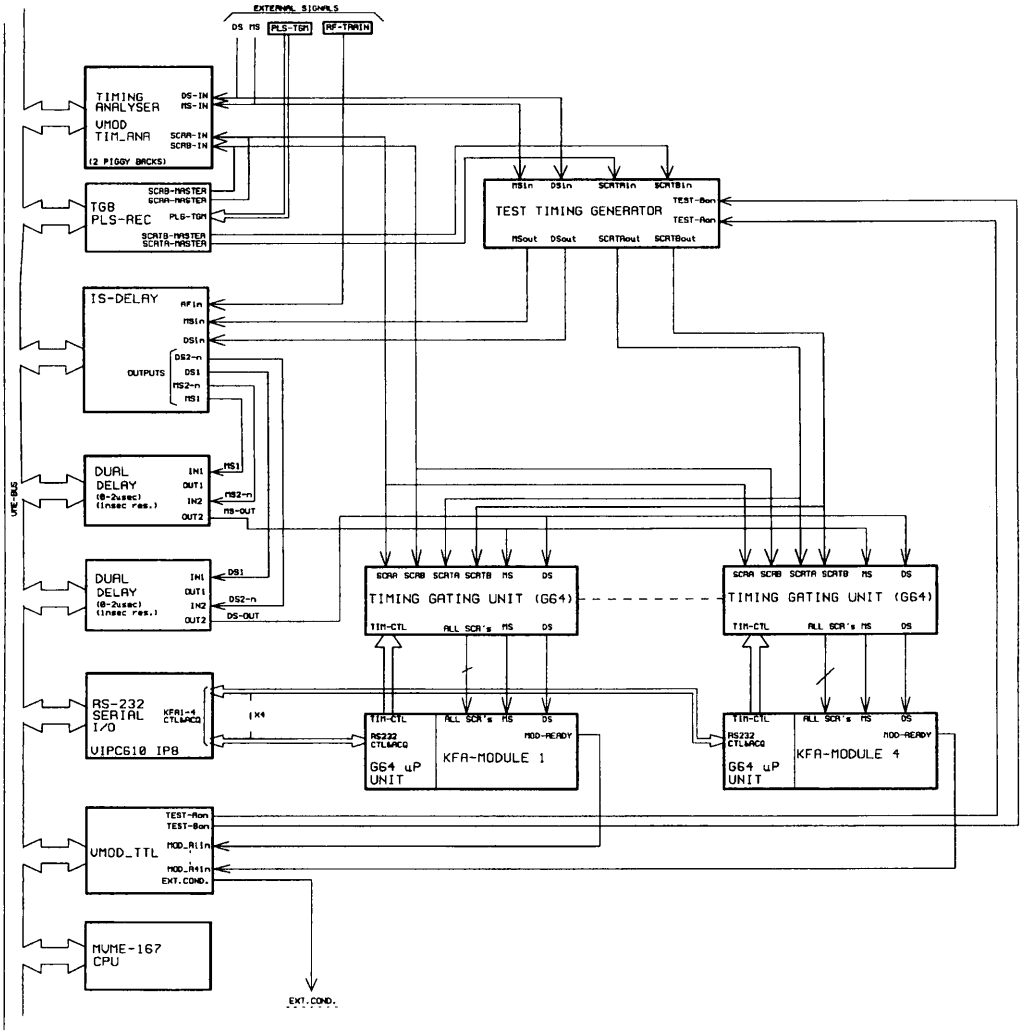


Figure 3

The block diagram above shows the lay-out of the KFA control and acquisition system.
In the following paragraphs the global functions of the system will be discussed.
Furthermore a short description will be given of the modules that form the interface between kicker equipment and MCR workstations. (i.e. the VME-modules).

8.2 Global features of the KFA45

The KFA45 can produce an ensemble of kick pulses, as can be seen in the figure below, to obtain the desired injection of the particle beam.

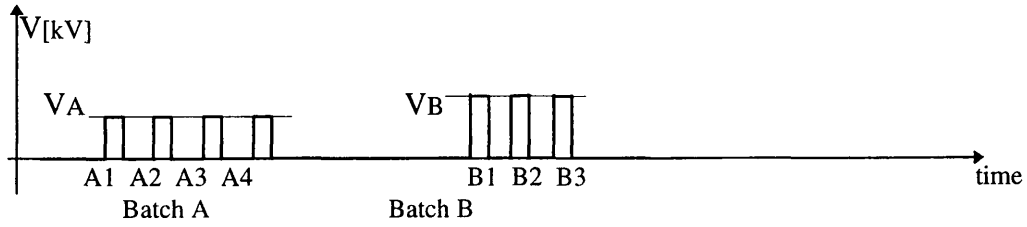


Figure 4

Kick: A voltage pulse causing a deflection of the particle beam.
Batch: Group of several 'kicks' of the same amplitude.

In a given cycle there can be a maximum of two batches (batch A and batch B), the order of activation is transparent to the KSU, i.e. batch B can start before batch A.

In the example batch A has 4 pulses A1-A4 with amplitude VA and batch B has three pulses B1-B3 with amplitude VB, the parameters for batch A and batch B are independently controllable and have been selected to obtain a flexible control system from the operators environment.

Note : The following equation has to be met when setting up a batch :

int (Nk / Np) > = Vbatch / Vmax-mod

Np = number of pulses per batch
Nk = number of kicker modules (4 modules)
Vmax-mod = maximum kick amplitude per module (83kV)
Vbatch = requested kick amplitude (minimum = 30kV)

The PPM control parameters for batch A are:
- Kick on/off (batch A)
- Pulse amplitude (VA)
- MS 1 fine delay (delays start of first pulse on batch A)
- DS 1 fine delay (delays stop of first pulse on batch A)
- Pulse number (Pulses to be generated for batch A)
- Intershot delay (delay between two pulses in batch A, based on the RF pulse train)
- MS 2-n fine delay (delays start of second to last pulse on batch A)
- DS 2-n fine delay (delays stop of second to last pulse on batch A)

The non-PPM control parameters are:
- Deselect modules, this control input gives the user the option to deselect (a) module(s), i.e. the de-selected modules can not be used for any of the 24 USERs.
- Set-up, activating this variable resets all kickers and resets acquisition and interlock table.
- Module control (on/off, standby, reset for each individual module).
- Magnet termination control per module (SC/TRM).

The control parameters for batch B are identical to the ones for batch A.
The timing and (MS, DS and Intershot) delay parameters will be discussed in the next chapter.

The module assignment to the different users is calculated inside the DSC along a given algorithm, all information needed by a kicker module is sent shortly after reception of the PLS telegram to the LPU. (ANNEX1) .

8.3 Timing

RF- and fine delays

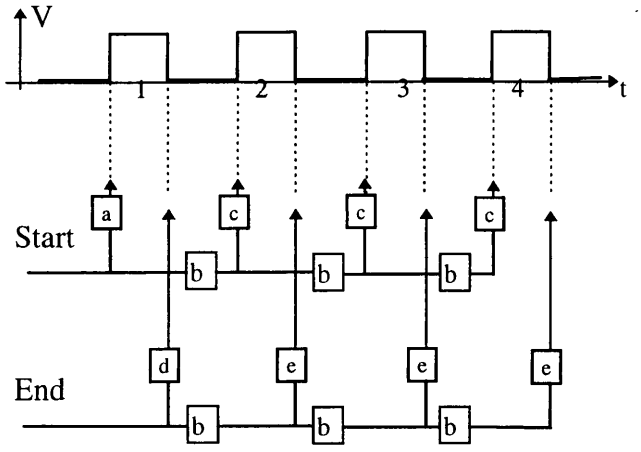


Figure5

Every batch is composed out of three major timing signals which are named :

- SCR (warning), for charging the PFN.
- MS (start), controlling the rising edge of the kick pulse.
- DS (end), controlling the falling edge of the kick pulse.

MS and DS are externally generated, not inside the local TG8.

In the example of Figure5 there are four pulses in a batch, implying that there must be three more 'start' and 'end' pulses, this is correct but they are generated locally by means of the Intershot Delay Unit (IDU ref.8).
The IDU (VME-module) is programmed by the KSU after an SCR pulse has arrived.
The KSU programs the IDU with the desired RF-delay and pulse number.
With this information the IDU generates the required burst of start and end pulses.

The IDU also makes a separation between the first MS (MS 1) and the following burst (MS 2-n), the same is done for the DS pulses. (DS 1 and DS 2-n)
This makes it possible to delay the first pulse independently from the following burst of pulses.

The delays are set up with the DUAL-DELAY VME-module (0-2μsec, 1nsec resolution.) (ref.6), developed in the PS kicker section.

Summary of independently controllable delays per batch :

a. MS 1 fine delay (0-2μsec, 1nsec resolution)	PIX.S-KFA45-FD
b. RF-intershot delay (delay in RF-periods)	
c. MS 2-n fine delay (0-2μsec, 1nsec resolution)	PIX.S2-KFA45-FD
d. DS 1 fine delay (0-2μsec, 1nsec resolution)	PIX.E-KFA45-FD
e. DS 2-n fine delay (0-2μsec, 1nsec resolution)	PIX.E2-KFA45-FD

The second column describes the equipment names used in the PTIMD equipment module, for batch B the PIX should be replaced by PI2X.
In chapter 9 is described how to access the listing of these properties.

8.4 SCR-generation (WARNING SIGNALS)

The different SCR signals are generated inside the DSC-KSU, by a so called TG8 module.
The TG8 is a multi purpose VME timing module, which receives messages distributed over a timing network (PLS-telegram.)
These messages include timing information, clock plus calendar and telegrams instructing the accelerator on the characteristics of the next beam to be produced.
The TG8 supplies the KSU with the active user and particle type at the start of a cycle, furthermore it supplies the following timing signals :

- ELFT (PX.ELFT-K45) end of last flat top
- SCR A (PIX.WKFA45) warning batch a
- SCR B (PI2X.WKFA45) warning batch b
- SCR TA (PX.WKFA45) warning batch a test (@ ELFT + C50)
- SCR TB (P2X.WKFA45) warning batch b test (@ ELFT + C80)

These signals will provoke an interrupt signal for the real time task.

Furthermore a check will be performed on the timing sequence, (SCR, MS and DS)for each batch and a timing fault status will be returned. (ANNEX 1)
This is realised with the **VMOD_TIM_ANA** card, a VMOD-IO piggy back VME card.(ref. 7)

8.5 Modules Ready & External Conditions.

In order for the KSU to select kicker modules which are in the ready state, i.e. kickers that are ready to pulse, there has to be a feedback from all the kicker modules indicating this status.
For reliability reasons this feedback is hard wired.

If there is an operation, with 'kick on' that the KSU can not perform, it will set the 'external condition' feed to the MTG (Main Timing Generator) to ERROR, with this information further injections can be blocked.

These 'ready' and 'external condition' signals are handled by the DSC by means of the so called **VMOD-TTL** I/O board, a VMOD-IO piggy back board. (ref.10 & 11)

8.6 Local Processor Unit (LPU)

Communication from DSC-KSU to the kicker modules is obtained via a local processor, which is positioned in every kicker module.
Connections from and to the processor are based on the RS232 serial I/O principle, with the communication speed set at 19200 baud.
The VME module performing this task in the DSC are two **IP-Octal 232** (ref. 13) piggy back boards installed on the **VIPC610** (ref.12) mother board. (Greenspring computers)
The VIPC610 conforms to the IndustryPack Logic Interface Specification.

The LPU receives its instructions from the DSC, passes it on to the kicker module, and returns a set of status & acquisition parameters after cycle end.

The control parameters are:
- On/off, standby and reset commands.
- Kick on/off.
- Pulse in SC or TRM mode.
- Pulse amplitude.

The acquisition parameters returned from the local processor to the DSC are:
- Interlock status.
- Status of KFA module (on/off, standby etc.).
- H.V. kick strength (pulse amplitude in kV).

A special feature of the link between KSU and LPU is that the LPU can be downloaded with its latest software changes from the KSU without affecting the present operation, taking into account that the module which is downloaded can not be used.

9. EQUIPMENT MODULE SPECIFICATIONS

The properties with their description for the KSU45 can be found by 'browsing' the web:

start **NETSCAPE**
connect to http://psas01/
PS Accelerator Control System
Select **control modules**
and enter **ksu, ptimd** or **ptim-v**.

KSU:
Equipment names:
1. PI.KFA45 for batch A
2. PI2.KFA45 for batch B

PTIMD :
Equipment names:
1. PIX.S-KFA45-FD (MS1 fine delay batch A)
2. PIX.E-KFA45-FD (DS1 fine delay batch A)
3. PIX.S2-KFA45-FD (MS2-n fine delay batch A)
4. PIX.E2-KFA45-FD (DS2-n fine delay batch A)
5. PI2X.S-KFA45-FD (MS1 fine delay batch B)
6. PI2X.E-KFA45-FD (DS1 fine delay batch B)
7. PI2X.S2-KFA45-FD (MS2-n fine delay batch B)
8. PI2X.E2-KFA45-FD (DS2-n fine delay batch B)

PTIM-V
Equipment names :
1. PX.ELFT-K45 (end of last flat top)
2. PX.WKFA45 (warning test batch A)
3. P2X.WKFA45 (warning test batch B)
4. PIX.WKFA45 (warning batch A)
5. PI2X.WKFA45 (warning batch B)

For **detailed** property information of the KFA45 system see **ANNEX 1**

This summarizes the hardware implementations for the KFA45 control and acquisition system.
On the following pages the software part i.e. the real-time program will be described.

10. REAL-TIME PROGRAM FOR THE PS KFA 45 HADRON INJECTION KICKER SYSTEM

10.1 Communication KSU-DSC and Local Processor Unit (LPU)

brief review:

The KSU-DSC handles all control and acquisition for the KFA45, it does this by communicating via a RS232 link with a local processor unit (LPU) installed on every kicker module.

The LPU obeys to all commands coming from the KSU.
The LPU collects all status, acquisition and interlock information received from a kicker module, and returns this to the KSU on demand.

A special feature of the LPU is that it can be downloaded with 'its' program from the KSU, this simplifies the process of performing eventual updates for the LPU program.
The downloading doesn't influence the actual operation, considering that enough modules are available to perform this operation.

10.2 r-t task KSU45

Description of the real-time multi-threaded program under LynxOS for the KFA 45 hadron injection system.
(A multi-threaded process can be thought of as a process with many paths or "threads" of execution which can all be executed at the same time.)

10.3 Initialisation phase

Sequence of actions taken after start of **main().**

- Attach to the PLS telegram received by the TG8
- Connect to the interrupts generated by the TG8
- Initialise hardware
- Create threads - **pls()** - **action()** - **download()**

10.4 Threads

The threads created at start-up are **main() - pls() - action() - download()**.

main() can also be seen as a thread**, main()** has the highest priority and checks for 'signals'.
The rt-task supports the signals SIGHUP, SIGINT, SIGQUIT, SIGTERM, when it receives one of these signals the program terminates after 'cleaning up'.

The threads **pls()** and **action()** are set at the same priority, but a lower priority than **main()** and perform the real-time task for the KFA45 .
The thread **download()** is set at the lowest priority and is woken up when there is a request for a reload of the LPU program.

pls() ; actions followed by the arrival of a CPS telegram, received by the TG8.

Action taken upon arrival :

- read user number and particle type.
- if control data has changed perform the following actions :

    1. Perform control action(s) if requested. (on, off, standby, reset)
    2. Check for download request KSU and register request.

- calculate kickers to be used on this cycle.
- check if the particle type is heavy ion, if so perform reflection compensation.
- sent kicker information table to all kickers
  Here the kickers will receive all information they require for a complete machine cycle.

  Each LPU receives the following information from the KSU (via its RS232 link) :

    1. Protocol - 2 bytes
    2. Pulse number module is active on, for batch A & B - 1 byte.
    3. Pulse number module is active on, for batch test A & test B - 1 byte.
    4. Kick on/off and magnet with short circuit or termination resistor (for all batches) - 1 byte.
    5. Reflection compensation on/off for all batches - 1 byte.
    6. Voltage reference for all batches - 8 bytes (2 bytes/batch).

- set kick on/off for all users in data table (if changes have occurred).
- set external condition signal (to MTG).
- sleep until next pls-telegram.

action() ; thread which waits for one of the following interrupt from the TG8 module :

1. ELFT end of last flat top
2. SCR A warning batch a
3. SCR B warning batch b
4. SCR TA warning batch a test
5. SCR TB warning batch b test

On arrival of an ELFT signal perform the following actions :

- Sent acquisition request to LPU (2-bytes), the LPU will sent the following acquisition results :

    1. Status of the module - 1 byte (on, off, standby ...).
    2. Interlock information - 1 byte.
    3. HV kick strength - 8 bytes (2 bytes/batch).

  Exception :
  If the LPU replies to a previously made download request from the KSU the first byte sent is 0xF0 acknowledging download request, the KSU registers 'down load request approved'.

- Calculate ΣHV kick strength
- Set acquisition, status and interlock information into data table
- Check if there is a download request registered, if so sent request to LPU
- Check if download request has been approved by LPU, if so wake up download thread
- Sleep till new interrupt signal ELFT arrives

On arrival of one of the SCR (warning) signals perform the following actions :

1. Program dual delay cards for MS (start) and DS (stop) fine delays.
2. Program Intershot delay unit with required RF delay and pulse number.

download() ; thread set at the lowest priority and is woken up by the thread **action()**

Check which LPU unit has requested for a download and sent the LPU program to this module via the RS232 link dedicated to this LPU unit.
This thread is running at the lowest priority to prevent interrupting the rt-task.

10.5 USER-TEST FOR SPECIALISTS

A special test operation has been included which can be seen as an additional USER (USER25).
With this user injections can be simulated, without interfering with the particle beam.
Its use is intended for kicker specialists only and it can perform the same operations as on any other USER.

The warning signals are generated by the TG8 module and are activated on every USER.
SCR TA, warning batch A is active @ ELFT + C50.
SCR TB, warning batch B is active @ ELFT + C80.

These signals are fed to the timing simulator unit which generates the start and stop pulses, further functions are identical to the ones under normal operation.
The timing simulator can be switched 'on' and 'off' by the KSU.

The start (MS) and end (DS) signals can be fine delayed like the normal operations mentioned in chapter 8.2 and 8.3 (**ANNEX 1).**
The equipment names used in the PTIMD equipment module are the following :

- MS 1 fine delay (TEST) PX.S-KFA45-FD
- MS 2-n fine delay (TEST) PX.E-KFA45-FD
- DS 1 fine delay (TEST) PX.S2-KFA45-FD
- DS 2-n fine delay (TEST) PX.E2-KFA45-FD

(for batch b replace PX by P2X)

11. CONCLUSION

The described system with one central control system (DSC-KSU) via which all external communications are routed and with every kicker individually controllable (via the LPU), allows a very flexible system.

The flexibility obtained with this set-up allows compatibility for the installation of other kicker control and acquisition systems, for example the already existing KFA71-79 system (ref. 9).
Furthermore the downloading facility for the LPU allows flexibility in the updating of the LPU software.

For more details refer to the source code of the ksu45 real-time program on the PS network in the directory **/ps/local/home/schipper/ksu45** and
/ps/local/home/schipper/ksu45/include

The source files forming the real-time task are :

- ksu45main.c
- ini45.c
- ksu45_calc.c
- pls45.c
- download.c

+ header files

- ksu45.h
- download.h
- st_int.h
- decl45.h

This concludes the general description of the hard- and software control and acquisition system for the KFA 45 hadron injection kickers.

In **ANNEX1** a detailed listing of the properties for the KFA45 system can be found.

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11. VMOD-TTL Version 1.0 Data sheet (November 1990)
    VME MODULbus 20 channel TTL-I/O
    JANZ Computer AG, Germany

12. VIPC610 User Manual
    Quad IndustryPack Carrier for 6U VMEbus Systems
    GREENSPRING Computers

13. IP-Octal 232 User Manual
    IndustryPack 8 channel RS232 piggy back
    GREENSPRING Computers

14. LynxOS Device Driver for IP-Octal Serial
    Software Installation Manual
    SYSGO Mainz, Germany

ANNEX 1

DETAILED PROPERTY INFORMATION FOR THE KFA45 KICKER SYSTEM (KSU)

The 'KSU' equipment module has two members and are defined as follows :

Member no	Equipment name	DSC	Description
6003	PI.KFA45	dcpsk45	KFA45 batch A
6004	PI2.KFA45	dcpsk45	KFA45 batch B

NOTE
All properties mentioned in this note are of the variable type EQM_TYP_INT, unless specified otherwise.

CONTROL PARAMETERS (ppm)	**Property name**
1. Actuation batch (Kick on)	**CCSACT**
2. Kick strength (Pulse amplitude in kV)	**CCV** (EQM_TYP_REAL)
3. Number of pulses	**NUMBER**
4. Intershot delay in RF periods	**DELAY**

ad.1 Kick on
bit 0 = '1' => ON

CONTROL PARAMETERS FOR SHORT CIRCUIT OR TERMINATED MAGNET

CONTROL PARAMETERS (non-ppm)	**Property name**
1. PPM controllable termination	**SWITCH**
2. Fixed status SHRT/TRM	**LOCL**

ad.1 PPM controllable termination '1'=TRUE ('0'=FALSE)
ad.2 '1'= SHORT CIRCUIT ('0'=TERMINATED)
(bit 0 module 1, bit 1 module 2 etc.)

If a kicker module has a magnet that is PPM controllable (SC/TRM) i.e. the corresponding bit in SWITCH is TRUE, then the KSU decides the magnet termination.

If in SWITCH a module is set to FALSE, then the setting of the modules magnet termination is given by LOCL.

Note that a kicker magnet can only be PPM controllable (SC/TRM), if the hardware switches are present.

CONTROL PARAMETERS FOR KICKER LIMIT SETTING (non-ppm)

CONTROL PARAMETERS (non-ppm)	**Property name**
1. minimum kick amplitude in kV (KFA45)	**MINV**
2. maximum kick amplitude in kV (KFA45)	**MAXV**
3. minimum kick voltage in kV per module	**MINV1**
4. maximum kick voltage in kV per module	**MAXV1**

MINV1 and MAXV1 are arrays containing limits for all kicker module
MINV1[0] = minimum limit for module 1 ...etc.
MAXV1[0] = maximum limit for module 1 ...etc.

GLOBAL CONTROLS (non-ppm) — **Property name**

- De-select module(s) — **SELECT**
  (Select = '0', De-select = '1')
  (bit 0 module 1, bit 1 module 2 etc.)

- Reset (SET-UP) - (bit 0 = '1' => reset) — **RSET**
  Reset modules and reset acquisition and interlock table
  (RT-task will reset bit 0 to '0')

- Module control operations (x = module number) — **ONOFx**

  definition :
  bit 0 = 1 => MODULE OFF
  bit 1 = 1 => MODULE ON
  bit 2 = 1 => STANDBY
  bit 3 = 1 => RESET
  bit 4 = 1 => DOWNLOAD REQUEST

  (only one bit should be active, reset of ONOFx to '0' will be done by RT-task)

STATUS and ACQUISITION

Property name - STAQ(ppm)

STAQ is a three dimensional array containing the following information :

- STAQ[0] - Global Status

  Global status has the following structure :
  (active high)
  bit 0 = KICK ON
  bit 1 = not used
  bit 2 = TIMING ERROR
  bit 3 = EQUIPMENT ERROR
  bit 4 = OPERATIONAL ERROR
  bit 5 = not used
  bit 6 = U- ACT (user has had 'kick on' in super cycle after start rt-task)

- STAQ[1] - Timing Error

  1 byte of timing error information defined as following :
  (active high)
  bit 0 = not used
  bit 1 = EARLY
  bit 2 = LATE
  bit 3 = MISSING
  bit 4 = STOP (DS)
  bit 5 = START (MS)
  bit 6 = SCR

  bit 6, 2, 1 SCR MULTI-PULSING
  bit 5, 4, 2, 1 PULSE TOO LONG

- STAQ[2] - Selected modules on last operation

(bit 0 - bit 3 modules selected, bit 0 module 1 selected, bit 1 module 2 selected etc. active high)

Property name - STAQ1 (ppm)

Kick on/off status
'1' = ON
'0' = OFF

Property name - TERM (ppm)

Kicker magnet termination status
'1' = short circuit
'0' = terminated
(bit 0 module 1, bit 1 module 2 etc.)

Property name - AQN (ppm)

AQN is a four dimensional array containing the following acquisition information :

- AQN[0] - Kick strength - sum of kick strength of selected modules in 0.1 kV
- AQN[1] - Pulse width - pulse width of first pulse in batch, kick sum return
- AQN[2] - Pulse width - pulse width of first pulse in batch, theoretical
- AQN[3] - Pulse width - pulse width of second pulse in batch, kick sum return

At the moment of writing this report the pulse width measurements were not available yet

Property name - AQN1 (EQM_TYP_REAL) (ppm)

Acquisition kick amplitude (in kV.)

Property name - AQN2 (ppm)

AQN2 is a ten dimensional array containing STAQ(3), CCV(1), NUMBER(1), DELAY(1), AQN(4)

ACQUISITION PER MODULE (non-ppm)

Property name - SELECTx (x indicating the module number)

SELECTx is a five dimensional array containing the following information :

- SELECTx[0] - Status of module x

  definition :

  (set **low** = true)

  bit 0 - STANDBY
  bit 1 - MODULE ON
  bit 2 - MODULE OFF
  bit 3 - HV INTERLOCK
  bit 4 - LV INTERLOCK
  bit 5 - REMOTE CTL
  bit 6 - TRANSITION
  bit 7 - MAINS ON (presence of 3-phase)
  bit 8 - MODULE SELECTED
  bit 9 - DATA TRANSMISSION OK (KSU - LPU)
  bit 10 - MODULE READY

- SELECTx[1] - Interlock of module x

  definition :

hex	**interlock description**
0x01	HT SWITCH
0x02	POWER CONTROL UNIT
0x03	CAPACITOR BANK UNDER VOLTAGE
0x04	CAPACITOR BANK OVER VOLTAGE
0x05	IP PROTECTION
0x06	UNDER VOLTAGE
0x07	OVER VOLTAGE
0x08	PULSE LENGTH COMPARATOR
0x09	MAIN SWICH FAULTY SHOT
0x0a	NO MAIN SWICH I+
0x0b	DUMP SWICH_FAULTY SHOT
0x0c	NO DUMP SWITCH I+
0x0d	MAIN SWICH DRIFT STABILISER
0x0e	DUMP SWITCH DRIFT STABILISER
0x0f	CHARGE CONTROL UNIT
0x10	TRIGGER AMPLIFIER
0x11	HIGH TENSION KEY
0x12	220V STABILISER
0x13	SF6
0x14	VACUUM
0x15	OIL RESERVOIR
0x16	MAIN SWITCH OIL FLOW
0x17	DUMP SWITCH OIL FLOW
0x18	SHORT CIRCUIT OIL FLOW
0x20	SAFETY KEY

  if bit7 is high a termination error has occurred bit0 to bit3 indicate on which batch :

bit0	-	batch A
bit1	-	batch B
bit2	-	batch test A
bit3	-	batch test B

- SELECTx[2] - Latest down load time to LPU x in seconds from 1 Jan 1970. (Specialist)
- SELECTx[3] - Down load error to LPU x (bit0 - '1' => DOWNLOAD ERROR)
- SELECTx[4] - not used

SELECT1 to SELECT4 are packed into one array with the property name **STATN**

STATUS INDICATOR OF MODULES CAUSING INTERLOCK (non-ppm)
Property name - INTLK

definition :

active high = > interlock
(bit 0 module 1, bit 1 module 2 etc.)

DETAILED MODULE INFORMATION (ppm)
Property name - SREF

Data blocks per module containing:

0- Vreference (in Volts)
1- Pulse (module active on this pulse)
2- Kick on/off and short circuit or terminated
3- Vacquisition (in Volts)
4- Specialist information

ad.2 bit 0 => kick on ('1' = ON)
bit 4 => SC/TRM ('1' = SC)

SREF[0] to SREF[4] data block for module 1
SREF[5] to SREF[9] data block for module 2
SREF[10] to SREF[14] data block for module 3
SREF[15] to SREF[19] data block for module 4

DETAILED MODULE INFORMATION - OPERATION TEST (non-ppm)
Property name - TREF

Data blocks per module containing:

0- Vreference (in Volts)
1- Pulse (module active on this pulse)
2- Kick on/off and short circuit or terminated
3- Vacquisition (in Volts)
4- Specialist information

ad.2 bit 0 => kick on ('1' = ON)
bit 4 => SC/TRM ('1' = SC)

TREF[0] to TREF[4] data block for module 1
TREF[5] to TREF[9] data block for module 2
TREF[10] to TREF[14] data block for module 3
TREF[15] to TREF[19] data block for module 4

TEST OPERATION PARAMETERS
Property name - TEST1

TEST1 is a six dimensional array containing the following control values :

- TEST1[0] - Kick on/off (bit 0 = '1' => ON) (bit 1 = '1' => heavy ion simulation ON)
- TEST1[1] - Pulse amplitude in **0.1kV** steps
- TEST1[2] - Intershot delay in RF-periods
- TEST1[3] - Pulse number
- TEST1[4] - Modules selected (bit 0 = mod 1, bit 3 = mod 4)
- TEST1[5] - Modules with short circuited magnet (bit 0 = mod 1, bit 1 = mod 2 etc..)
  ('1' => SC '0' => TRM)

ACQUISITION AND STATUS FOR OPERATION TEST

The acquisition and status parameters for the operation test have the same format as the ones for normal operations
Property name - TESTAQ (equivalent to AQN)
Property name - TESTAT (equivalent to STAQ)

VME DUAL DELAY - fine delays (ppm)

The fine delay parameters are seen as a part of the timing system and are therefore organised in a different equipment module named PTIMD.
The 'PTIMD' equipment module has 16 members and are defined as follows :

Member no	Equipment name	DSC	Description
6624	PIX.S-KFA45-FD	dcpsk45	MS1 fine delay batch A
6625	PIX.E-KFA45-FD	dcpsk45	DS1 fine delay batch A
6626	PIX.S2-KFA45-FD	dcpsk45	MS2-n fine delay batch A
6627	PIX.E2-KFA45-FD	dcpsk45	DS2-n fine delay batch A
6628	PI2X.S-KFA45-FD	dcpsk45	MS1 fine delay batch B
6629	PI2X.E-KFA45-FD	dcpsk45	DS1 fine delay batch B
6630	PI2X.S2-KFA45-FD	dcpsk45	MS2-n fine delay batch B
6631	PI2X.E2-KFA45-FD	dcpsk45	DS2-n fine delay batch B
6632	PX.S-KFA45-FD	dcpsk45	MS1 fine delay test batch A
6633	PX.E-KFA45-FD	dcpsk45	DS1 fine delay test batch A
6634	PX.S2-KFA45-FD	dcpsk45	MS2-n fine delay test batch A
6635	PX.E2-KFA45-FD	dcpsk45	DS2-n fine delay test batch A
6636	P2X.S-KFA45-FD	dcpsk45	MS1 fine delay test batch B
6637	P2X.E-KFA45-FD	dcpsk45	DS1 fine delay test batch B
6638	P2X.S2-KFA45-FD	dcpsk45	MS2-n fine delay test batch B
6639	P2X.E2-KFA45-FD	dcpsk45	DS2-n fine delay test batch B

Property name - CCV (ccv's of the above mentioned fine delays in nsec)
Property name - AQN (acquisitions of the above mentioned fine delays in nsec)

The acquisition of the fine delays can also be found in the KSU equipment module
Property name - DTAB (for 'users')
Property name - TEST3 (for operation test)

Distribution

Groupe OP
Section Kicker Magnets
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