

## Latest developments and characterisation results of the MALTA sensors in TowerJazz 180nm for the High Luminosity LHC

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The MALTA sensors are Depleted Monolithic Active Pixel Sensors (DMAPS) made using 180nm TowerJazz CMOS technology. These have been iteratively designed towards achieving a high radiation tolerance for applications such as in the outer layers of the HL-LHC's ATLAS Inner Tracker. To date several design enhancements have been implemented to attain a high time resolution (<2ns), granularity as well as achieving excellent charge collection efficiency uniformly across the pixel geometries. This technology promises to drastically cut the production cost of silicon sensors due to their monolithic design, bypassing the costly stage of bump bonding in hybrid sensors. This talk will provide a detailed overview of the comprehensive characterisation studies conducted on the MALTA and Mini-MALTA sensors as well as present newer functionalities being introduced in the latest iteration, the MALTA2.

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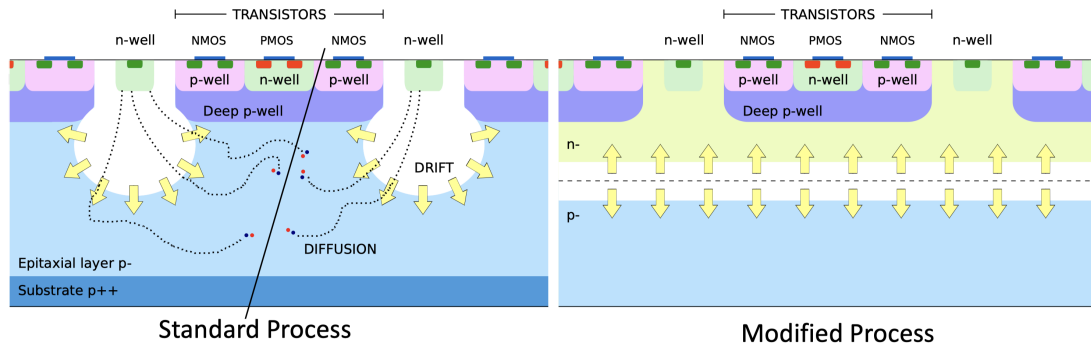
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## 1. Introduction

Once operational in 2026, the upgraded high-luminosity LHC is expected to deliver an integrated luminosity of  $3000 \text{ fb}^{-1}$  and an instantaneous luminosity ranging between  $7.5$  to  $30 \times 10^{34} \text{ cm}^2\text{s}^{-1}$ . The all new silicon tracking detector will also be expected to experience between 200 to 1000 interactions per bunch crossing. These upgrades present many challenges for electronics and radiation hardness and in turn require the use of high granularity and time resolution to contribute to the physics searches. Sensor designs thus aim for a small pitch size of approximately  $30 \mu\text{m}^2$  and sub-nanosecond time resolution. Monolithic pixel detectors could address these challenges for the HL-LHC and beyond.

## 2. Sensor Design

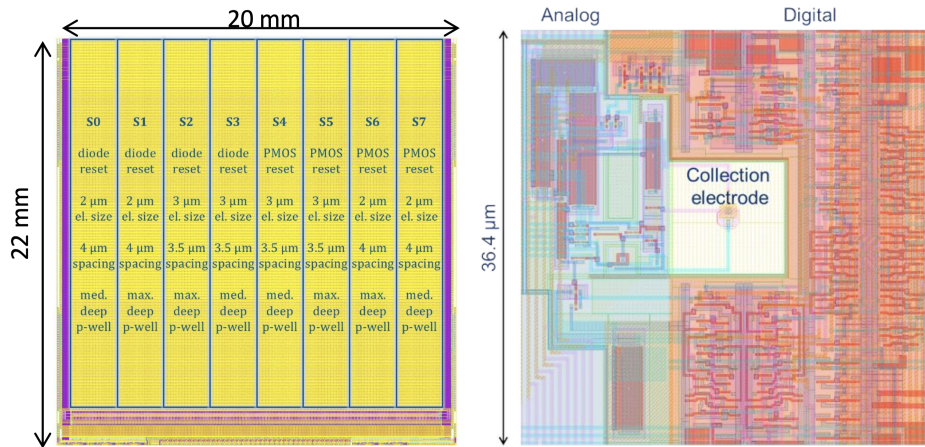
The MALTA sensor is designed in the commercial TowerJazz 180 nm CMOS technology [1], an imaging process with quadruple well with high resistivity ( $>1 \text{ k}\Omega\text{cm}$ ) epitaxial layers. This is supplemented with small collection electrodes of  $3 \mu\text{m}^2$  and in turn a small input capacitance of under  $5 \text{ fF}$ . The shallow epi-taxial layer allows for a small depletion depth of approximately  $20 \mu\text{m}$  with high signal to noise ratio. In addition, a modified process is incorporated to ensure full lateral depletion. These features were successfully implemented for the ALICE ITS and subsequently further optimised over the course of the MALTA development.



**Figure 1:** Left: cross sectional diagram of the standard process as implemented for the ALICE ITS. Right: the modified process used in the MALTA chips.

## 3. Readout Architecture

MALTA chip design represents a new R&D development for radiation hard large area monolithic pixel chips. This full size demonstrator chip spans an area of  $22 \times 20 \text{ mm}^2$  populated with  $512 \times 512$  pixels subdivided into 8 distinct sectors that house different pixel flavours. These flavour variations include changes in the collection electrode size, p-well depth, and spacings around the collection electrode. The matrix architecture is fully clock-less leading to significant reductions in power consumption, namely  $10 \text{ mW/cm}^2$  for digital power and  $70 \text{ mW/cm}^2$  for the analog power. Finally, the particle charge information is inferred from the time-walk of the signal. The pixel



**Figure 2:** Left: overview schematic of the MALTA1 chip with sector sub-divisions. Right: pixel-level diagram showing the distinct analog and digital circuitry.

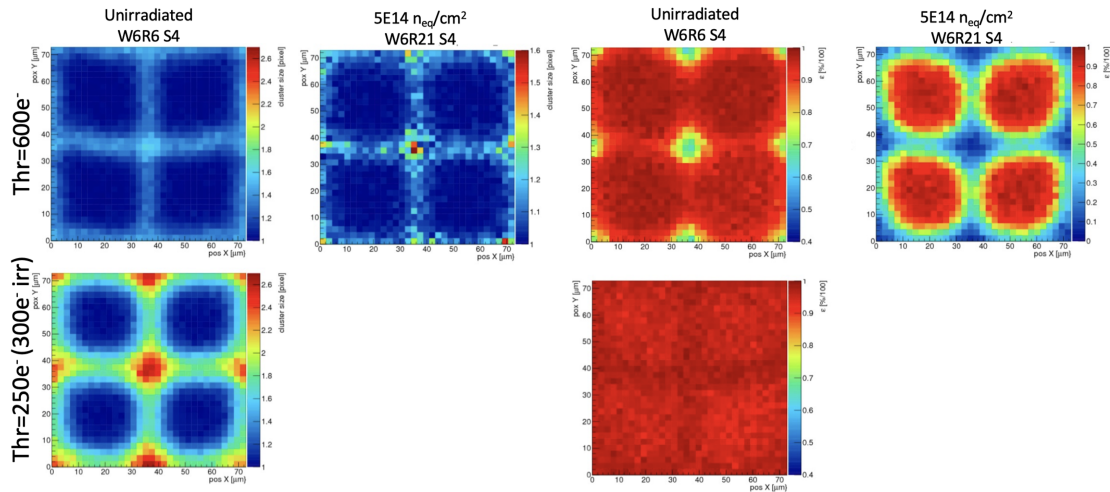
size itself is  $36.4 \times 36.4 \mu\text{m}^2$  with a collection electrode of just 2 to 3  $\mu\text{m}$  leading to a small input capacitance. A spacing of 3.4 to 4  $\mu\text{m}$  to the electronics is ensured to achieve low cross talk.

A novel asynchronous readout architecture is implemented [2] for high hit rate capability with 37 bit parallel data bus for data streaming. Double pixel columns are subdivided into groups, defined as  $2 \times 8$  pixels with pattern assignment to reduce data size from clusters. The front-end discriminator output is processed by a double-column digital logic. The pulse width is adjustable between 0.5 ns and 2 ns with the data being transmitted asynchronously over a high-speed bus to the end of column. Timing information itself is stored in dedicated bits and the output signals are transmitted by 5 Gbps LVDS drivers.

#### 4. Performance Results

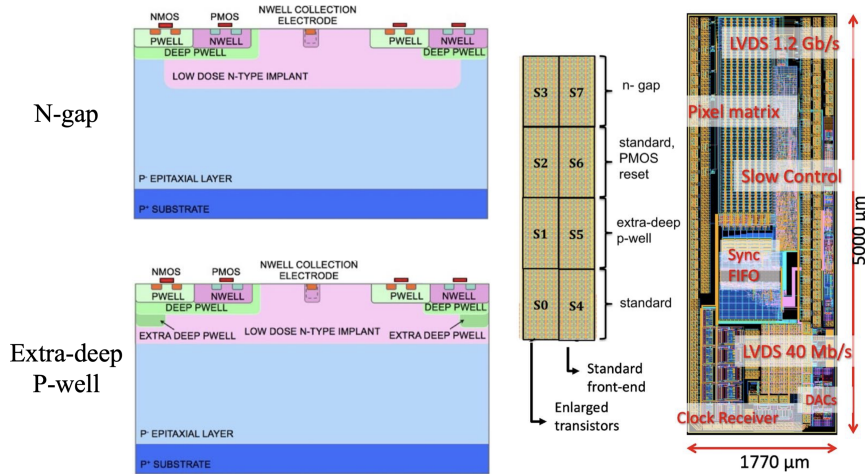
Several test-beam campaigns were undertaken to evaluate the performance of the various chip designs. Fig. 3 shows the results for MALTA1 chips measured at CERN's SPS facility, with the first two columns showing the cluster size for an unirradiated and irradiated samples. On the last two columns the efficiency results are shown for these same two samples. The top and bottom rows correspond to a threshold setting of 600 and 300 electrons respectively. The cluster size is seen to increase as we decrease this threshold and this is an expected behaviour given the larger charge sharing collected at lower thresholds. Similarly in the efficiency decreases at the pixel corners, this is particularly evident in the case of the irradiated sensor with considerably lower efficiency in the corners. In the case of the irradiated sample a lower threshold could not be reached and in order to counter the efficiency losses observed in MALTA1 at pixel corners changes were made in the subsequent chip design iterations.

This was one of the primary aims of the next iteration, the Mini-MALTA chip. In its case the matrix comprises of  $64 \times 16$  pixels, 8 sectors with different analog front-end designs and a single serial data stream capable of 40 Mbps or 1.2 Gbps with 8b10b encoding. It features improved implementation of the slow control, pixel designs comprising of a gap in the n-layer as well as an extra deep p-well process modification. The periphery data synchronization uses a custom RAM



**Figure 3:** Cluster size and Efficiency results for the MALTA1 chip measured during a SPS test-beam campaign.

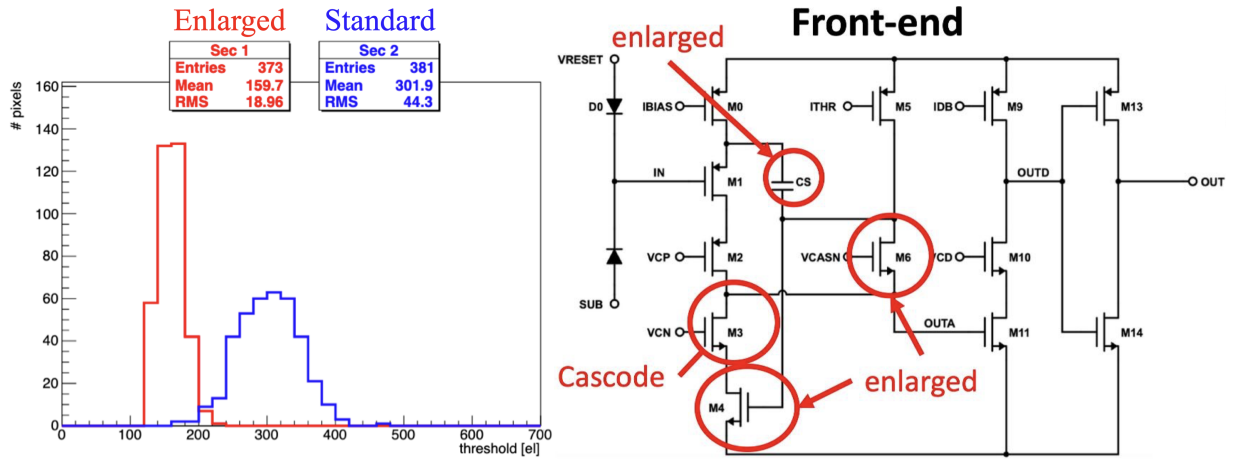
memory and the chip also houses larger capacitors to reduce noise, as shown in Fig. 5 with the reduced width of the threshold dispersion.



**Figure 4:** Left: cross sectional diagrams of the n-gap and extra-deep p-well designs respectively. Right: layout of the Mini-Malta sectors and circuitry.

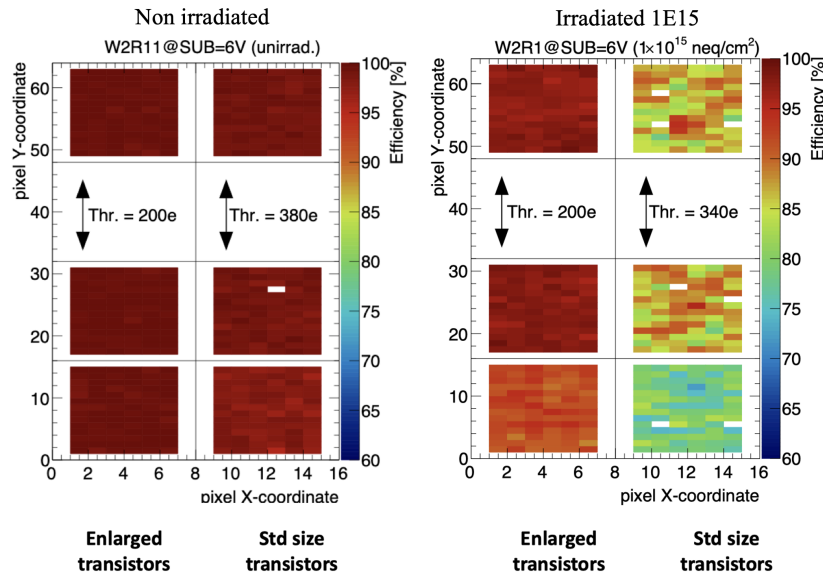
A further update to this design, known as the Mini-MALTA Split 7 introduced a cascoded front-end and enlarged transistors for all sectors as shown in Fig. 5.

The Mini-MALTA’s performance in test-beam was also assessed with the efficiencies for each sector, shown in Fig. 6. Full efficiency was observed after irradiation at 200e<sup>-</sup> threshold at 6 V bias on sectors with enlarged transistors. This is due to the improved charge collection in the pixel corners with respect to the previous MALTA1 design. This increased efficiency was also observed with a focused x-ray beam [3] at the Diamond Light Source. The higher efficiency for enlarged transistors, was consistently above 97%. These measurements were conducted on an unirradiated



**Figure 5:** Left: threshold dispersion of the Mini-MALTA chip sectors 1 (blue) and 2 (red) with enlarged and standard-sized transistors respectively. Right: circuit diagram of the Mini-MALTA split 7 front-end.

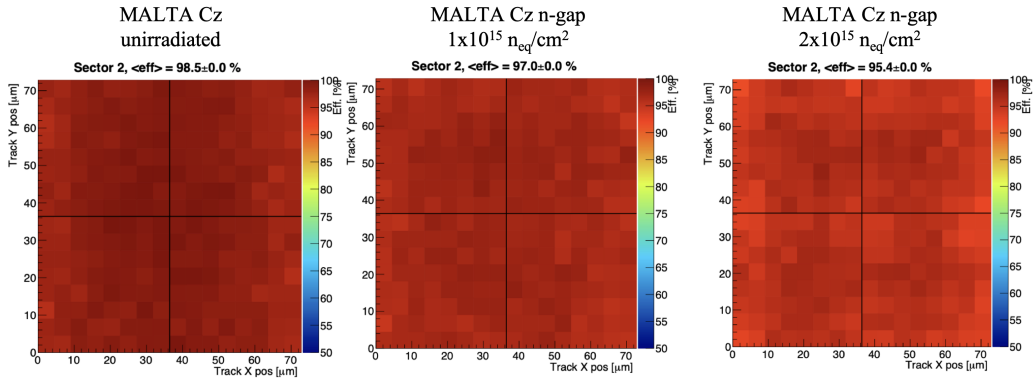
sample as well as one irradiated to  $1 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ , and measured with a 2 GeV electron beam at ELSA, with 6 V of bias voltage.



**Figure 6:** Efficiency results for each sector of an unirradiated (left) and  $1 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$  irradiated (right) Mini-MALTA chip.

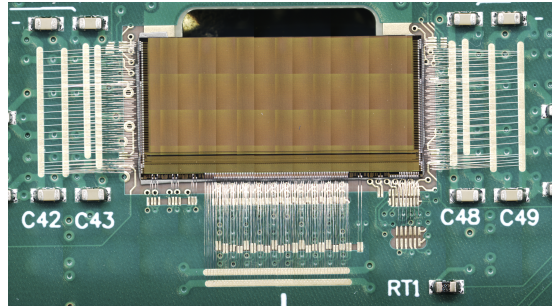
A full-sized MALTA was produced with a high resistivity Czochralski substrate material. This allowed for a larger depletion voltage and in turn a higher signal, as well as a greater level of radiation hardness through the ability to apply a high operational voltage of up to 50 V. The efficiency as shown in Fig. 7 was measured to be from 98.5% for an unirradiated sample to 95.4% after an irradiation of  $2 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ . These samples were measured at DESY using a 4 GeV electron beam [4].

The latest iteration in the MALTA sensor family currently being tested is the MALTA2. It was returned from the foundry in January 2021 and is half the size of the MALTA1, namely,



**Figure 7:** Left: threshold dispersion of the Mini-MALTA chip sectors 1 (blue) and 2 (red) with enlarged and standard-sized transistors respectively. Right: circuit diagram of the Mini-MALTA split 7 front-end.

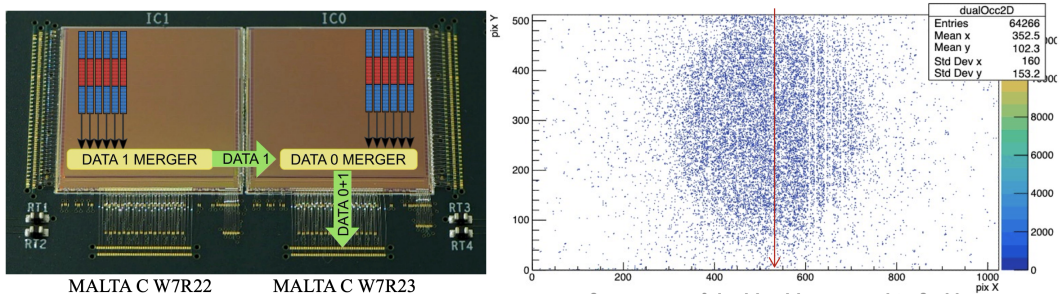
$20.2 \times 10.1 \text{ mm}^2$ , shown on Fig. 8. Its pixel matrix comprises of  $224 \times 512$  pixels of the same pitch size as the previous MALTA chips. It includes a faster analog front-end which improves time resolution, a new slow control implemented as a 4322 bit shift register and inherits the enlarged transistors as implemented in Mini-MALTA. It also houses a cascaded front-end for higher gain and reduced RTS noise with under 10 electrons of noise observed on unirradiated samples. MALTA2 applies the combined knowledge acquired from MALTA1, Mini-MALTA, Mini-MALTA split 7 and the MALTA Czochralski chip versions.



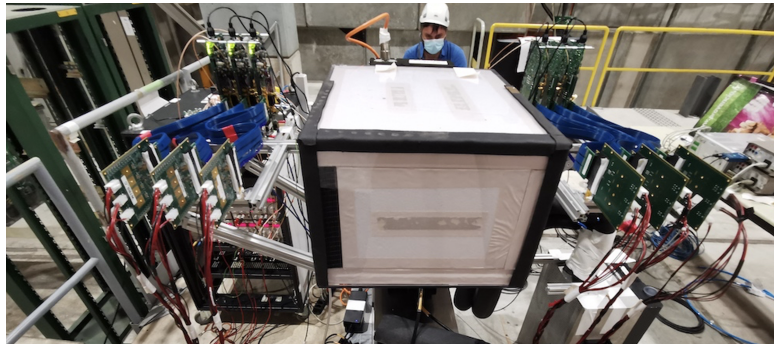
**Figure 8:** The MALTA2 chip wire-bonded on its dedicated carrier PCB.

An additional functionality of the MALTA chips is the ability to transfer data from chip-to-chip. Data from MALTA can be routed to another MALTA to the left or to the right through CMOS outputs with the aim being to target larger sensing surfaces and reduce services. Fig. 9 shows both a diagram of the data transfer route from chip-to-chip as well as a Sr-90 source exposure test conducted across two interconnected chips.

Finally, in order to facilitate test-beam measurements, a telescope comprised of MALTA chips was developed, as shown on Fig. 10. Using MALTA1 chips to trigger the telescope and a Xilinx Kintex-7 KC705 FPGA for readout, the trigger from MALTA planes was defined as combination reference signals and designed to be compatible with AIDA telescopes. Its key features include 4 to 6 MALTA1 reference planes that are  $100 \mu\text{m}$  thick, achieving  $9 \mu\text{m}$  track-hit resolution using only 3 tracking planes and the General Broken Line (GBL) algorithm in the Proteus track reconstruction software with a 4 GeV electron beam in DESY.



**Figure 9:** Left: Diagram showing chip-to-chip data transfer route. Right: Occupancy map of to interconnected MALTA chips exposed to a Sr-90 source.



**Figure 10:** The MALTA telescope deployed at CERN's SPS facility.

## 5. Conclusions & Outlook

Through these developments, a large area monolithic chip with chip-to-chip data transfer was shown to operate within specifications. It was also routinely thinned down to  $100\ \mu\text{m}$ . A portable self-contained telescope system was also developed and used in multiple test-beam campaigns including at CERN's SPS facility as well as at DESY. The MALTA monolithic CMOS sensors continuously improved with excellent performance of Mini-MALTA and Czochralski iterations. Modifications such as the n-gap and extra deep p-well have shown full efficiency after 100 Mrad and  $1 \times 10^{15}\ \text{n}_{\text{eq}}/\text{cm}^2$ . Many improvements have been applied to the design of MALTA2 and are currently under test at SPS with early measurements showing very promising results. The MALTA3 design is already under way and will be incorporating the latest process modifications, the front-end design with improved time resolution as well as asynchronous read-out in a large form-factor device.

## References

- [1] W. Snoeys et al, *NIM A*, **871** (2017), 90-96
- [2] I. Berdalovic et al, *JINST* **13** (2018), C01023-C01023
- [3] H. Pernegger et al, *NIM A*, **986** (2021), 164381
- [4] M. Dyndal et al, *JINST*, **15** (2020), P02005