ATLAS High Granularity Timing Detector

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on behalf of the ATLAS collaboration

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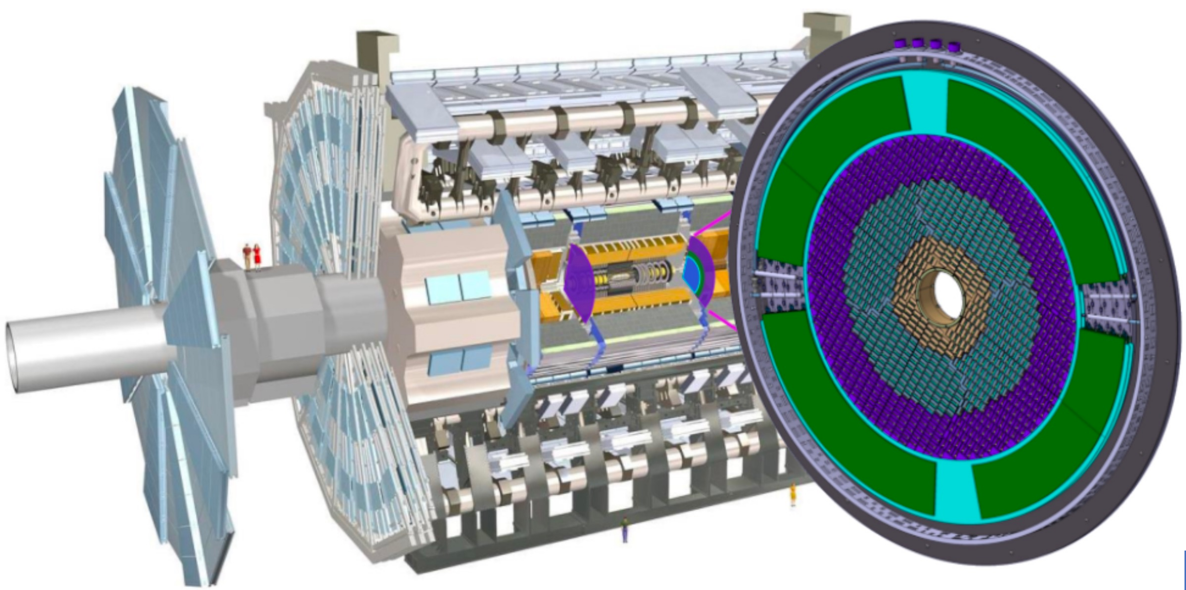
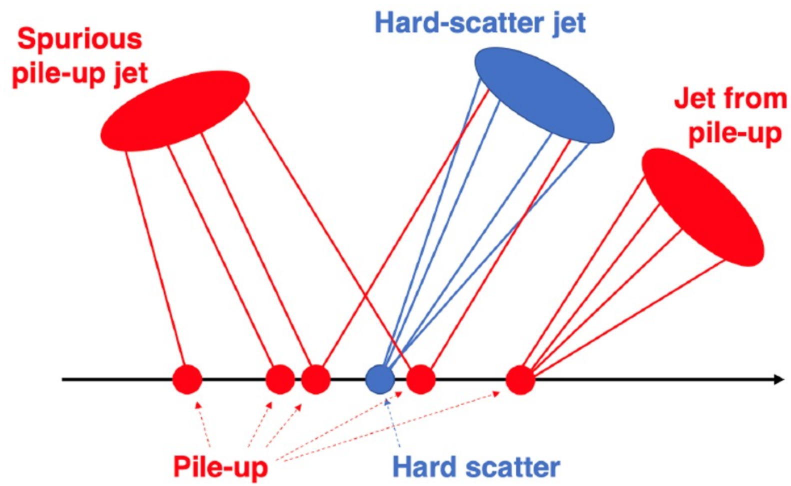
High Granularity Timing Detector (HGTD)

- **HGTD aim to reduce pileup contribution at HL-LHC**
  - **Timing resolution is required to be better than 50ps**
  - **Approved by CERN LHCC in September 2020**
- **6.4m^2 area silicon detector and ~ 3.6x10^6 channels**
- **High Granularity: Pixel pad size: 1.3mm × 1.3mm**
- **Radiation hardness : 2.5x10^{15} N$_{eq}$ /cm^2 and 2MGy**



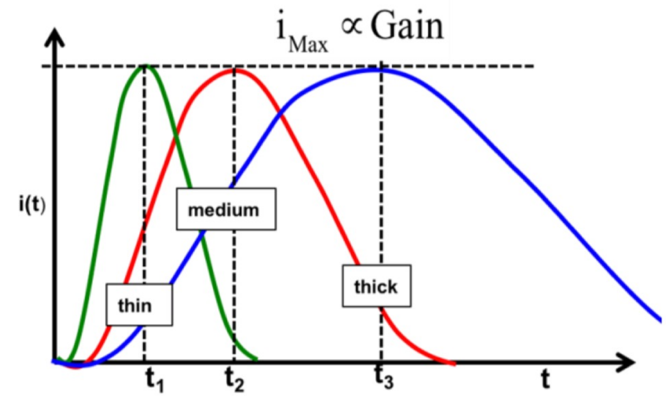


Low Gain Avalanche Detectors (LGAD)

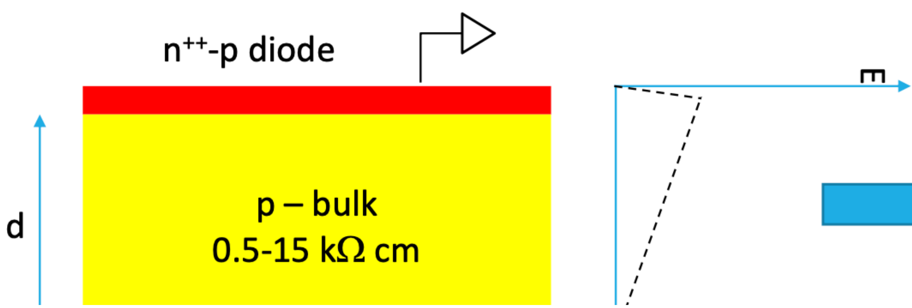
- Compared to APD and SiPM, LGAD has modest gain (10-50)
- High drift velocity, thin active layer (fast timing)
- High S/B, no self-triggering

$$\sigma^2_{jitter} = \left(\frac{t_{rise}}{S/N}\right)^2$$

- **Modest gain to increase S/N**
- **Need thin detector to decrease t_{rise}**

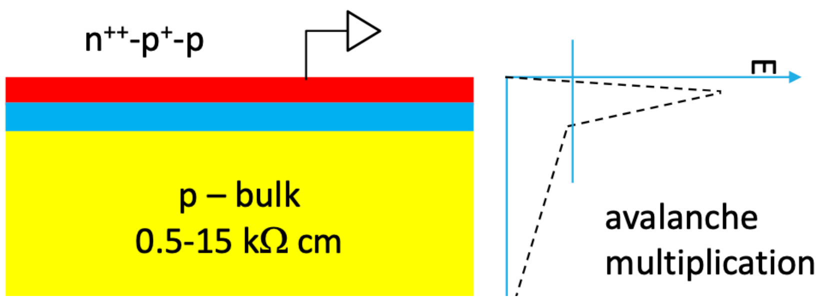


Conventional PiN diode



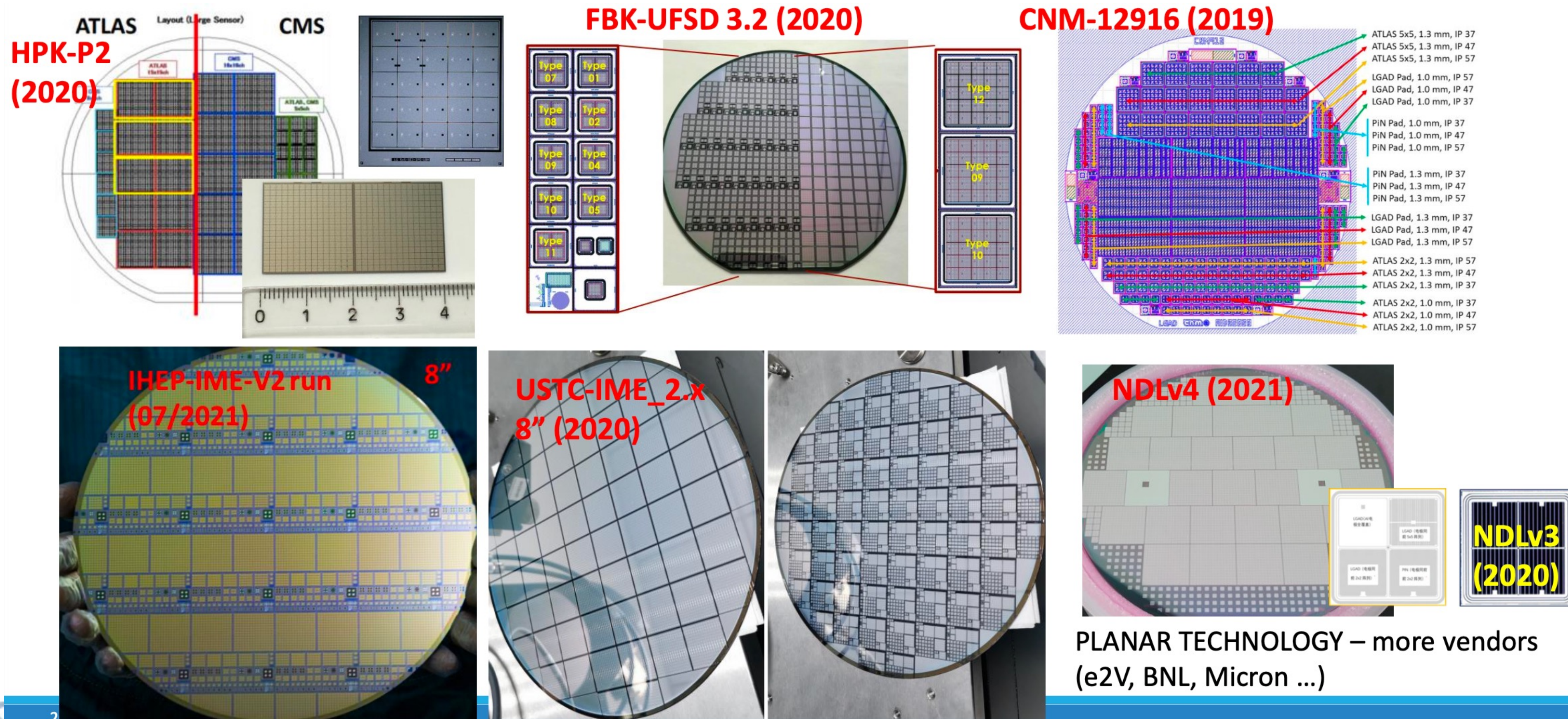
LGAD

P+ gain layer on top of PIN diode



Latest prototypes produced by different vendors

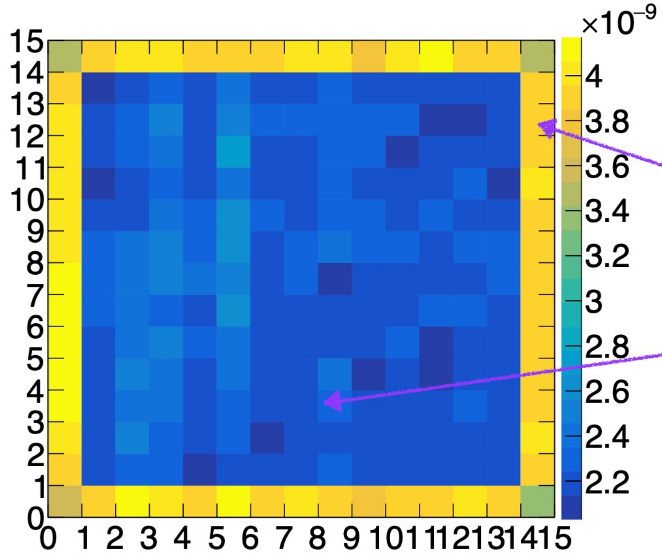
- Lots of prototypes R & D in LGAD in last few years, active vendors includes:
  - IHEP-IME (China), USTC-IME (China), IHEP-NDL(China), FBK (Italy), CNM (Spain), HPK (Japan) …

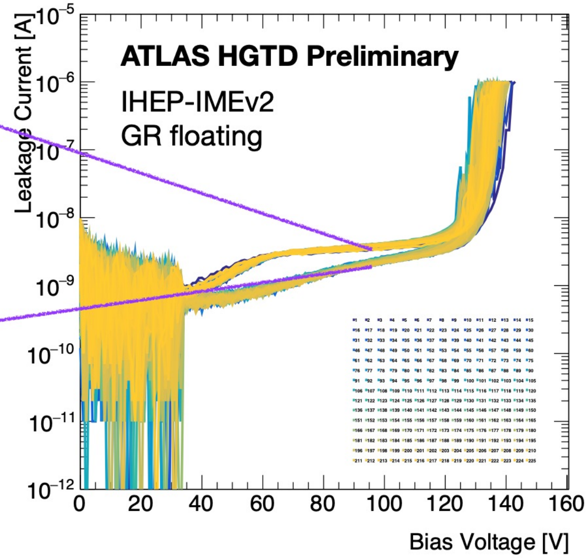


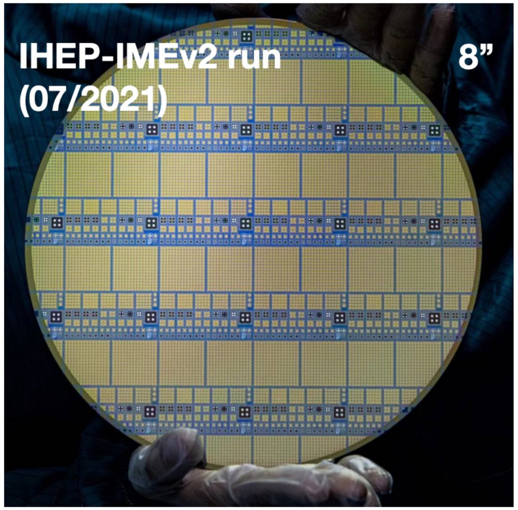
PLANAR TECHNOLOGY – more vendors (e2V, BNL, Micron …)

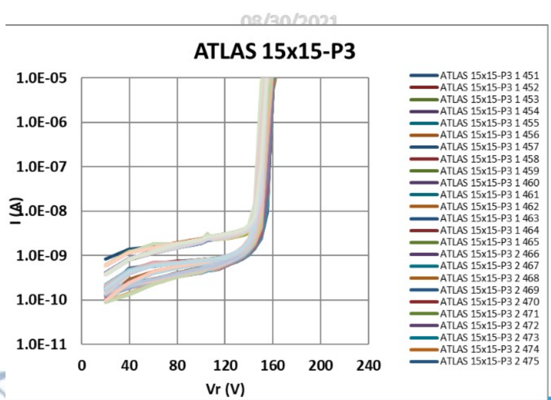
Full size LGAD sensor prototype

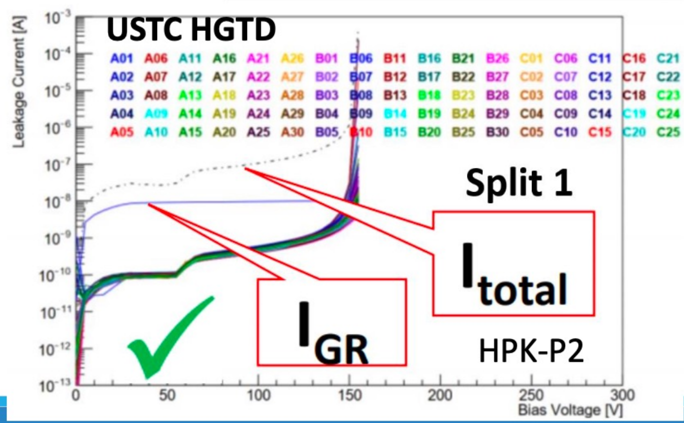
- Good uniformity of full size LGAD prototype (15*15 channels)
  - IHEP-IME, USTC-IME,HPK, FPK, CNM has produced good full-size LGAD prototype.

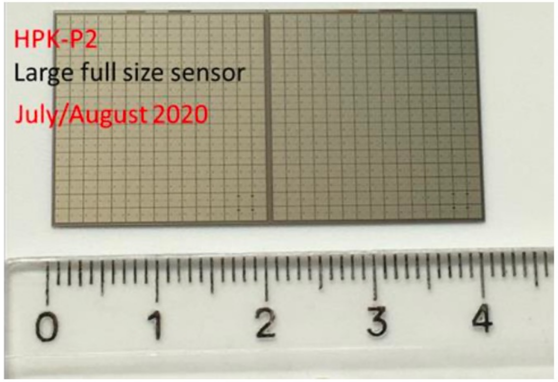






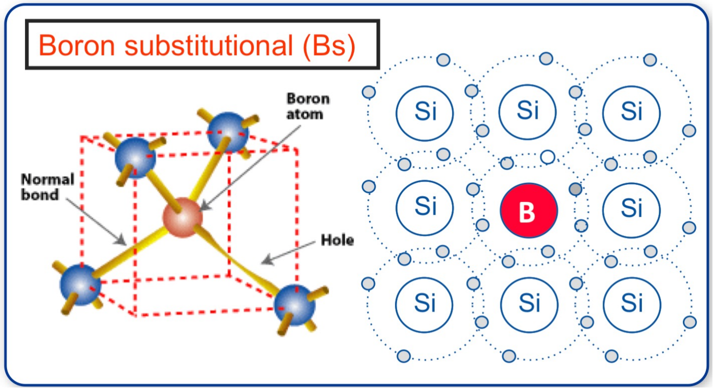




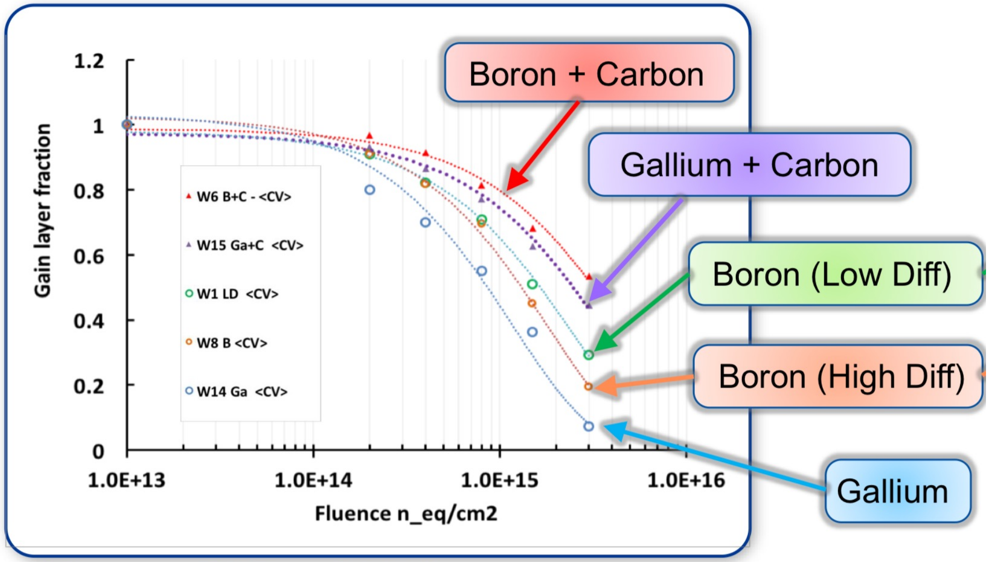


LGAD sensor after Irradiation

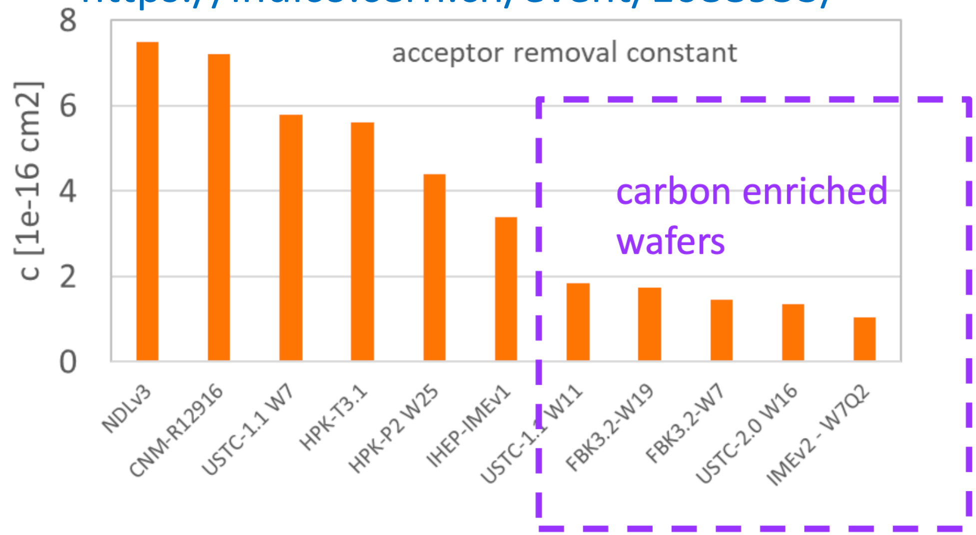
- After irradiation, Boron doping in gain layer became less active (Acceptor removal)
- Carbon-enriched LGAD is more radiation hard
  - Carbon “stabilized” boron doping
- IHEP-IME/FBK/USTC-IME LGAD with carbon
  - Significantly lower acceptor removal ratio
  - Significantly more radiation hard



From Gregor’s talk at CERN Detector seminar
https://indico.cern.ch/event/1088953/



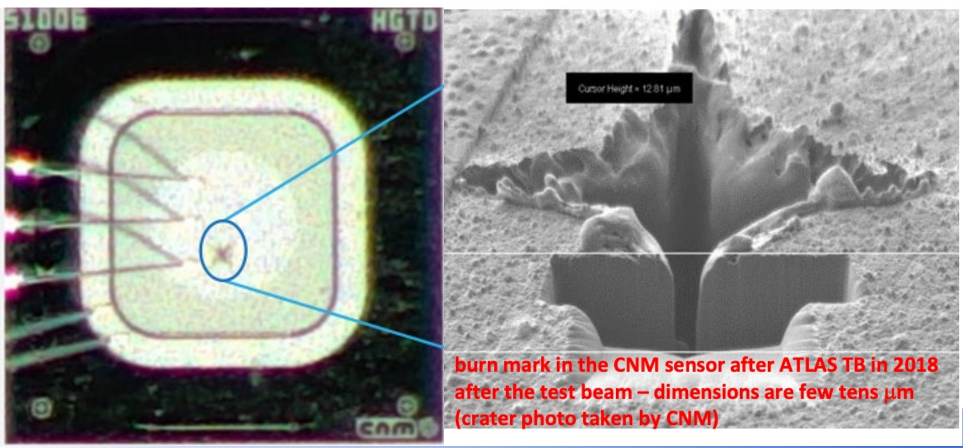
[G.Paternoster, FBK, Trento, Feb.2019]



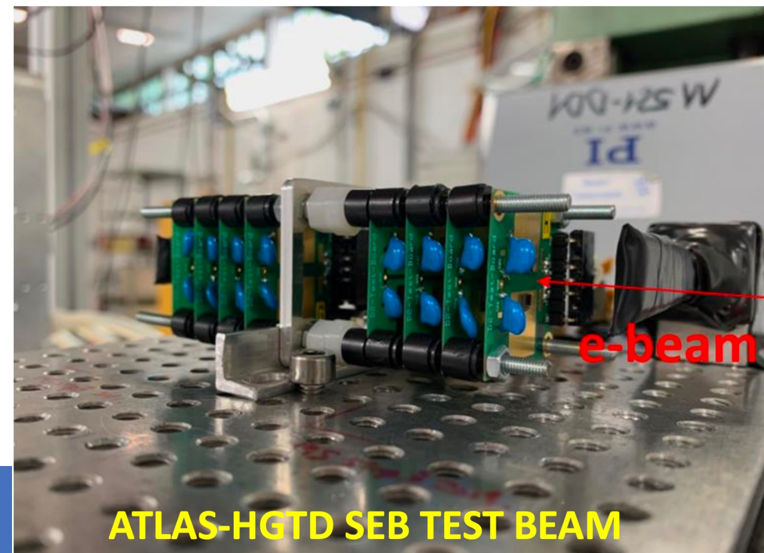
LGAD Single Event Burnout effect (HV stability in the beam)

- RD50, CMS and ATLAS confirmed Single Event Burnout (SEB) effect in testbeam
- The key to avoid burnout effect is to operate at low HV
  - Safe region: < 11 V/um
  - Operate volage needed to be <550V (assuming 50um thick EPI layer)
- HGTD performed test beam at CERN recently
  - LGADs with HV on in 120 GeV high intensity proton beam
  - Good performance for Carbon-enriched LGAD
    - Survived at operational volage

Burn mark of Single Event Burnout



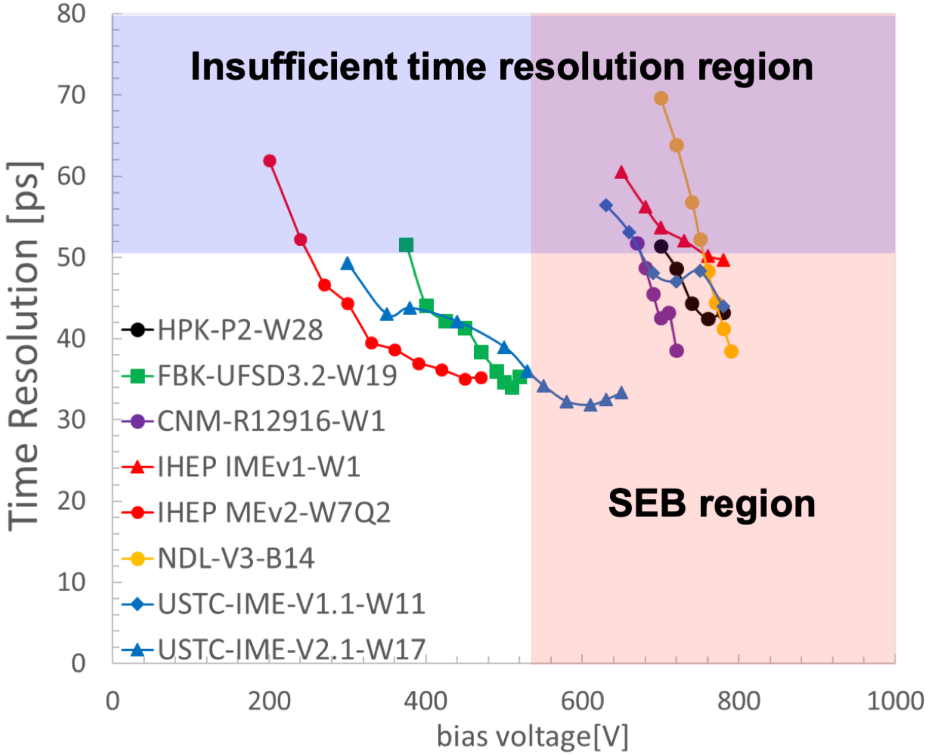
CERN test beam: 120GeV proton



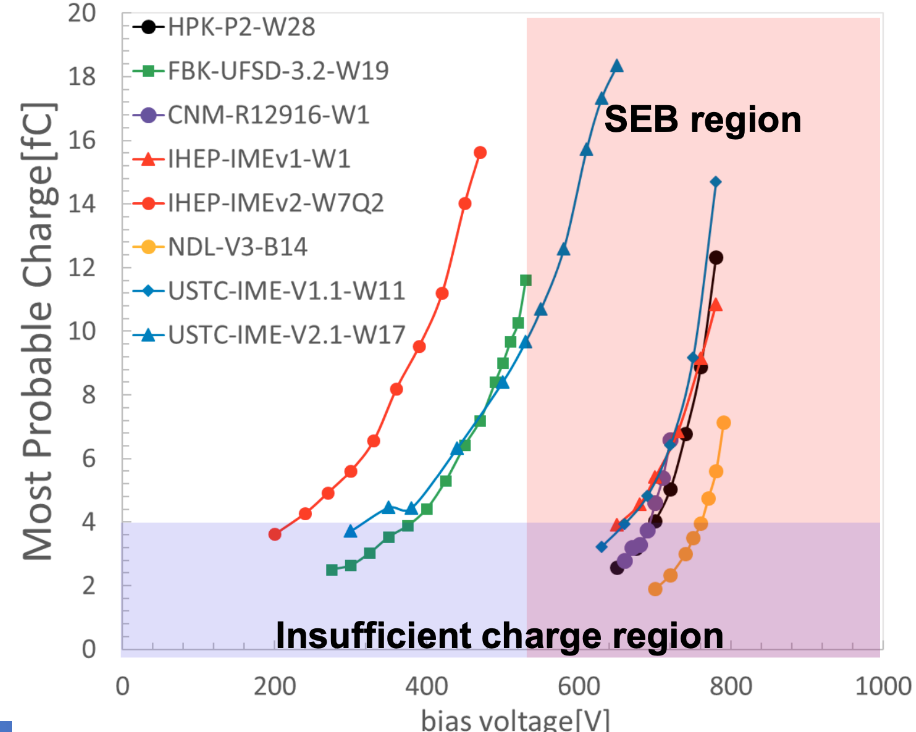
Performance of various LGAD prototypes at 2.5e15 cm^{-2} fluence

- Carbon enriched LGADs fulfil HGTD sensor requirements after irradiation
- The effect of the Carbon-enrichment is clearly very beneficial and allows the sensors to be operated at much smaller voltages
  - Eg: IHEP-IME sensor can reach 4fC at below 300V after irradiation

Time resolution of LGADs Vs Bias Voltage

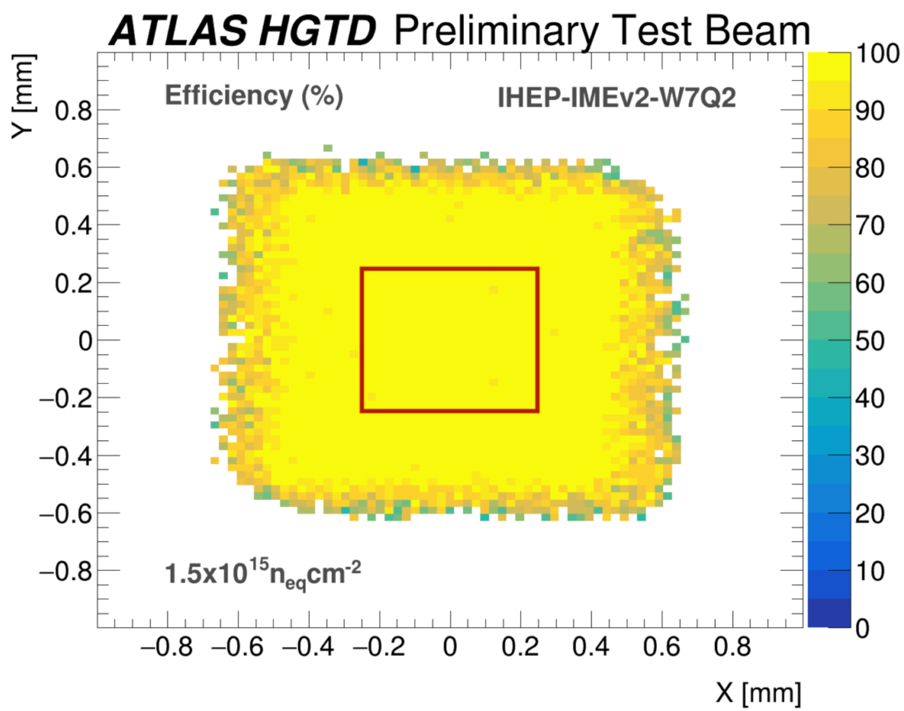


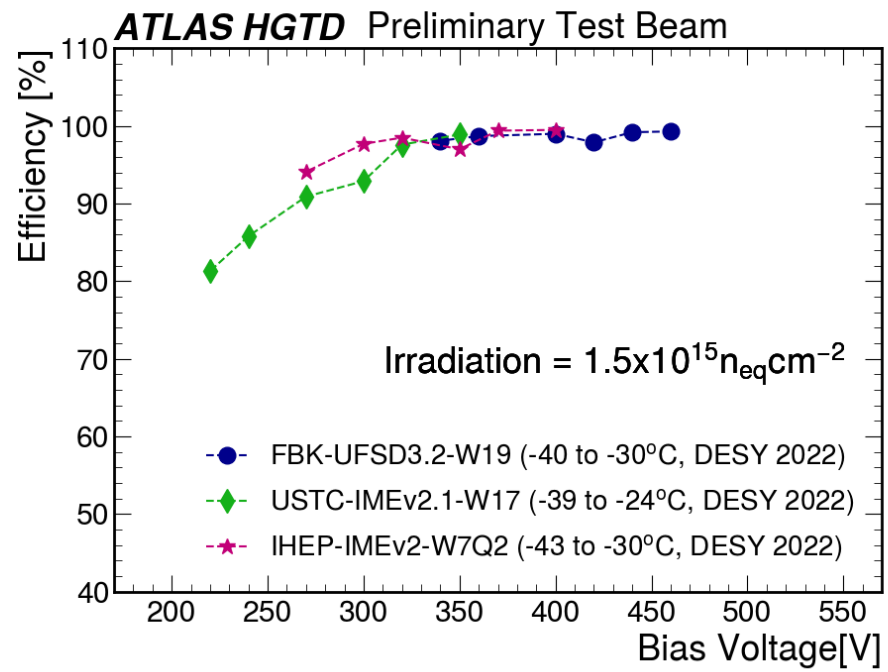
Charge collection Vs bias voltage



Performance of irradiated LGAD prototypes at testbeam

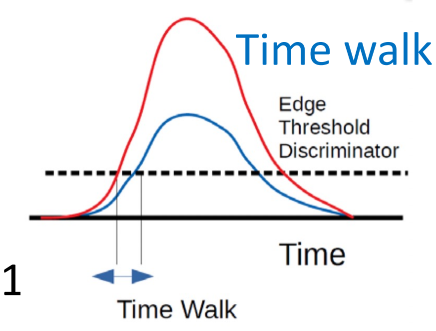
- Carbon-enriched sensors reached specification requirements.
- Close to 100% hit efficiency for irradiated LGAD at DESY/CERN test beam



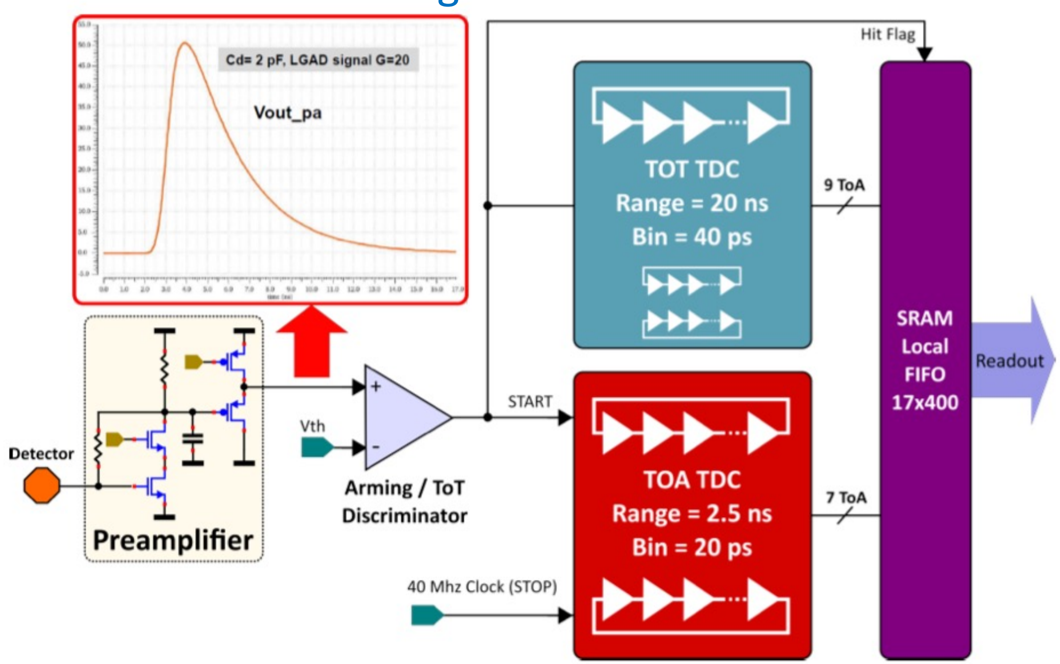


ALTIROC : Fast Timing ASIC

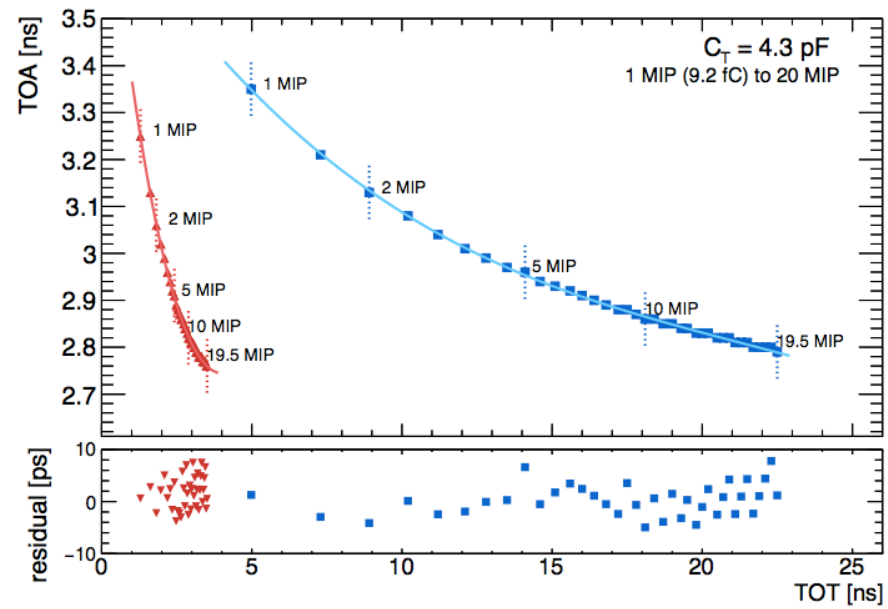
- 225 front-end channels in ALTIROC, each channel has
  - A preamplifier followed by a discriminator:
  - Two TDC (Time to Digital Converter) to provide digital **Hit data**
    - Time of Arrival (TOA) : Range of 2.5 ns and a bin of 20 ps (7 bits)
    - Time Over Threshold (TOT) : range of 20 ns and a bin of 40 ps (9 bits)
  - One Local memory: to store the 17 bits of the time measurement until L0/L1



ALTIROC timing ASIC in nutshell



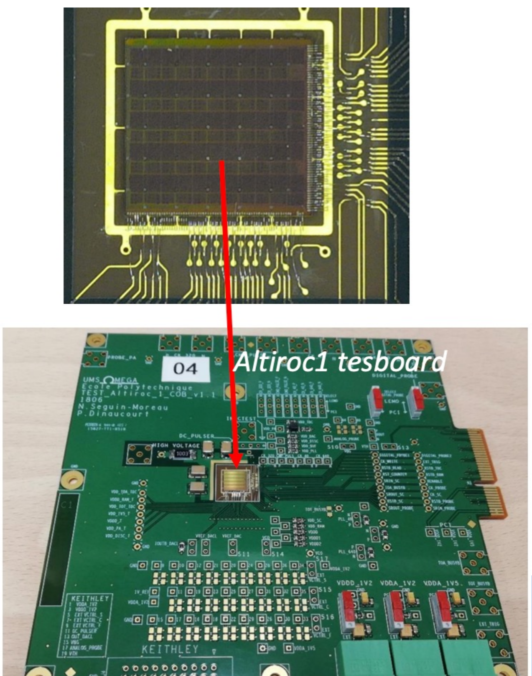
Time walk correction with TOT



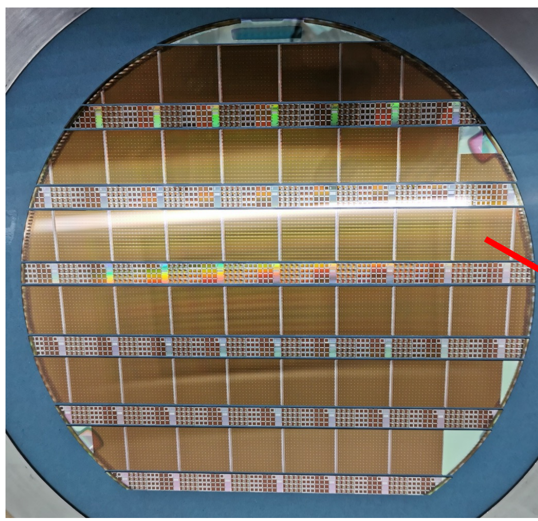
ALTIROC R & D

- ALTIROC0 – preamplifier + discriminator waveform sampling on the oscilloscope
- ALTROC1– 5x5 array with complete analogue front end (discriminator + TDC)
- ALTIROC2– 15x15 array with almost complete functionalities
  - Full-size ASIC prototype ~2x2 cm^2 with 225 readout channels
  - Large amount of digital data, limited power consumption (1.2W/ASIC → 5.3 mW/ channel)
  - data serializers @ up to 1.28 Gb/s,

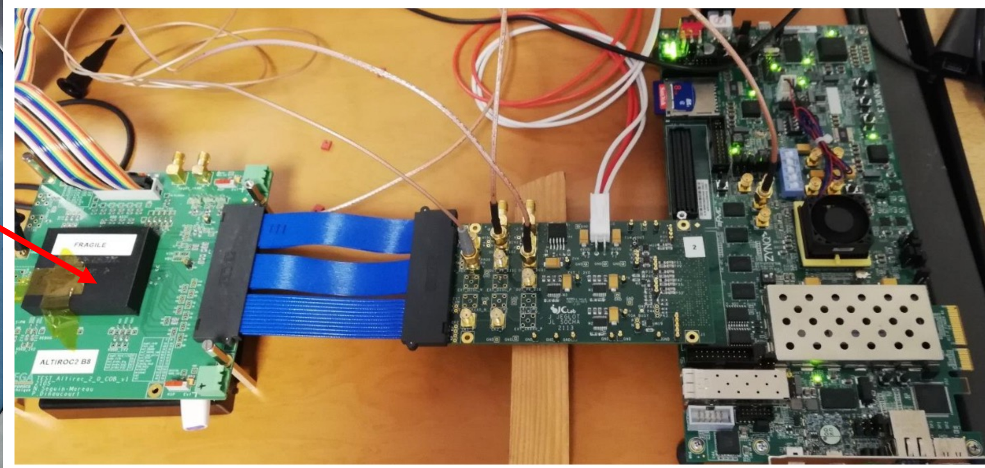
ALTIROC1 and testboad



ALTIROC2 wafer



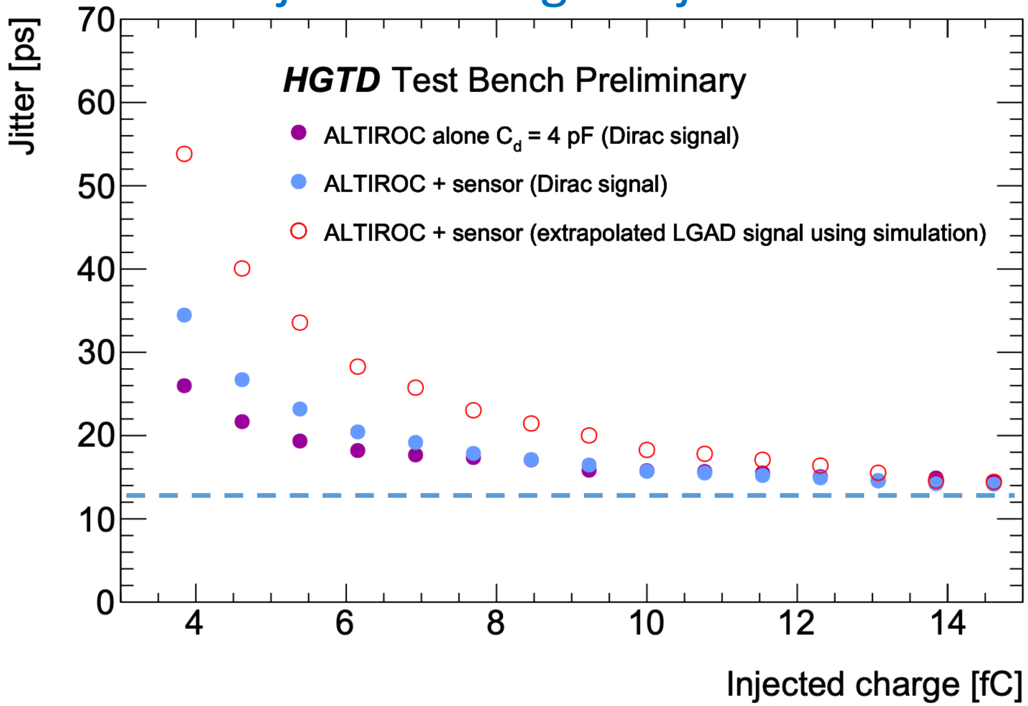
ALTIROC2 test bench setup



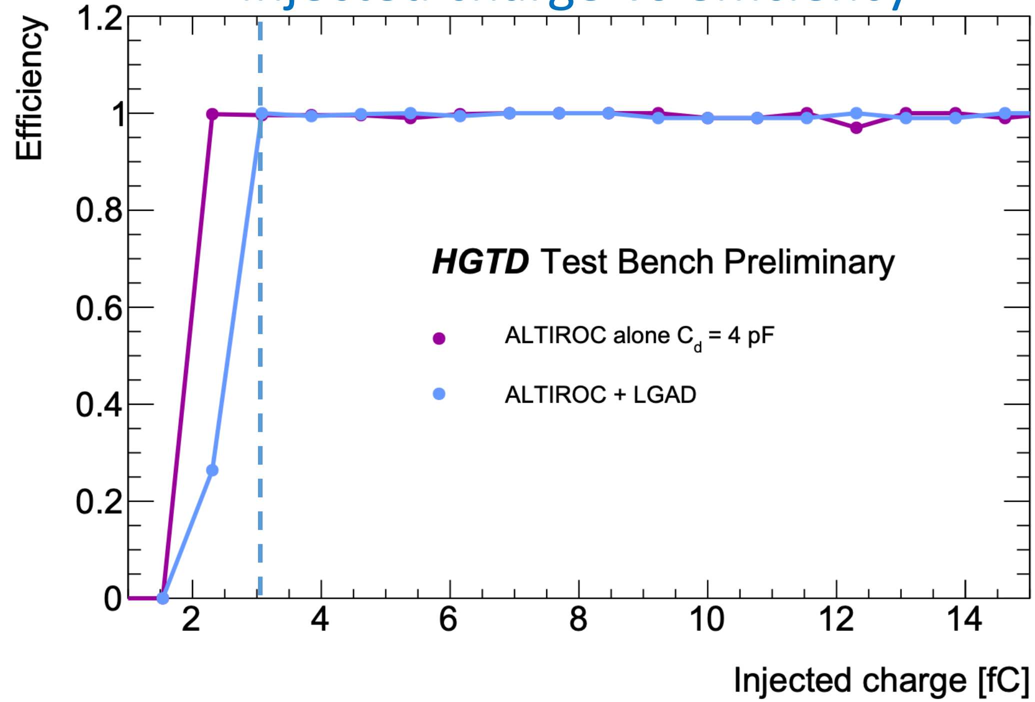
ALTIROC1 testing

- Very demanding requirement of <70 ps time resolution @ 4fC
  - LGAD collected charge >15fC (>4fC) before (after) irradiation
- Charge injection self-calibration test in ALTIROC
  - Thresholds can be as low as 2 fC - full efficiency reached at **~3 fC**
  - ~15ps jitter @ 15fC, better than 70ps jitter@ 4fC

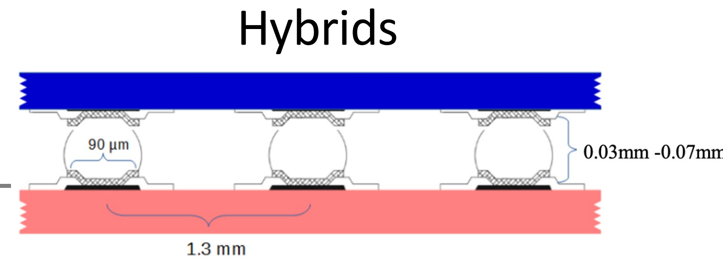
Injected charge Vs jitter



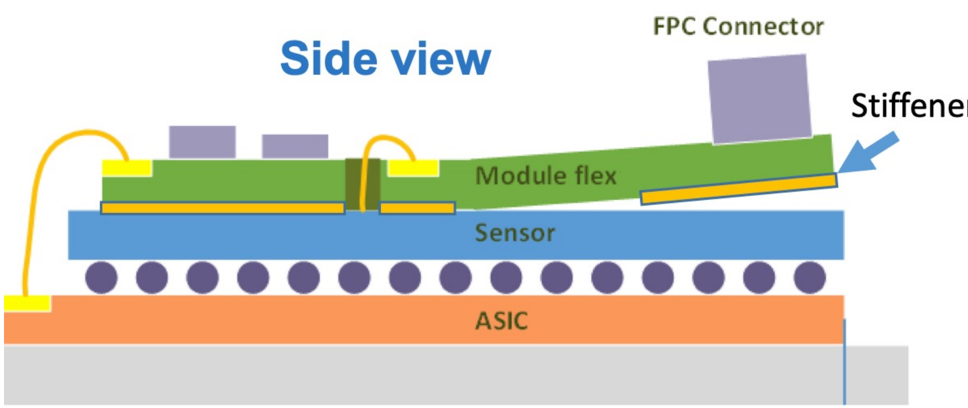
Injected charge Vs efficiency

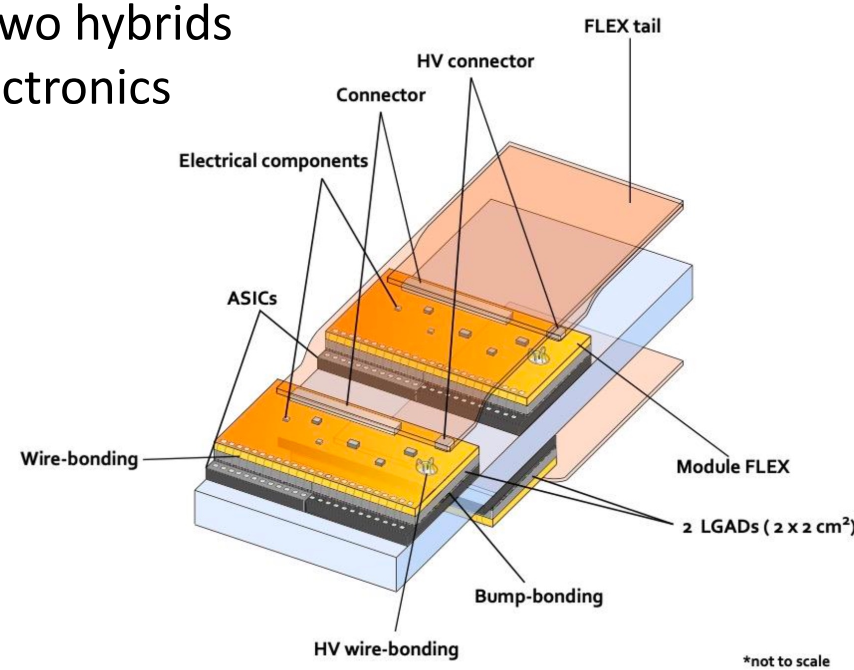


HGTD Modules



- HGTD has 8032 total modules, 3.6 M channels, 6.4 m^2
  - There are six module production sites in HGTD project
  - France and China are major module production sites
- **A module consists of one module flex and two hybrids.**
  - **Low-Gain Avalanche sensors (LGAD) (15 × 15 pads of 1.3 x 1.3 mm^2)**
- **Hybrid: One LGAD sensor bump bonded to one readout ASIC (ALTIROC chip)**
- **One Flexible -PCB (module flex)** glued on top of two hybrids
- Flexible tail connected module to outer radius electronics



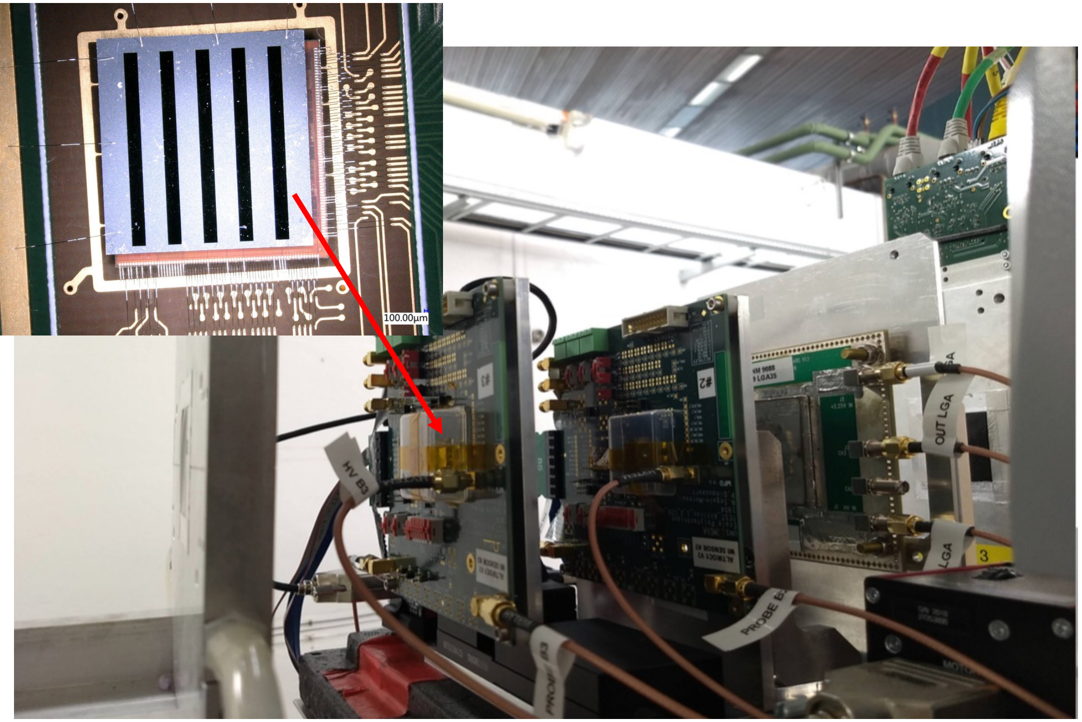


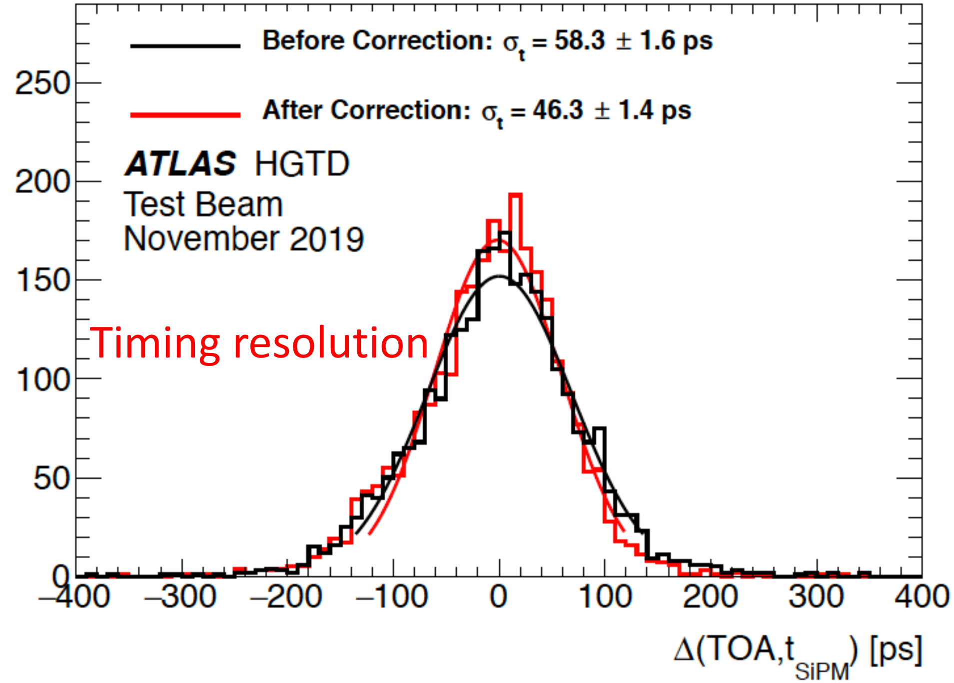
ALTIROC1 mini-modules performance at test beam

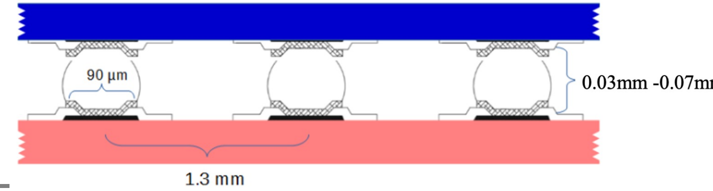
- 5*5 channels Mini-modules (ALTIROC1+LGAD) was tested at testbeam
  - 46ps timing resolution after time walk correction

LGAD Landau	25 ps	the reason for part of the high jitter found **26 (known reasons)**
Jitter+system/internal clock+time walk residual	37 ps	
TDC clock	7 ps	Total resolution: 36 ps (likely achievable for 20 fC)/ 70 ps for (4 fC)
Per hit total	46 ps	

ALTIROC1 mini-modules @ test beam



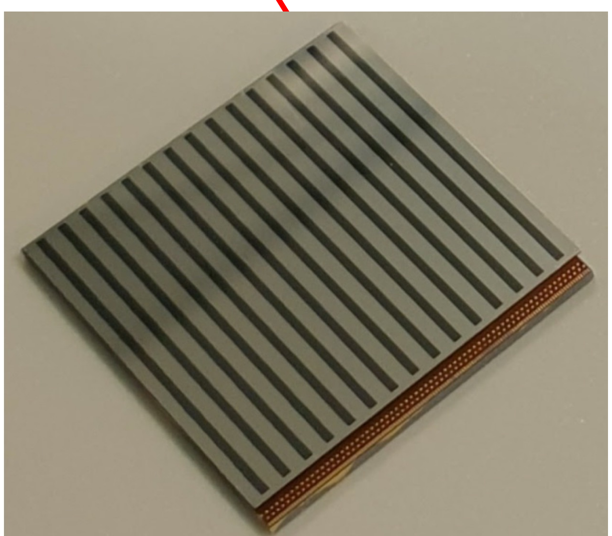




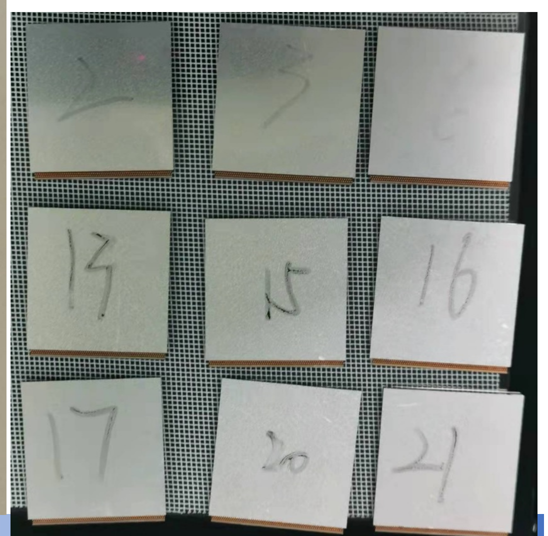
ALTIROC2 full-size hybrid

- IFAE already made 15+ bare module prototype (ALTIROC2 + HPK LGAD)
- IHEP worked with NCAP company, made 40+ bare module prototype by far
  - ALTIROC2 + IHEP-IME v2 LGAD sensors
- AEMtec (Germany) company made 30 prototype
  - ALTIROC2 + FBK LGAD sensors

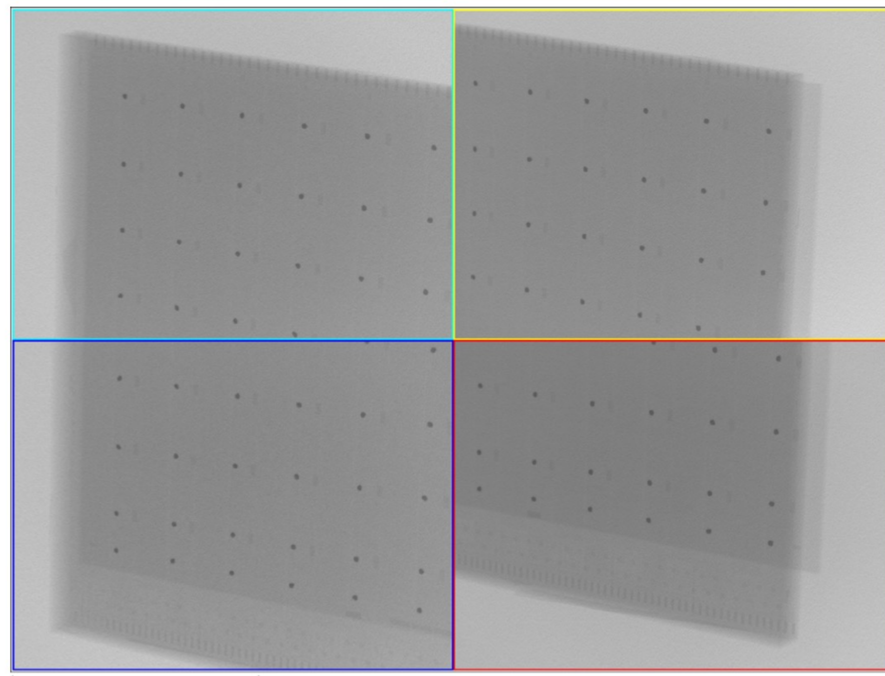
ALTIROC2 + HPK LGAD



ALTIROC2 + IHEP-IME LGAD

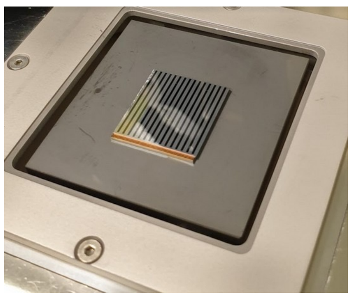


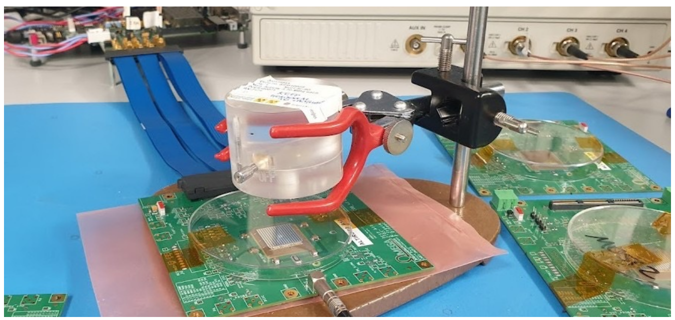
X-ray image of full-size hybrid

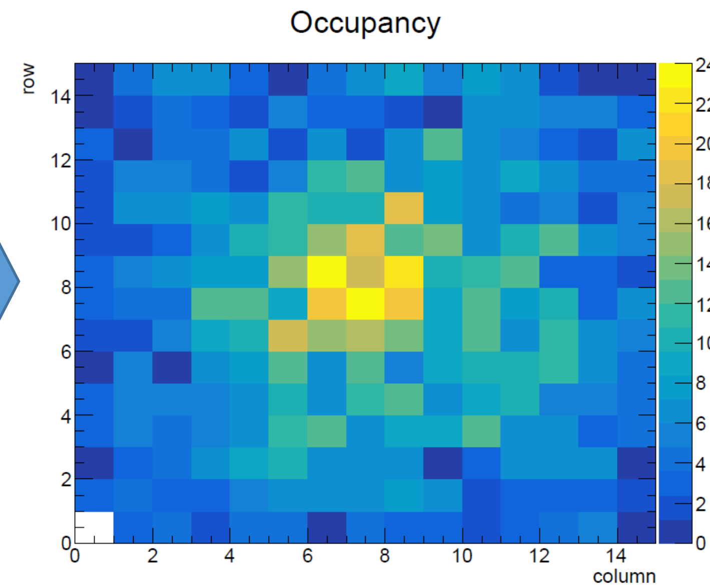


Hybrid functional test

- Sr-90 Source tests
  - Very collimated, it was moved to cover the whole area
  - Basically a noise scan, but pixels with more hits just indicate that the area was exposed for longer time
  - So far 5 hybrids fully tested and the yield is 100% (1080/1080) connected bumps , as well as all ALTIROC2 chips operational"

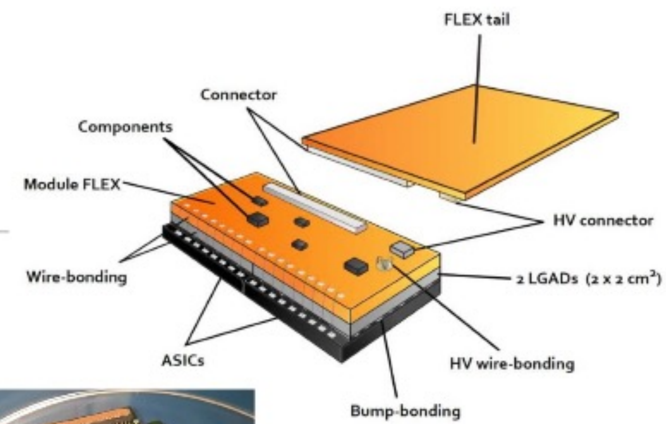


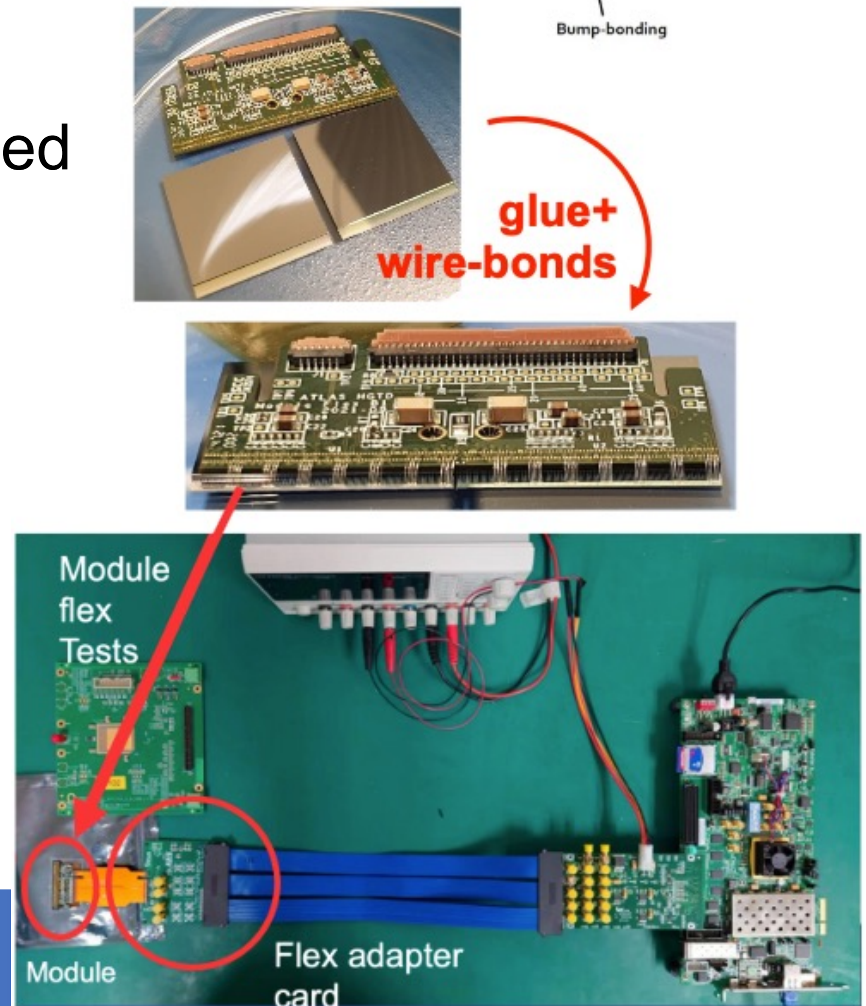


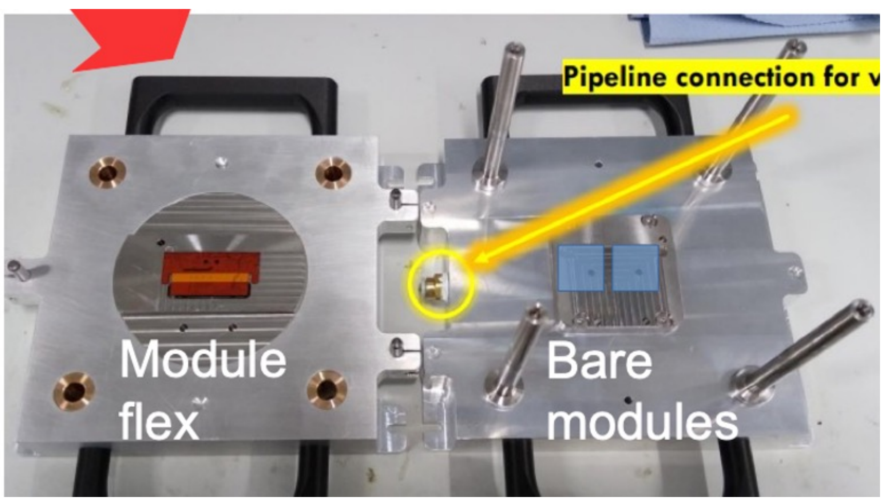


Module assembly

- HGTD detector has 8032 modules
  - Each has 1 flexible PCB + 2 hybrids
  - 2cm *4 cm, 450 channels
  - 6 production sites around the world
- Jigs tools for module assembly developed
- Module-level test system developed



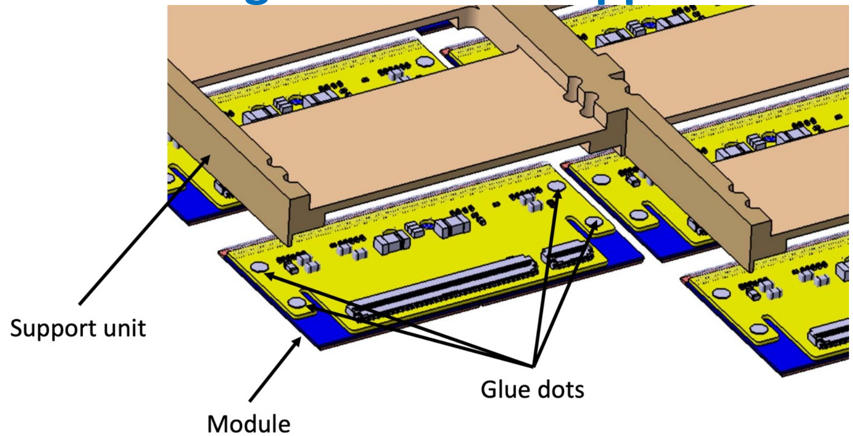




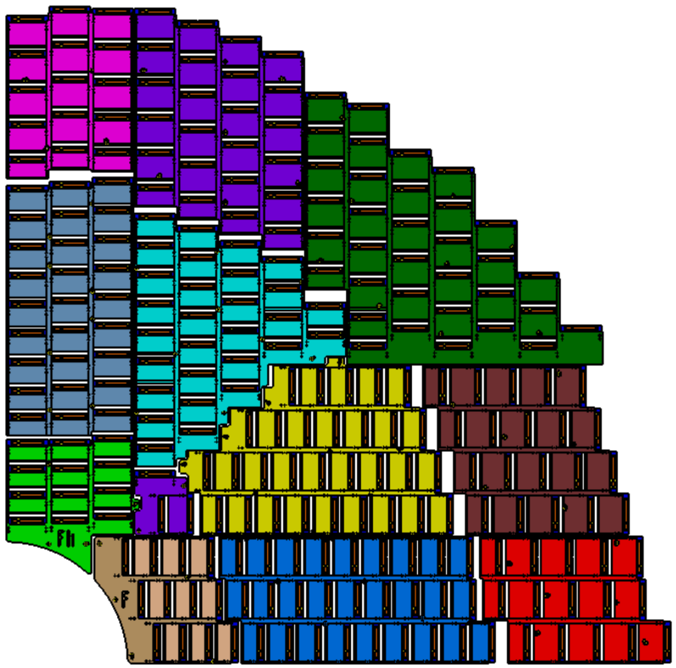
Detector units

- **Modules are installed and glued on support units (PEEK)**
  - Challenges :machining or 3D printing of PEEK (flatness <200µm)

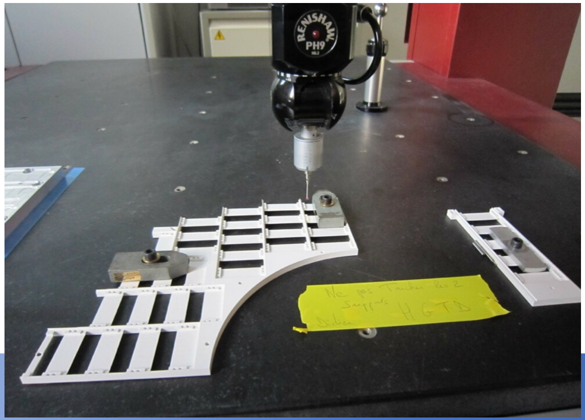
Loading modules on support units



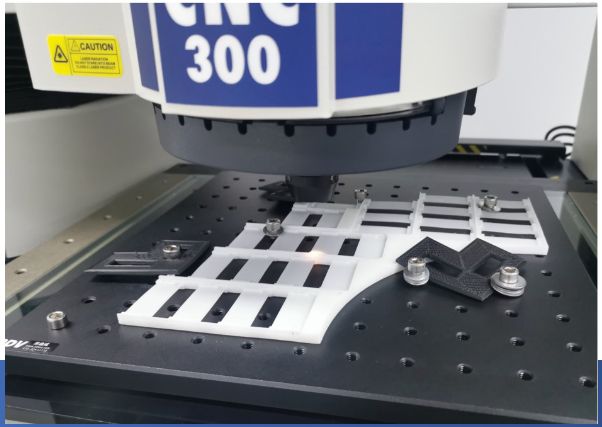
Different color represents different support units.



Support unit metrology



Support units metrology

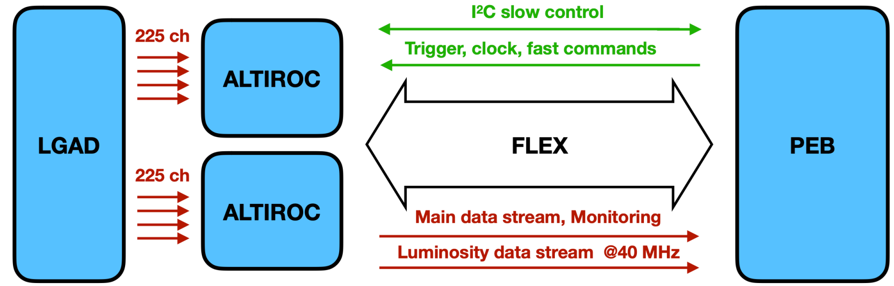


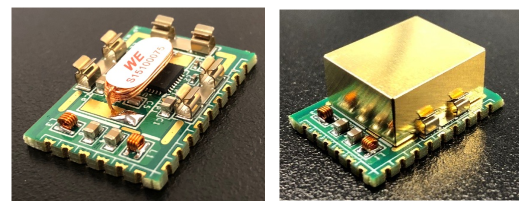
Peripheral board (PEB)

- Work on the characterization of all individual components, prototypes under production:
  - Detailed testing of the DC/DC converter (bPOL12V), different options under consideration

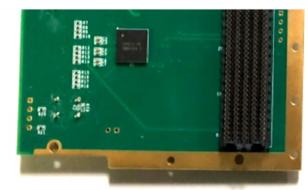
    ↠ need to fulfil space constraints, power efficiency measured
  - Started tests on lpGBT with evaluation board
  - VTRX+: successfully tested 2.56G/10.24G communication, bit error rate ($<10^{-12}$), passed eye diagram test
  - MUX64: analogue multiplexer (for monitoring of ASIC power supply and temperature)

  ↠ basic functionality confirmed, On-resistance larger than expected (further investigations necessary)

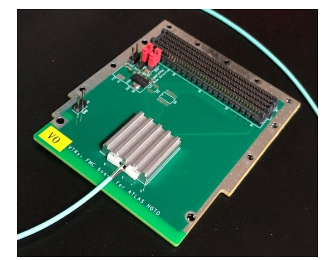




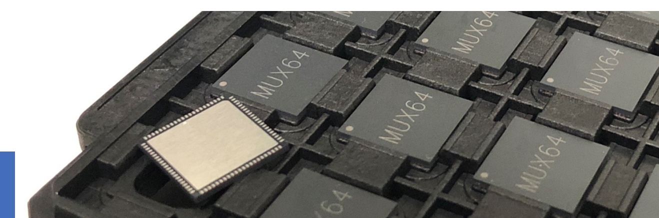
DC/DC converter



lpGBT eval. board



VTRx+ eval. board

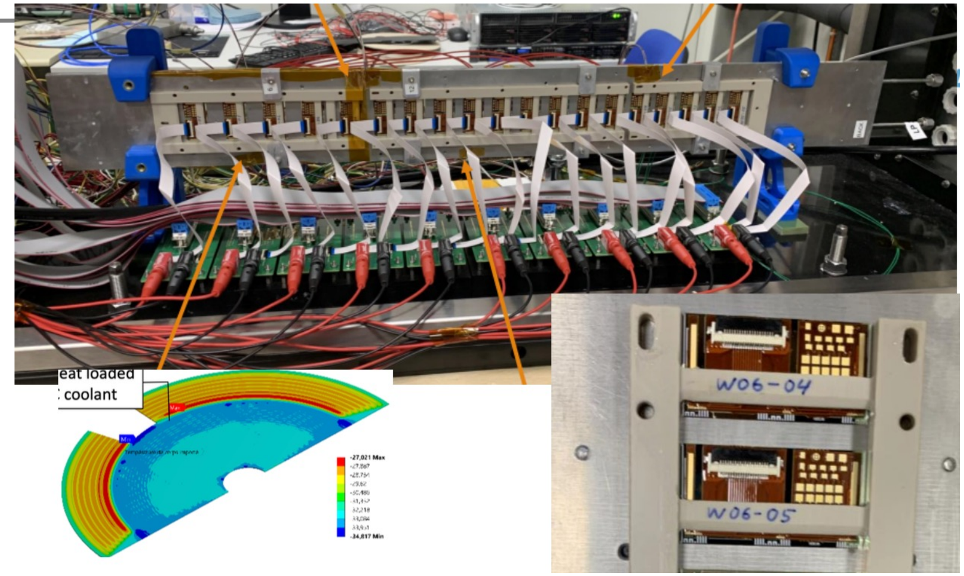


MUX64 in QFN88

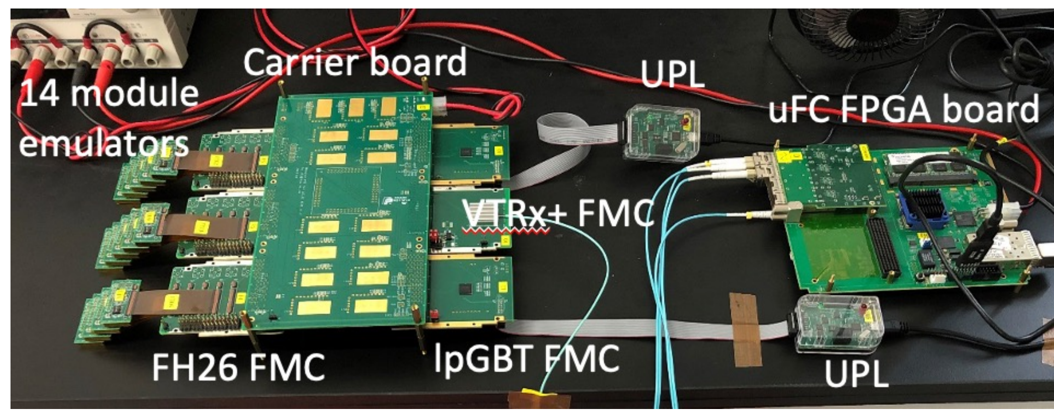
Demonstrator

- Heater demonstrator
  - 19 silicon heaters mounted on a single stave
  - Representing modules dissipating heat
  - on the cooling plate (CO2 cooling)
- Modular Peripheral electronics board demonstrator
  - Minimum system for full chain readout, from module emulator boards to FELIX board
  - Support up to 14 modules with two lpGBTs and one VTRx+
  - Timing
    - Up to 3 modules @ 1.28Gbps
    - Up to 7 modules @ 640Mbps
    - Up to 14 modules @ 320Mbps
  - Luminosity
    - 7 modules @ 640Mbps

Heater demonstrator @ CERN



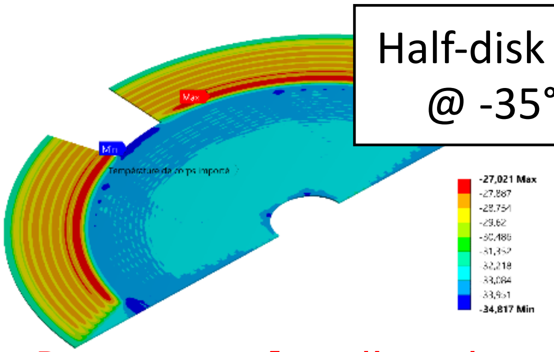
Modular PEB demonstrator @ IHEP



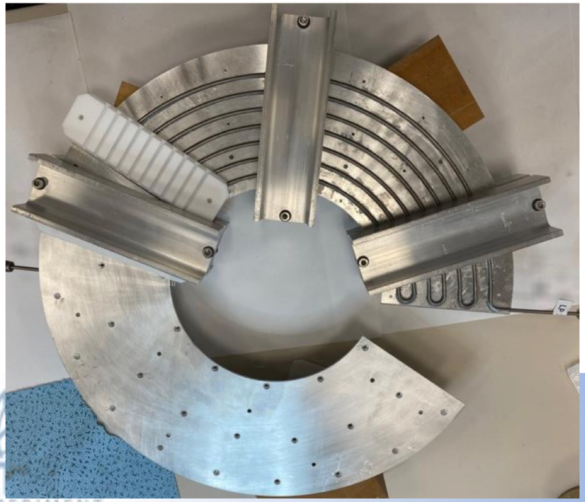
HGTD Mechanics and service

- Hermetic vessel and on-detector cooling passed SPR review
- Cooling plate with CO2 loops design and prototyping in good Progress
- Outer ring in progress: Challenging tight junction design with lots of feed-through

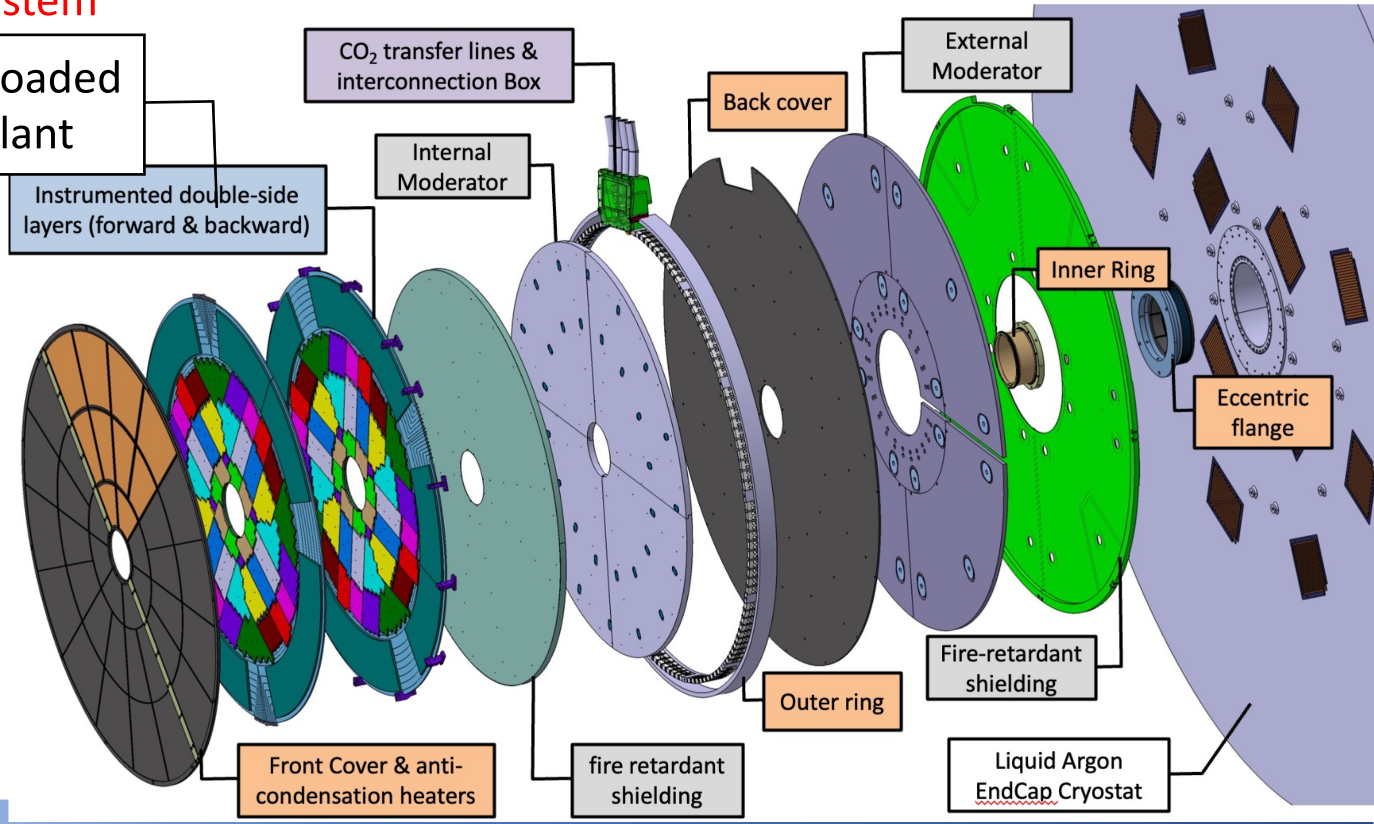
Thermal simulation of cooling system



Prototype of cooling plate



Overall view with mechanics main items

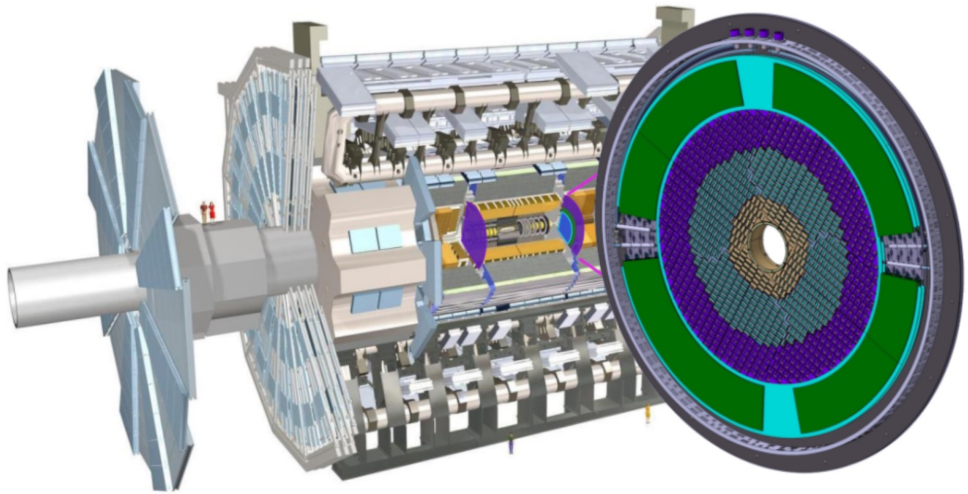


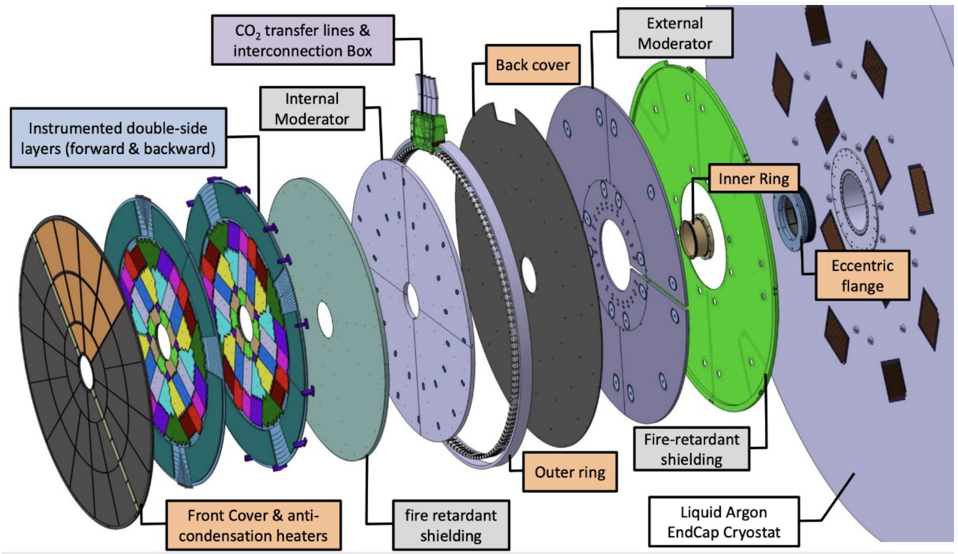
Summary: HGTD detector for ATLAS phase II upgrade

- Good progress in LGAD design fulfilling the the radiation hardness requirements
  - Carbon enriched LGADs fulfil HGTD sensor requirements up to 2.5e15 n_{eq}/cm^2
- ALTIROC 2 (full size ASIC) on schedule, under study, so far all blocks functional
- Concrete implementation of Peripheral electronics components are under test
- full-size hybrids are in production and showed good results in functional tests
- Demonstrator activities ramping up
- Next milestones:
  - 2022: HGTD Demonstrator completed
  - 2023: Peripheral electronics boards and LGAD sensors production started
  - 2024: ASICs, Modules and detector units production started
  - 2026-2027: HGTD detector Integration at CERN, installation

Backup: High Granularity Timing Detector (HGTD)

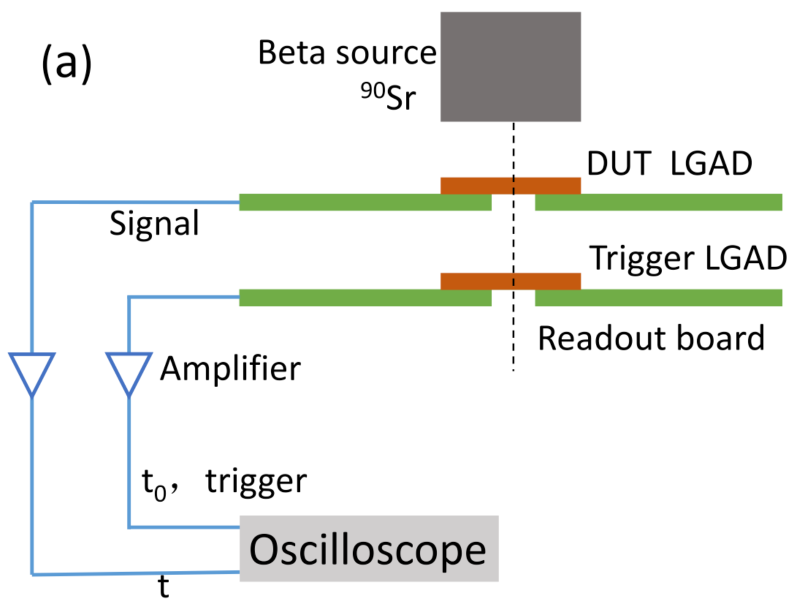
- High precision timing (per-track resolution of **35-50ps** up to 4000 fb-1) to mitigate pileup effects and improve the ATLAS performance in the forward region (**2.4 ≤ |η| < 4.0**)
- Provide online and offline luminosity measurements by transmitting N_{Hits} per ASIC at 40MHz in outer region
  - 2 disks (one per endcap) outside of ITk volume, upstream of the fwd. calorimeters, consisting of **2 double-sided layers** each
  - Very limited space in z-direction ↠ overall thickness of 12.5 cm for each disk
- Silicon sensor technology (LGAD)
- Max expected fluence in "3-ring layout" is **2.5e15 neq/cm²** and sets the radiation hardness requirements for the sensors and electronics

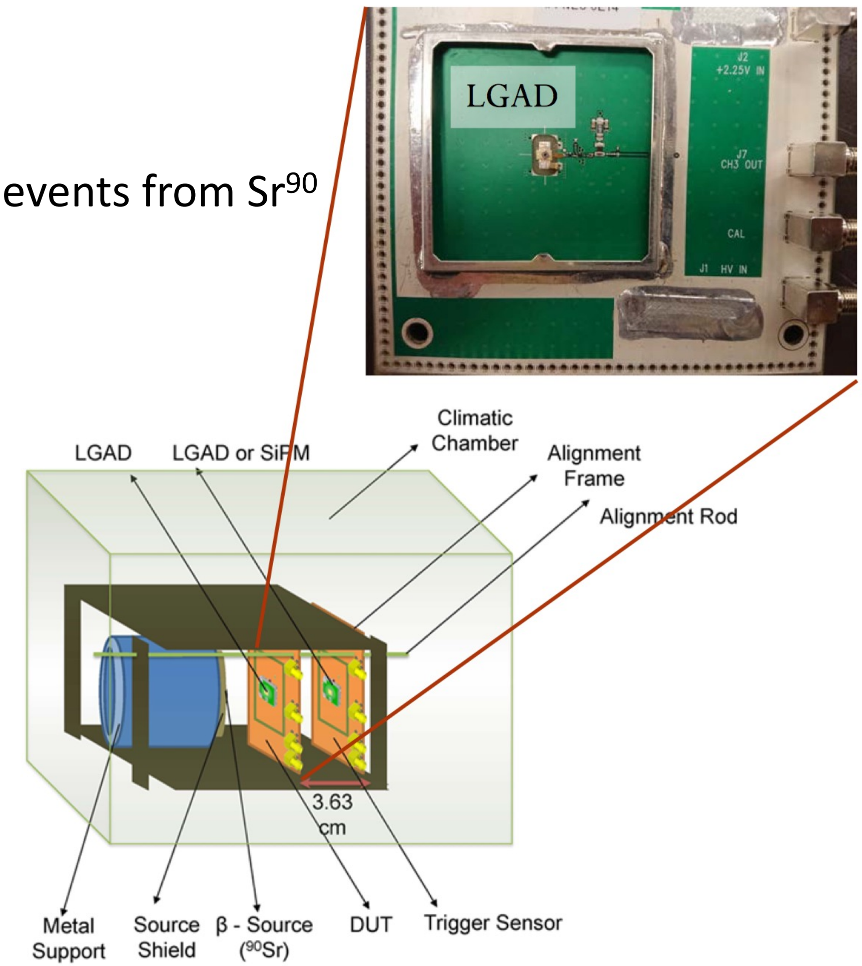




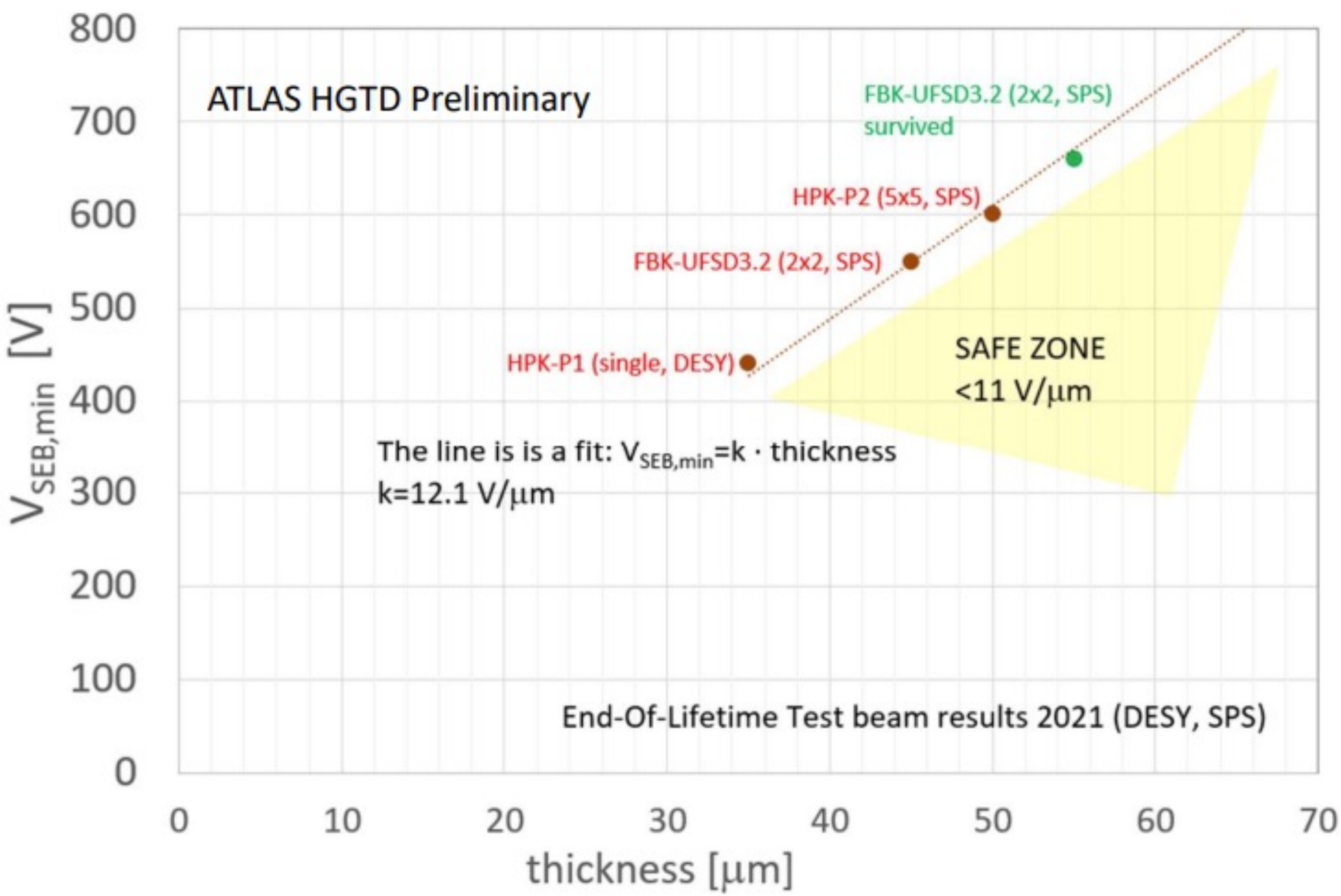
Beta source tests: LGAD timing resolution measurements

- Sr^{90} Beta telescope test (collected charge, gain, time resolution)
- UCSC boards with commercial amplifier and analog readout by Oscilloscope
  - Less constraints with respect to the ASICs – exploring the limits of the sensors.
- Two UCSC boards with two LGAD
  - One LGAD is device under test (DUT)
  - Another LGAD is used to trigger electrons events from Sr^{90}





LGAD Single Event Burnout effect (HV stability in the beam)



Peripheral board (PEB)

- PEB connects FE to the DAQ system, provides LV&HV to the modules