Performance of the ATLAS New Small Wheels in Preparation for LHC Run-3 Data Taking

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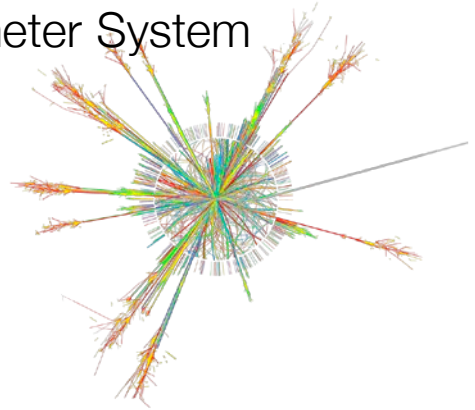
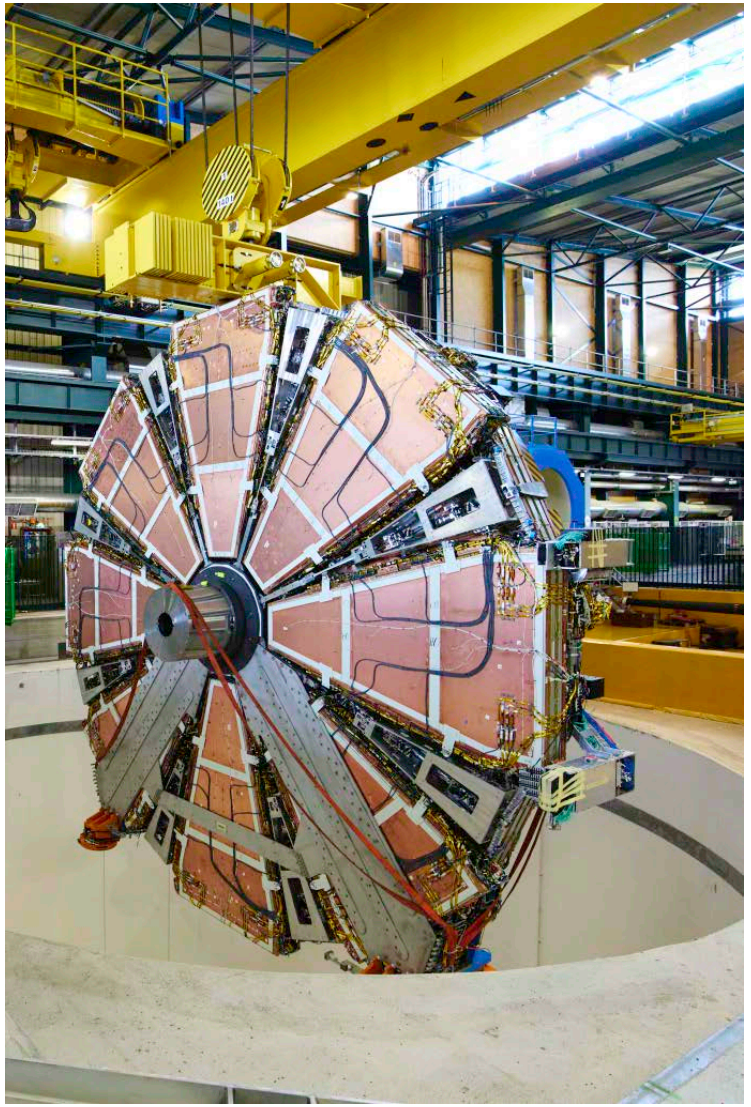


ICHEP 2022 Bologna, Italy
09-07-2022

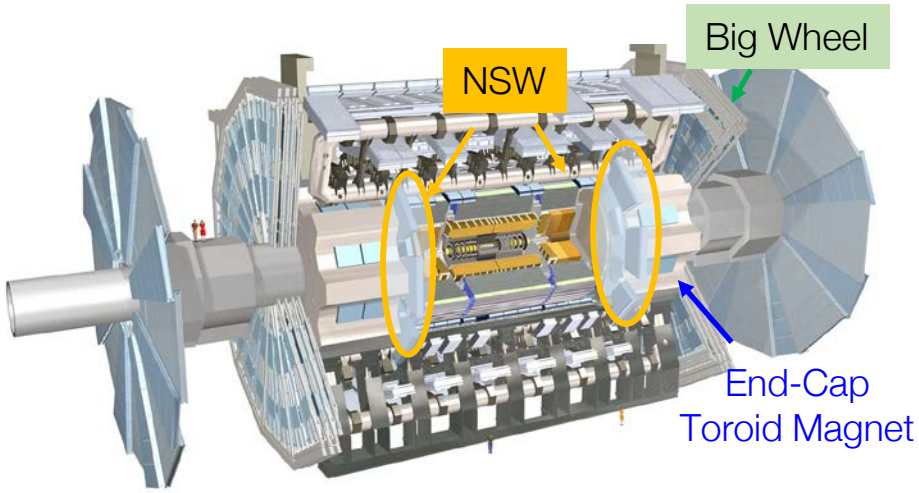
Outline

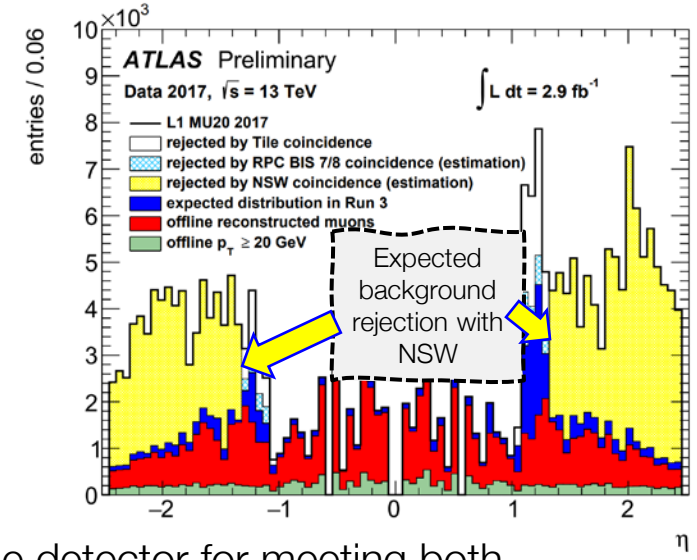
- Introduction: ATLAS New Small Wheel (NSW)
- NSW timeline
- Detector Status: HV, LV, Gas & DCS
- Readout and DAQ
- Commissioning runs with beam
- Trigger Commissioning
- Alignment
- Conclusions



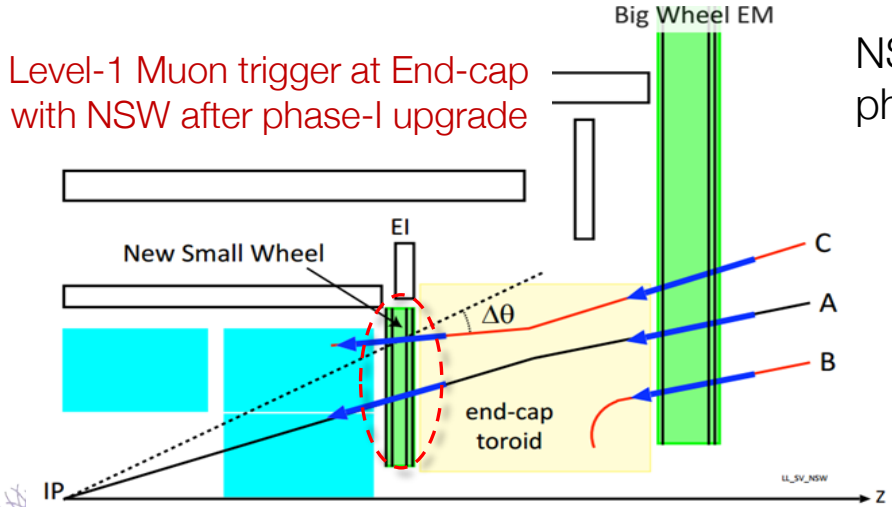
Introduction: ATLAS New Small Wheel

- ATLAS Muon New Small Wheel (NSW) Upgrade: Replace innermost Muon station in the forward region (Small Wheel) to improve LV1 trigger & maintain good tracking at End-cap towards HL-LHC runs with high background rates (up to 20 kHz/cm^2) .





Level-1 Muon trigger at End-cap with NSW after phase-I upgrade



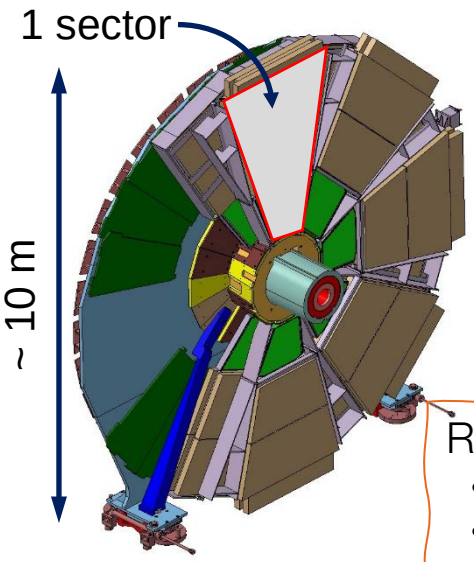
NSW-- One detector for meeting both phase-I and phase-II upgrade goals:

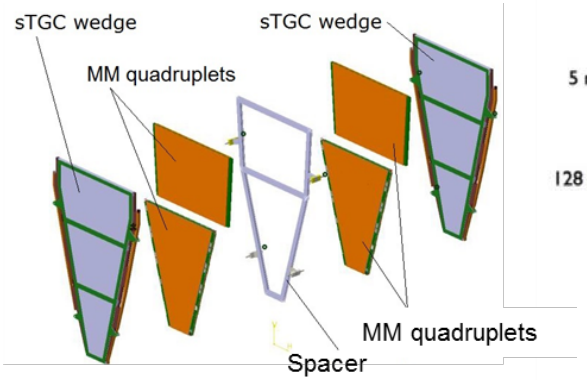
- For offline muon construction: 15% p_T resolution at ~1TeV (~100 μm spatial resolution per detector plane). 97% segment reconstruction efficiency for muon p_T >10 GeV.
- For online (Level-1) triggering: segments measurements with up to 1 mrad pointing accuracy (Phase-II requirement)

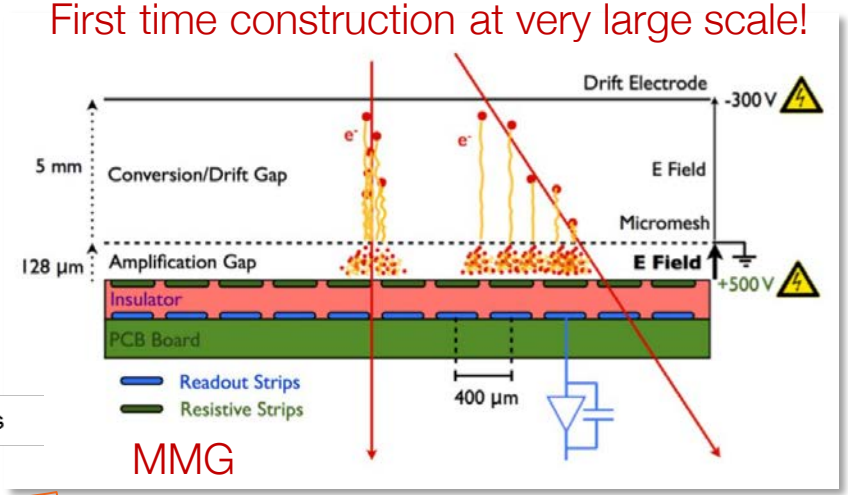
Introduction: NSW Detector

- Two Novel Gaseous Detector Technologies Employed:
  - Micromesh Gaseous Structure Detector, Micromegas (MMG)
  - Small-strip Thin Gap Chamber (STGC)

First time construction at very large scale!

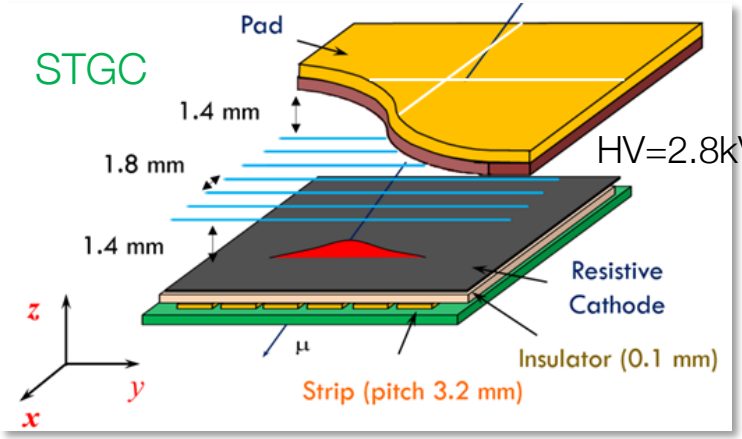






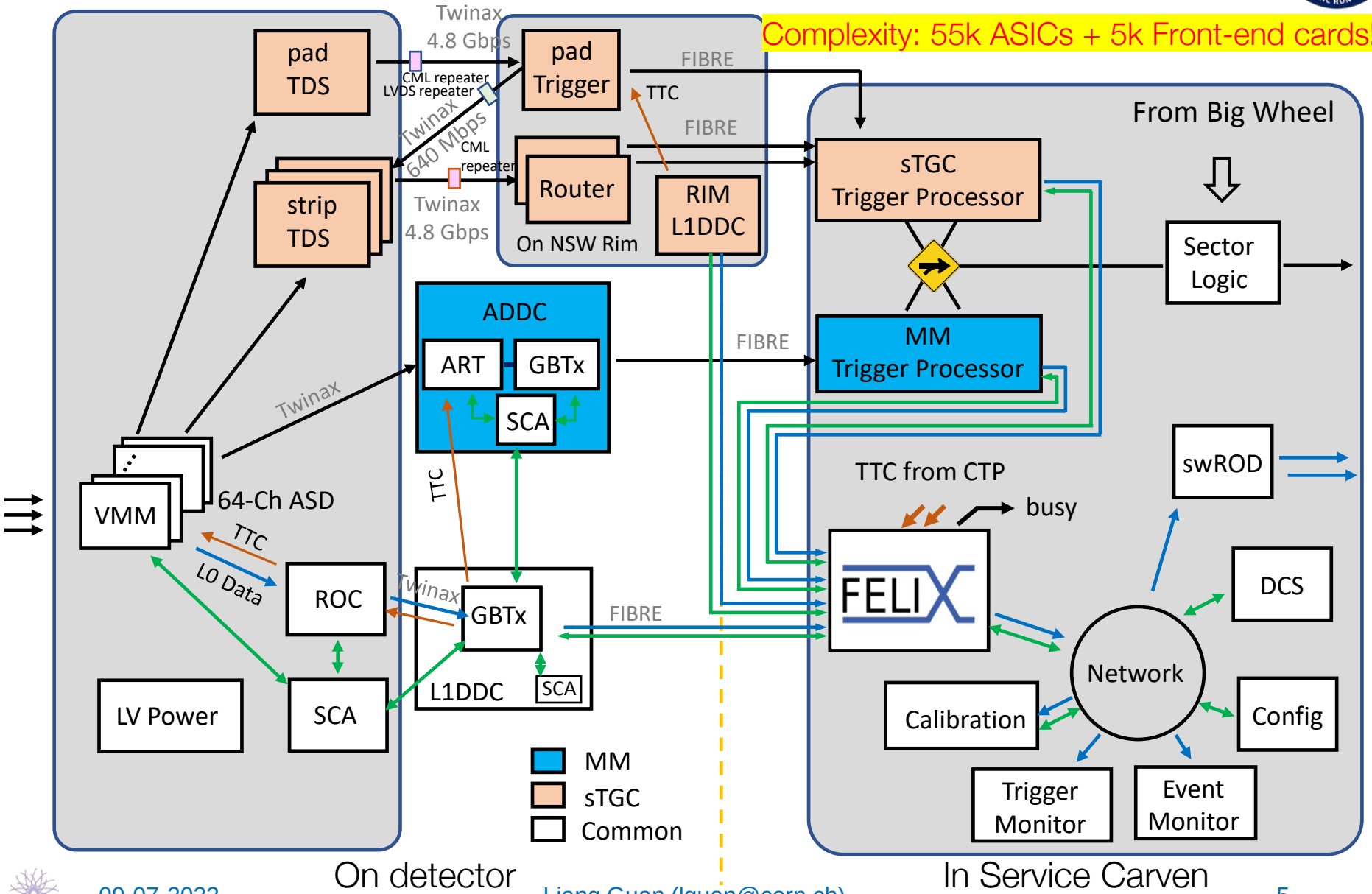
Readout channels (25x old SW):
- MM: ~ 2.1 M
- sTGC: ~ 280 k (strip) + 46 k (pads) + 28 k (wires)

Detector area: ~2400 m^2



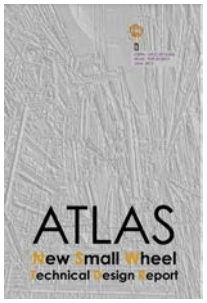
- Both detector technologies provide precision trigger and tracking for muons in the ATLAS forward region.

Introduction: NSW Electronics



NSW Timeline: 10+ years efforts!

TDR
June 2013

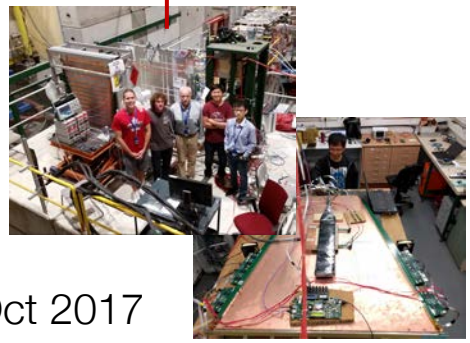


MMG+sTGC detector integration
Dec 2018

Side-A wheel completion
July 2021

August 2021

Commissioning in ATLAS
Now



Oct 2017
R&D and detector construction

Dec 2019
First sector installation on JD

Oct 2021
Side-C wheel completion

Expect NSW for new physics exploration in the next two decades!

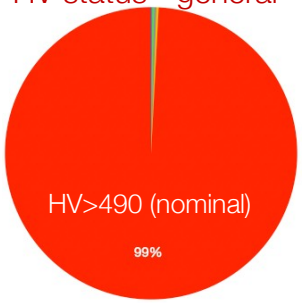
This talk is more biased towards preparation than performances for Run 3 ...

NSW HV, LV, Cooling and Gas system

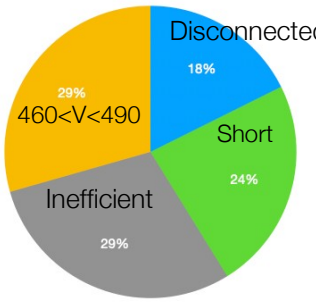
MMG Detector

- HV: ~1% channels observed with defects
  - Observed HV trips with ATLAS toroid magnet ramping -- MMG micro-particle polarization effect.

HV status - general



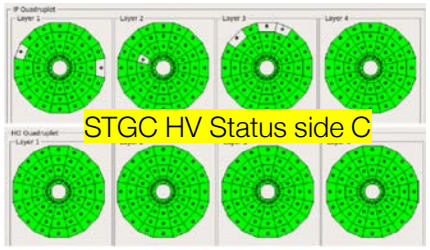
HV defects - breakdown

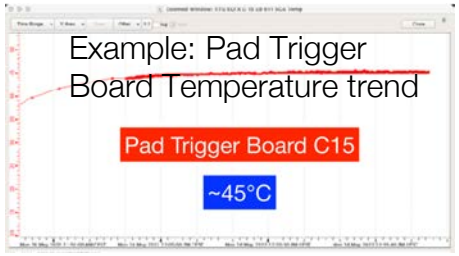


- Gas: Green light to use Ar:CO2:iC_4H_{10} (93:5:2) to improve detector HV stability. Gas flowing since the beginning of the year.

STGC Detector

- HV: < 2% channels observed with defects
  - Mostly known since surface commissioning.
  - 3 quadruplet layers have resistive behavior which could run with high current.





- Gas: Operational gas mixture CO_2:n-pentane (55:45) flushing since March

- Cooling: water cooling loops ON for all sectors all the time.

- LV: Constant on and being monitored. ~1% (13/1024) LV channel failures from Intermediate Power Conversion boards observed since installation and most (9) channels fixed.

Both detectors and service infrastructures are ready for RUN-3.

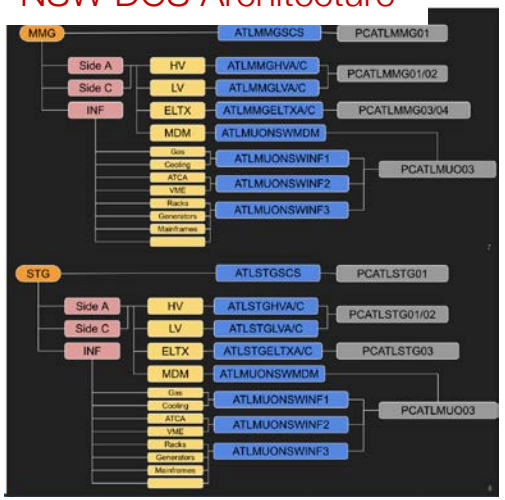
NSW Detector Control System (DCS)

- NSW DCS system is responsible for the control and monitoring of:
  - Detector HV, Electronics LV
  - Electronics (GBT-SCA, FEAST, VMM)
  - MDM (T&B sensors)
  - VME&ATCA crates
  - Cooling and Gas, etc.

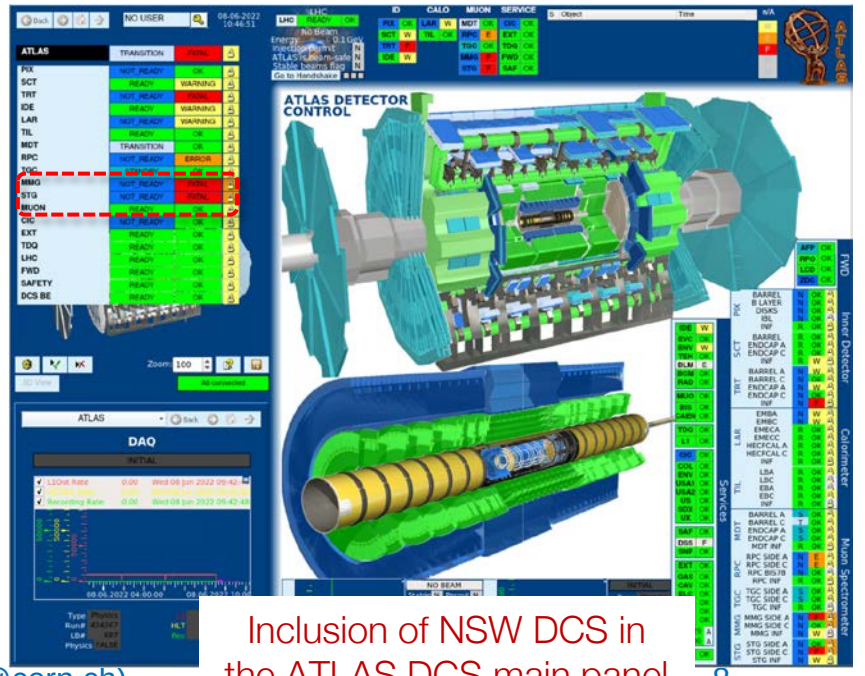
- NSW DCS operational at ATLAS control room and provides continuous support to the integration and commissioning since NSW installation.

- Recently, successful integration of NSW MMG & STGC DCS into ATLAS Muon Central DCS: Milestone!
- Gaining experiences for long term operations (state & status propagation, alarms). Continued development to support hardware changes, better user interface.

NSW DCS Architecture



DCS Rack in Service Carven

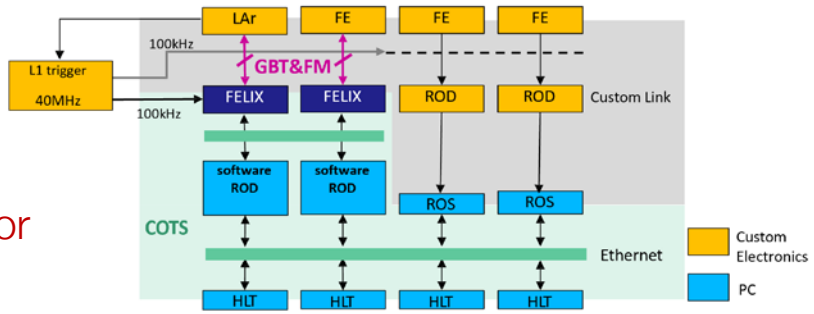


Inclusion of NSW DCS in the ATLAS DCS main panel

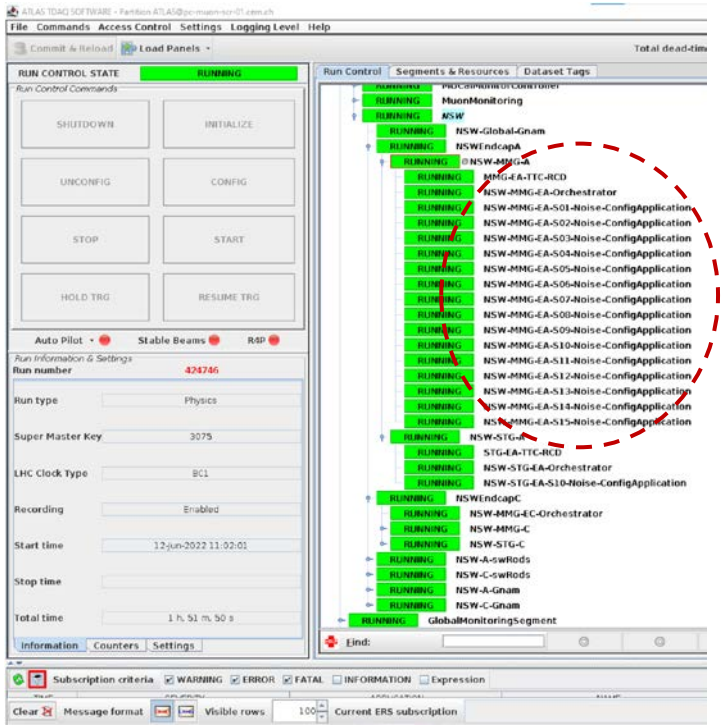
NSW Level-1 Readout and DAQ

- NSW employs new generation DAQ developed for ATLAS Run-3: FELIX (Front End LInk eXchange) system + software ROD (swROD). In addition, slow control via OPC servers.
- Extremely busy and tight schedule for DAQ (used for the first time at large-scale) commissioning: enormous efforts.
- Integration in the ATLAS TDAQ partition since May: from a few sectors to entire wheel.
- Progresses made to understand & solve issues:
  - filtering noisy GBT-SCA packets to keep FELIX/OPC server stable.
  - swROD parameter adjustment ...
- Participated ATLAS collisions and special runs (see next slides).
- Experience DAQ instabilities with Felix buffer filling and data link de-synchronization as more sectors included or at high (>10kHz) trigger rate.

ATLAS RUN-3 DAQ



Inclusion of NSW in the ATLAS TDAQ

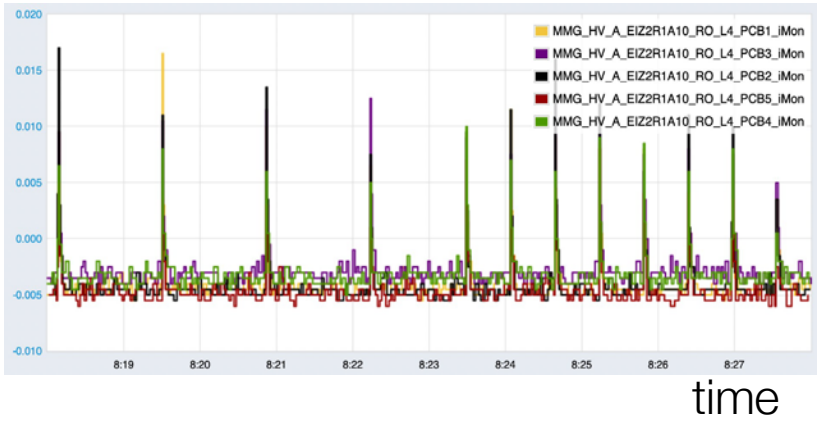


NSW Readout and DAQ: Calibrations

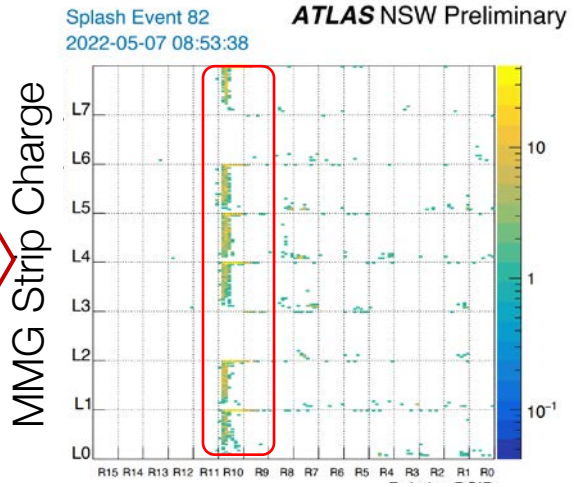
- Many crucial calibrations required for the detector and DAQ operation: from optimization of Front-end analog circuits, correct time-in of detectors to ensuring electronics synchronization and data communication stabilities
  - VMM[1] ASIC: baseline, threshold, pulser, charge & time
    [1] 64-channel mixed signal ASIC with charge amplifiers and ADCs for charge, time measurements
  - ROC ASIC[2]: internal phase - TTC & VMM data decoding
    [2] Readout control ASIC distributes TTC signals and aggregate L0 data from 8 VMMs per Front-end Board
  - TDS[3] ASIC: strip charge, pad trigger, BCR sampling
    [3] Trigger Data Serializer ASIC prepares and serializes trigger data and performs pad-strip matching for sTGC trigger purposes
  - GBTx[4]: elink (up to 320 Mbps) data sampling phase
    [4] Gigabit transceiver for the transmission of readout, TTC and slow control data between Front-end and Back-end
  - GBT-SCA: slow control data sampling phase
    [5] Slow control ASIC for the configuration of Front-end ASICs and the environmental monitoring of Front-end electronics
- Complicated calibration procedures as many clock/data phases are interconnected.
- Intensive work to develop and validate dedicated calibration methods for future automated calibrations by shifters during LHC inter-fills.

Commission runs: Highlights

- Beam splashes from LHC (7 May 2022)

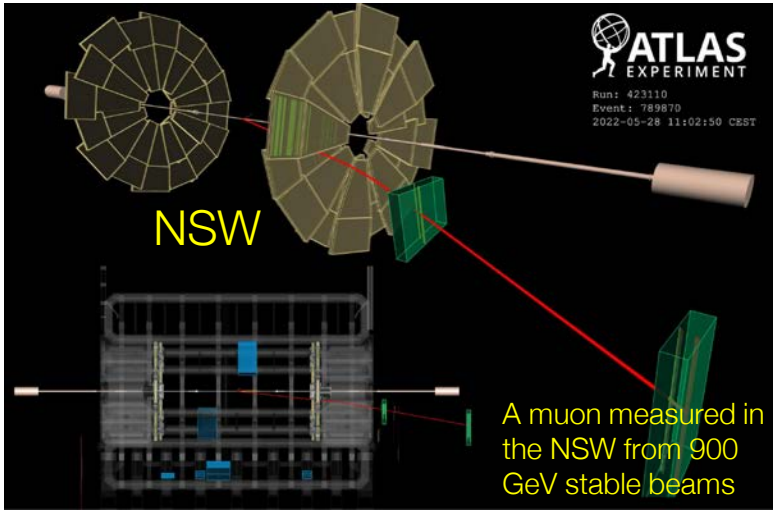


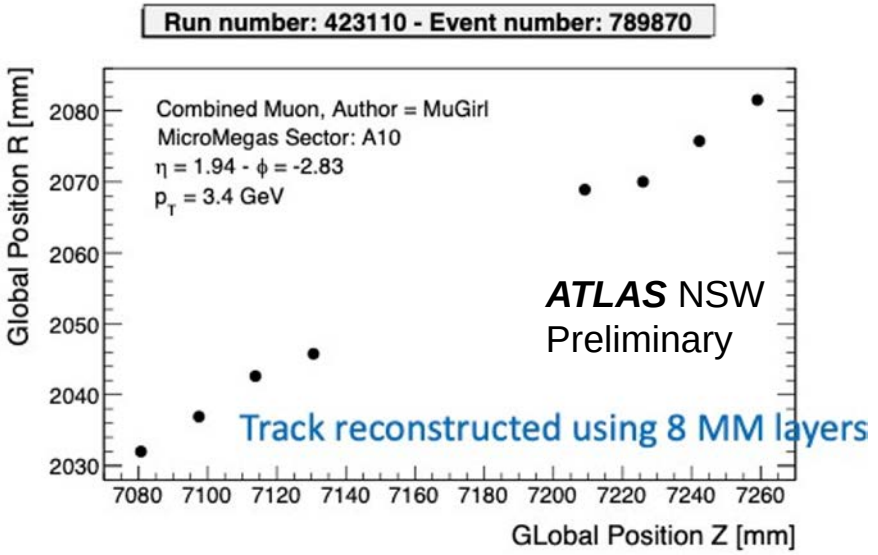
MMG hits seen timed-in with ATLAS trigger as the bunch blown up by the LHC collimator



Staggering BCID window along radius

- 900 GeV stable beam collisions (28 May 2022)



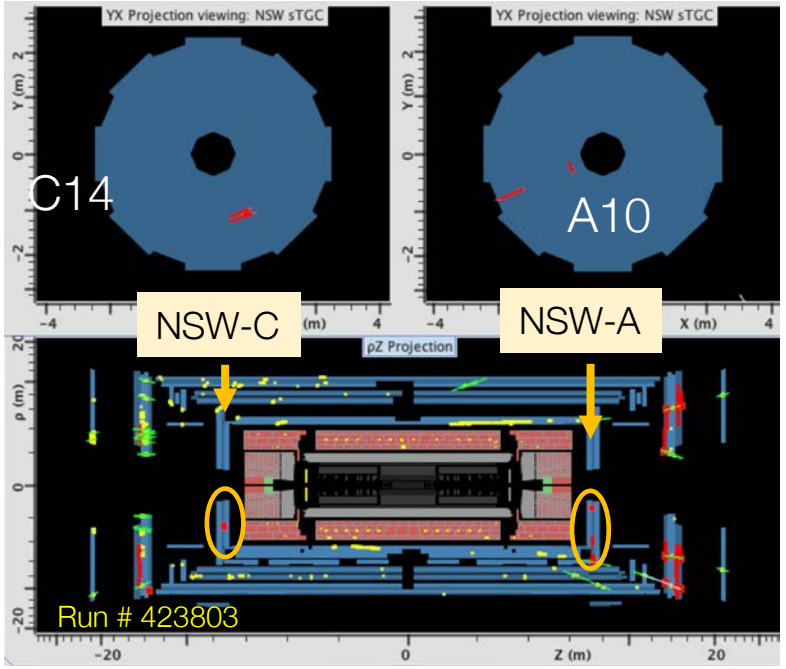


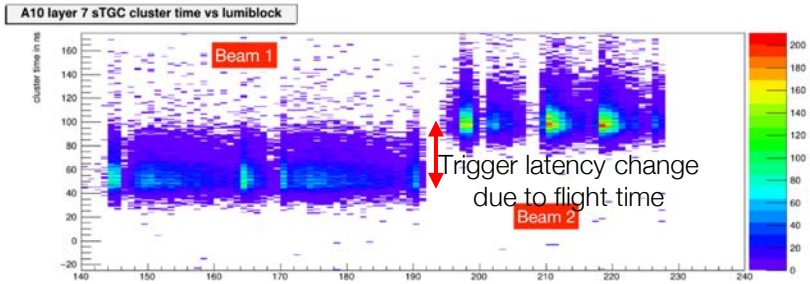
Special run: Horizontal Muon Beam

- Horizontal muon beam for ATLAS TileCalo calibration on 2 June: scraping off bunches from both LHC beam 1&2 with TCT collimators
- Five NSW sectors joined the ATLAS combined run.
- sTGC sectors configured with conservative threshold and staggering BCID offsets per layer -- only one layer timed-in.
- Smooth data taking for sTGC up to 2kHz trigger rate and first time sTGC hits seen in the ATLAS even display!
- MM A10 registered nice segments before Felix buffer issues kicked in.

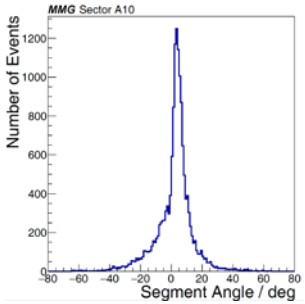
Horizontal muon run trigger from far-side TGC

First sTGC hits seen in the ATLAS event display!





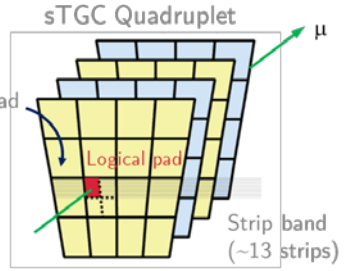
sTGC strip cluster timing vs Luminosity block



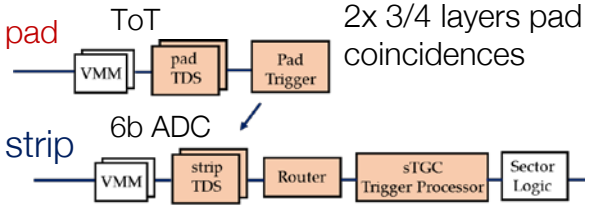
MM segments angular distribution

NSW Trigger Commissioning: sTGC

- Concept for sTGC participating Level-1 Trigger: pad coincidences (at NSW rim and on Pad Trigger Board) to define a smaller region of interest and select fast charge information from a band of strips for centroid reconstruction.

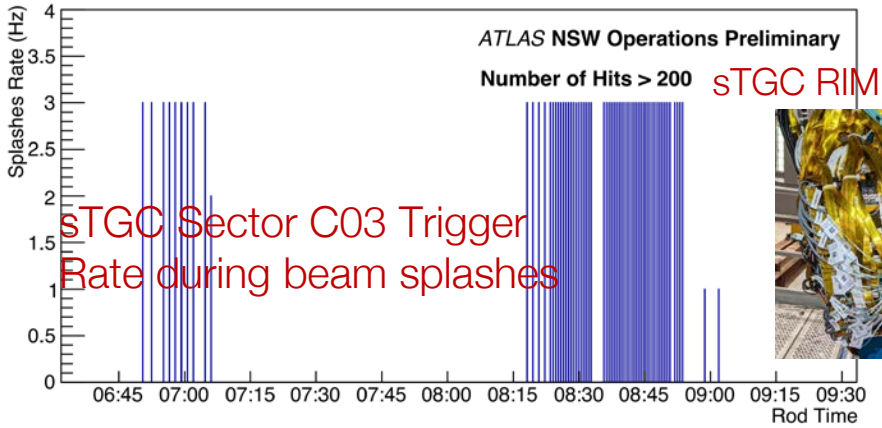


sTGC Trigger Path



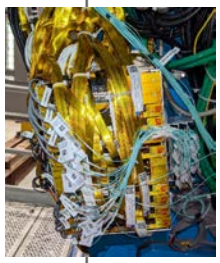
TDS: trigger data serialize ASIC for trigger data preparation, strip-pad match

- NSW-C sTGC successfully took data in self-trigger mode with 2x 3/4 pad coincidences during the LHC beam splashes run.



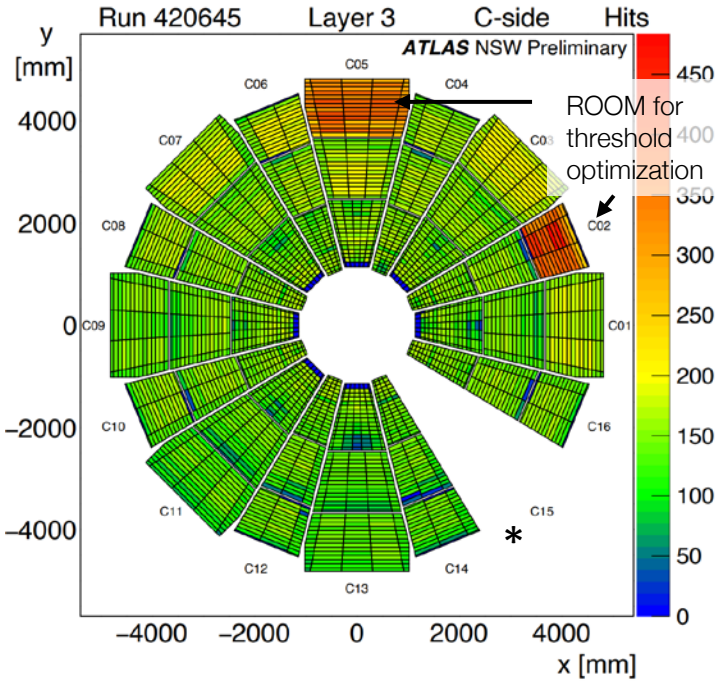
sTGC Sector C03 Trigger Rate during beam splashes

sTGC RIM electronics



- Complete testing and validation of the full chain including pad-strip matching ongoing

Pad trigger occupancy during splashes



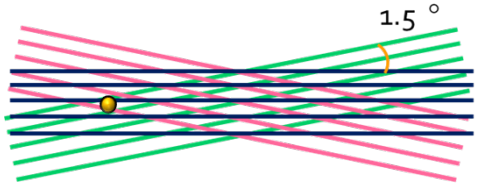
* Disabled due to pending cooling intervention

NSW Trigger Commissioning: MMG

- Concept for MMG participating Level-1 Trigger: reconstruct slopes pointing to IP based on addresses of earliest threshold-crossing strips among multiple layers.

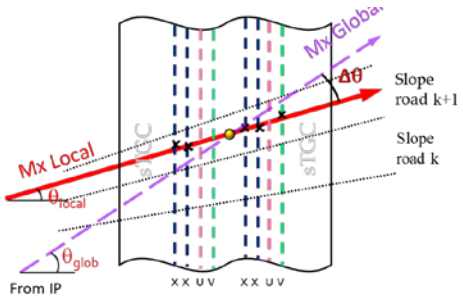
Muon bending direction

MMG Strip pattern

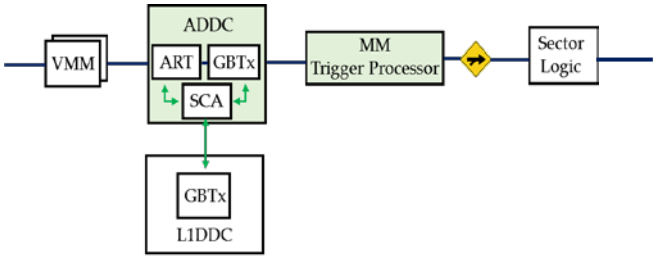


x: horizontal strip (2 plans per quad.)
u,v: stereo strip (1 each per quad.)

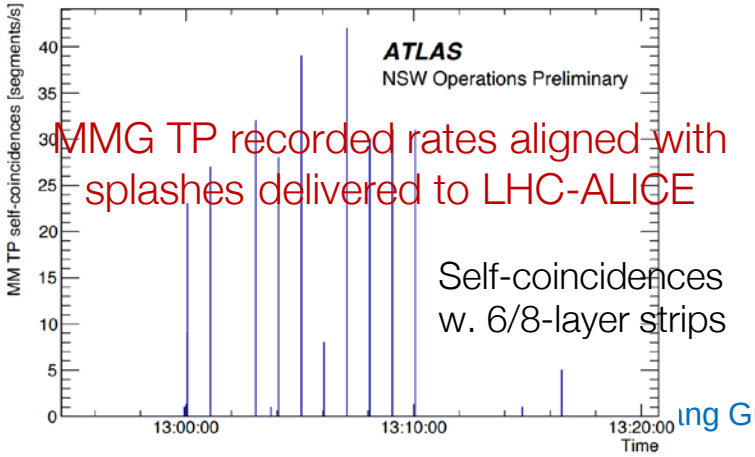
MMG Trigger Algorithm



MMG Trigger Path



- Progress-1: One sector joined the beam splash run and Trigger Processor (TP) successfully reconstructed trigger candidates.

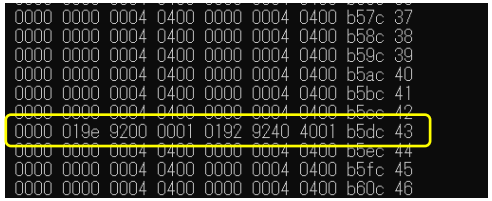


MMG TP recorded rates aligned with splashes delivered to LHC-ALICE

Self-coincidences w. 6/8-layer strips

- Progress-2: Success full trigger chain integration with End-cap Level-1 high-level trigger electronics (Sector Logic board).

End-cap SL observed segments from MMTP with pulsed pattern from Front-end electronics

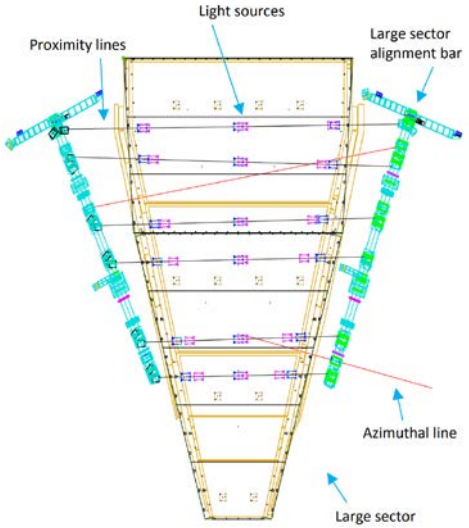


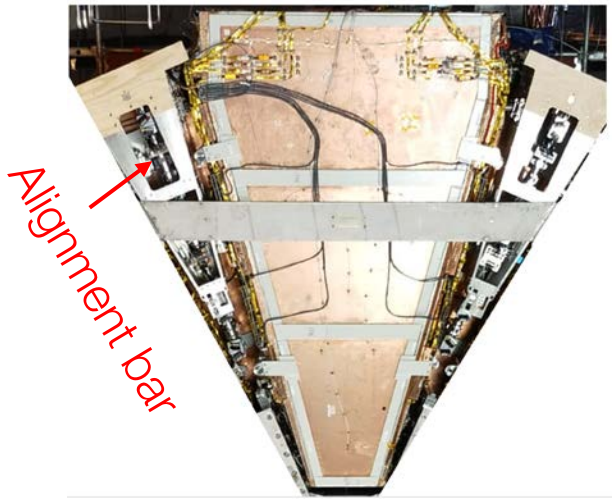
- Segment merging and global synchronization integration with sTGC TP ongoing.

NSW Alignment

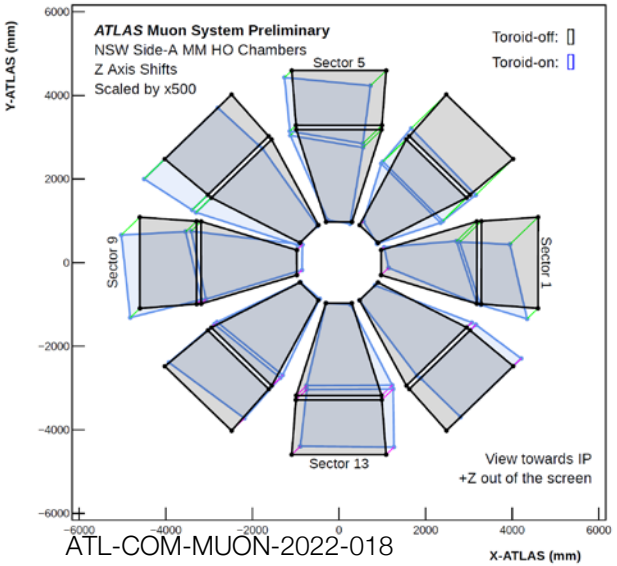
- An optical based alignment system installed and commissioned for tracking the movement, deformation of the NSW detectors.

Alignment system for an NSW large sector





Example of NSW MMG Z shifts measured by the alignment system



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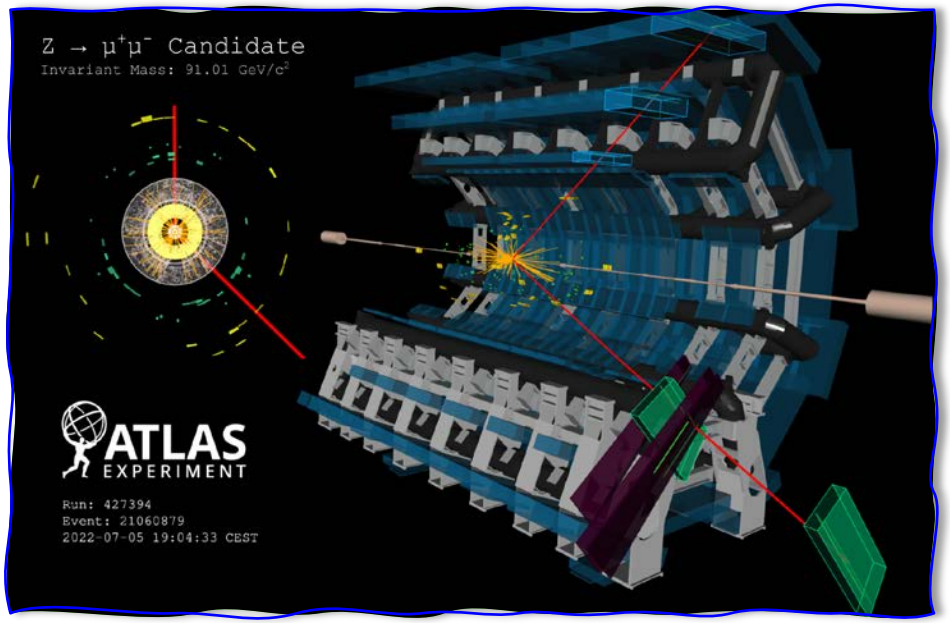
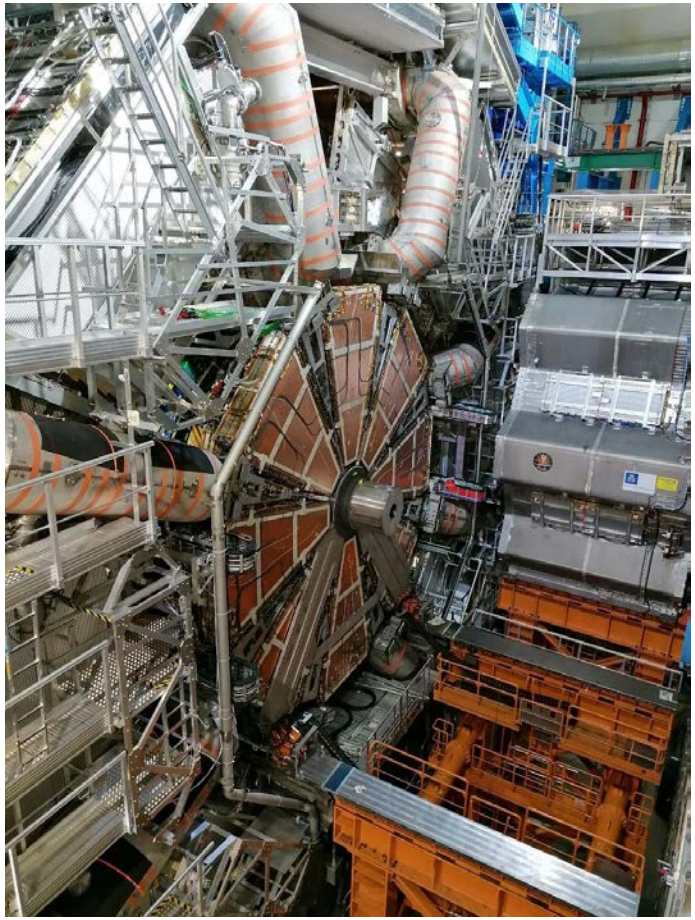
- NSW alignment well integrated with the rest End-cap alignment system. Routine production of stable detector position results.
- Detailed studies will follow to understand the detector movement and NSW alignment performance with offline tracks.

Conclusions

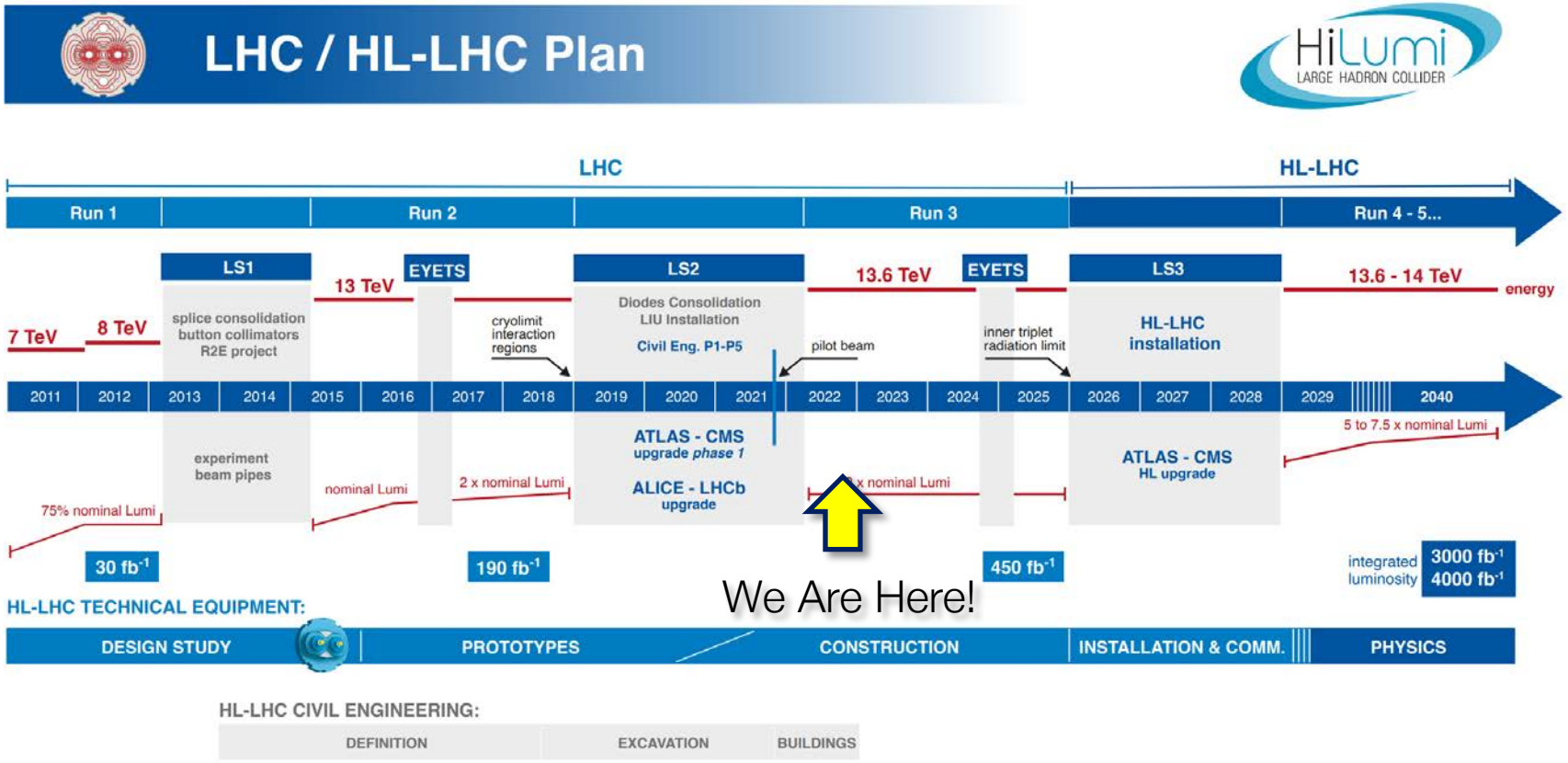
- The New Small Wheel upgrade: largest ATLAS phase-I upgrade project. It aims at improving Level-1 muon trigger and tracking in the ATLAS forward region towards HL-LHC runs.
- NSW with two innovative sub-detectors, Micromegas (MMG) and small-strip Thin Gap Chambers (sTGC) fully commissioned and installed in the ATLAS cavern: Milestone for ATLAS during LHC Long Shutdown 2.
- Intense and continuous efforts to integrate NSW into ATLAS DAQ and time-in NSW detectors.
- Trigger integration made good progresses and activities expected to be staged and continued in parallel with ATLAS data-taking.
- ATLAS Run-3 data taking officially started on 5th July with NSW!



Backup

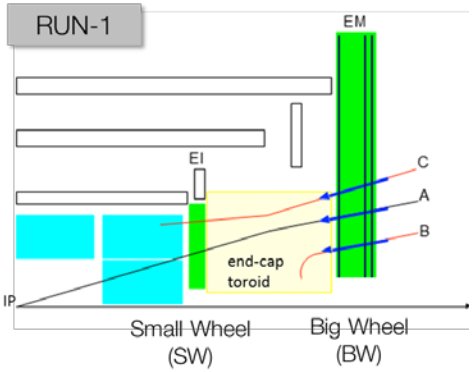


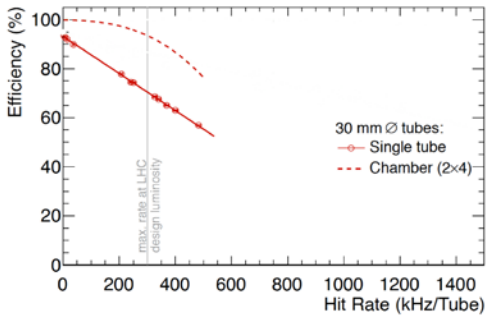
Backup: HL-LHC Schedule



Backup: NSW Trigger and Rates

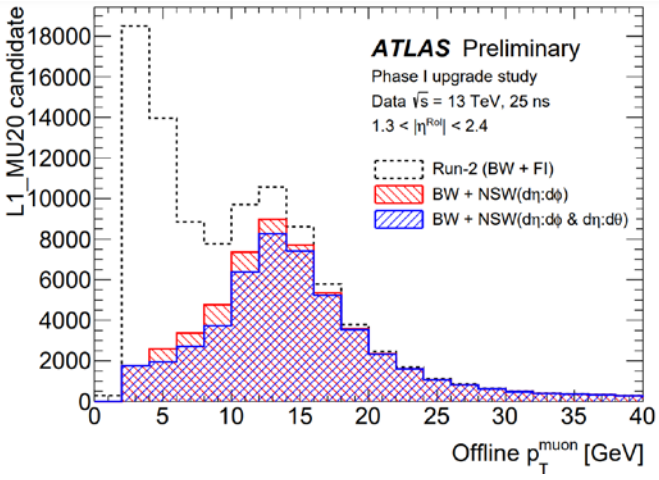
- RUN-1 ATLAS Level-1 Muon Trigger in the End-cap region relied solely on segment measurements at the Big Wheel using Thin Gap Chambers.

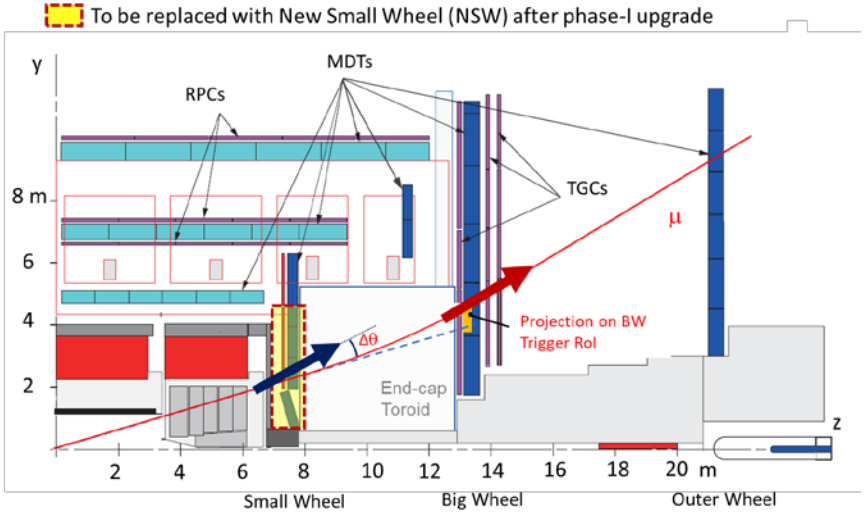




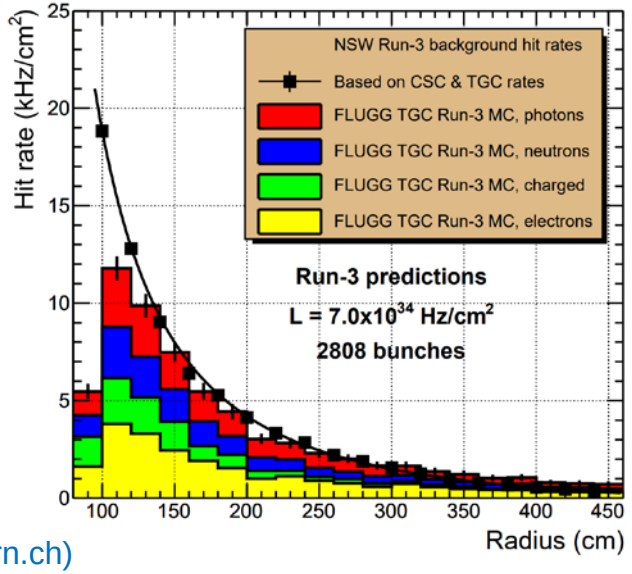
MDT efficiency vs. hit rate

Expected low p_T fake rejection with NSW





Simulated NSW rate at HL-LHC runs



Backup: NSW Impact on Physics

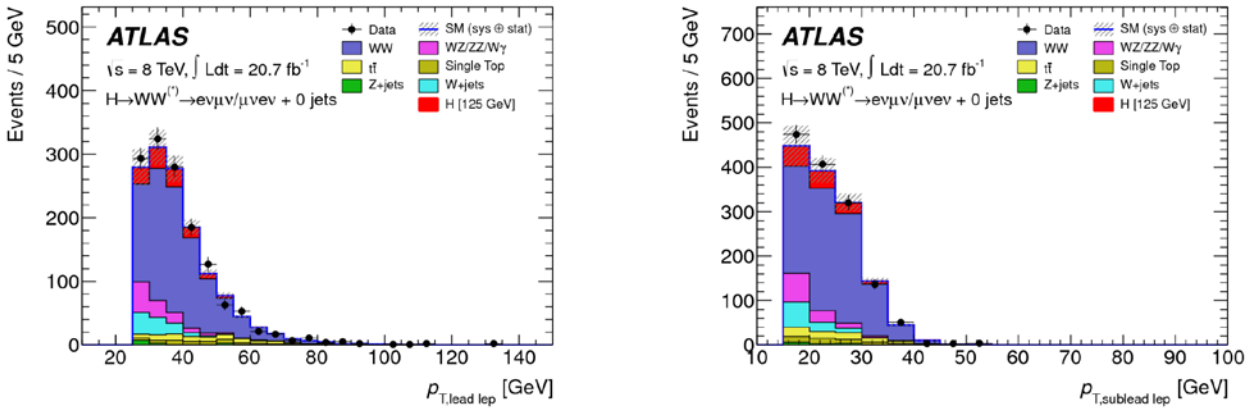


Figure 1.3: p_{T} of the leading (left) and the next to leading (right) leptons, in the candidate events for the $H \to WW^* \to \ell\nu\ell\nu$ channel. The Higgs signal is indicated by the red histogram.

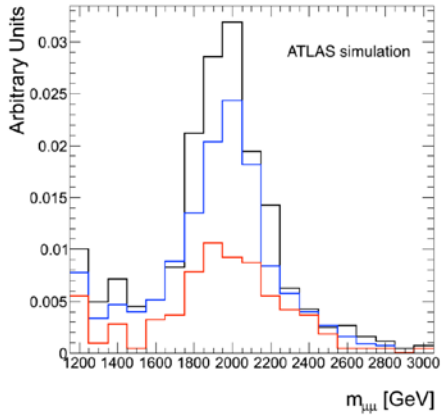


Figure 1.7: Reconstructed $\mu\mu$ mass in the simulated $Z' \to \mu\mu$ events with three different levels of background realized by the data overlay technique. The black, blue and red histograms correspond to luminosity of 0.3, 3 and $5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ respectively.

CERN-LHCC-2013-006;
ATLAS-TDR-020

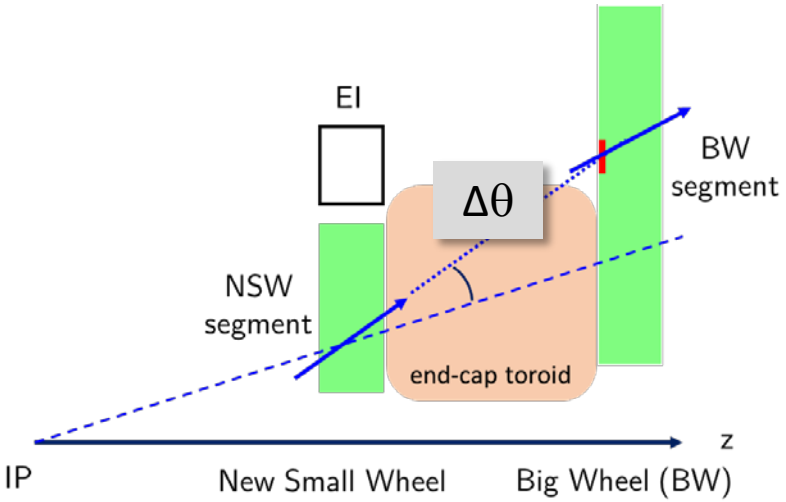
Backup: NSW Trigger Primitives

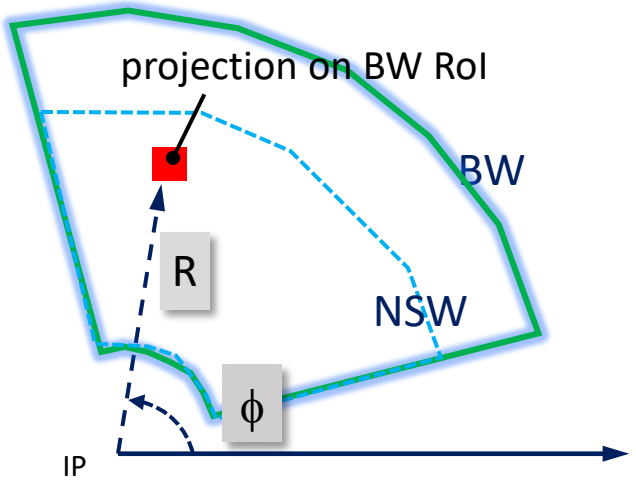
Segment pointing

Projection on BW RoI

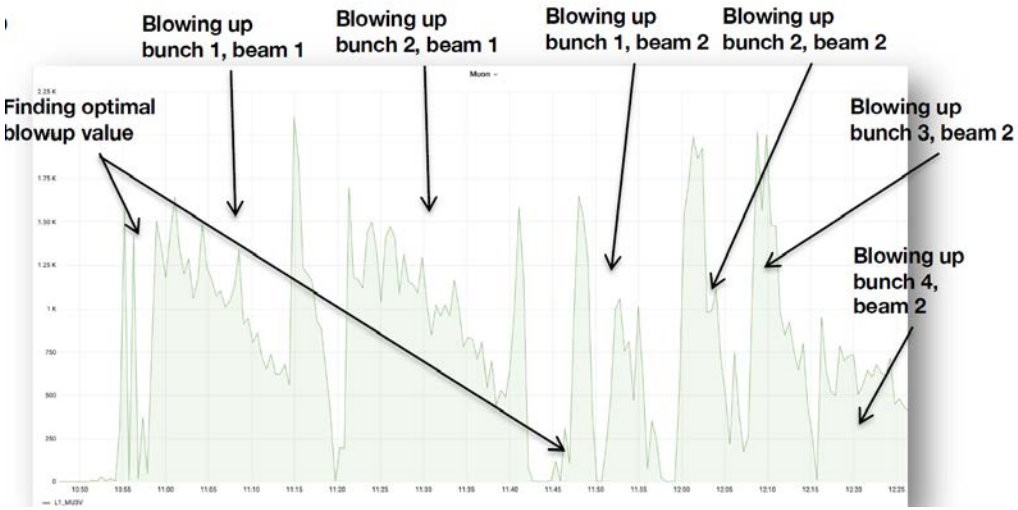
Data format for 1 segment

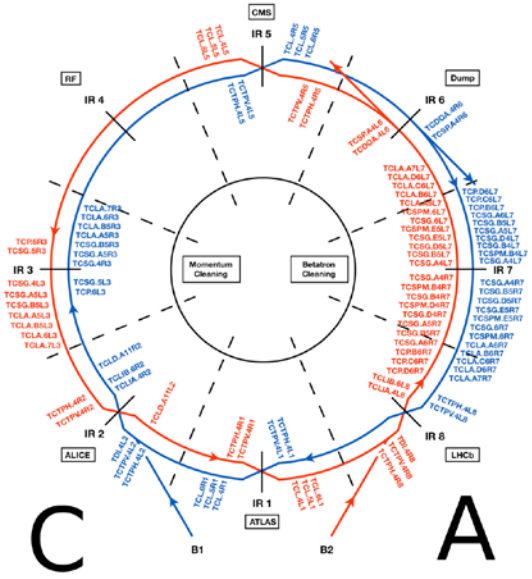
Field	sTGC hit	MM hit	Δθ (mrad)	ϕ index	R index	Spare
#. of bits	2	2	5	6	8	1
Resolution:			1 mrad	20 mrad	0.005 (η)	

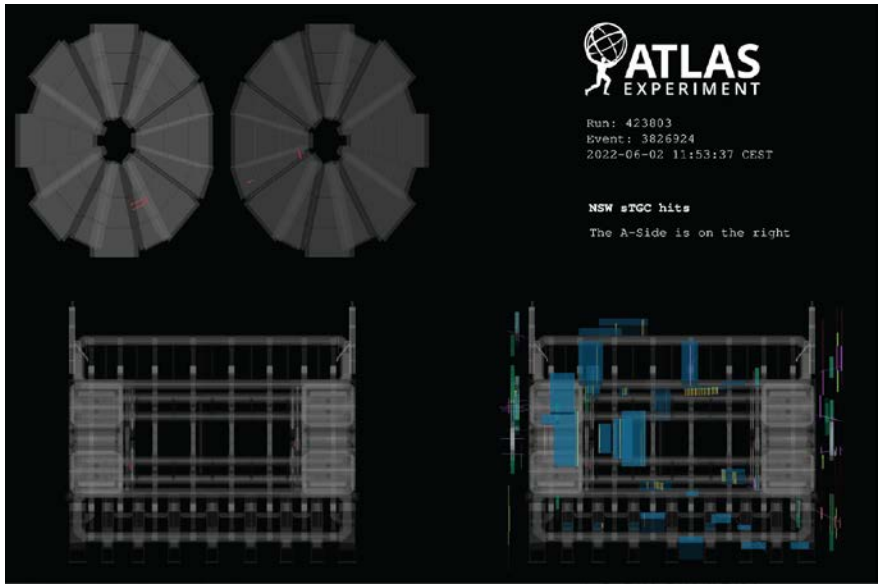


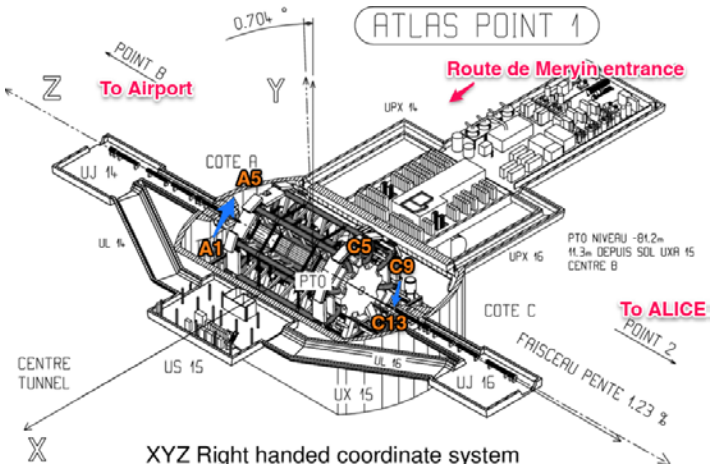


Backup: Horizontal muon beam

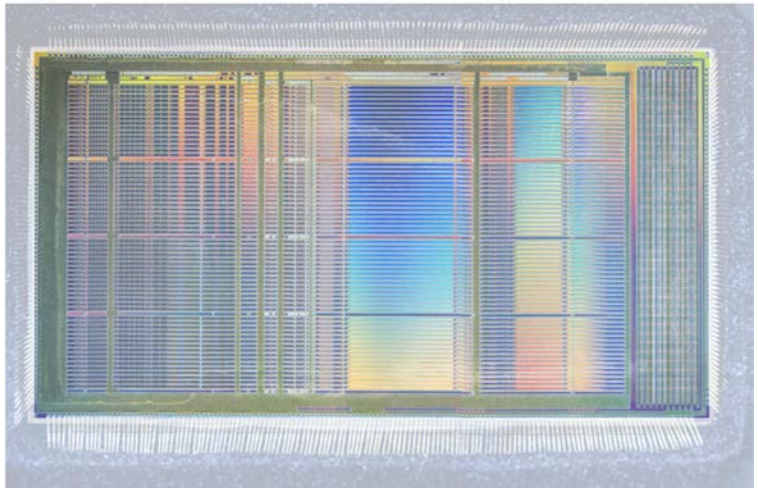


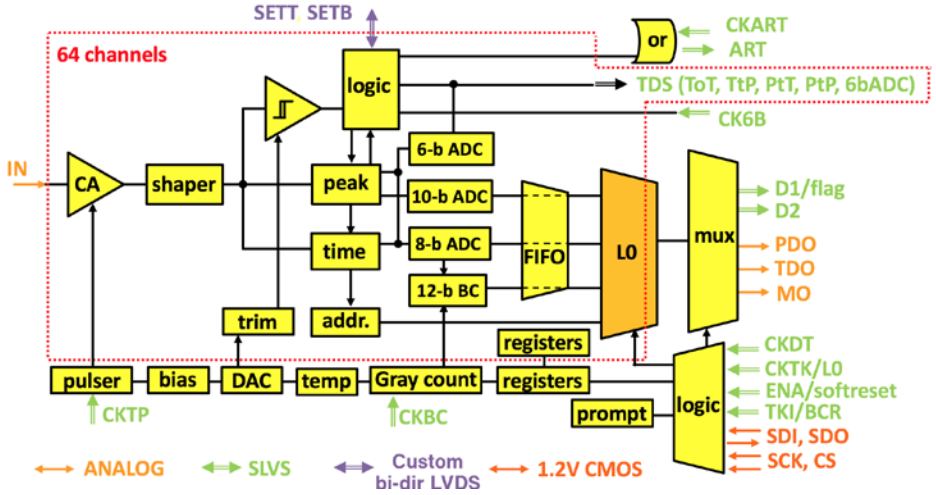






Backup: VMM3a ASIC

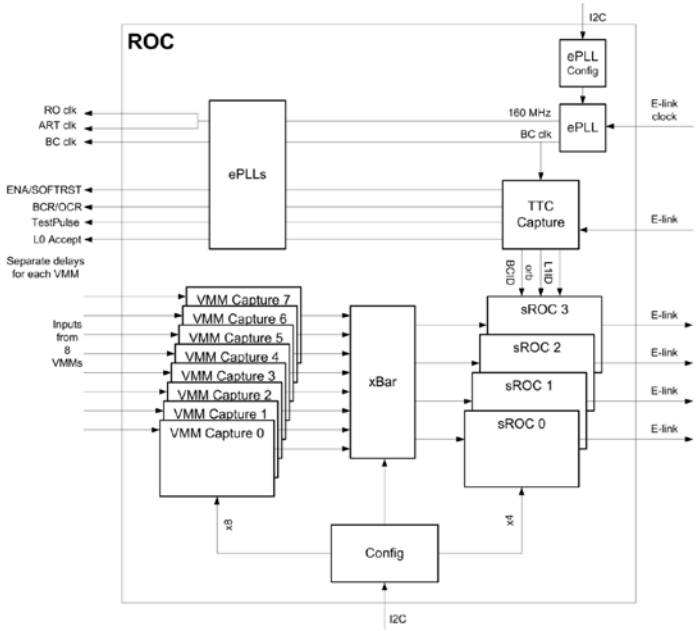




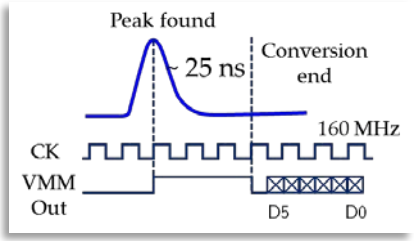
- 64 channels. 130nm CMOS
- Selectable sensitivity (0.5-16mV/fC)and peaking time (25-200ns)
- Three ADCs per channel
- Direct output per channel for triggering:
  - 6b ADC
  - Timing pulses: ToT, Time at peak etc.)
  - Address in real time: output address for first threshold-crossing channel in an event
  - Embedded test pulse, DAC for threshold, charge and timing calibration
  - L0 data buffer and trigger matching logic for ATLAS readout

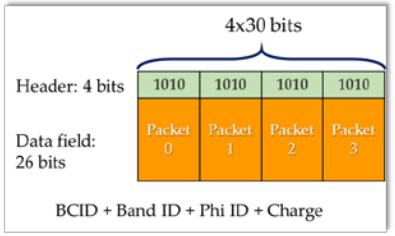
Backup: ROC and TDS, ART ASICs

ROC: Readout Controller ASIC

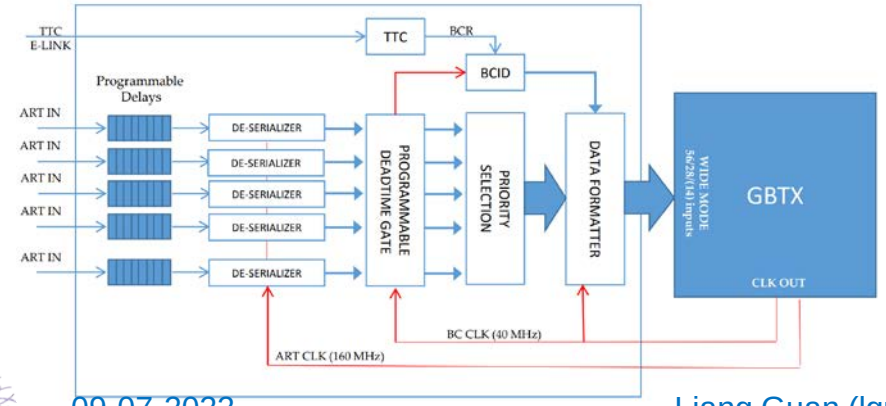


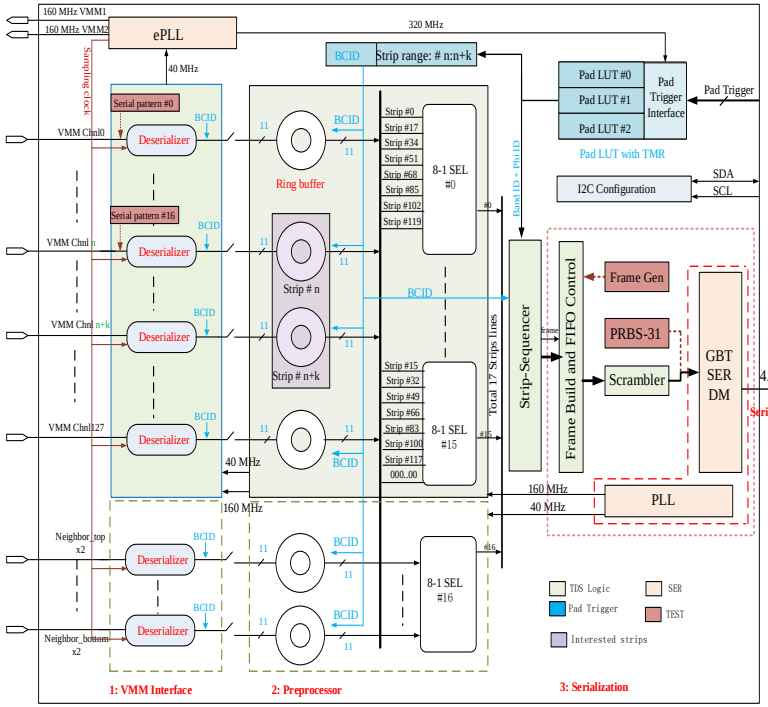
sTGC TDS: Trigger Data Serializer





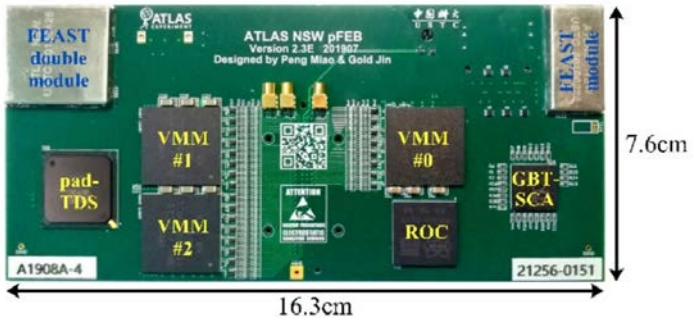
MMG ART: Address in Real Time ASIC



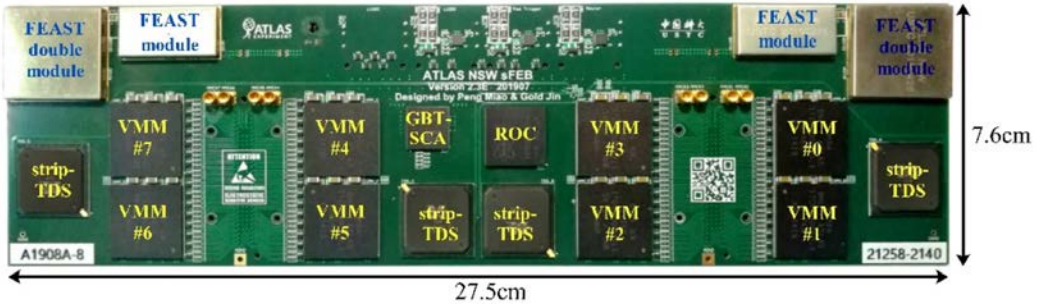


Backup: sTGC Front-end Electronics

pFEB



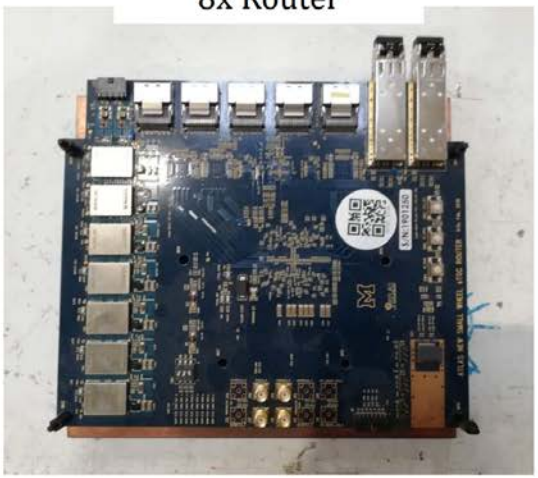
sFEB



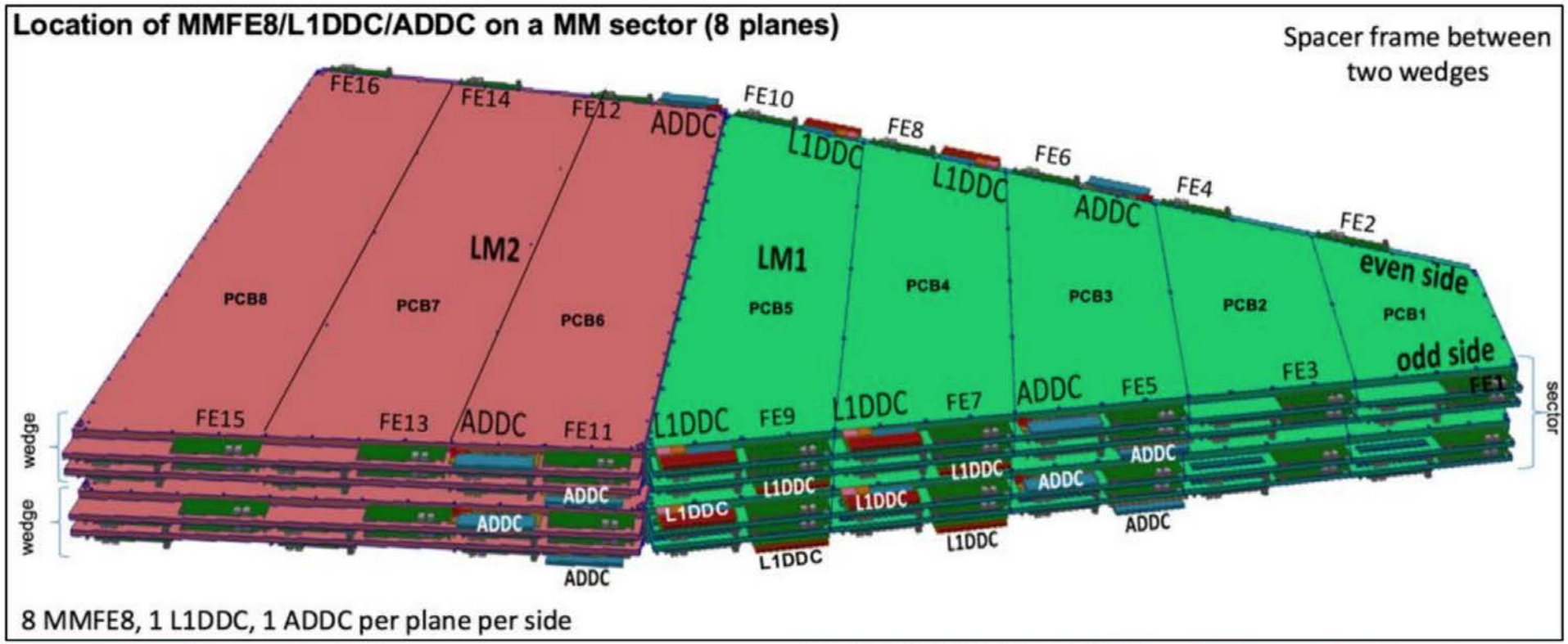
Pad Trigger Board

Rim L1DDC

8x Router

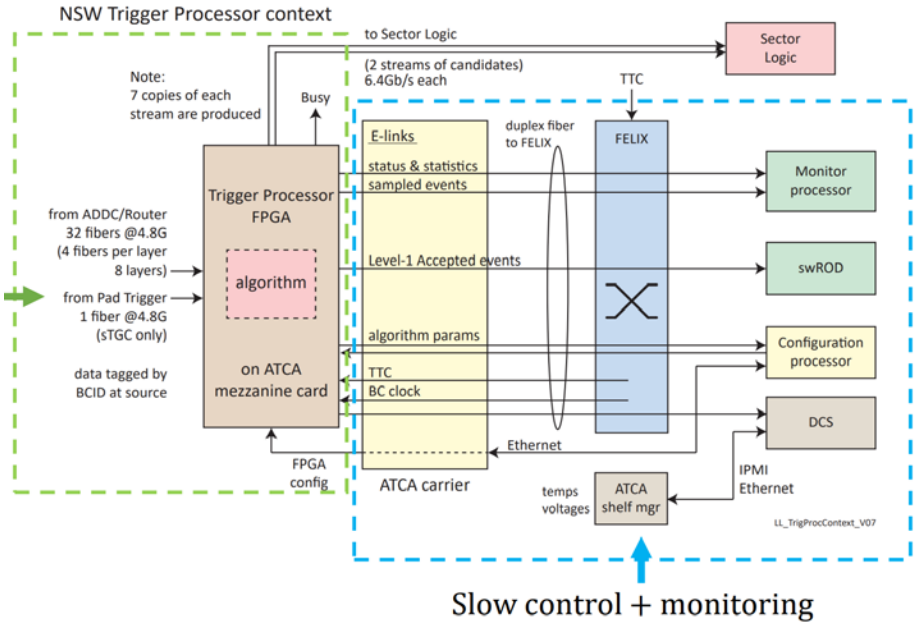


Backup: MMG Front-end Electronics

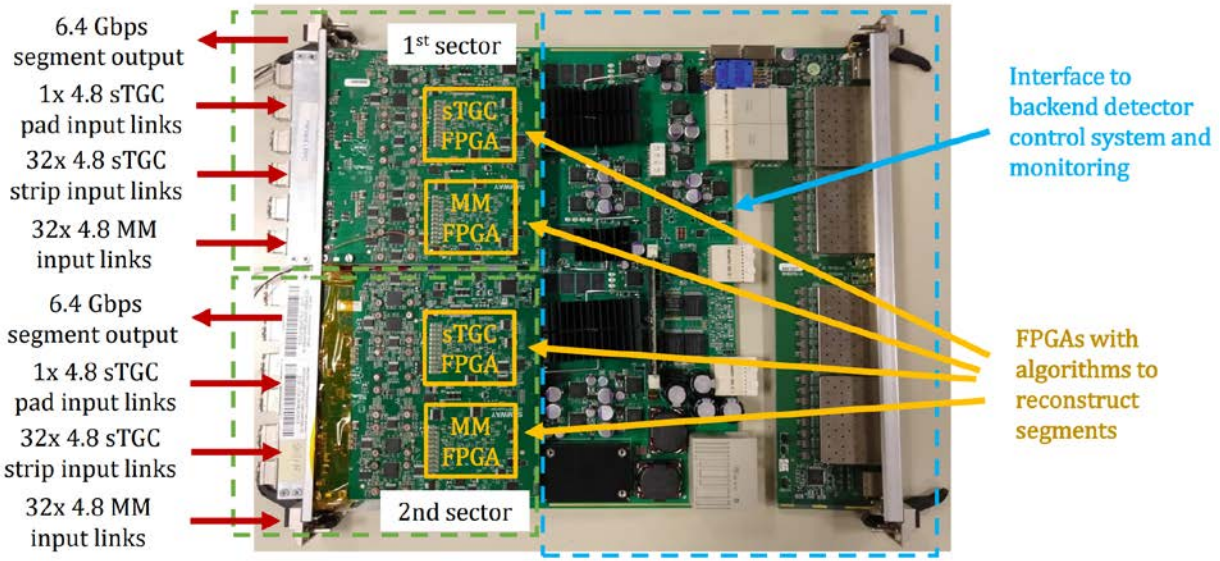


Backup: NSW Trigger Processors

NSW Trigger Processor Firmware Building blocks



NSW Trigger Processor Blade with sTGC and MM TP mezzanine cards and RTM module



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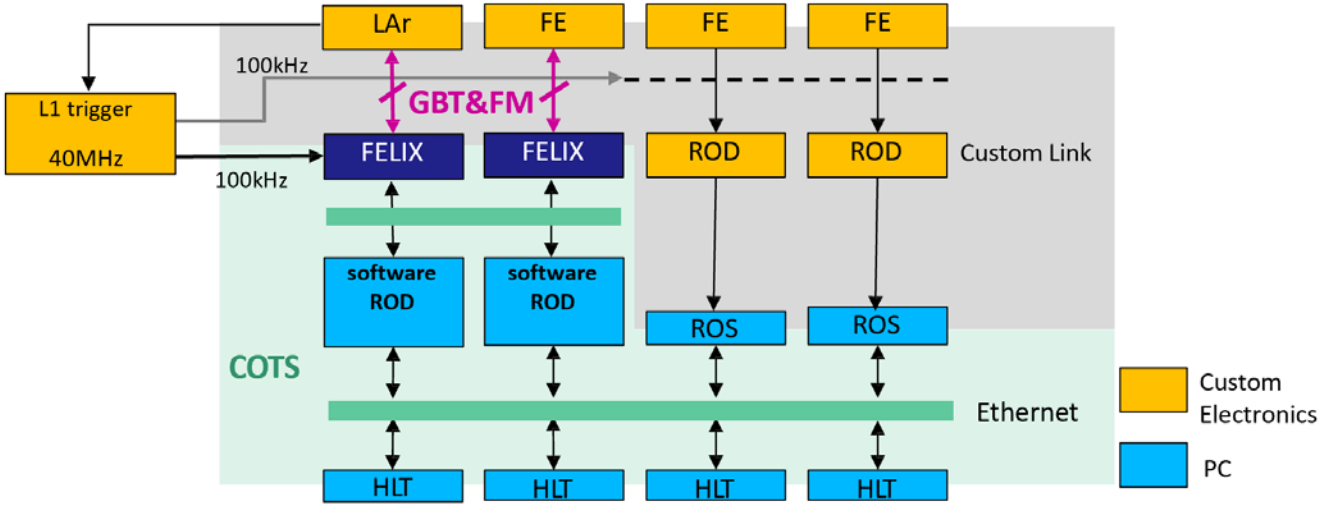
Backup: ATLAS DAQ for RUN-3

ROD : ReadOut Driver,
ROS : ReadOut System,
HLT : High Level Trigger

GBT : synchronous serial protocol at 4.8 Gb/s
FM: 8b/10b RX link at 9.6 Gb/s (Full Mode)

ATLAS DAQ and Level-1 Readout for RUN-3



https://cds.cern.ch/record/2766062