Development of the PreProcessor Modules for the Upgrade of the ATLAS Tile Calorimeter Towards the HL-LHC

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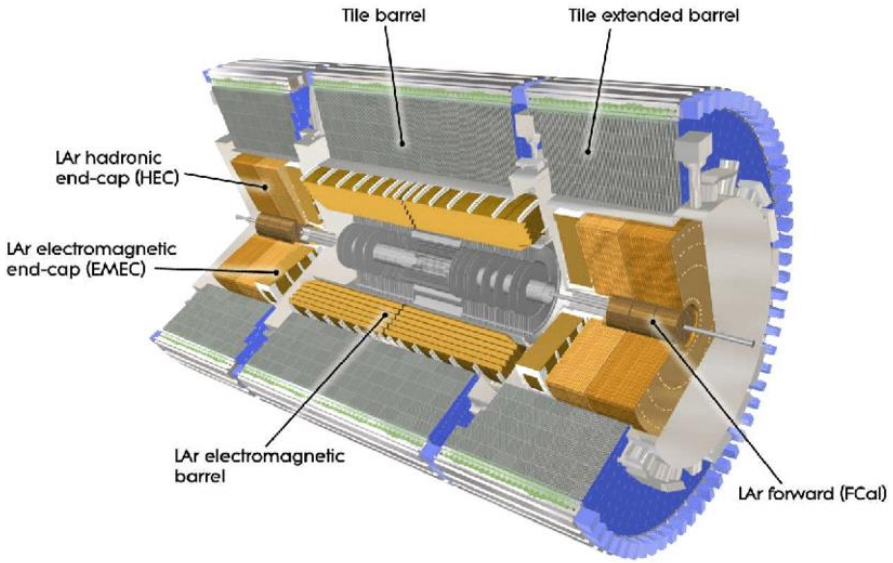
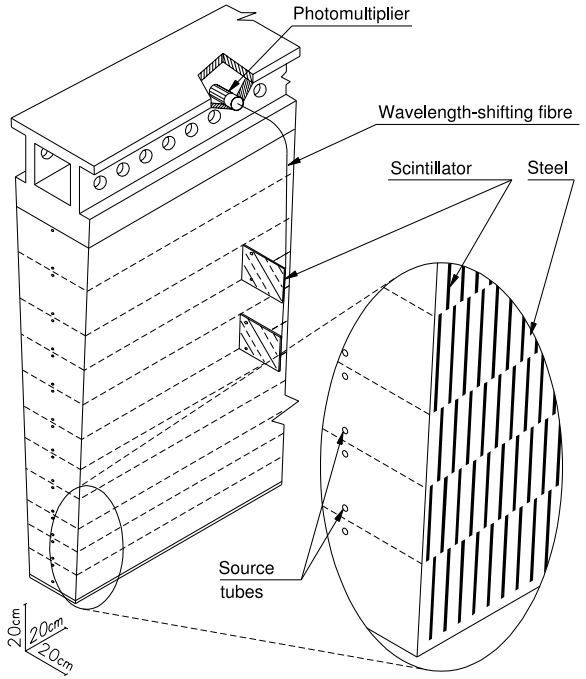
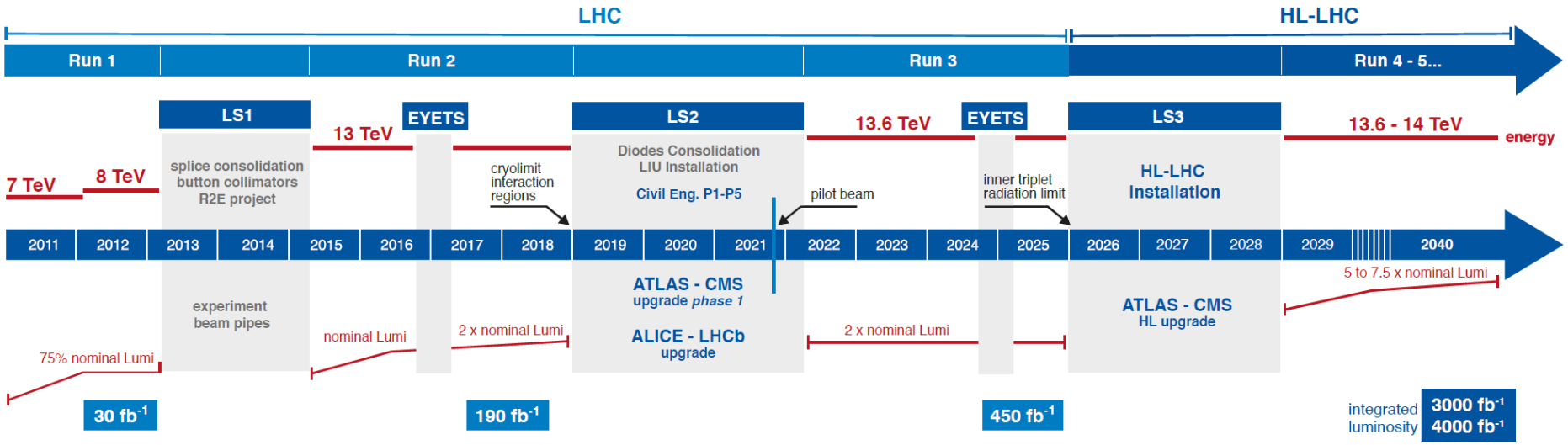
ATLAS Tile Calorimeter





- Central part of the ATLAS hadronic calorimeter
  - Measurement of energies of hadrons, jets, τ-leptons and E_T^{miss}
  - Covering the central region |η|<1.7
- Granularity of Δη × Δφ = 0.1 × 0.1 in most cells
- 4 partitions: EBA, LBA, LBC, EBC
  - Each partition has 64 wedges modules
- Sampling calorimeter made of steel plates and plastic scintillator tiles
  - Wavelength shifting fibers and 2 PhotoMultiplier Tubes (PMTs) per cell
  - Dynamic range from ~10 MeV to ~2 TeV per calorimeter cell
  - About 10,000 PMTs in total

High Luminosity-LHC

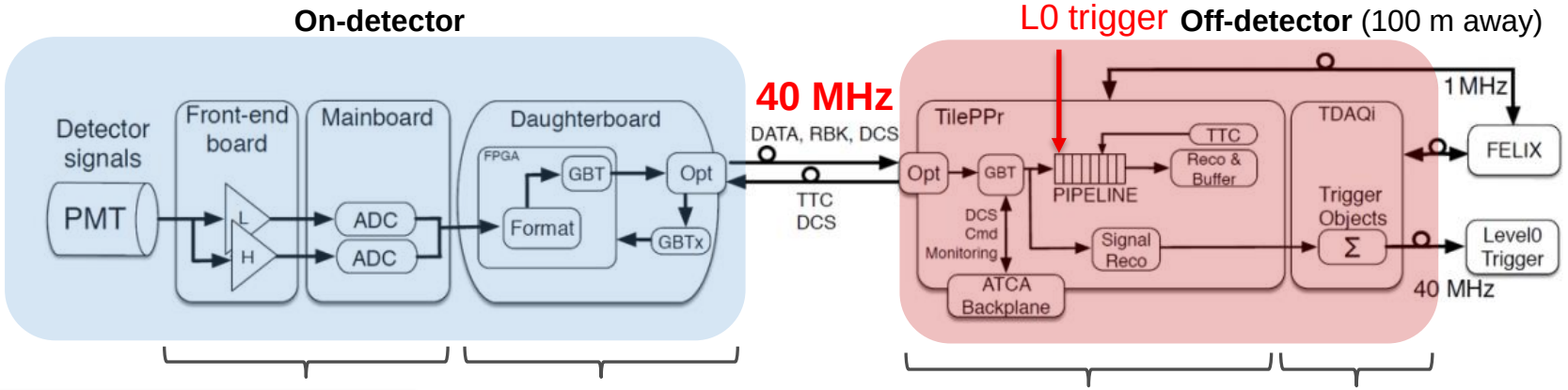


- The High Luminosity-LHC aims to increase the instantaneous luminosity of the current LHC by a factor 5-7 around 2029
  - Expected number of collision will increase up to 200 per bunch crossing
  - New Trigger and Data AcQuisition (TDAQ) architecture with full granularity and digital inputs
- TileCal: Major replacement of on-detector and off-detector readout electronics
  - Aging of electronics due to time and radiation
  - Current readout system will not be compatible with the upgraded TDAQ architecture
  - 10% of the most radiation exposed PMTs will be replaced

TileCal at the HL-LHC

- **New readout and clocking distribution strategy**
  - On-detector electronics will transmit full digital data to the off-electronics at the HL-LHC frequency → **40 Tbps to read out the entire detector and ~6,000 optical fibres**
    - Buffer pipelines are moved to off-detector electronics
    - Maximum readout rate of 1 MHz
  - Redundancy in data links and power distribution
  - Provides digital trigger objects to the ATLAS trigger system at the HL-LHC frequency

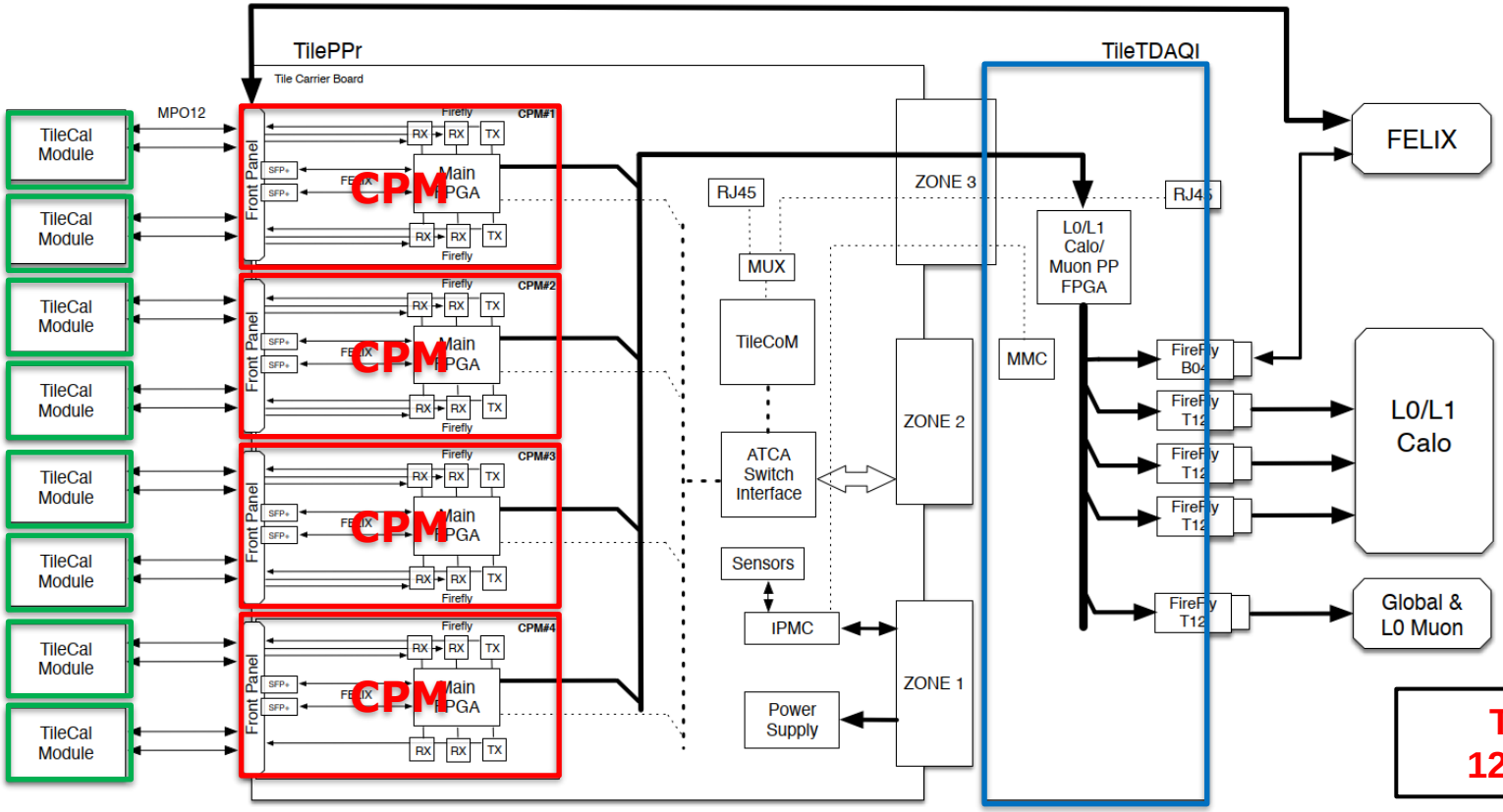
HL-LHC architecture (2029-2040)



-Shaping -Amplification (2 gains) -Digitization -Calibration for electronics	- High-speed communication - Slow control and clock distribution - Data packing	- Data acquisition - Clock distribution - Pipelines buffer - Online energy & time reco	- Trigger objects computation - Interface with ATLAS TDAQ subsystems

TileCal off-detector electronics

- **The Tile PreProcessor is the core element of the off-detector electronics**
  - Data processing, handling, and energy reconstruction per cell
  - Provides the accelerator clock and configuration to the on-detector electronics
  - Interface with the ATLAS trigger and readout systems (FELIX)

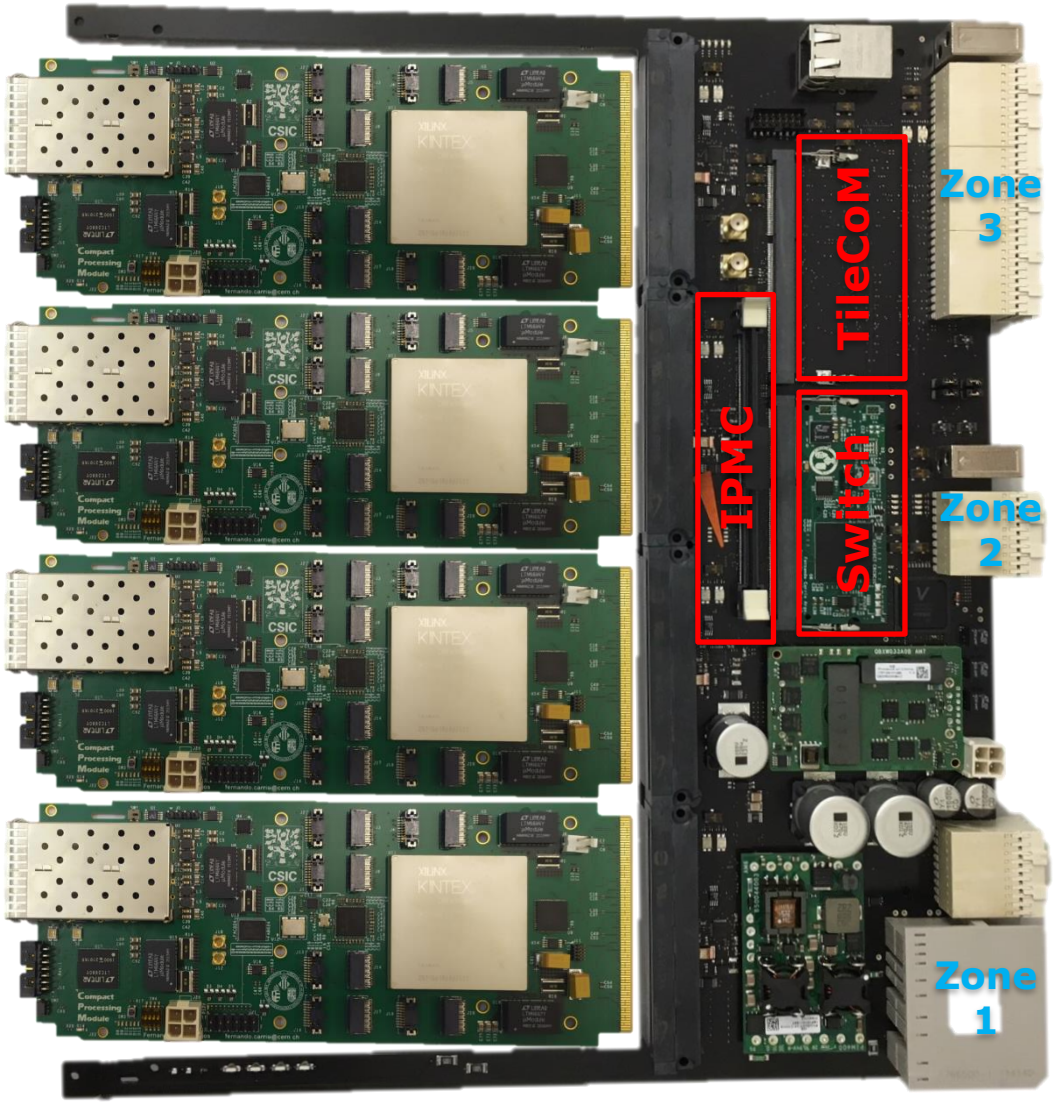


- **32 TilePPr** boards**:** ATCA carrier + 4 Compact Processing Modules
- **32 TileTDAQi:** Interfaces with L0Calo, Global and L0Muon

} 4 ATCA shelves

ATCA Carrier Base Board

- Full-size ATCA blade
  - 14-layer PCB with Megtron 6 material
  - Cutaway version to improve cooling
- Zone 1: Power distribution
  - 4 × CPMs → 240W
  - 1 × TDAQi → 50W
- Zone 2: GbE + XAUI 10G
  - Base & Fabric: Communication with rest of the ecosystem
- Zone 3: High-speed communication path between CPMs and TDAQi
  - 7 links @ 9.6 Gbps per CPM
- Three on-board mezzanines
  - CERN IPMC board
  - TileCoM Zynq-based board
  - 16 GbE port switch module



Carrier Mezzanine Boards

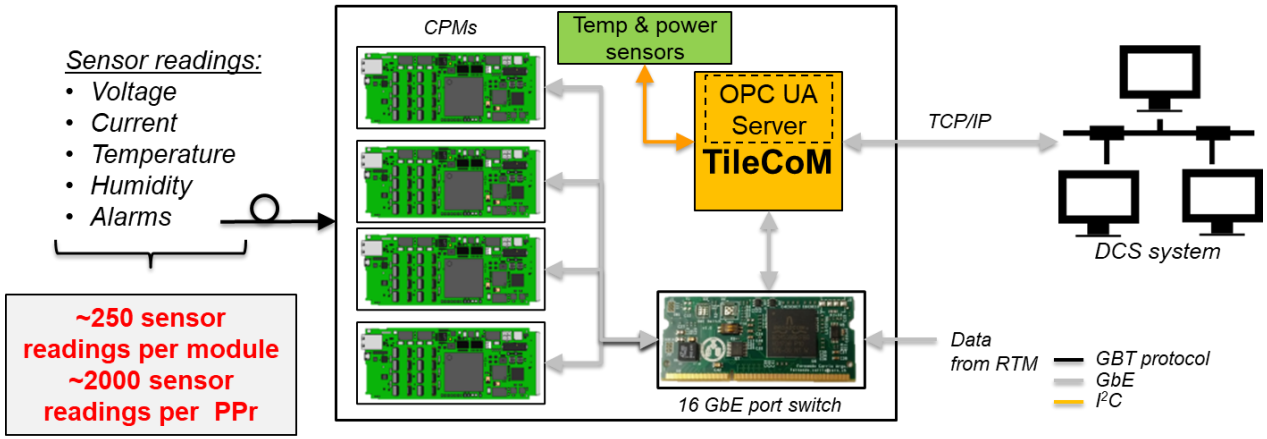
- Mezzanine designs as compact, replaceable and upgradeable solutions

- TileCoM - *Computer on Module*
  - Xilinx Zynq UltraScale+ XCZU2CG + 512 MB DDR4
  - DDR4 SODIMM-240 pin form factor
  - Main functionalities
    - Remote programming of all on-detector and off-detector electronics
    - Interface with the ATLAS TDAQ system for detector configuration
    - OPC servers to provide monitoring data to the ATLAS Detector Control System

TileCoM

- 16 GbE ports switch module
  - Unmanaged Ethernet Switch chip Broadcom BCM5396
  - DDR3 SODIMM-204 pin form factor

GbE Switch

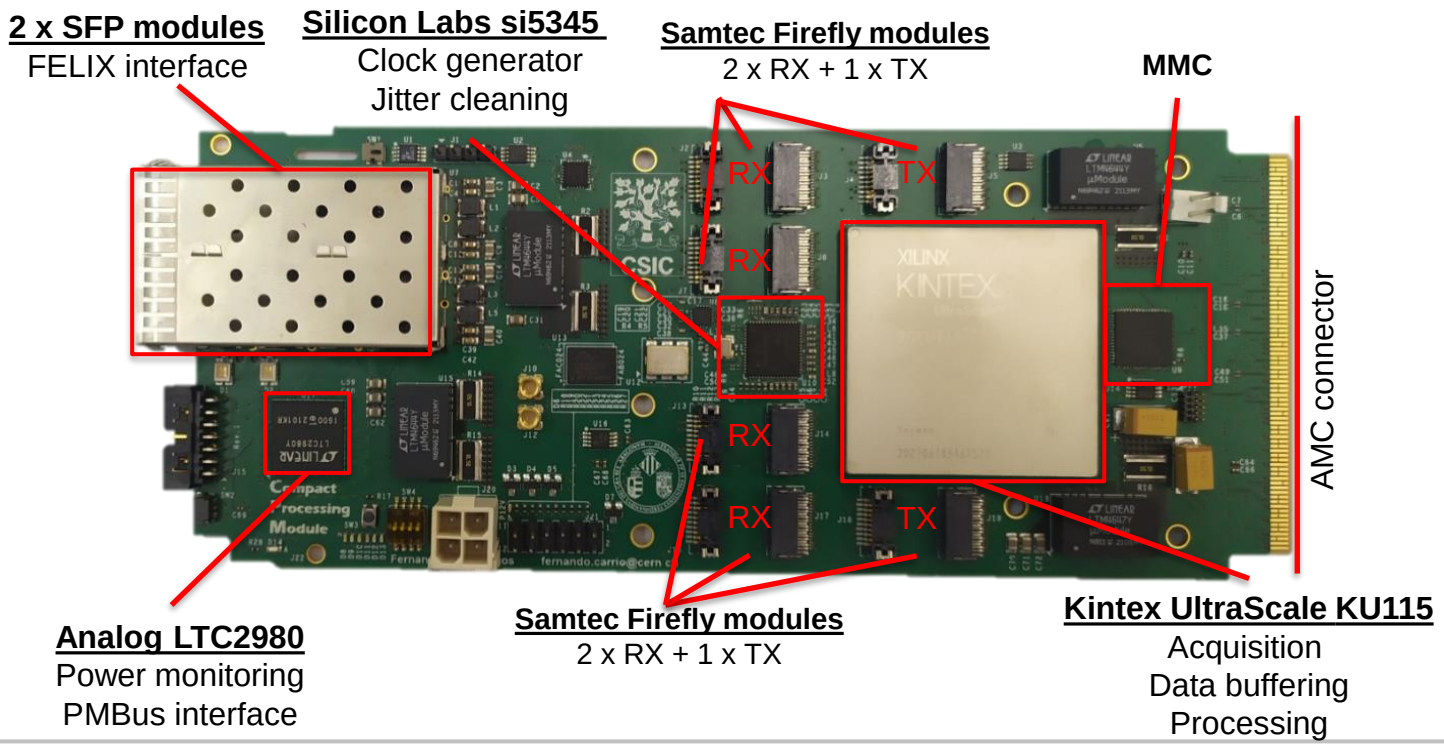


Compact Processing Module version 2

- Readout and operation of 2 TileCal modules (8 per TilePPr)
  - Data handling, buffering, clock distribution, energy reconstruction

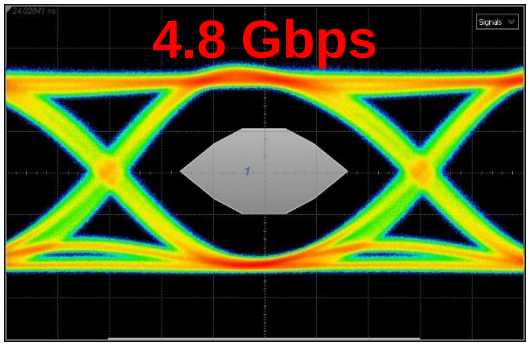
- **Single AMC board** with full-size form factor
  - 6 Samtec Firefly modules (4 RX + 2 TX)
  - 14 channels through AMC connector
  - 2 SFP modules
  - Xilinx Kintex Ultrascale KU115 FPGA

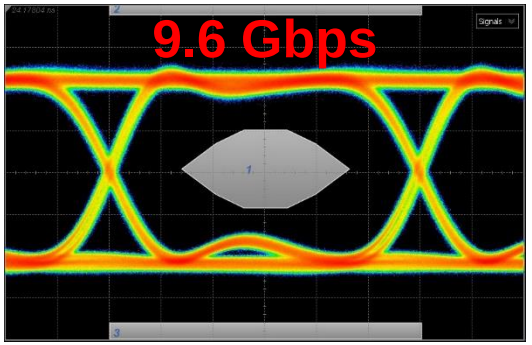
- High bandwidth readout system
  - On-detector readout path
  - TDAQi interface, GbE, CPM-CPM
  - ATLAS readout path (FELIX)

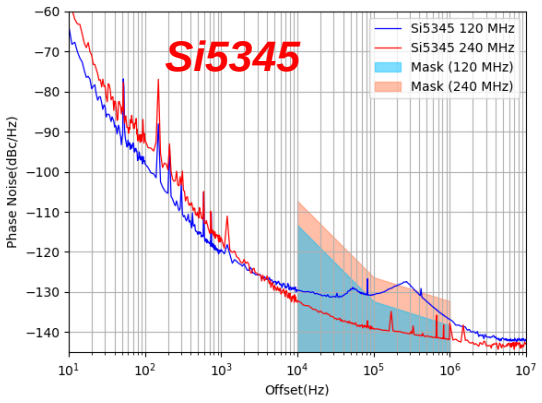


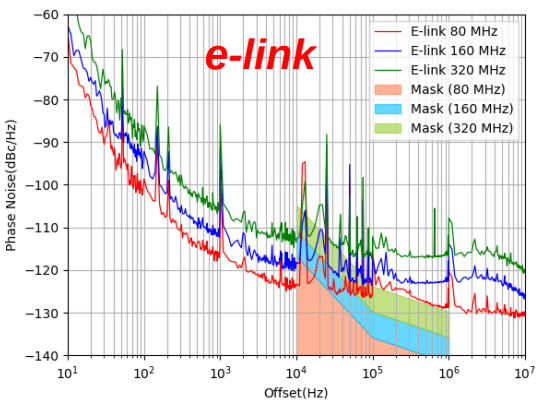
Validation Tests

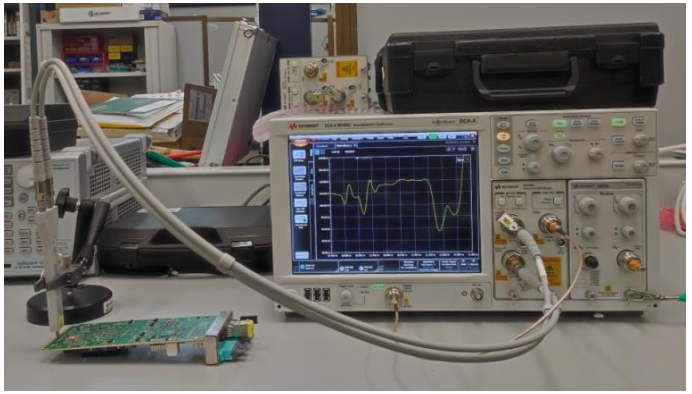
- Low jitter values measured in the on-detector path
  - Samtec Firefly modules @ 4.8 Gbps & 9.6 Gbps
  - Eye diagrams good performance for transmitters and receivers
- Validated clock distribution to the on-detector electronics
  - Measured low phase noise values after the GBTx
    - Sampling clocks distributed to the ADCs
    - Clocks driving the high-speed transceivers in the on-detector FPGAs
- Link stability tests with latest version of the on-detector
  - GigaBit Transceiver protocol at 4.8 Gbps / 9.6 Gbps
  - Operating with fixed and deterministic latency





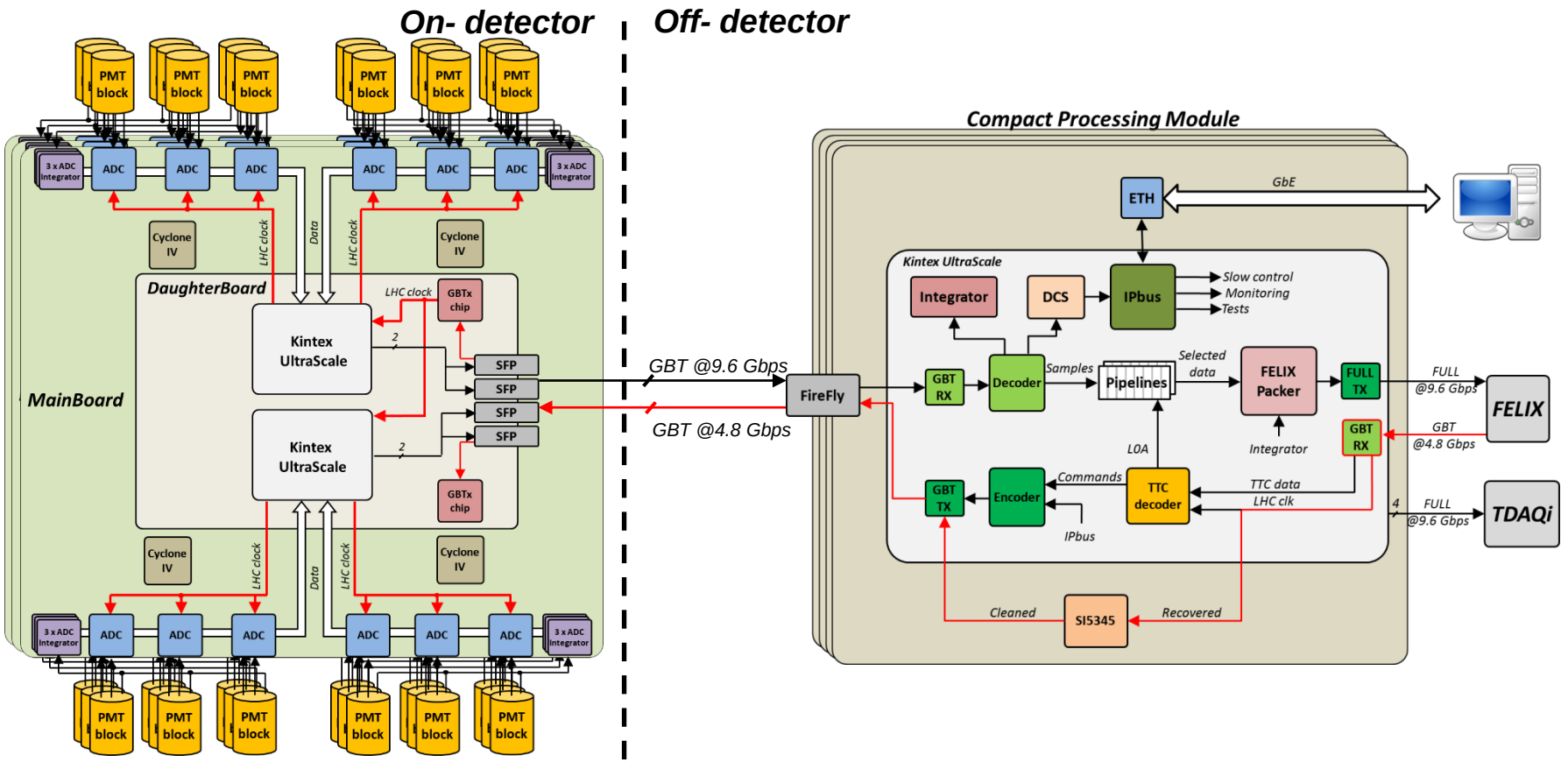






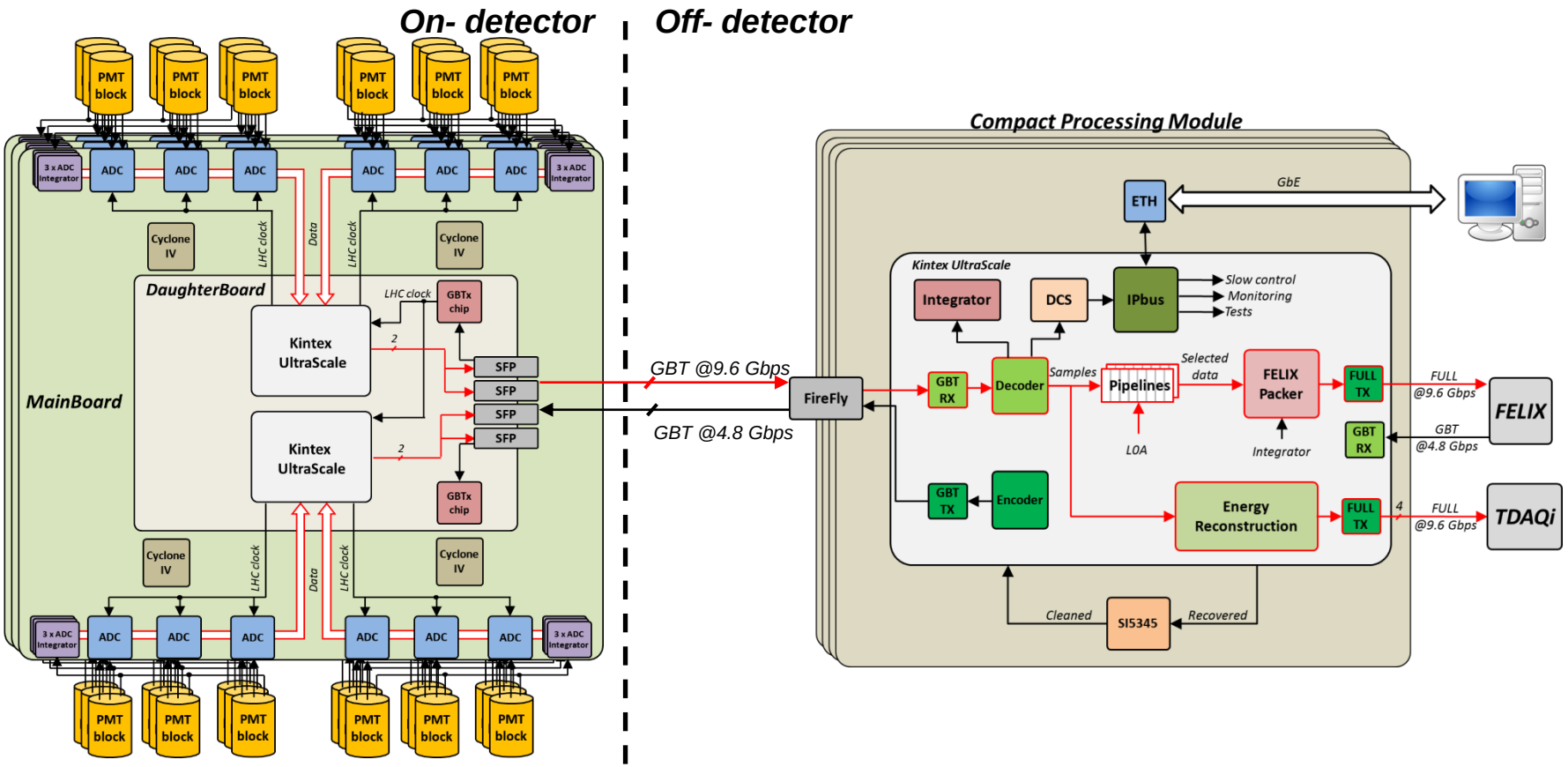
On-detector Readout and Operation

- Links using the GigaBit Transceiver (GBT) protocol from CERN
  - 16 downlinks@4.8 Gbps per CPM: configuration and sampling clock distribution
  - 32 uplinks@9.6 Gbps per CPM: detector data and monitoring with redundancy
  - 1 link from FELIX@4.8 Gbps: clock, configuration commands and trigger acceptance signal (L0A)
- Data buffering of 10 μs per channel until the reception of the L0A



Trigger and DAQ path

- Transmission of Level-0 trigger selected events at a maximum rate of 1 MHz
  - 1 FULL mode link to FELIX (9.6 Gbps)
- Energy reconstruction to TDAQi @40 MHz → generation of trigger objects for the ATLAS trigger system
  - 4 FULL mode links to TDAQi (9.6 Gbps)

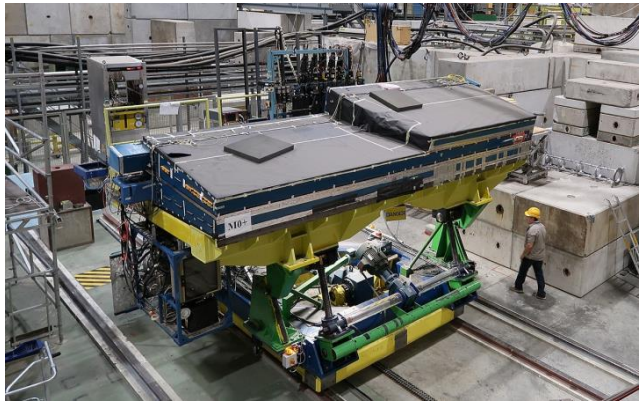


Upcoming System Integration and Production Plans

- Fully integration of the system planned for test beam November 2022
  - Two complete TileCal modules operated with one CPM + ATCA carrier + FELIX system
  - Validation of all the high-speed interfaces at full capacity
    - FELIX interfaces for readout and clock recovery
    - Study link stability with on-detector electronics
    - Analyze and optimize latency in the trigger path
- Complete thermal tests at the end of August at CERN facilities with a PreProcessor and TDAQi
- ***Production plans***
  - Preliminary Design Review passed in 2020
    - Validated first designs of Carrier/CPM (version 1 and 2)
  - Final Design Review in Q3 2022
    - Preproduction (25%) from Q4 2022 to Q2 2023
    - 8 ATCA carriers, 32 CPMs
  - Production Readiness Review in Q4 2023
    - Final production (75%) from Q4 2023 to Q2 2025
    - 24 ATCA carriers, 96 CPMs
  - Installation and commissioning in ATLAS from 2026-2028

PPr ATCA shelf

FELIX system (BNL-712)



TileCal modules @ test beam area

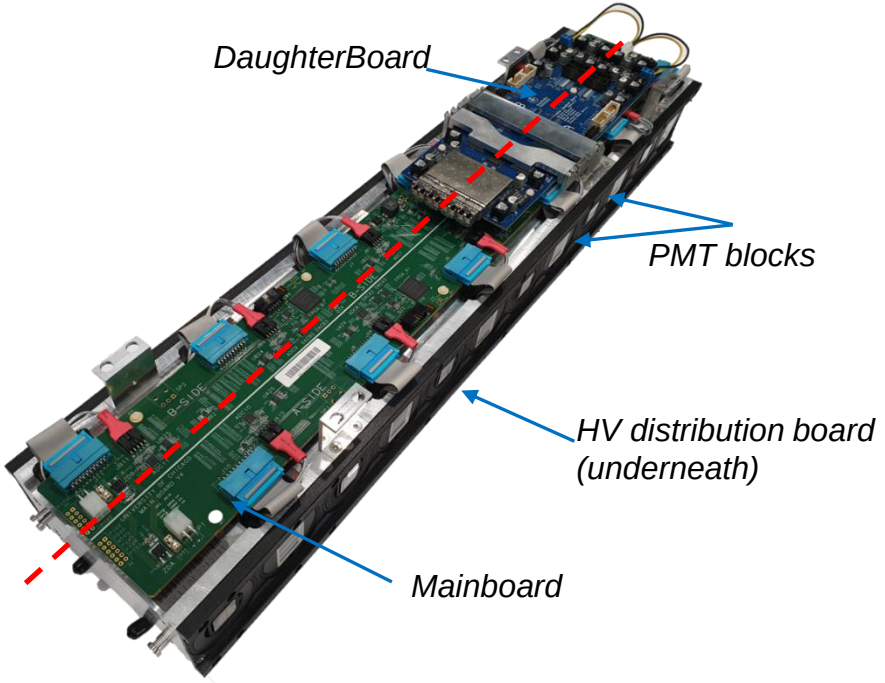
Summary

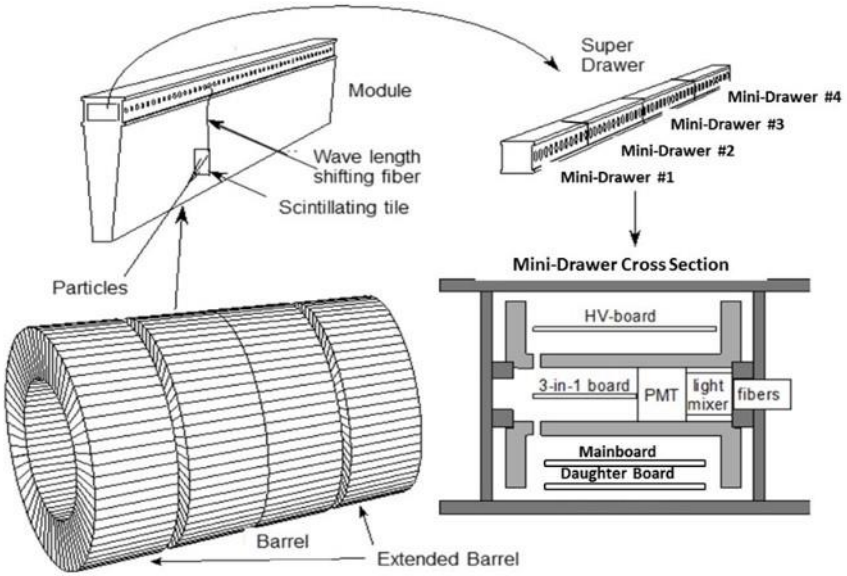
- Complete redesign of the TileCal on-detector and off-detector electronics for the HL-LHC
- The PreProcessor is the core element of the TileCal off-detector electronics
  - Each one composed of 4 Compact Processing Modules + 1 ATCA carrier: capable of operating 8 TileCal modules
    - Clock distribution, readout and control of the on-detector electronics
    - Transmission of triggered detector data to the ATLAS FELIX system
    - Reconstructed cell energy transmission to the TDAQi system
- Development of the final PreProcessors is well advanced
  - Prototypes show a good performance: signal integrity, link stability, low noise clocks
- System integration and validation tests planned for this year
  - Operation of two upgraded modules in the upcoming test beam of November 2022
  - Stress thermal tests to validate the performance under edge conditions
- Preparing towards the final pre/production in 2022/2023 and installation in 2026
  - 32 ATCA carrier and 128 Compact Processing Modules to read out TileCal

THANKS FOR YOUR ATTENTION

Upgraded on-detector electronics

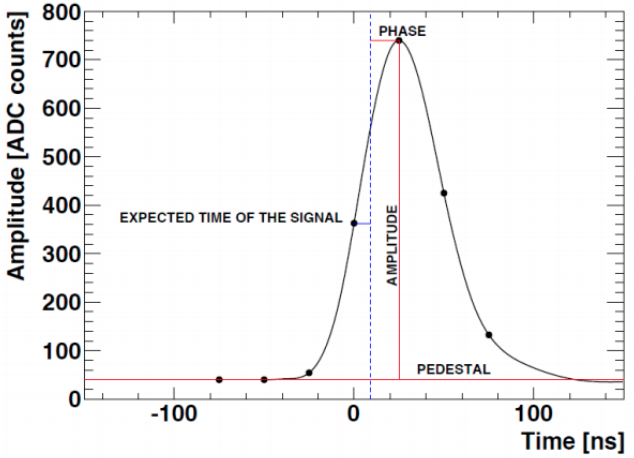
- The Upgraded modules are composed of 4 mini-drawers (up to 48 PMTs). Each mini-drawer has 2 independent read out sections for redundant cell readout
  - 12 PMTs + 12 front-end boards reading out 6 TileCal cells
  - 1 × MainBoard: operation of the front-end boards
  - 1 × DaughterBoard: data high speed link with the off-detector electronics
  - 1 × High Voltage distribution board
  - 2 × Low Voltage Power Supply bricks: low voltage power distribution, one for each independent side → 8 bricks form a Low Voltage Power Supply (LVPS).



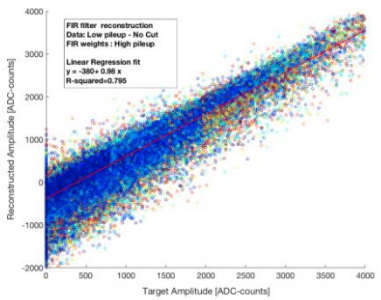


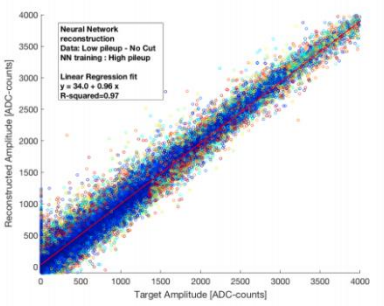
Energy Reconstruction

- Extra pile-up noise in harsh conditions with μ = 200 in HL-LHC
  - Signal alterations
- Energy reconstruction implemented in FPGA
  - Current: Optimal filtering (FIR filter)
  - Deep Learning MLP with 1 hidden layer
    - Excellent precision under mu = 80
    - More advanced studies ongoing
      - 12-bit weights
- Resources per channel
  - Latency 5 CLK cycles
  - Fullfil requirements



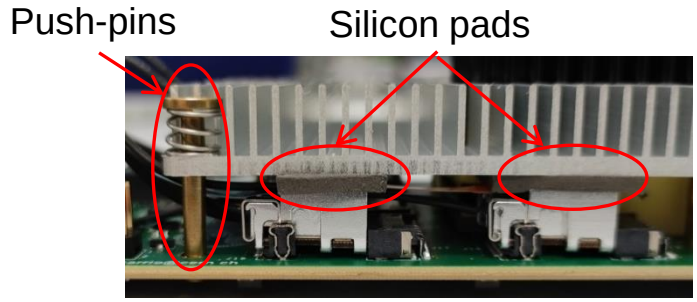
Resource summary	Available	Utilization		
		ANN	OF-FPGA	OF-DSP
Slice registers	607,200	695	98	-
Slice LUTs	303,600	1297	87	-
RAM blocks	1,030	4	0	-
DSPs	2,800	13	3	-
Performance summary				
Operation mode		Parallel (pipelined)	Parallel (pipelined)	Sequential
Latency	-	125 ns	25 ns	10 μs
Operation frequency	-	40 MHz	40 MHz	100 KHz

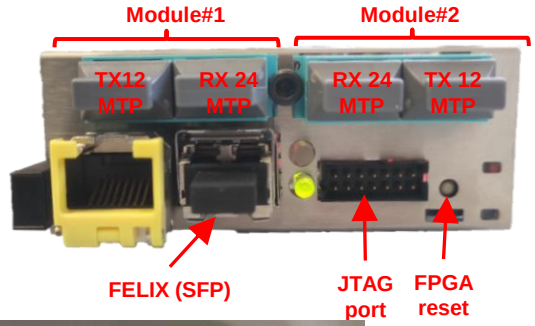




Mechanics & Thermal Tests

- Custom heatsink design for the FPGA and FireFly modules
  - Preliminary results shows a good thermal performance





- Complete thermal tests to be performed at the end of August at CERN facilities with a full PreProcessor and TDAQi
  - ATLAS specs: maximum power consumption of 400W per blade
  - 2 x ATCA shelves with 14 slots in 63U racks with cooling
  - Load blades dissipating 400W per blade
  - Temperature monitoring via LabView and IPbus for the CPMs

Thermal test bench with 63U rack