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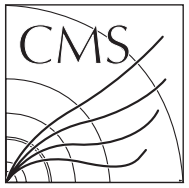

The Compact Muon Solenoid Experiment

Conference Report

Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland

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The CMS Tracker for the High Luminosity LHC

Alessandro Rossi for the CMS Collaboration

Abstract

The LHC machine is planning an upgrade program which will smoothly bring the instantaneous luminosity to about $5 - 7.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, to reach an integrated luminosity of $3000 - 4500\,\mathrm{fb}^{-1}$ by the end of 2039. This High Luminosity LHC scenario, HL-LHC, will require an upgrade program of the LHC detectors known as Phase-2 upgrade. The current CMS Tracker, already running beyond design specifications, and CMS Pixel Detector will not be able to survive HL-LHC radiation conditions and CMS will need completely new devices, in order to fully exploit the HL-LHC data which will be recorded under highly demanding background conditions.

The Phase-2 Tracker will be made of two sections, an Inner Tracker and an Outer Tracker. Both detectors will feature increased radiation hardness, higher granularity and capability to handle higher data rate and longer trigger latency in order to ensure at least the same performances of the current detector, in terms of tracking and vertex reconstruction capabilities, at the high pileup (140-200 collisions per bunch crossing) expected at HL-LHC. Moreover the Phase-2 Outer Tracker will have also trigger capabilities since tracking information will be used at L1 trigger stage.

This report is focusing on the replacement of the CMS Tracker system, describing new layout and technological choices together with some highlights of research and development activities.

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The CMS Tracker for the High Luminosity LHC

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Abstract

The LHC machine is planning an upgrade program which will smoothly bring the instantaneous luminosity to about $5 - 7.5 \times 10^{34}\,\mathrm{cm^{-2}s^{-1}}$, to reach an integrated luminosity of $3000 - 4500\,\mathrm{fb^{-1}}$ by the end of 2039. This High Luminosity LHC scenario, HL-LHC, will require an upgrade program of the LHC detectors known as Phase-2 upgrade. The current CMS Tracker, already running beyond design specifications, and CMS Pixel Detector will not be able to survive HL-LHC radiation conditions and CMS will need completely new devices, in order to fully exploit the HL-LHC data which will be recorded under highly demanding background conditions.
The Phase-2 Tracker will be made of two sections, an Inner Tracker and an Outer Tracker. Both detectors will feature increased radiation hardness, higher granularity and capability to handle higher data rate and longer trigger latency in order to ensure at least the same performances of the current detector, in terms of tracking and vertex reconstruction capabilities, at the high pileup (140-200 collisions per bunch crossing) expected at HL-LHC. Moreover the Phase-2 Outer Tracker will have also trigger capabilities since tracking information will be used at L1 trigger stage.
This report is focusing on the replacement of the CMS Tracker system, describing new layout and technological choices together with some highlights of research and development activities.

1. Introduction

The innermost device of the CMS detector [1] at the CERN LHC is a silicon tracker composed of a pixel detector and a strip tracker whose main purpose is to measure the trajectories of charged particles. The CMS Tracker was designed to cope with the nominal LHC instantaneous luminosity, $1 \times 10^{34}\,\mathrm{cm^{-2}s^{-1}}$, which corresponds to an average of 25 proton-proton interaction per bunch crossing (pileup). In 2017, due to the performance attained by the LHC, the CMS Collaboration upgraded the pixel detector [2] with a completely new one able to handle the luminosity expected for the Run 2 (2015-2018) and Run 3 (2022-2025) data taking periods.

After the end of Run 3, LHC will move towards the High Luminosity phase (HL-LHC) where instantaneous luminosities of $5 - 7.5 \times 10^{34}\,\mathrm{cm^{-2}s^{-1}}$ are expected. The CMS Collaboration will replace the full tracking system during the LHC Long Shutdown 3 (2026-2028) as part of the Phase-2 upgrade [3] in order to cope with the extreme conditions foreseen for the HL-LHC. The main reason to completely replace the tracking system is related to the increased radiation level at which the detector will operate with fluences up to $2.3 \times 10^{16}\,n_{eq}/\mathrm{cm^2}$ and a total ionising dose up to 1.2 Grad. In order to have good tracking performance the Phase-2 Tracker will have a higher granularity and increased readout bandwidth to sustain the larger hit and trigger rates expected. Furthermore the tracking acceptance region will be extended in the forward region up to a pseudorapidity of $|\eta| < 4$.

The Phase-2 Tracker is composed of two parts, as shown in Fig. 1: the Inner Tracker (IT) made of silicon pixel detectors and the Outer Tracker (OT) made of micro-strips and macro-pixel silicon detectors. This report will describe the main design feature of the two parts and will give some highlights on the ongoing activities.

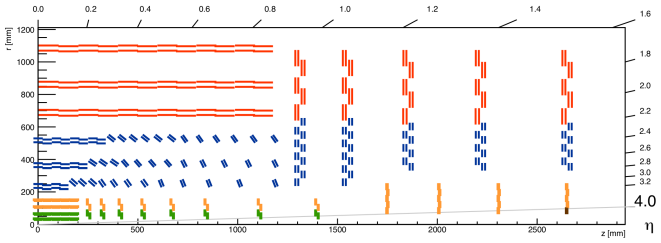

Figure 1: The Phase-2 CMS tracker layout where each coloured line indicates a detector module. Pixel modules, in orange (quad-chip modules) and green (double-chip modules), form the Inner Tracker system. The Outer Tracker is composed of two different types of modules indicated with blue (PS modules) and red (2S modules) lines. One quarter of the detector is shown.

2. The Inner Tracker

The IT is composed of three different substructures: a barrel part (TBPX) made of four concentric layers where the modules are hosted in ladder-like structures; a forward part (TFPX) made of eight small disks with module arranged in 4 different rings and an endcap part (TEPX) made of 4 large disks with 5 rings of modules each. The TEPX will have the functionality to perform also luminosity measurements, the innermost ring of the last TEPX disk is completely devoted to the bunch-by-bunch luminosity measurement. The IT will cover a total

area of 4.9 m^2 with 3892 silicon pixel modules. In order to optimise the module production and to have a higher modularity and flexibility the detector will have only two types of modules: double-chip (1x2) modules, Fig. 2 left, which will be hosted in the inner layers and rings and quad-chip (2x2) modules, Fig. 2 right, which will be installed in the outer layers and rings. How modules are arranged in the detector is shown in Fig. 1, double-chip modules are shown in green and quad-chip modules are shown in orange. In Fig. 3 a schematic view of an IT module is shown, the module is made of the silicon sensor, the Read Out Chips (ROCs) bump-bonded to the sensor and a High-Density Interconnection (HDI) printed circuit board. HDI and ROCs are wire-bonded to each other. The only active elements on the module are the ROCs since the HDI is a completely passive object.

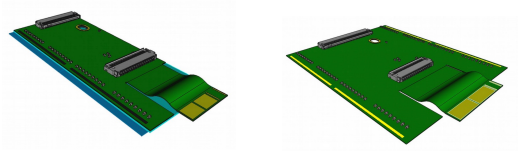

Figure 2: Layout of an IT double-chip module (left) and of an IT quad-chip module (right).

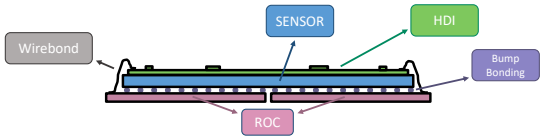

Figure 3: Schematic transverse view of an IT module, the different components are shown in different colour.

In the last years different pixel sensors had been under investigation, mainly 3D and thin n-in-p planar sensors [4, 5, 6] with pixel cells of different dimensions (i.e. $25 \times 100\,\mu m^2$, $50 \times 50\,\mu m^2$). After all the studies carried out, the project baseline has now adopted two different types of sensors both with $25 \times 100\,\mu m^2$ cells and a thickness of 150 µm. The innermost layer of the TBPX will be instrumented with 3D pixel sensors which will assure a lower power consumption with respect to planar sensors and stable hit resolution performance up to a fluence of $10^{16}\,n_{eq}/cm^2$. The rest of the detector will instead use n-in-p planar pixel sensors with a bitten implant design and no punch-through bias dot which have a hit efficiency greater than 99% also after being irradiated with the ionising dose expected during the HL-LHC phase.

The ROCs are ASICs based on a 65 nm technology, developed by the RD53 collaboration, a common project by the ATLAS and CMS collaborations. The main features are a radiation tolerance up to 1 Grad, a strong protection against Single Event Upsets (SEU), a power consumption lower than 1 W/cm^2 and an on-chip shunt-LDO regulator for serial powering. A first prototype version, RD53A [7], has been used to perform a series of tests and studies in order to verify the chip performance [8]. The final CMS chip will be a flavour of the RD53B chip [9], called C-ROC, which contains an active matrix of 432×336 channels each one with a linear analogue front-end. The C-ROC size is $21.6 \times 8.6\,cm^2$. The first wafer-lever test of the C-ROC is ongoing.

The module communication with the back-end is performed via dedicated boards: service opto-electronics portcards. Each portcard houses three Low Power GigaBit Transceivers (lpGBTs) [10] and three Versatile Link Plus Transceivers (VTRx+) [11]. Everything is powered by dedicated DC-DC converters. The components on the portcards have only a limited radiation tolerance so they have been separated from the detector modules in order to be installed in a position further from the collision point, this will also keep the material budget in the tracking volume as low as possible. Modules and portcards are connected via one electrical down-link at 160 Mb/s for chip configuration commands, trigger and clock distribution and up to 6 electrical up-links at 1.28 Gb/s for data transmission. The portcards send data to the back-end electronics via optical links; a schematic of the readout system is shown in Fig. 4. Readout links (green and blue) send data from events accepted by the first trigger-stage and monitoring information to the DAQ and control system. Control links (pink and red) send clock, trigger, and configuration commands to the detector. A dedicated custom ATCA (Advanced Telecom Computer Architecture) board based on commercial FPGAs called DTC (Data, Trigger & Control) acts as intermediate step between the portcards and the CMS DAQ. Each DTC can handle up to 72 fibres and a total of 28 boards will be needed to read out the full IT.

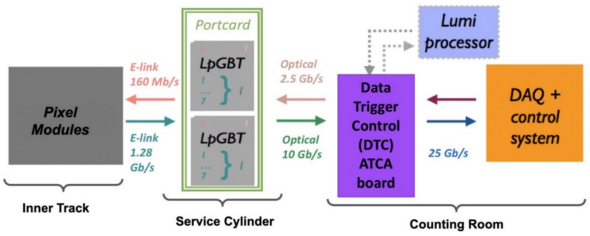

Figure 4: Schematic representation of the data acquisition system of the Phase-2 Inner Tracker

Powering all the 13488 ROCs of the CMS IT will require a power of the order of 50 kW. If this power would be supplied via a conventional parallel scheme where the power losses are minimised about six tons of cables would be needed. This approach is not feasible since the material in the path of the particles to be detected would be too high. The solution found to minimise the material used to power the detector was to develop a system with a constant current consumption where a chain of modules are powered in series [12], this concept is called serial powering. The IT will have 500 serial power chains, each with up to 12 modules. Inside the module the chips will be powered in parallel. The sensor bias high voltage lines will follow the serial power chains with a single return line. Everything will be supplied by a single power supply module which will have a current source for the serial powering and a high voltage source for the sensors.

The mechanical structure of the IT is completely made of light carbon fibre with embedded cooling pipes to keep the ma-

terial budget as low as possible. The cooling system is based on evaporative CO_2 with a working temperature of $-35\,^{\circ}C$.

3. Outer Tracker

In order to be able to maintain the current trigger thresholds also under the higher pileup conditions it is fundamental for CMS to have tracking information contributions at the L1 trigger level since this will improve the selection performance. To have this kind of feature a readout at the bunch crossing frequency of 40 MHz is needed but it is not possible to read out the whole OT at such high frequency due to bandwidth limitation. A novel module concept that allows a data reduction at the

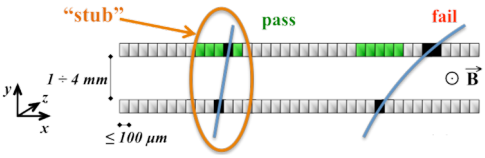

Figure 5: Schematic, enlarged view of the two silicon sensors with indicated trajectories of two particles. Strips with a hit are black; the search windows in the top sensor are indicated in green. The right track has a p_T too low to create a valid stub

front-end level based on transverse momentum (p_T) track discrimination has been developed to overcome this problem. The p_T module concept is based on two closely spaced silicon sensors read out by the same electronics. A charged particle which traverses the module will leave a signal in both sensors and the readout electronics can compare the two hit positions. Once the position on the first sensor is known the position on the second one will depend on the track curvature in the 3.8 T CMS magnetic field and therefore on the p_T of the particle itself. If the hit in the second sensor is inside a correlation window relative to the hit in the first sensor a track segment (called stub) is generated and sent to a fully FPGA-based system which will reconstruct the tracks which be used by the L1 trigger (Track-Trigger). The width of the correlation window will result in a cut on the track p_T and can be programmed in order to have a threshold in a range between 2 and 3 GeV. At this point the stub information can be sent to the trigger system with a rate of 40 MHz and only in the case the L1 trigger will select an event the whole OT will be read out. The expected L1 trigger rate is 750 kHz.

A layout of the OT is shown in Fig. 1. It consists of three parts : a barrel part (TBPS) made of three layers with modules with strips and macro-pixel sensors (PS modules), a barrel part (TB2S) made of three layers with modules with two strips sensors (2S modules) and two endcaps (TEDD) made of five double disks with both PS and 2S modules. In Fig. 1 the position of the different module types are shown, 2S modules in red and PS modules in blue. The three layers of the TBPS have a section with modules progressively tilted along the increasing η direction in order to minimise the number of modules and to have better trigger performance.

The 2S modules consist of two $10 \times 10\,cm^2$ n-in-p silicon strip sensors. Each sensor is divided in two columns of 1016 strips with a pitch of 90 μm and a length of 5 cm. There are two different types of 2S modules with different sensor spacings: 1.8 mm and 4.0 mm. A schematic view of a 2S module is

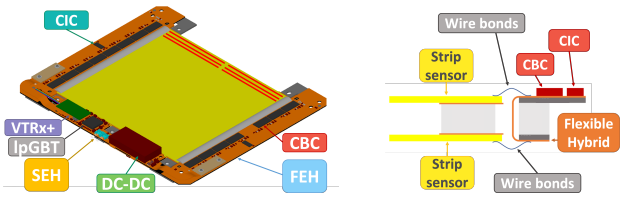

Figure 6: Left: Schematic view of a 2S module, the most relevant components are indicated. Right: Enlarged transversal view of the two sensors and the Front-End hybrid.

shown in Fig. 6 left. The strips sensors are wire bonded to the Front-End Hybrids (FEHs), the strips columns are bonded on the two different FEHs on the module. One FEH is bonded to both top and bottom sensors. Each FEH houses 8 readout chips, the CMS Binary Chips (CBCs), each CBC has 254 channels (127 for the top sensor and 127 for the bottom). It performs a binary readout of the signal with a programmable threshold and has all the correlation logic for stubs building integrated. FEH are made with a flexible fold-over substrate, this feature allow the connection of both sensors to the same chips, as can be seen in Fig. 6 right. The FEH also hosts a Concentrator Integrated Circuit (CIC) which receives stubs and readout data from the CBCs and acts as data hub towards the Service Hybrid (SEH). The SEH hosts a lpGBT and a VTRx+ for the communication with the back-end and two DC-DC converters for the module powering.

The PS modules, instead, consist of a n-in-p silicon strip sensor of $5 \times 10\,cm^2$ and a silicon macro-pixel sensor. The strip sensor is divided in two columns of 960 strips with a pitch of 100 μm and a length of 2.4 cm. The macro-pixel sensor is composed of about 30000 cells with a size of 1.5 mm×100 μm. There are three PS module types with three different sensor spacings: 1.6 mm, 2.6 mm and 4.0 mm. A schematic view of a PS module

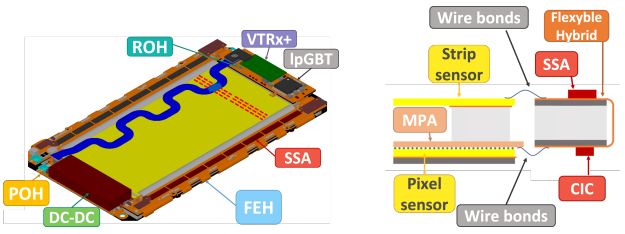

Figure 7: Left: Schematic view of a PS module, the most relevant components are indicated. Right: Enlarged transversal view of the two sensors and the Front-End hybrid.

is shown in Fig. 7 left. The pixelated sensors are read out by 16 Macro Pixel ASICs (MPAs) which are bump-bonded to the sensor. The strip sensor is instead wire-bonded to two FEHs (one on each side) which house 8 Short Strip ASICs (SSAs) which perform the strips signal binary readout. Also in the PS case the FEH are made with a flexible fold-over substrate which allow to

put in communication the SSAs with the MPAs via wire-bonds from the back of the FEH to the MPAs themselves, Fig. 7 right. In this way the SSAs can transmit the data to the MPAs where the correlation logic for the building of the stubs is housed. The stubs and the readout data are then passed back to the FEH and to the CIC which, as for the 2S modules, acts as concentrator and data hub. The PS module has the same services as the 2S: one lpGBT and one VTRX+ for back-end communication and DC-DC converters for the powering, in the PS case the former are housed in the Read-Out Hybrid (ROH) while the latter are located on the Power Hybrid (POH).

Each module, either 2S or PS, is an independent functional unit individually connected to the power system and the back-end system. The back-end is made of an equivalent DTC card as for the IT and each module is directly connected to a DTC with a bi-directional optical link. The down-link has a bandwidth of 2.56 Gb/s and sends clock, trigger and programming information from the DTC to the module while the up-link can have a bandwidth of 5.12 or 10.24 Gb/s and sends L1 information (at 40 MHz) and readout data from module to the DTC. The DTC can then pass L1 information to the TrackTrigger system for the Level-1 trac k finding and the readout data to the CMS DAQ.

The OT has a power budget of about 100 kW. The powering system is parallel with on-module conversion via DC-DC converters. As for the IT the mechanical structure is completely made of light carbon fibre and the cooling is an evaporative CO_2 system with a set point around $-35\,^{\circ}$C.

In the last couple of years different 2S and PS prototypes have been built in order to perform tests and electronics validation [13, 14]. In the last months few fully functional modules with almost the final version of the electronics have been assembled and additional beam tests studies are planned by the end of the year.

4. Performance

The Phase-2 tracker will have a huge increase in terms of number of channels with respect the current tracker. An increased granularity is a key factor for good performance at HL-LHC. Despite this increase the material budget is reduced as can be seen in Fig. 8 where the current material budget is shown on the left and the projected Phase-2 one is shown on the right. The increase in granularity, the material budget reduction and tracking capability extension to higher η result in an expected tracker performance better than the present one even with a pileup level up to 200 collisions per bunch crossing. All the studies performed on the tracking performance can be found in Ref. [3].

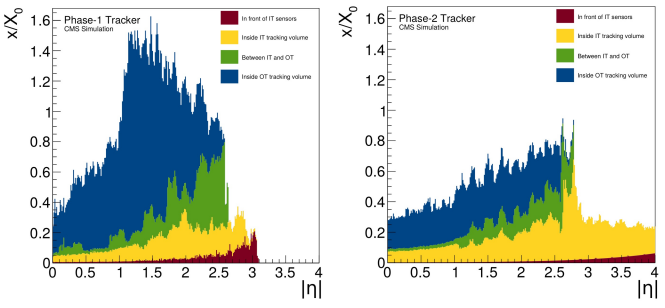

Figure 8: Material budget of the current CMS Tracker (left) and the projected material budget for the Phase-2 tracker (right) in unit of radiation length.

5. Conclusions

The Phase-2 upgrade of the CMS tracker is a fundamental project to ensure excellent CMS detector performance at HL-LHC. The most relevant aspects of the upgrade have been described in this report. The CMS tracker community will enter soon in the production phase of all the components of the upgrade. At the moment the IT C-ROC and OT module prototypes are under test in order to validate and finalise the last details in view of the pre-production stage next year. The pre-production stage will be extremely important to validate the design of all the different components before the start of the full mass production.

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