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The H1 detector at HERA at DESY undergoes presently a major upgrade. In this context silicon strip detectors have been installed at beginning of 1995. The high bunch crossing frequency of HERA (10.4 MHz) demands a novel readout architecture which includes pipelining, signal processing and data reduction at a very early stage. The front end readout is hierarchically organized. The detector elements are read out by the APC chip which contains an analog pipeline and performs first background subtraction. Up to five readout chips are controlled by a Decoder Chip. The readout processor module (OnSiRoC) operates the detectors, controls the Decoder Chips and performs a first level data reduction. The paper describes the readout architecture of the H1 Silicon Detectors and performance data of the complete readout chain.

1. H1 Silicon Detectors

The H1 detector operating at the electron proton collider HERA at DESY in Hamburg is one of two big multipurpose detectors. The H1 detector is mainly designed to observe deep inelastic e-p scattering at highest transferred momentum Q^2 and has special features to detect leptons [1]. However, there are also other interesting fields of particle physics which can be investigated with H1. Two of them led to the proposal to improve the physics potential by installing silicon detectors near the beam pipe, namely low x physics and heavy quark physics [2].

The H1 Silicon detectors are located inside the innermost chambers of the central tracking detectors around the beam pipe. There are two independent devices, the **C**entral **S**ilicon **T**racker (CST) for vertex determination and the **B**ackward **S**ilicon **T**racker (BST) for measuring particles at small angles with respect to the electron beam direction. Both detectors are arranged around a new beam pipe with an inner radius of 45 mm.
The CST consists of two barrel shaped layers of double sided silicon strip detectors. The inner layer (radius r = 57.5 mm) is a regular prism with 12 faces, the outer (r = 97 mm) with 20 faces. Each face consists of six silicon detectors (total length 356 mm) with readout at both ends. With these detectors the impact parameter resolution at 1 GeV/c can be improved to 60 μm.

The BST is composed of eight disks mounted perpendicularly to the beam line at distances between 390 mm and 1050 mm from the nominal interaction point in the electron direction. The disks have an inner hole of 56.5 mm radius and are segmented into 16 azimuthal sectors. The outer radius is 123 mm. Each disk is built as a composite of two different kinds of single sided silicon strip detectors: with arc shaped strips at constant radii to measure the polar angle (*r-strip*) and with strips at constant azimuthal angles to determine $p_\perp$ (φ-*strip*). The r-strip detectors permit an angular resolution of 0.5 mrad, the momentum resolution of the φ-strip detectors is 10% at 1 GeV/c. Each disk is complemented by a silicon *pad* detector for fast triggering [3]. CST and BST have in total about 214,000 strips which have to be processed by the readout system.

2. Readout System

Particular challenges of the readout of the H1 silicon tracking detectors are:

- it has to be matched to the HERA bunch repetition rate of 10.4 MHz, requiring a multi-event pipeline buffer and
- it has to be fast and efficient in order to produce no additional deadtime and reduce the large data volume.

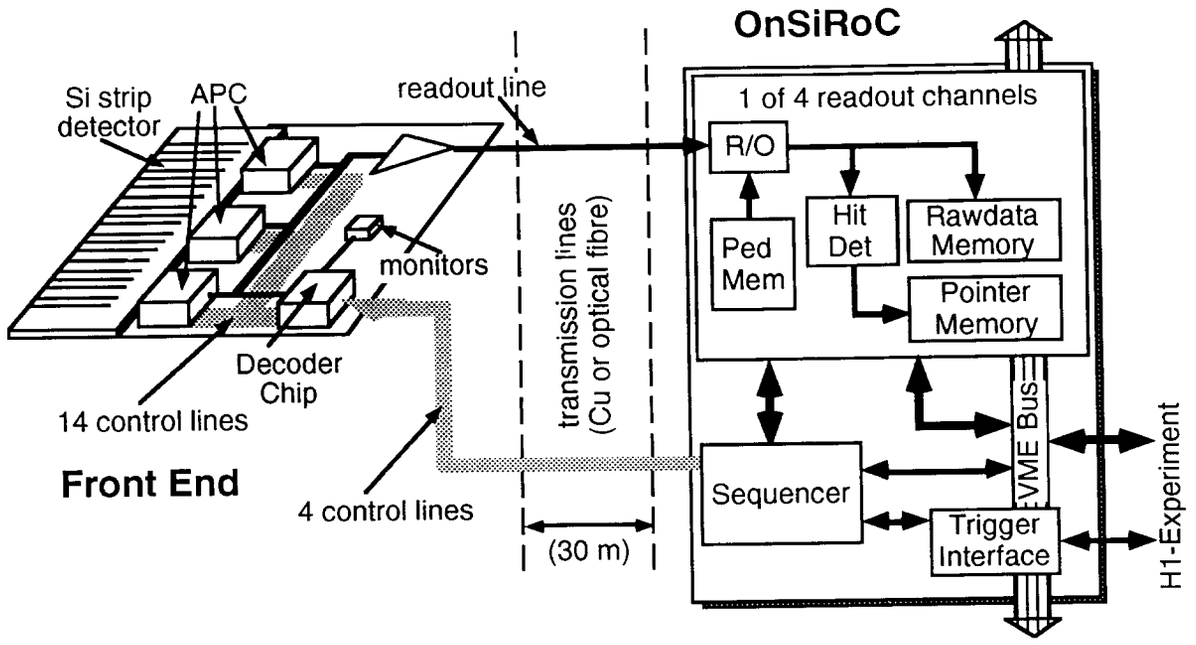

Fig. 1: Schematic diagram of the strip detector readout

The readout chain of the strip detectors (fig. 1) comprises the following elements:

— a front end hybrid with readout chips (APC) and a Decoder Chip
— a line driver for conventional Cu cable or optical fibre transmission lines (at present only the CST is read out by optical fibres)
— a readout processor module (OnSiRoC)
— a system to implement the data stream into the H1 data acquisition.

The architecture of this readout system is very versatile and thus the usage in other applications, e.g. micro strip gas chambers, is feasible with minor or no modifications.

2.1. Front end readout

The front end readout is located directly at the detectors in order to process the small signal charges generated by a m.i.p. traversing the 300 µm thick, fully depleted silicon substrate. The readout chip (APC) serves 128 silicon strips.

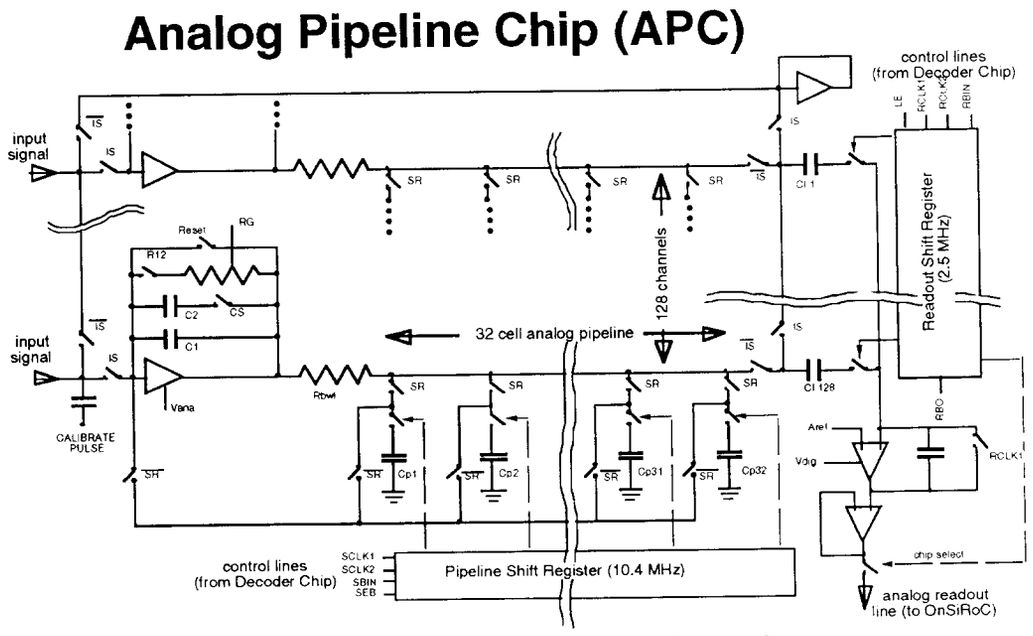

Fig. 2: Functional diagram of the APC

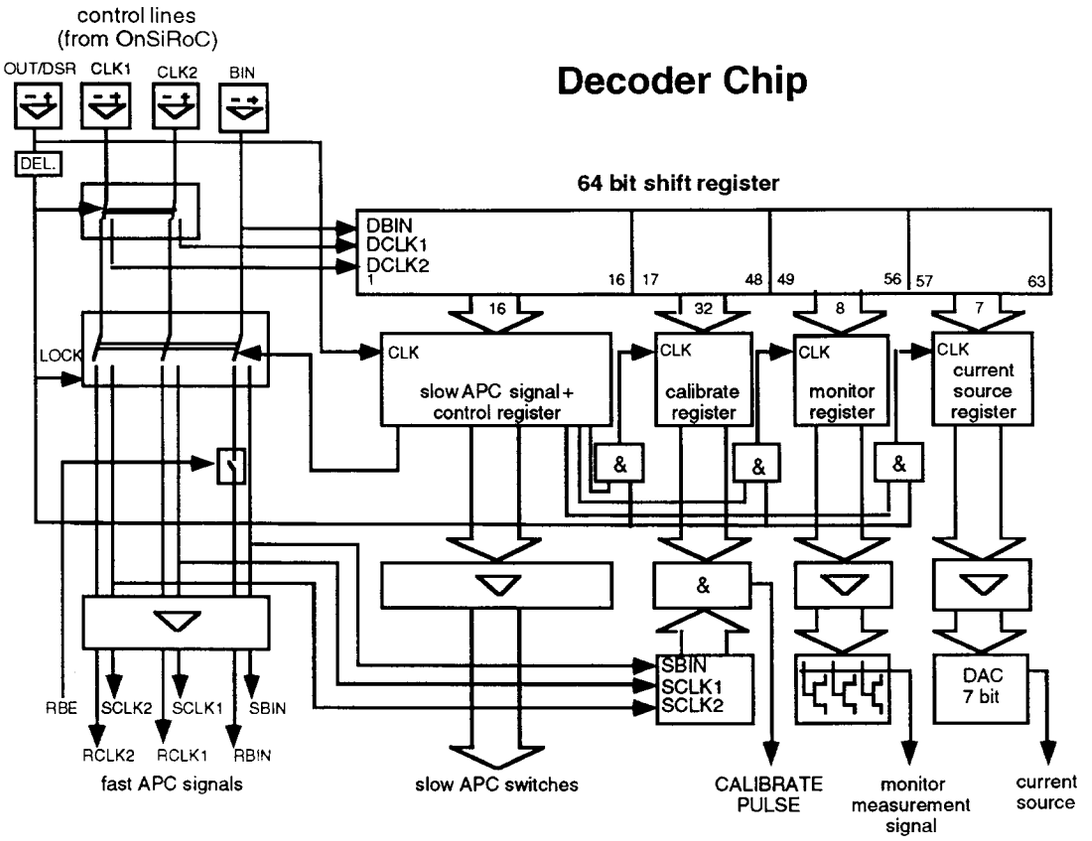

Fig. 3: Functional Diagram of the Decoder Chip

Each channel consists of a preamplifier and an analog pipeline. Given the complex controlling of the APC a Decoder Chip is added which controls several APCs in a hierarchical structure. The main advantage is a considerable reduction of control signals. Furthermore the Decoder Chip takes over additional control and monitor tasks.

The **A**nalog **P**ipeline **C**hip (APC, see fig. 2) has been developed to cope with the timing requirements of HERA [4]. It has 128 channels for strip readout, each with an analog pipeline with 32 cells of switched capacitors. The chip has been designed and build in a 1 µm SACMOS (**S**elf **A**ligned **C**ontact C**MOS**) process [5]. It is sufficiently radiation hard for the application at HERA and has an overall size of is 3.5 x 6.3 mm^2. The pipeline is clocked by the HERA bunch crossing frequency of about 10.4 MHz (sample mode). The depth of 32 pipeline elements is well matched to the first level trigger decision, which has to be taken within about 2.5 µs. When a trigger occurs the pipeline is stopped and the information stored at a given position in the pipeline is read out sequentially with a frequency of 2.5 MHz (readout mode).

To compensate radiation induced shifts in the threshold voltages of the preamplifier the chip is powered by an external current source rather than by a voltage source [4].

The chips have a power consumption of 280 µW/channel and achieve a signal to noise ratio of 15:1 for a m.i.p. at a capacitive load of 30 pF.The Decoder Chip (fig. 3) serves as a multiplexing/demultiplexing unit and is part of the front end system. It allows to control the numerous switches of the APC by a minimum number of signals and to read out several monitor voltages.

In total 14 signals are necessary to control the APC during data sampling and readout. These signals are generated by the Decoder Chip, which needs only 4 input lines. In the *sample mode* when the information per bunch crossing is stored into the pipeline capacitors (@ 10.4 MHz), and in the *readout* mode, when the information of a given time slice is read out sequentially (@ 2.5 MHz) the clock pulses are directly passed to the APC. For set up steps between the two modes a sequential information is demultiplexed and downloaded to set the control switches of the APC.

For calibration purposes the Decoder Chip contains a duplicate of the pipeline shift register of the APC. This allows to serve each pipeline cell individually with calibration pulses.

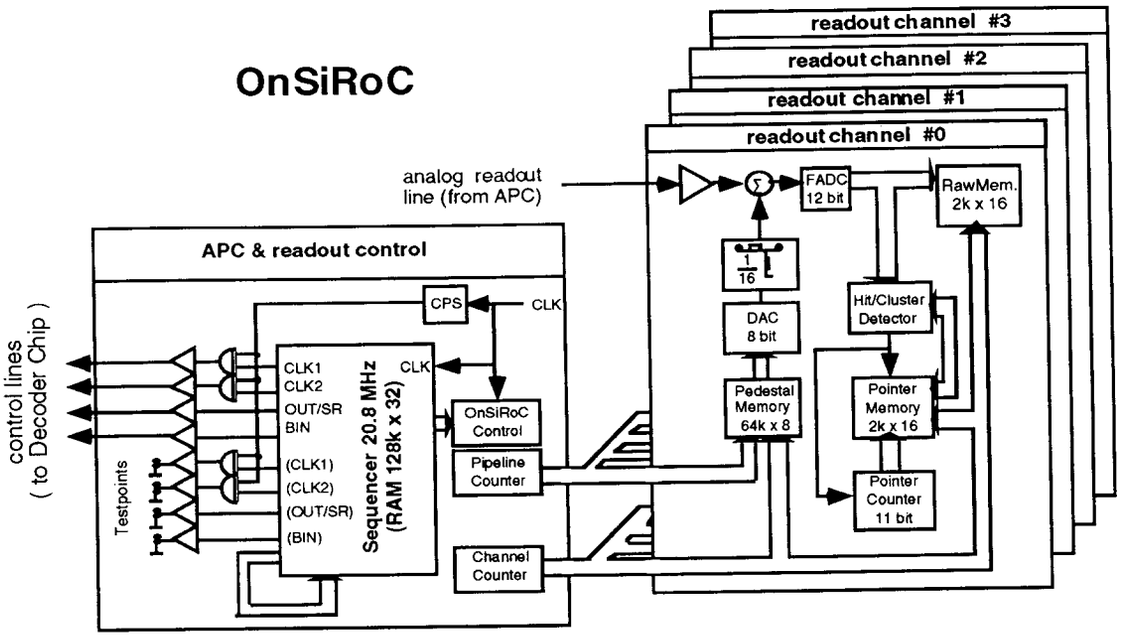

Fig. 4: Blockdiagram of the OnSiRoC

The current source for the preamplifier of the APC is realized by an external transistor which is controlled by a 7 bit register and a digital to analog converter on the Decoder.
To perform monitor measurements, e.g. temperature, it is possible to put up to 8 different voltages to the analog signal output line. With an appropriate sequence a *slow control event* can be created in which the readout corresponds to these voltages.

2.2. Readout Processor

In order to cope with the complex requirements of controlling and recording the information of the APC a new readout processor module has been developed. This module (*OnSiRoC* = **On**line **Si**licon **R**eado**u**t **C**ontroller, fig. 4) provides all services needed to operate the APC namely:

— 4 parallel readout channels each to process the signals of up to 2048 silicon strip channels (16 APCs sequentially),
— the sequencer, a programmable unit which controls the OnSiRoC functions and drives the Decoder Chip and
— 4 independent sets of each 3 power supplies (analog and digital voltage for the APC, and bias voltage for the strip detector).

This architecture allows a simple implementation in the H1 detector: only two cables are necessary to operate up to 8192 silicon strips.

The OnSiRoC has a complete VME bus slave interface. Hence all its functions are controllable by a standard VME architecture, which is commonly used in the H1 experiment. All memories are down-loadable via the VME bus.
For each readout channel a complete set of voltages to drive a strip detector and the front end electronics is available. The voltages are generated potential independent. Thus the different needs of the components can be served easily (e.g. driving the electronics on the n-side level of the double sided strip detectors) and optimized grounding can be performed. The bias voltage settings are remotely controlled and the bias current readings can be recorded in order to monitor e.g. radiation damages. All voltage sources can be switched off separately.

In the readout path the analog signals are pedestal subtracted, digitized and stored. A *hit detector* searches the digital data for hits and stores them in a pointer memory.
The sequential readout of the silicon strips is presently performed at a rate of 2.5 MHz limited by the front end system, while the OnSiRoC allows up to 10 MHz. A further limitation is given by the H1 data acquisition organization, which allows 800 µs for the readout of the detector components. In the H1 experiment up to 12 APC will be read out by one channel.
Before being digitized by a 12 bit, 10 MHz FADC the analog signal undergoes a pedestal subtraction. Pedestal values for all pipeline

buffers of all APC strip channels are available in a memory (4 x 64 kbyte per OnSiRoC module). Pedestal changes are recorded by CPU processor cards (RAID 8239) in a Master Silicon Readout Crate and the pedestals appropriate updated. It is expected to download new values not more often than once an hour. An update of an OnSiRoC pedestal memory takes about 13 ms.
The digitized pulse values are stored in a raw data memory and in parallel they are examined on the occurence of useful signals by a *hit detector* with programmable thresholds and cluster widths. If the subsystem trigger controller requires a readout, the candidate hits are forwarded in a quite condensed form (address, pulse height and width): some 2.5 Mbits of raw data are reduced to about 3-4 kbytes for CST and BST. Nevertheless it is still possible to read out the whole raw data memory e.g. for test and calibration purposes.
The pedestal memory can also be used to test all functions of the readout channel in a stand alone mode. To this end the pedestal memories are filled with test patterns or simulated pulses and then processed as usual pulses.

The OnSiRoC is controlled by a programmable unit called *Sequencer*. It consists of memories and transceivers with registers which are connected in a way that the program path is defined parallel to the control bit code and runs sequentially. Application specific programs for different operation modes can be stored and started through different start addresses.
The sequencer memory contains all command sequences to control the functions of the OnSiRoC and the Decoder Chip. Each sequence consists of 32 bits: 16 address bits and 16 control bits. The address bits define the next sequence i.e. each sequence has a unique successor. This structure allows the programming of endless loops which can be interrupted by an external trigger decision e.g. during data sampling.
In the sequencer memory 128k sequences can be stored. The maximum size of a program is 64k sequences although a typical program is much shorter e.g. 3k for the readout. The program code for sample and readout mode is stored at defined addresses so they can be started on external trigger signals. Programs for slow control or test purposes can be started via VME at any address in the sequencer memory.
4 command bits control the Decoder Chip while the remaining 12 bits control the OnSiRoC e.g. pipeline cell counting and clock frequency.
To code the sequencer in a convenient way a compiler for a high level programming language has been developed.

2.3. Readout Cycle

A typical readout cycle is started by a signal from the H1 Central Trigger Controller setting up the APC switches for the data sampling mode in less than 2.5 μs. This initializes the APC pipeline to run in an endless loop waiting for the trigger readout signal which arrives with 25 bunch crossings latency. On that signal the pipeline is stopped and the pointer is forwarded to the cell containing the event. Up to 12 daisy chained APCs, which are connected to one OnSiRoC channel are read out sequentially. The digitally stored pedestal values of the appropriate cell are converted to an analog signal and subtracted off the input signal. Afterwards they are digitized and stored in the raw data memory and analyzed by the hit detector which stores the hit addresses in the pointer memory. This operation takes less than 800 μs and can be interrupted by a higher level trigger rejection. After the readout has been finished or a trigger rejection the next readout cycle starts. While the pipeline is running again the OnSiRoC data is read out by the Master Silicon Readout Crate. By this method first order deadtime is minimized.

3. Data Acquisition

The H1 data acquisition system is a modular multi-processing environment that has been designed around the VMEbus standard [6]. Several subdetectors are read out in parallel before being merged into a central coordinating framework. The readout of the silicon tracker has been organized such that it fits easily into this architecture.
The complete readout is split into three partitions and a master crate that communicates with the H1 central data acquisition. The silicon subsystem crates are interconnected through a fibre optic ring with VMEtaxi modules [7], which allow a data transfer rate of up to 55 Mbyte per second, which is sufficient to transfer even the raw data.
Readout and reconstruction processing is carried out in the *Master Silicon Readout Crate* by R3000-RISC-based cards (RAID 8239). The dual ported memory boards (DPM 8242) provide the necessary buffer for readout and

monitor purposes. Some additional 10 Mbyte are required for the fast access of stored pedestal and sequencer values.
The data quality will be monitored via event displays and histograms of with purpose-written programs layered on top of the existing base software packages of the H1 data acquisition system.
Finally each detector crate has a Subsystem Trigger Controller card (STC) to communicate with the Subsystem Trigger Control Crate. This crate is also connected via the fibre optic ring to the Master Silicon Readout Crate and the silicon subsystems.

4. Project Status and Outlook

In February 1995 the lower half of the CST and 4 half-disks of the BST each equipped with 2 r-strip and 8 pad detectors have been installed. The detector modules are equipped with APCs and Decoder Chips. The full strip detector readout chain in the H1 environment has already been successfully tested with recent prototypes of the OnSiRoC. At the start of the 1995 run period all strip detectors will be read out by a presently produced version of the OnSiRoC. The full data acquisition system has already been installed last year and is operational. The remaining parts of the detector system will be installed during fall 1995.

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