

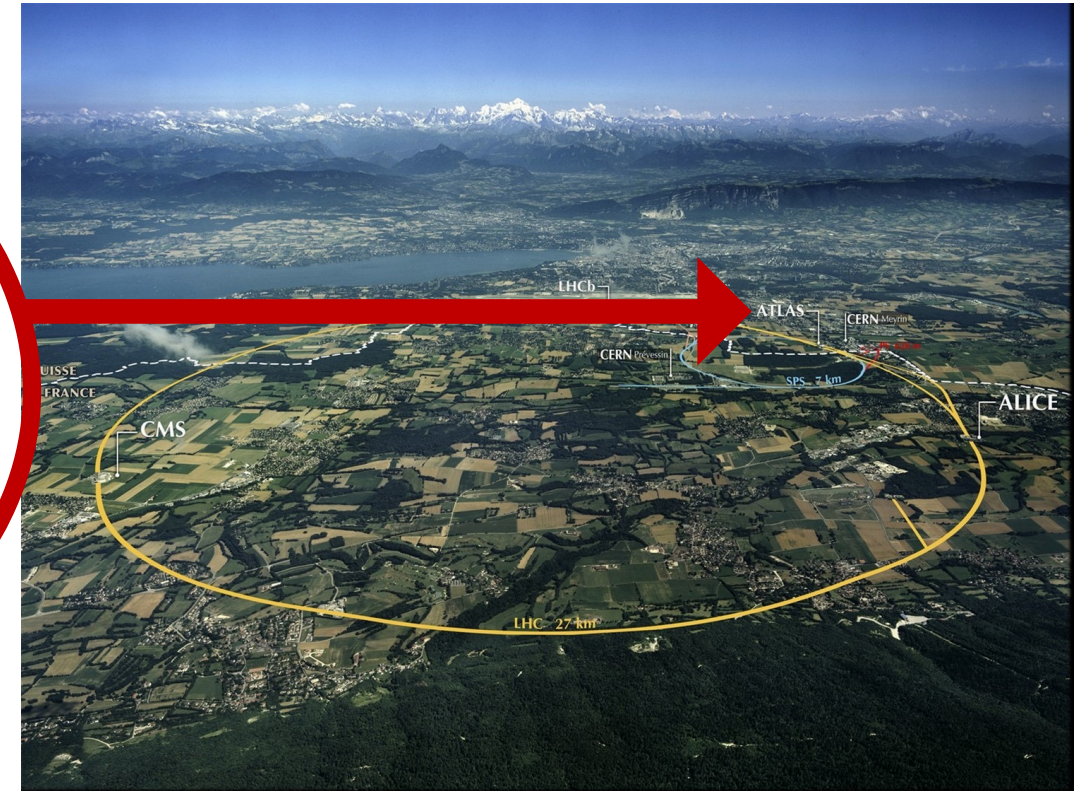
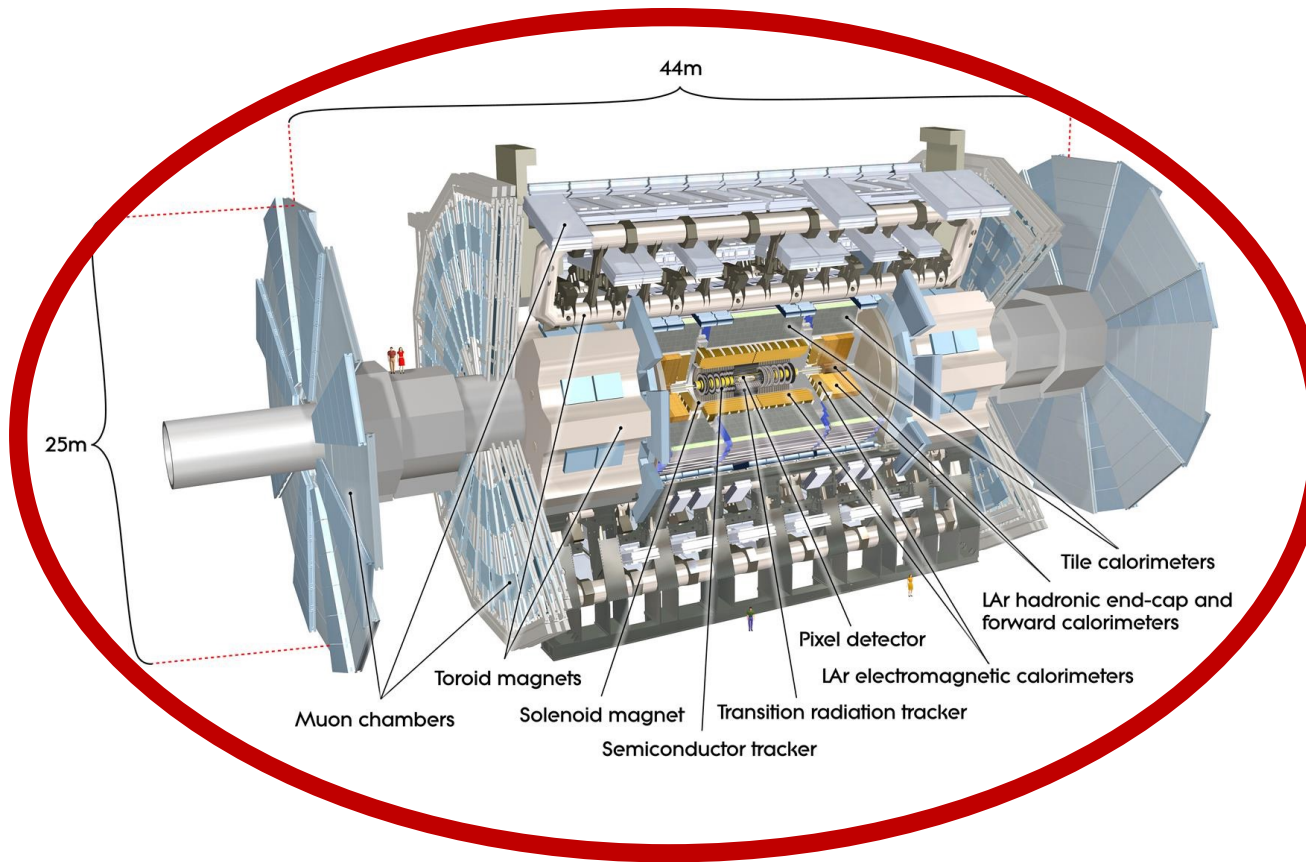
# Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

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On behalf of the ATLAS LAr Collaboration

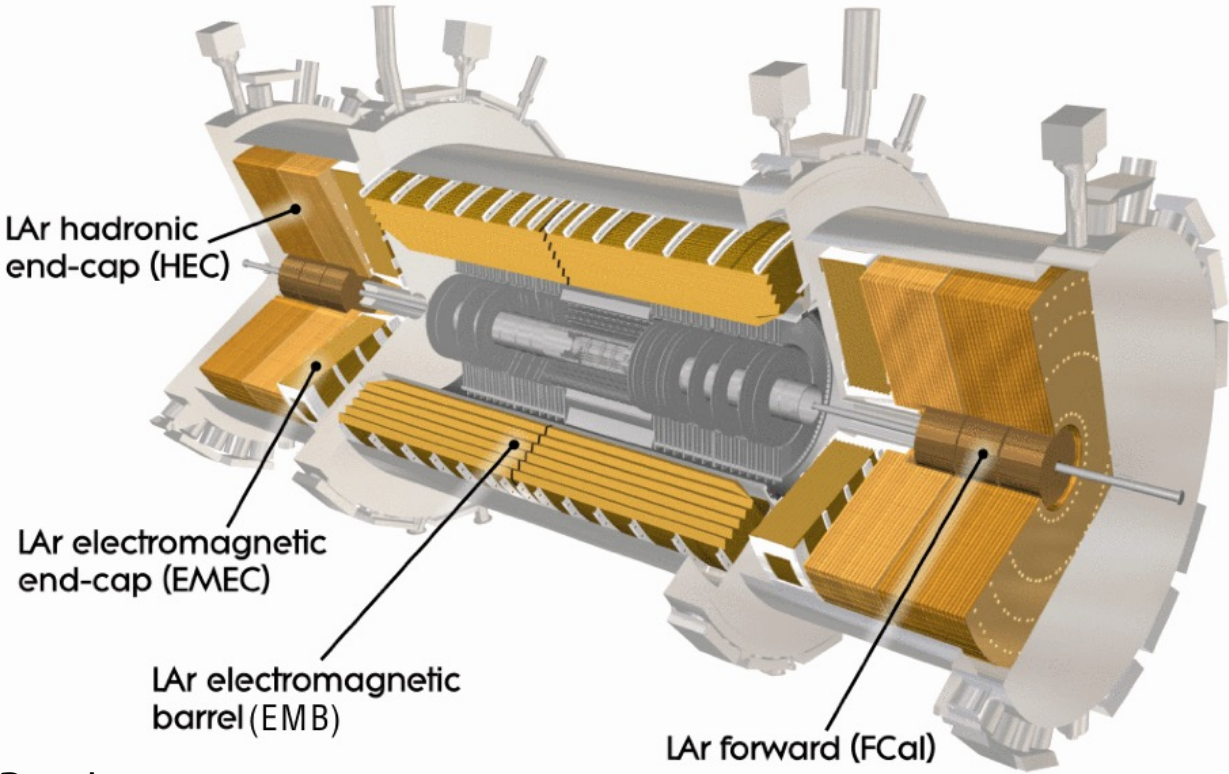
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# The ATLAS Detector & the Large Hadron Collider (LHC)



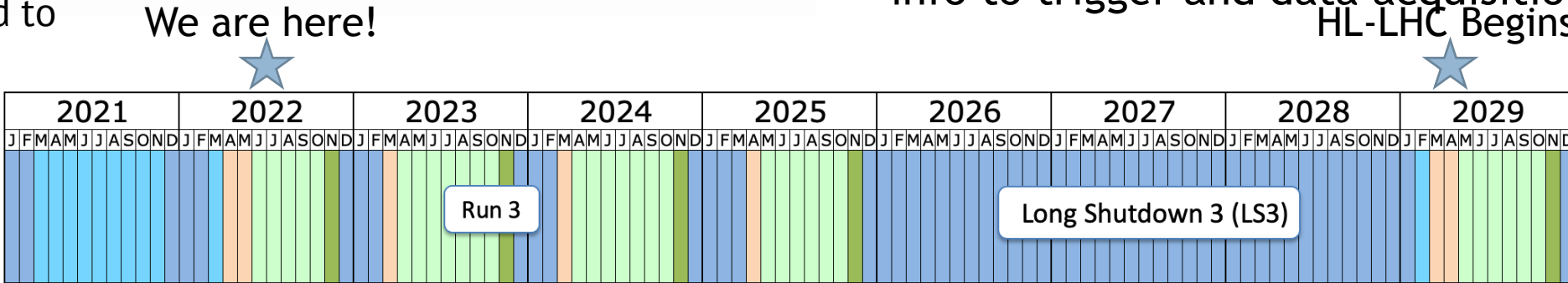
The LHC accelerates protons to produce beams of energy up to 7 TeV, which collide in the ATLAS detector with a frequency of 40 MHz.

# Overview of Liquid Argon (LAr) Calorimeter



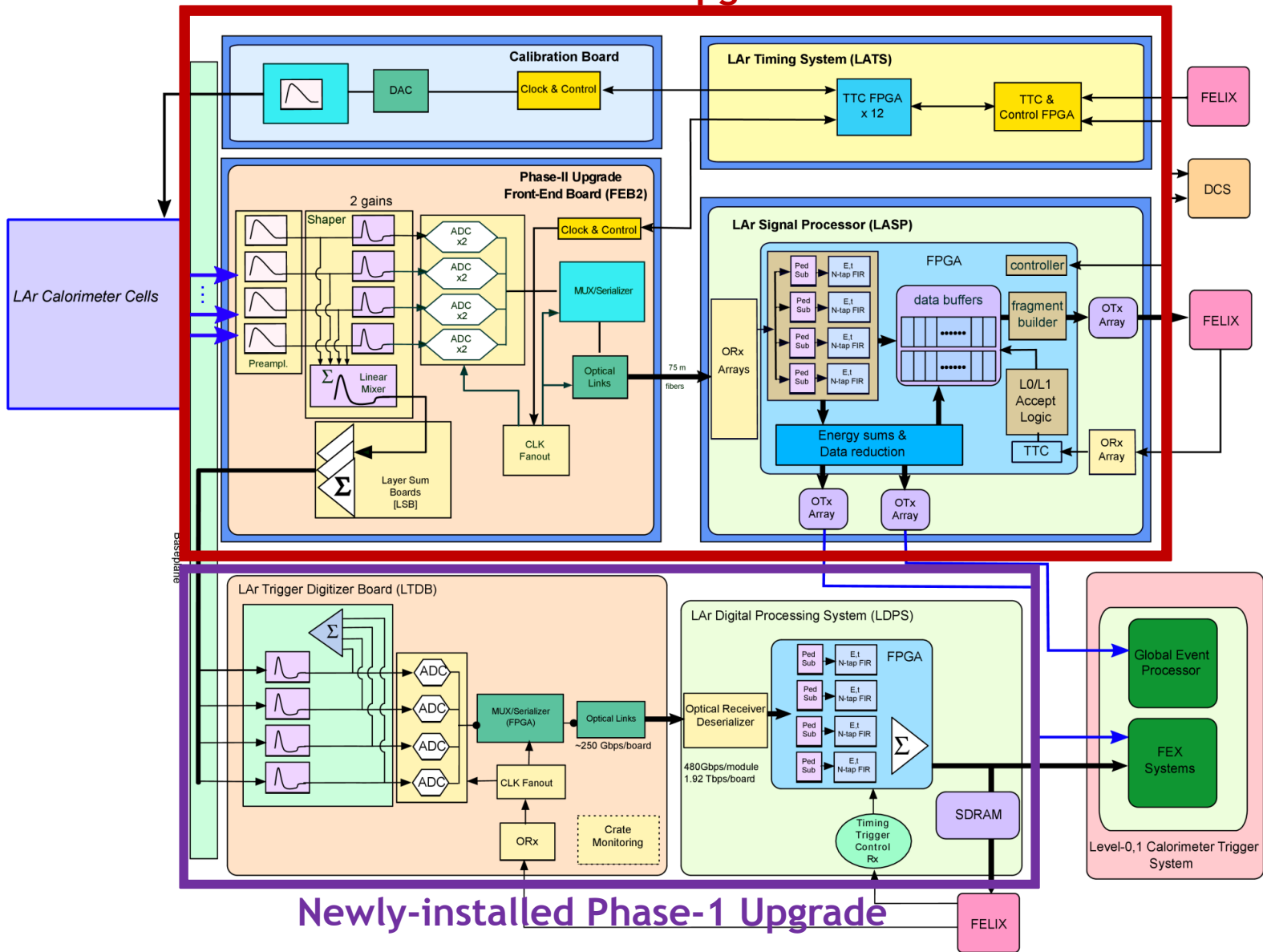
- Sampling calorimeter with liquid argon as the active medium.
- Captures energy information of interacting objects (e.g. electrons, photons, jets, for the EM calorimeter)
- This information is processed and propagated off the detector via the **readout electronics system**.
- **On-detector:** Samples cells at 40 MHz and sends digitized pulse off-detector for signal analysis and triggering.
- **Off-detector:** Applies digital filtering to extract energy and time for each cell, passes info to trigger and data acquisition system.

Readout electronics are being upgraded to handle HL-LHC conditions.



# LAr HL-LHC Upgrade Overview

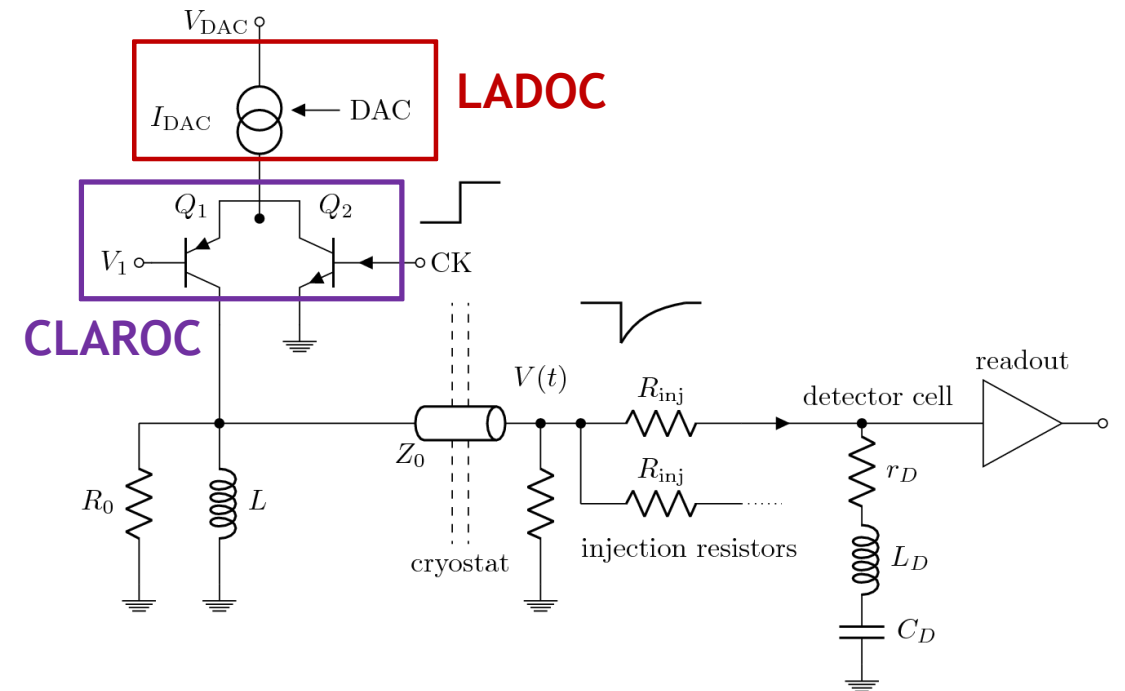
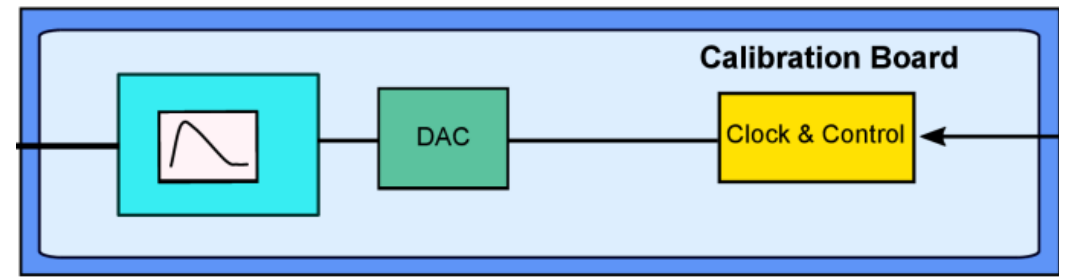
## HL-LHC Upgrade



- For HL-LHC, full upgrade of main readout chain.
- New readout will provide full granularity of the LAr calorimeter to hardware trigger.
  - Average number of interactions per bunch crossing increasing from 35 to up to 200 in HL-LHC
  - Provide data for trigger improvements, needed to maintain efficiency for physics analysis.
- New on-detector components: Front-End Board 2 (FEB2), Calibration Board
- New off-detector components: LAr Timing System (LATS) and LAr Signal Processor (LASP)

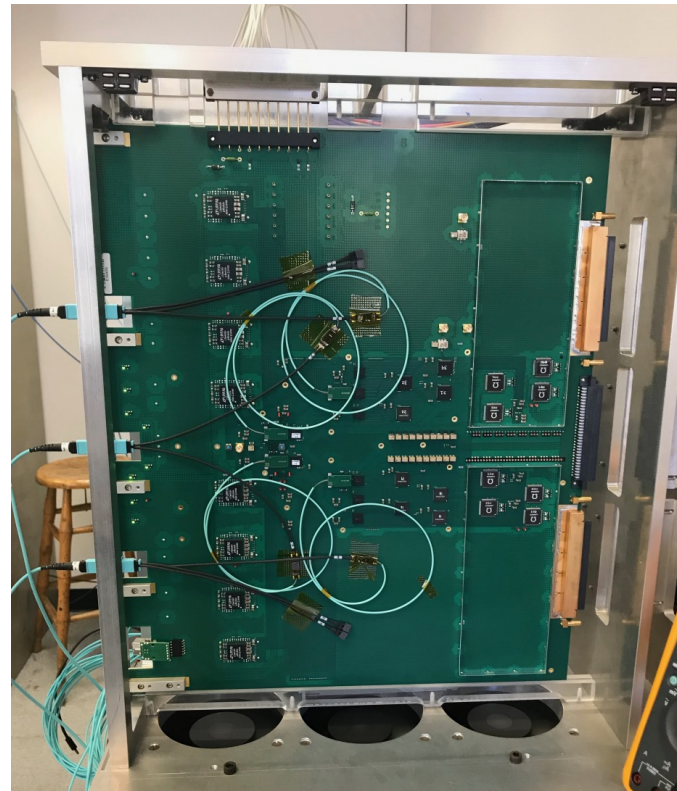
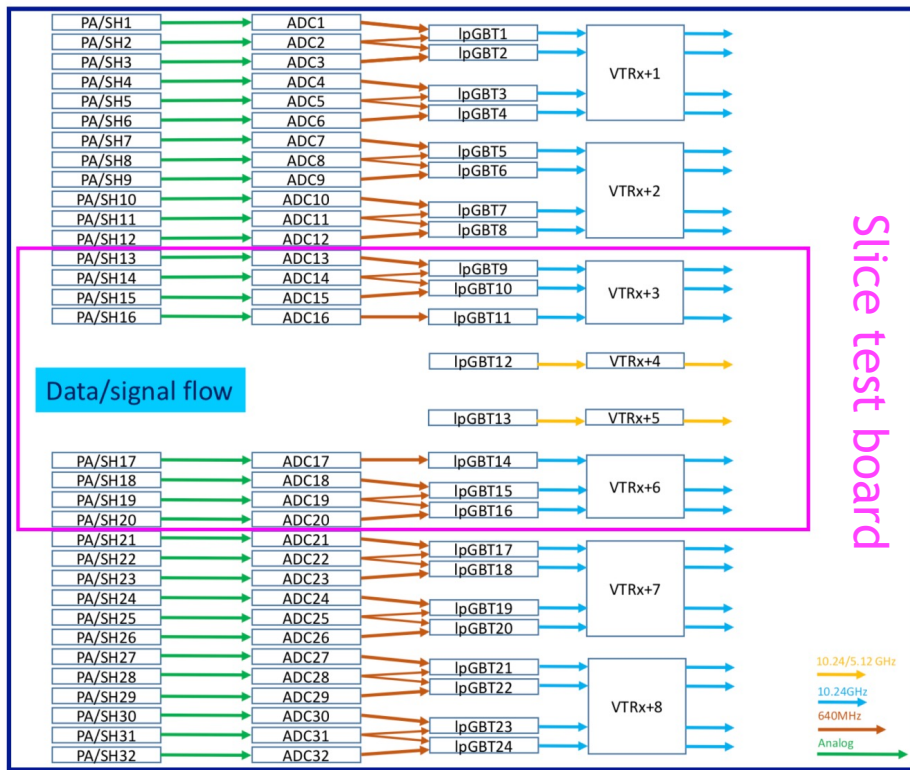
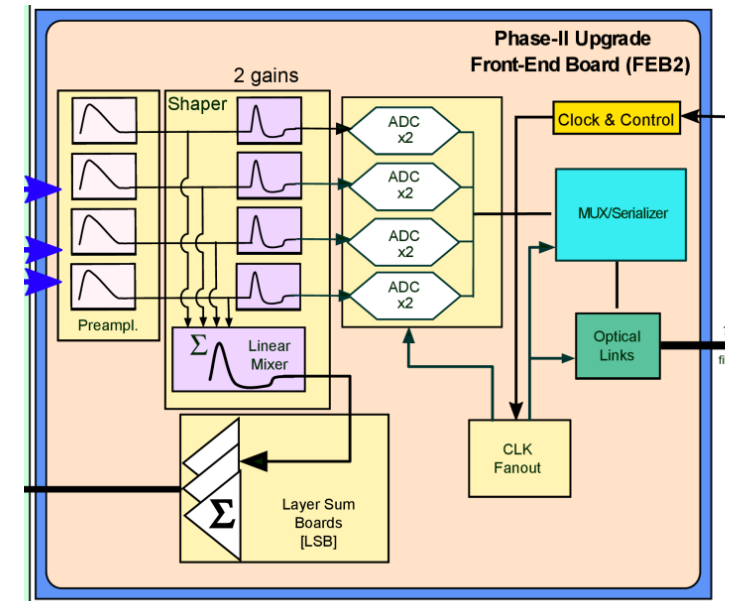
# Calibration Board

- Used to inject accurate calibrated signals directly in the liquid argon onto the calorimeter cells.
  - Provides pulse of known amplitude and shape for the calibration and testing of the readout board channels
  - 16-bit dynamic range, < 0.1% Linearity, radiation hard up to 14 kGy
- Need to calibrate 180k calorimeter cells = 122 boards with 128 channels each
- Using custom ASICs:
  - CLAROC** = creates pulse by opening high frequency switch (180 nm XFAB technology)
  - LADOC** = custom 16-bit DAC used to select the calibration current.
  - v4 of these ASICs are being produced to overcome radiation hardness and non-linearity, to be tested this year.
- 32-channel pre-prototype board (CABANON) passed specification review.
- Next up is prototype development and testing.



# Front End Board (FEB2)

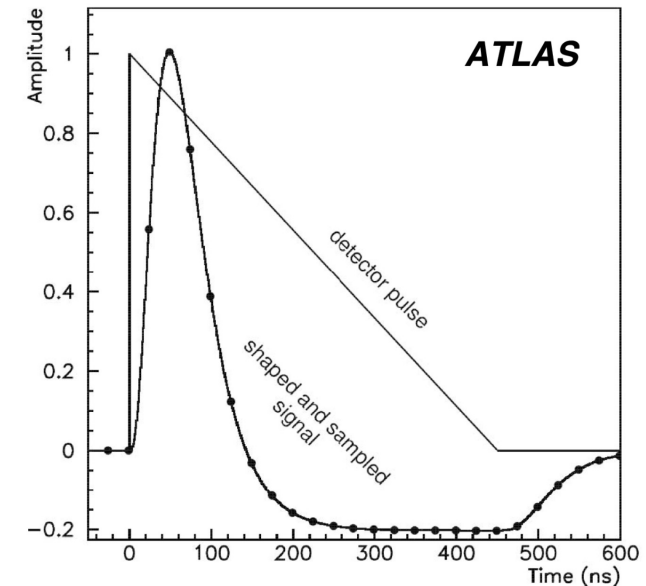
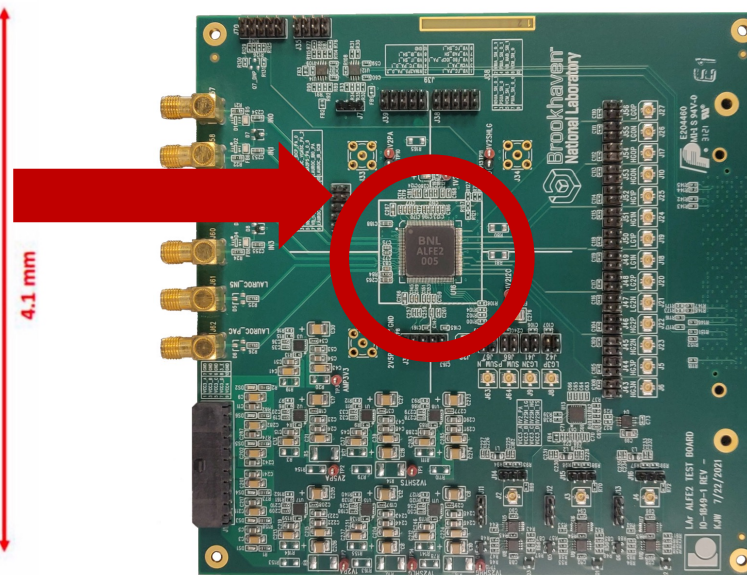
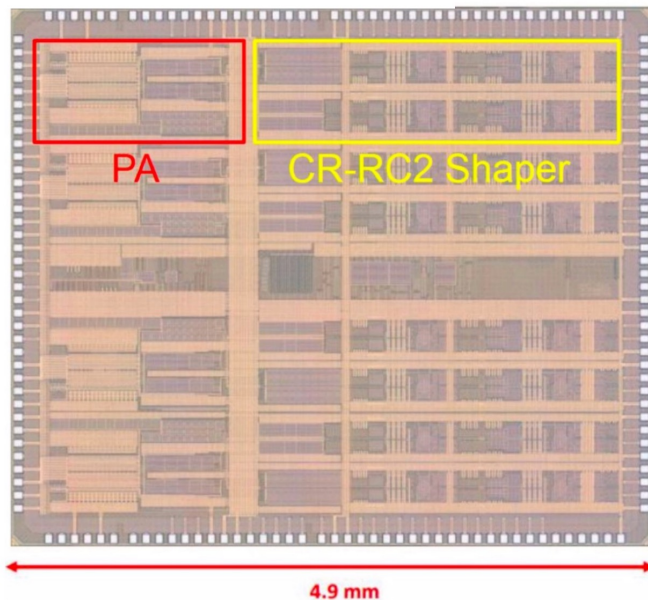
- Each FEB2 board will handle 128 channels (1524 total boards) and includes:
  - pre-amplifier/shaper ASIC (ALFE)
  - ADC ASIC (COLUTA)
  - lpGBT chips connected to bidirectional VersatileLink+ transceiver modules.



- FEB2 Test Boards produced with 32 channels
  - Validated multi-channel performance.
  - Control and readout on all channels tested.
- Next steps: towards the 128 channel FEB2 prototype

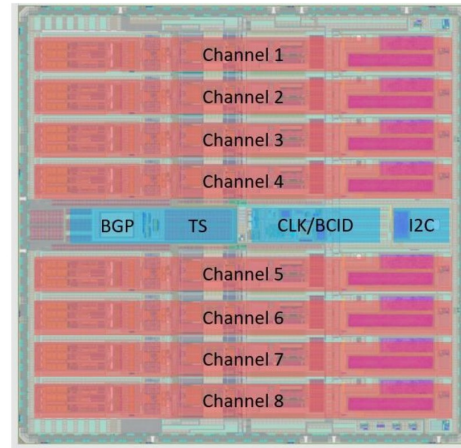
# FEB2 ASIC: Pre-Amplifier/Shaper

- Analog processing on signals:
  - Amplifies and shapes ionization pulses in two overlapping gain scales
  - 4 channel summing for hardware trigger
  - CR-RC<sup>2</sup> shaping
  - Large dynamic range : 10 mA for 25  $\Omega$  channels and 2 mA for 50  $\Omega$  channels
  - Noise : < 350 nA for 10 mA channels, Linearity: < 0.2%
  - Radiation tolerance: performant after 12 kGy dose (c.f. spec. 1.4 kGy)
- ALFE2: Current ASIC version meets analog precision and radiation tolerance specifications.

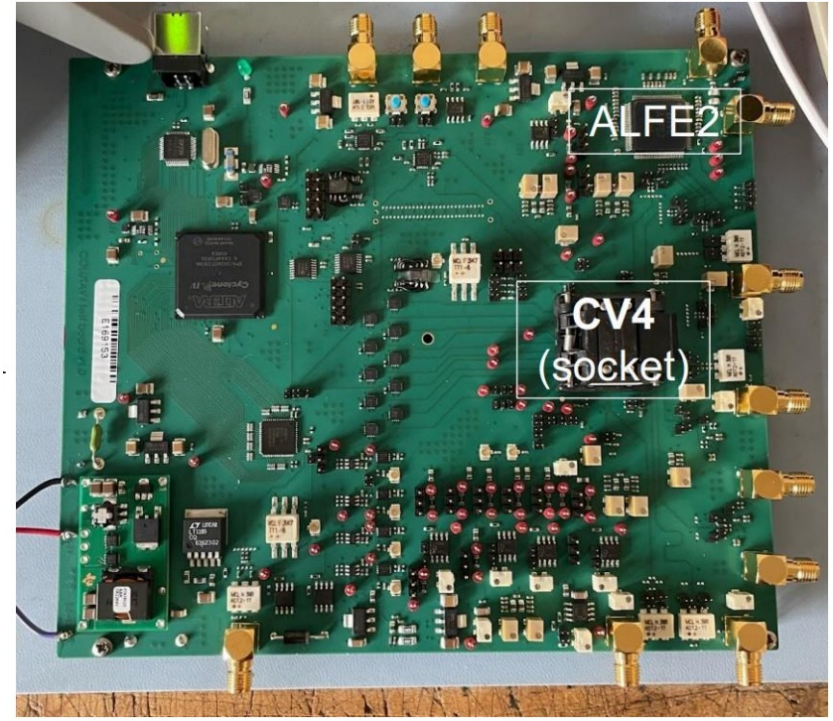
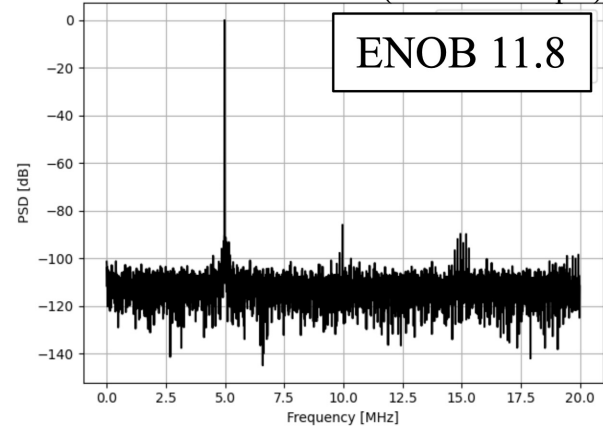


# FEB2 ASIC: Analog to Digital Converter (ADC)

- COLUTAv4 ASIC:
  - 8 channel, 15-bit ADC
  - MDAC+SAR+DDPU Architecture
  - TSMC 65nm
  - 40 MSPS
  - 5.854 x 5.456 mm<sup>2</sup>
  - 4.3 million transistors
  - 1.2 V operation with 2 V<sub>pp</sub> differential input
- Performance tests:
  - 18 ADCs tested over (almost) full dynamic range → achieved > 11 bit ENOB
  - Pre-amp/shaper integration using ALFEv2
  - Radiation test boards received, tests planned for August



Socketed chip performance  
Near full-scale amplitude, frequency of 5 MHz  
and measured on channel 1 (transformer input)



COLUTA v4 ASIC test board

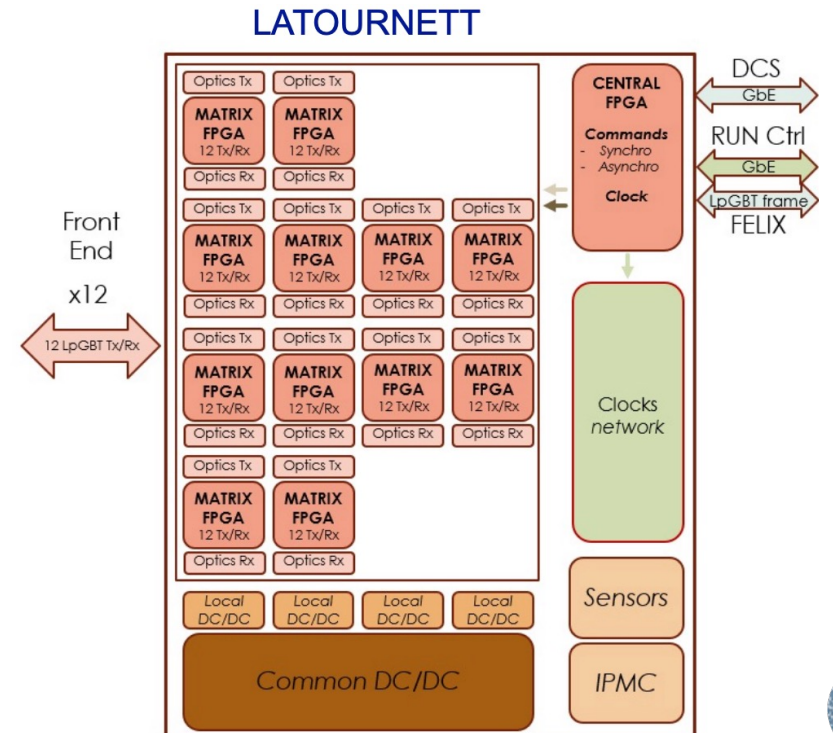
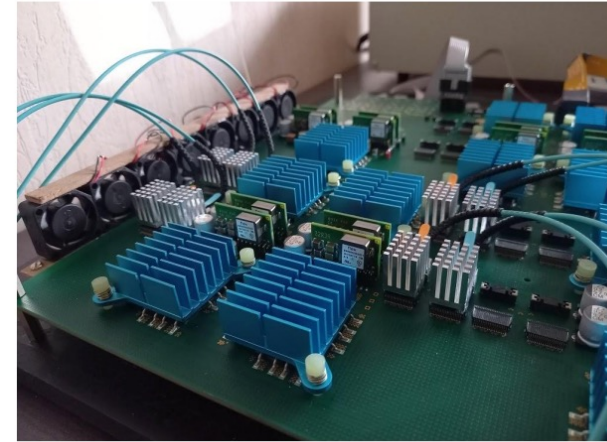
Soldered chip achieves ENOB > 12



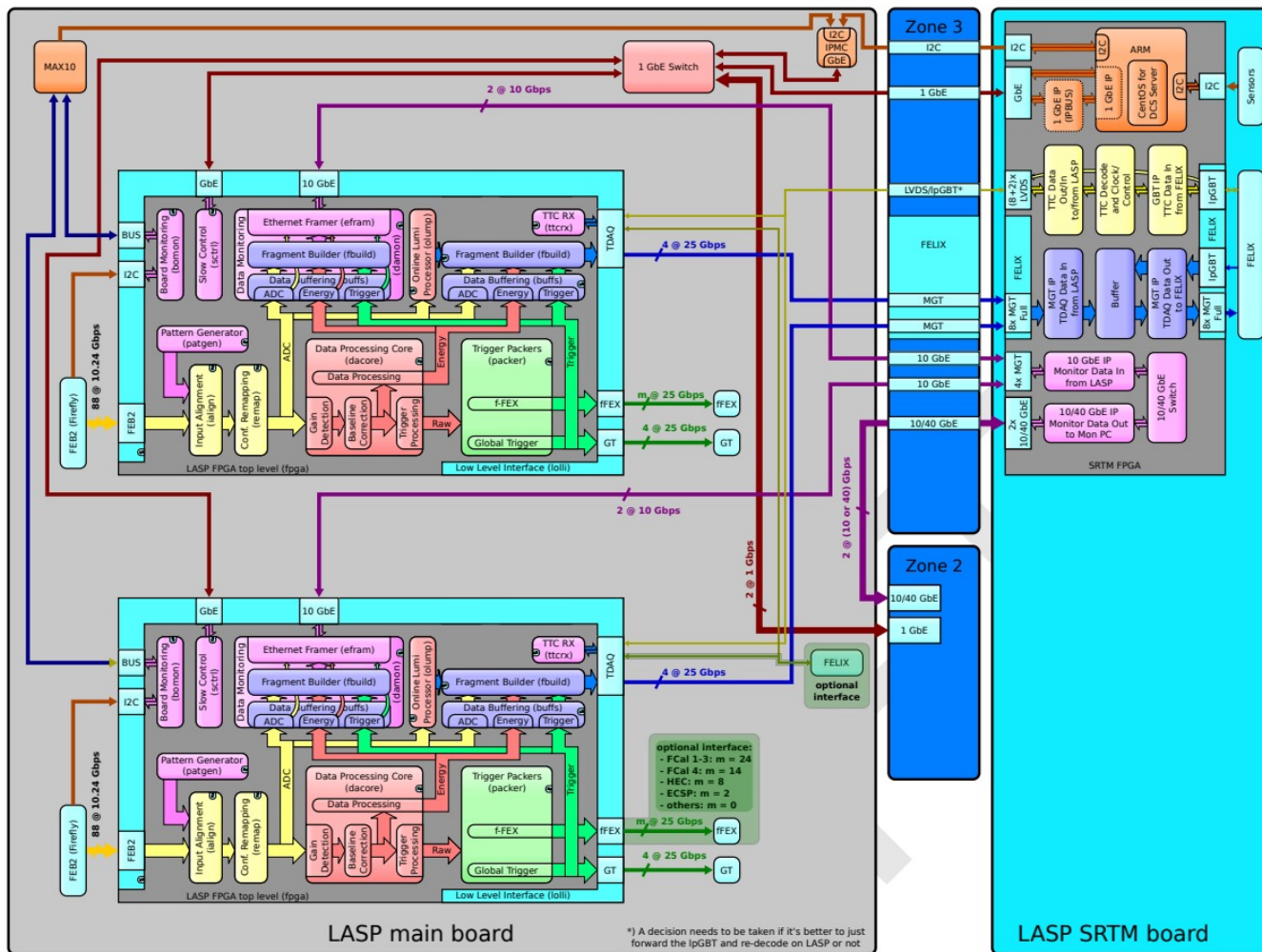
# LAr Timing System (LATS)

- Requirements:
  - Trigger, timing and control (TTC) for 1524 FEBs and 122 Calibration boards, 2 links per board, based on lpGBT protocol
- LATOURNETT: ATCA board
  - ~26 total
  - One central and 12 “matrix” Cyclone10 GX FPGAs
  - Schematic design underway & table test bench recently developed
- Current testing status:
  - Central and matrix FPGA firmware validated in simulation
  - Power-up sequence verified with POWERv2 board
  - Temperature tests inside crate
- Next up is prototype submission and integration with on-detector boards!

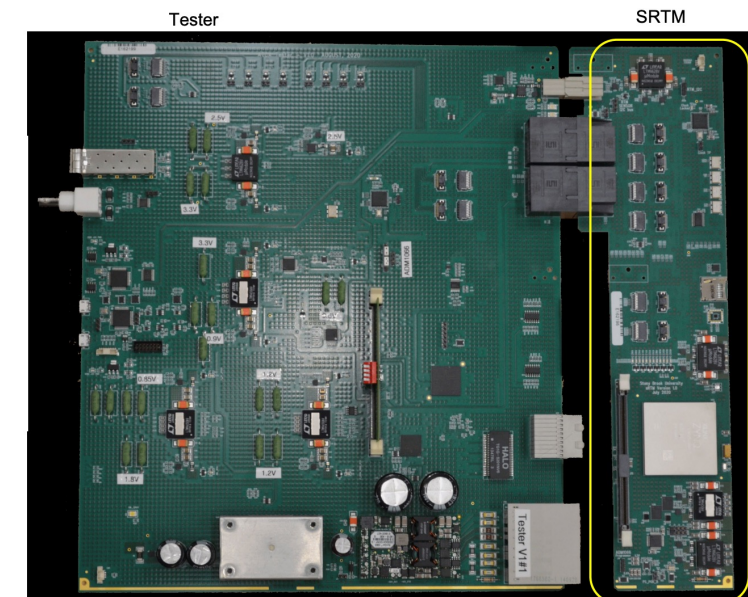
LATOURNETT Power v2: with Fireflies & heatsinks



# LAr Signal Processor (LASP) and Smart Rear Transition Module (SRTM)

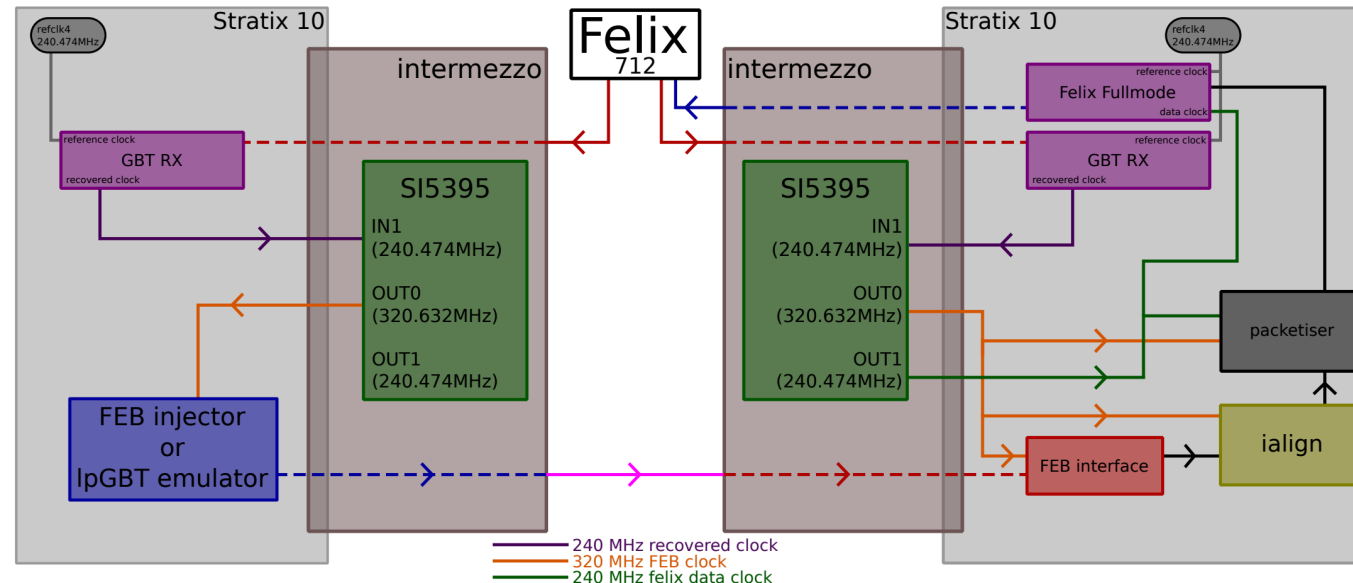


- **Purpose:** Apply digital filtering to digitized waveforms from FEB2, calculate energy & time, and transmit to trigger and DAQ.
- 200-278 of each board, 6 FEB2 per blade (2 FPGAs), outputs to L1 global and forward TDAQ at 25 Gbps.



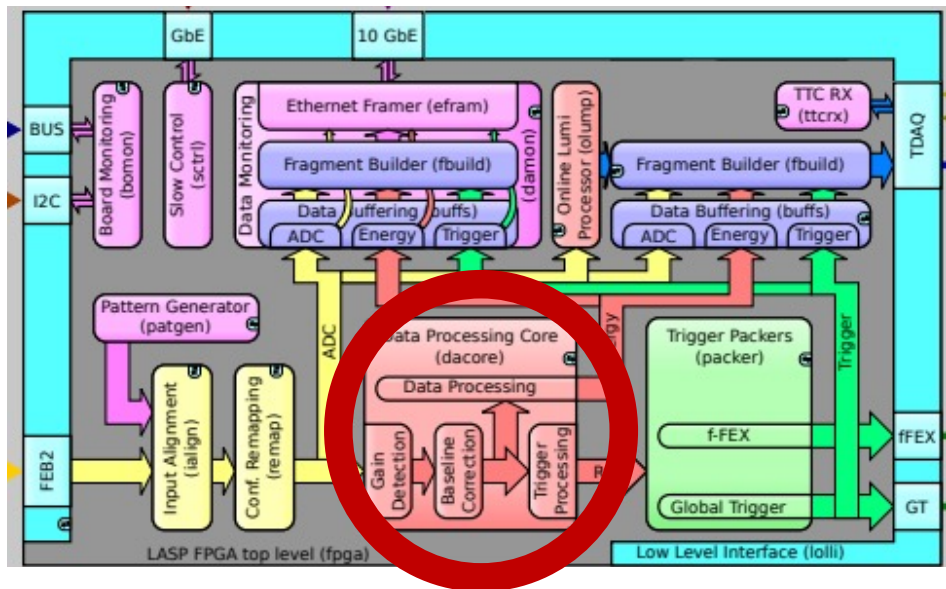
# LAr Signal Processor (LASP) and Smart Rear Transition Module (SRTM)

- Latest results:
  - v1 testboard with full capability: validation of power sequencing, i2c sensors, clock, FPGA configuration
  - Switched from Stratix-10 FPGA to Agilex.
  - Slice-test firmware developed to receive and process data from a FEB2 slice testboard (32 LAr cells, 6 data fibers)
- Next up are more measurements with test board and full prototype design

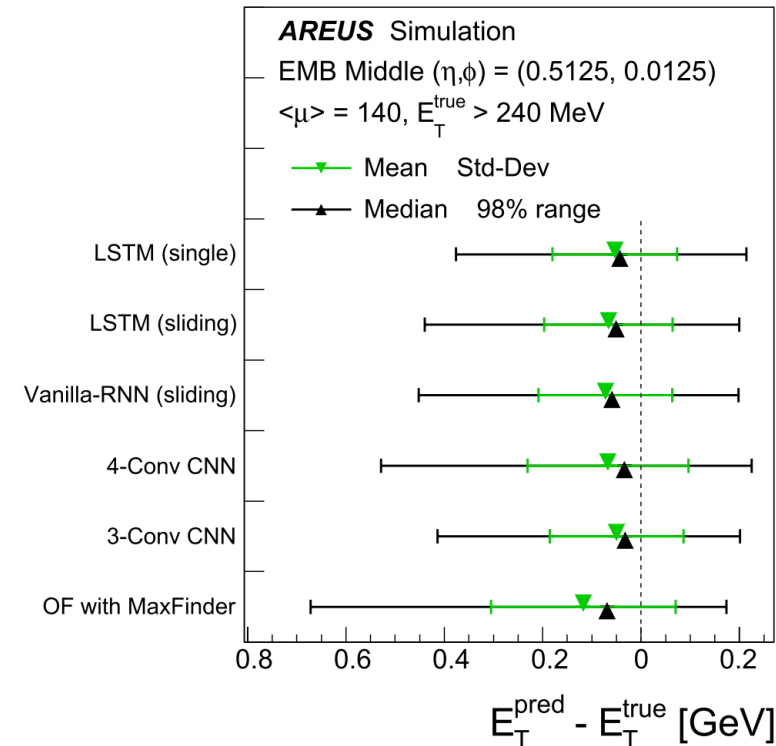


# LASP and Machine Learning

- Given the up to 200 pile-up collisions at HL-LHC, overlapping pulses are expected to lead to degradation in energy, timing and trigger performance.
- The current Optimal Filter approach to energy reconstruction may be improved by machine learning algorithms in FPGA's Data Processing Core!
- Recurrent and convolutional neural networks, and long short-term memory algorithms are being explored.



LASP FPGA Firmware Diagram



# Summary/Overview

- The LAr Calorimeter is necessary for the success of the physics program of the ATLAS Collaboration.
  - Challenges: Much higher pileup, possible increased energy, increased granularity of information for trigger, higher radiation.
  - Solution: Complete replacement of on- and off-detector readout electronics by 2029.
- Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC continues at a good pace.
  - Full custom LAr-specific ASICs at or approaching last “prototype” stage before production.
  - Work ongoing toward full slice + systems test.
  - Off-detector firmware is continuing to develop.
- On track for ATLAS installation after Run-3!