The TileCal PreProcessor Interface with the ATLAS Global Data Acquisition System at the HL-LHC

Antonio Cervelló, *Fernando Carrió, Raimundo García, Julio Martos, Jesús Soret, José Torres, Alberto Valero*
on behalf of the **ATLAS Collaboration**
Instituto de Física Corpuscular (CSIC - UV)

ATLAS TILE CALORIMETER PHASE-II UPGRADE

The **Large Hadron Collider (LHC)** has envisaged a series of **upgrades towards a High Luminosity LHC (HL-LHC)** delivering **five times the LHC nominal instantaneous luminosity**, that will take place throughout **2026-2028**, corresponding to the **Long Shutdown 3**. During this upgrade, the **ATLAS Tile Hadronic Calorimeter (TileCal) will replace** completely on- and off-detector electronics adopting a **new read-out architecture**.
Signals captured from TileCal are **digitized** by the on-detector electronics and **transmitted to the TileCal PreProcessor (TilePPr)** located off-detector, which provides the **interface with the ATLAS trigger and data acquisition systems.**
TilePPr receives, **process** and **transmits** the **data** from the on-detector and transmits it to the **Front-End Link eXchange (FELIX) system**. FELIX is the **ATLAS common hardware** in all the subdetectors **designed to act as a data router**, **receiving** and **forwarding data** to the **SoftWare Read-Out Driver (SWROD)** computers. **FELIX also distributes** the **Timing, Trigger and Control (TTC)** signals to the **TilePPr** to be propagated to the on-detector electronics. The **SWROD** is an **ATLAS common software** solution to **perform detector specific data processing**, including **configuration**, **calibration**, **control** and **monitoring** of the partition.
In this **contribution** we will **introduce the new read-out elements for TileCal at the HL-LHC**, the **interconnection** between the **off-detector electronics and the FELIX system**, **configuration** and **implementation** for the **test beam campaigns**, as well as **future developments** of the **preprocessing** and **monitoring** status of the **calorimeter modules** through the **SWROD infrastructure.**

DATA TRANSFER SCHEME IN THE TILE CALORIMETER FOR PHASE-II

TilePPR is the **core element** of the **back-end electronics.** Provides the interface between the front-end electronics and the ATLAS global data acquisition as well as the trigger systems. It is capable to **read up to 8 Tile super drawers.**
It is composed by an **ATCA Carrier board** that is equipped with **four Compact Processing Modules (CPM)** and one **Trigger and Data Acquisition interface (TDAQi)**. Along with these components, a **Tile Computer-on-Module (TileCoM)** is **connected** into the **ATCA carrier** board. **32 TilePPr modules** are needed to operate the **complete TileCal detector.**
The **CPMs are responsible** of the **distribution** of the **LHC clock** and the **TTC** command towards the on-detector electronics, **control and read-out of the Tile modules**, as well as the **cell energy reconstruction** and **transmission of data to TDAQi and FELIX.**
TileCoM provides **remote configuration** of **on-detector electronics**, **interface** the **TilePPr with the ATLAS Trigger and Data Acquisition (TDAQ)** system and with the **ATLAS Detector Control System (DCS).**
TDAQi receives reconstructed energy from the CPMs and **creates the trigger primitives** for L0Calo, L0muon and the global systems.

**Tile PPr system equipped with 4 CPMs and a TDAQi**
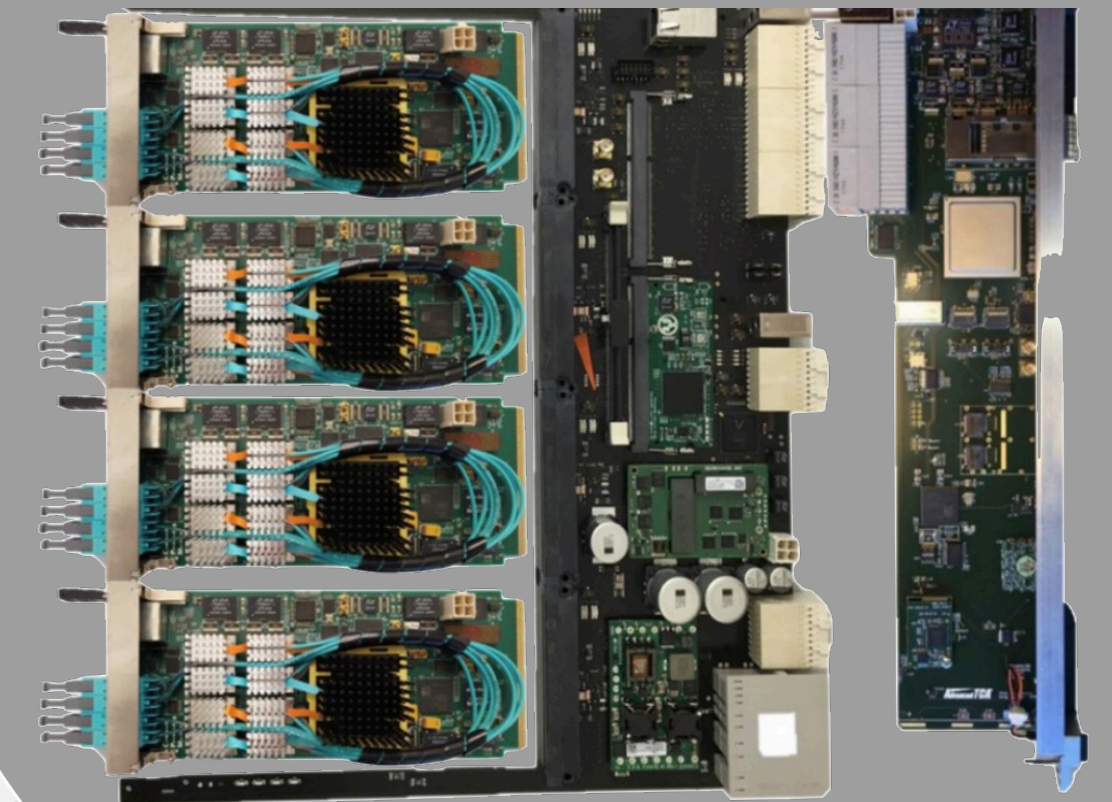
Downlink
4.8 Gbps (GBT MODE)

Uplink
9.6 Gbps (FULL MODE)

FELIX system has been developed to be the **primary interface** between the **front-end electronics and the DAQ system** of the detector, **acting as a router** for the transfer of the data packets from the front-end electronics. This is the **uplink path** which reaches up to **9.6 Gbps** in **Full Mode** configuration. This path demands high data bandwidth due to the amount of data coming from the detector.
FELIX will also serve as a **provider** of the **trigger acceptance signal and clock information** from the TTC system to the drawers in the detector. This is the **downlink**, which reaches data rates **up to 4.8 Gbps in GBT latency optimized protocol** given that in opposition of the downlink case, **we need deterministic latency** in this path to properly recover the LHC clock.
TileCal complete readout system will be composed of **161 bi-directional links** with FELIX, where **128** of them will be used for **data readout**, **32** for **trigger primitives** monitoring and **1** for the Interface of the LAser system to the New Acquisition infrastructure (**ILANA**).

FELIX card (FLX-712) used for Phase-I systems

SWROD

Network and
Commercial Off-the-shelf (COTS)
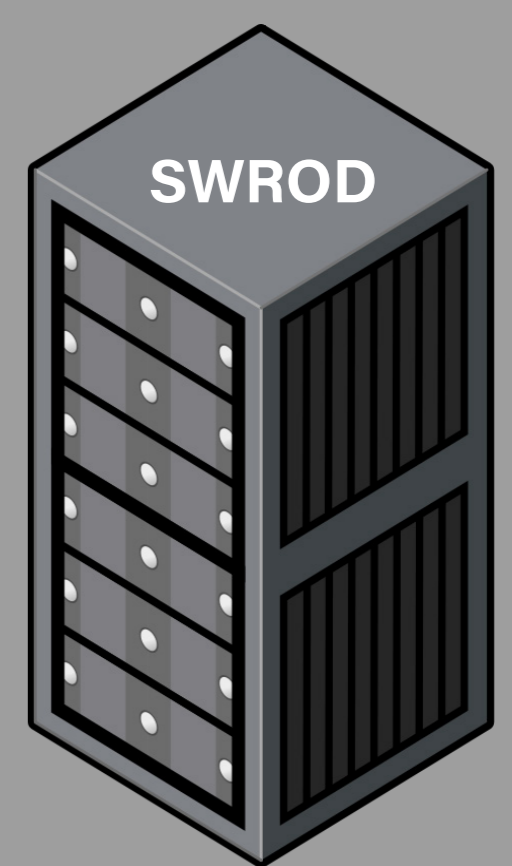
SWROD is envisaged to act in the ATLAS dataflow as the **handler between the FELIX system and the ATLAS HLT schema.**
Each **subsystem** has **custom functions in SWROD** regarding the data processing, formatting, verification and monitoring that were previously performed by the custom electronics like the RODs used during Run 1 and Run 2.
TileCal custom build function will be responsible for **TTC information**, **data integrity and small data processing**, as well as to provide for **online monitoring** to the Data Quality Monitoring Display (DQMD).

Test Beam Setup
3 Cherenkov Counters
2 wire chambers
TileCal Modules
2 trigger scintillators (S1 & S2)
Muon hodoscope

FRONT END DATA

Tile PPr

TTC Crate

TTC

TTC

FELIX

DATA

DATA

Legacy ROD

SWROD

DATA

TESTBEAM PERIODS AND POINT 1 FUTURE ACTIVITIES

Data acquired by the electronics of the **upgrade module** located in the **TestBeam** area is **sent to the PPr demonstrator**. This data is then formatted into a **new data packet** that is **forwarded to FELIX**. FELIX captures this packet and publish it via network at which point **SWROD** subscribes and **captures the data packets** to be **saved** into the system in the **ATLAS event format** for offline processing.
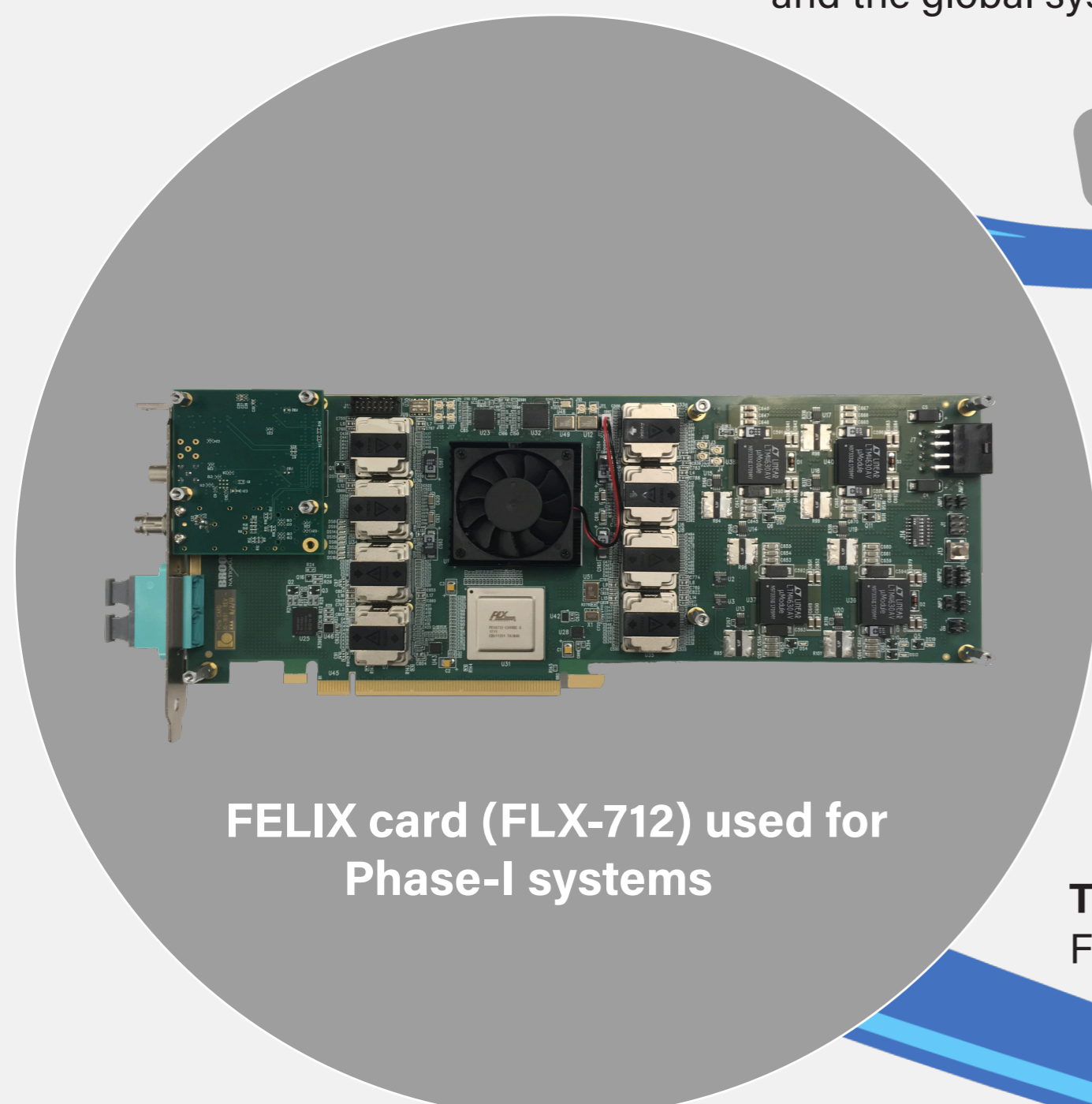For further verification of the data received, **same data that is captured** from the front-end electronics **and received in the PPr demonstrator** is **sent to one of the ROD inputs** from the legacy system to be analyzed and compared.

Future test beam periods will be followed by a numerous amount of upgrades for the readout. **Tile PPr** demonstrator will be **replaced by** the final prototype design composed by an **ATCA crate with an ATCA carrier, TDAQi and CPM.**
CPM will **provide** the **data output received by FELIX**, at the same time **FELIX will provide** the **TTC signals** to the CPM **to be propagated** into the front-end electronics
Monitoring systems of the acquired data **will be implemented** into the DQM system in TDAQ with the help of SWROD.
Further test of the electronics and the readout path will **validate the design** and provide access to the **installation of FELIX and SWROD into P1** to capture data from the **Tile demonstrator** located in the **ATLAS Experiment** for the **Run 3.**