

# A wide swing charge sensitive amplifier for a prototype Si-W EM calorimeter

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## Abstract

A wide swing charge sensitive amplifier (CSA) has been developed, as a part of a front-end electronics (FEE) readout ASIC, for a prototype silicon tungsten (Si-W) based electromagnetic (EM) calorimeter. The CSA, designed in 0.35  $\mu\text{m}$  N-well CMOS technology using 5V MOS transistors, has a wide linear operating range of 2.6 pC w.r.t the input charge with a power dissipation of 2.3 mW. A noise figure (ENC) of 820 e<sup>-</sup> at 0 pF of detector capacitance with a noise slope of 25 e<sup>-</sup>/pF has been achieved (when followed by a CR-RC<sup>2</sup> filter of 1.2  $\mu\text{s}$  peaking time). This design of CSA provides a dynamic range (ratio of maximum detectable signal to noise floor) of 79 dB for the maximum input charge of 2.6 pC when connected to a silicon detector with a capacitance of 40 pF. Using folded cascode architecture-based input stage and low voltage high swing current mirrors as the load, the CSA provides an enlarged output swing when biasing the output node towards one supply rail and utilizing the voltage range towards the opposite rail. The design philosophy works for both polarities of a large input signal. This paper presents the design of CSA with a wide negative output swing for an anticipated input signal of positive polarity in the target application with a known detector biasing scheme.

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## 1. Introduction

The continuous advancement in the field of particle accelerators for the next generation of high energy physics (HEP) experiments [1] puts forward significant challenges of particle identification, separation, and analysis. Advanced HEP detectors like highly granular calorimeters [2, 3, 4] demand high-density readout FEE with a wide dynamic range (about 80 dB) and a precision better than 1% [1]. Hence, the first stage preamplifier design in the readout FEE chain is critical and should satisfy the dynamic range requirements with adequate signal to noise ratio (SNR) in a power-efficient way to enable high-density integration.

As the first stage of FEE, the CSA is preferred primarily because of its low power, low noise configuration and charge gain's ( $A_Q$ ) insensitivity to a variation of detector capacitance ( $C_D$ ). For Si-W based EM calorimeter, which involves particle shower formation and dissolution, a wide dynamic range (simultaneous detection of maximum energy deposition  $\approx$  few pC in the shower maximum layers and detection of MIP particle, i.e.  $\approx$  4 fC for a silicon detector of  $300\mu\text{m}$  wafer thickness [5]) CSA is required as the first stage of FEE.

Various design approaches to address these critical requirements are reported in the literature. A switchable gain charge preamplifier is one of them with multiple feedback capacitances to improve the output swing [6]. Here, the gain variation has to be done either through slow peripheral control [7] or through additional gain selection circuitry involving comparator [8]. The latter option may introduce non-linear behaviour in the circuit during switching among the various gain modes. Two separate charge preamplifier channels with charge division/sharing methods using series capacitance is another reported design scheme [9]. However, this method requires one extra channel per detector element, leading to extra power dissipation, additional area consumption, a compromised low signal performance and increasing cost. A combination of

switchable gain CSA with ADC+ToT (Time over Threshold) technique is also reported [10] to extend the swing of the FEE. But, this method has faced few challenges like high cross-talk, long dead time, absence of smooth overlap between the ADC and ToT methods when the preamplifier goes from the non-saturation mode to saturation mode [11].

A wide swing CSA can facilitate all these design methods to achieve an even higher linear operating range. This paper thus reports a design technique to enhance the linear operating range of the charge preamplifier itself by optimizing the output dc point close to one supply rail while utilizing the voltage range toward the opposite supply rail as output swing. Section II presents the architecture of the CSA. The analysis for the major design parameters is provided in section III. Section IV describes the design methodology for the CSA. Simulation results and the layout view of the CSA are reported in section V. Section VI presents the test results of the fabricated and packaged CSA as a part of a bigger FEE ASIC. Finally, section VII concludes the paper.

## 2. Architecture: The CSA

The known detector biasing scheme in the target application for this CSA is shown in Figure 1a, where  $R_L$  is the detector bias resistance, D represents a P-N junction (diode) detector, and  $C_{cp}$  is the ac coupling capacitor between the detector and the CSA. In this biasing scheme with an N-type silicon PAD detector, the anode (p-type side) and cathode (n-type side) of the detector are connected to the negative HV and ground. As a result, the expected signal polarity at the output of the CSA is negative, and as it involves one polarity inversion, the equivalent signal polarity at the input will be positive, as shown in Figure 1a.

The CSA has been designed in 0.35  $\mu\text{m}$  CMOS technology using 5V MOS transistors with a typical  $V_{thn}=0.75$  V,  $V_{thp}=-1.0$  V, and  $k_n=100$   $\mu\text{A}/\text{V}^2$ ,  $k_p=30$   $\mu\text{A}/\text{V}^2$ . In this design, the CSA is optimized to have the output dc bias point close to the positive supply rail ( $\approx 4$  V) and utilize the voltage swing

towards the negative supply rail to allow a large negative signal swing. The threshold voltage of the input transistor ( $M_1$ ) puts the limit on the max output dc voltage. A schematic of the proposed CSA is shown in Figure 1b. The architecture of the CSA is based on three sections; a core amplifier stage ( $M_{1-9}$ ), a feedback network ( $C_f$  (an integrating capacitor) and  $R_f$  (a decay resistor)), and the biasing network ( $M_{10-14}$ ).

The core amplifier is designed using a folded cascode based input stage and low voltage high swing current mirror as the load. Folded cascode architecture facilitates high gain and wide bandwidth design with a minimum number of active components with enhanced output swing and ease of frequency compensation. Low voltage high swing current mirror architecture is chosen as the active load to satisfy the broader dynamic range requirement of the CSA. It reduces the voltage headroom requirement from  $2V_{dsat} + V_{th}$  of the cascode current mirror to  $2V_{dsat}$  apart from providing very high output resistance (of the order of  $g_m r_{ds}^2$ ) [12]. Assuming a conservative value of average  $V_{dsat}$  also, this architecture improves the output voltage swing to be wide enough into the supply rails ( $\sim V_{DD} - 4V_{dsat}$ ).

The value of  $C_f$  is a trade-off between the charge/conversion gain ( $A_Q$ ) and rise time (shown in Appendix A) of the CSA. This work aims to design a wide dynamic range CSA, so  $C_f$  was optimized to be 0.8 pF providing a  $A_Q$  of 1.25 mV/fC (lower  $A_Q$  leads to enhanced linear range w.r.t. input charge). The dc operating point is set by shunt-shunt feedback using a very high-value  $R_f$  (to reduce the thermal noise contribution  $4kT/R_f$ ).  $R_f$  is implemented by a series of transistors ( $M_{Rf1-27}$ ) operating in the linear/triode region with its gate voltage ( $V_f$ ) externally controlled to have a variable  $R_f$  (2 - 120 M $\Omega$ ) and adjustable fall time. Series connection of multiple transistors ensures low distortion and improved linearity over a large signal swing. In this design,  $V_f$  is externally adjusted for an equivalent feedback resistance of 75 M $\Omega$  providing a fall time constant of 60  $\mu$ s for the CSA output response, which again sets a limit in rate capability to  $\approx 10$  kHz.

The biasing network, consisting of transistor  $M_{10-14}$ , distributes the required

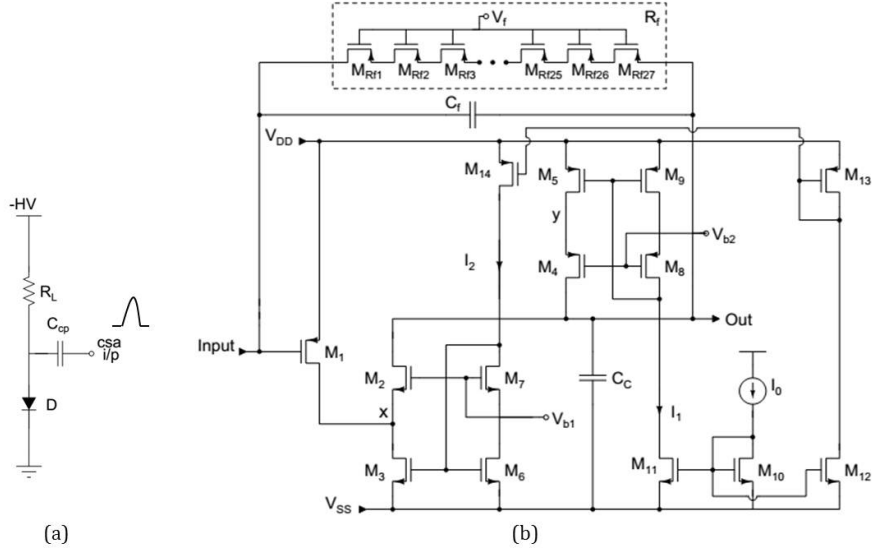


Figure 1: (a) Detector biasing scheme in the target application, (b) Schematic of the CSA.

current ( $I_1$  and  $I_2$ ) from a master current source ( $I_0$ ) through current mirroring action.  $V_{b1}$  and  $V_{b2}$  are optimized bias voltages for maximum swing.  $C_c$  is the compensating capacitor at the high impedance output node of the CSA to improve the stability response.

### 3. Design analysis

In this section, the analysis of the major design parameters (noise and ac performance) of the CSA is performed.

#### 3.1. Noise optimization

The primary noise contributors in a typical detector and front-end readout configuration (as shown in Figure A.7 in Appendix A) are the shot noise due to the detector leakage current and the electronic noise of the CSA. The expression for effective electronic noise at the input of the core amplifier (considering only

the thermal noise contribution of the transistors) of Figure 1b is

$$S_{vin,th}(f) = \frac{\frac{8kT}{3} \cdot (g_{m1} + g_{m3} + g_{m5})}{g_{m1}^2} \quad (1)$$

Where  $g_m$ 's are the trans-conductance of the respective transistors,  $k$  is the Boltzmann constant, and  $T$  is the temperature in Kelvin. By ensuring higher  $g_{m1}$ , the effective input noise will be dominated by  $M_1$ . Then, the total input-referred noise spectral density (including the 1/F noise) of the core amplifier can be expressed as [13],

$$S_{vin,tot}(f) = \frac{8kT}{3g_{m1}} + \frac{K_{1/f}}{c_{ox}^2 WLf} \quad (2)$$

Where  $g_{m1}$  is the trans-conductance of the  $M_1$ ,  $C_{ox}$  is the oxide capacitance per unit area,  $K_{1/f}$  is the flicker noise coefficient, and  $WL$  is the area of the input transistor. Equation 2 shows that the type of the input transistor, its working region, and operating parameters play a vital role in determining the noise level. In this work, the  $M_1$  is chosen to be PMOS as it is advantageous over NMOS regarding 1/F noise in submicron technology [14]. A very high aspect ratio (10,000) is used (discussed in section 4) for the  $M_1$  with a low bias current ( $I_d$ ) of 350  $\mu$ A to maximize the transistor  $g_m$  efficiency ( $g_m/I_d \approx 20$ ), with low current density ( $I_d/W \approx 0.07$  A/m) signifying the operation of the transistor in the sub-threshold region at the edge of weak/moderate inversion [15, 16].

### 3.2. ac analysis

The simplified small-signal equivalent model of the core amplifier is shown in Figure 2, where,  $c_{in} = c_{gs1}$ ,  $r_x = r_{ds1} || r_{ds3}$ ,  $c_x = c_{gd3} + c_{gs2} + c_{gd1} + c_{db1}$ ,  $G_{m2} = g_{m2} + g_{mb2}$ ,  $c_y = c_{gd5} + c_{gs4}$ ,  $c_{out} = c_c + c_{gd2} + c_{gd4}$ . Now ignoring the very high-frequency pole at node  $y$ , the above small-signal model can be approximated with a second-order system where the dominant pole is at the output high impedance node while the non-dominant pole is accompanied with the folded node ( $x$ ).

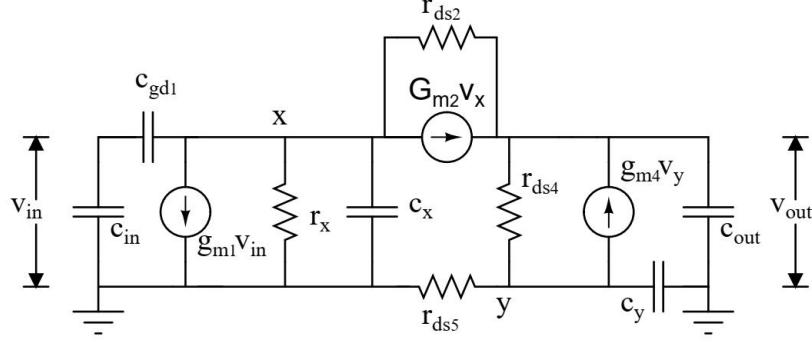


Figure 2: Simplified small-signal equivalent model of the core amplifier.

Hence the following expressions can be derived. The open-loop dc gain,

$$A_{v0} = g_{m1} \cdot r_{out} \quad (3)$$

The low frequency pole ( $p_1^*$ ) at the output,

$$p_1^* = -\frac{1}{2\pi \cdot r_{out} \cdot c_{out}} \quad (4)$$

Where,  $r_{out} = (g_{m2} \cdot r_{ds2} \cdot (r_{ds1} || r_{ds3})) || (g_{m4} \cdot r_{ds4} \cdot r_{ds5})$

The high frequency ( $p_2^*$ ) second pole,

$$p_2^* = -\frac{1}{2\pi} \cdot \frac{G_{m2}}{c_x} \quad (5)$$

The resultant UGB (Unity Gain Bandwidth) of the core amplifier,

$$UGB(f_0) = A_{v0} \cdot p_1^* = -\frac{1}{2\pi} \cdot \frac{g_{m1}}{c_{out}} \quad (6)$$

#### 4. Design methodology

The low power budget of 2 mW, defined by the application, roughly sets the maximum bias current for the CSA to be 400  $\mu$ A. The authors have set  $I_1$  to be 50  $\mu$ A, and  $I_2$  to be 400  $\mu$ A and reasonable  $V_{dsat}$  for each transistor according to the bias current, voltage swing, and transistor specific operating region requirements. Since  $M_3$  carries the maximum current, it has been assigned a larger

$V_{dsat}$  of 500 mV, while the cascode transistor  $M_2$  has been provided with 200 mV of  $V_{dsat}$ .  $V_{dsat}$  of 300 mV has been set for  $M_4$  and  $M_5$  in the current mirror load due to the lower mobility of the PMOS transistors.  $V_{b1}$  and  $V_{b2}$  are biased at  $V_{th,M2} + V_{dsat3} + V_{dsat2}$  and  $V_{DD} - V_{th,M4} - V_{dsat4} - V_{dsat5}$  respectively to ensure the output swing of the core amplifier is  $V_{DD} - V_{dsat5} - V_{dsat4} - V_{dsat3} - V_{dsat2}$ . A very low  $V_{dsat}$  of 50 mV has been considered for the input transistor  $M_1$ , to obtain a high  $g_m$  value with a low bias current. Aspect ratios are calculated based on the equation shown in Table 1, which are later optimized to achieve the high dc loop gain ( $A_{v0} > 80$  dB) for maximum charge transfer from the detector to the CSA, low input impedance ( $Z_{in}$ ), and subsequently low crosstalks among the adjacent channels [17]. Minimum allowed transistor length ( $L_{min}$ ) is used for the input transistor ( $M_1$ ) to ensure maximum  $g_m/C_{gs}$  ("Figure of Merit") [14, 18]. The cascode transistor ( $M_2$ ) is designed with a higher aspect ratio to place the non-dominant pole of the core amplifier away from the 3-dB frequency of the closed-loop system of CSA coupled with a detector, discussed in section 4.1 and Appendix A.  $M_3$  and  $M_5$  are designed with larger L and higher  $V_{dsat}$  to reduce their noise contribution. The calculated and the final aspect ratio of the transistors are given in Table 1. An aspect ratio of 0.5 is kept for the feedback transistors ( $M_{Rf1} - M_{Rf27}$ ) to ensure they work in the linear region.

Table 1: Aspect ratio of the transistors in the core amplifier

Transistor	$I_d$ ( $\mu A$ )	$K_{eff} = \mu C_{ox}$ ( $\mu A/V^2$ )	$V_{dsat}$ (V)	Calculated (W/L) $= 2 \cdot I_d / (K_{eff} \cdot V_{dsat}^2)$	Final (W/L)	Operating Region*
$M_1$	350	30	50m	10000	10000	3
$M_2$	50	100	200m	25	100	2
$M_3$	400	100	500m	32	50	2
$M_4$	50	30	300m	40	50	2
$M_5$	50	30	300m	40	50	2

\*3: Sub-threshold region (edge of weak/moderate inversion), 2: Saturation region.

Table 2 provides the dc bias voltages at different nodes in the circuit.



Table 2: Bias voltages at different nodes in the circuit

Sr Number	Node	dc bias point (V)
1.	Input	3.985
2.	x	0.42
3.	Out	3.985
4.	y	4.5
5.	$V_{b1}, V_{b2}$	1.5, 3.2

#### 4.1. Design calculation

In this design for the core amplifier, with the value of  $g_{m1} \approx 7$  mS,  $c_{out} \approx 4.5$  pF, the value of  $f_0$  is  $\approx 247$  MHz. According to 4 and 5, the low-frequency pole ( $p_1^*$ ) of the core amplifier is at 1.8 kHz, while the high-frequency pole ( $p_2^*$ ) is at 50 MHz with  $r_{out} \approx 20$  M $\Omega$ ,  $c_x \approx 3.5$  pF, and  $G_{m2} \approx 1.1$  mS. The calculated open-loop dc gain is 103 dB. The second-order transfer function of the closed-loop system incorporating the CSA coupled with a silicon detector (as shown in Appendix A), involves two poles  $p_{rfcf}$  due to the feedback network ( $R_f$  and  $C_f$ ) and  $p_{cfb}$  due to the network involving  $C_f$ ,  $C_t$ , the core amplifier. The location of these two poles can be calculated as (considering negligible load at the output),

$$p_{rfcf} = \frac{1}{2\pi \cdot R_f \cdot C_f} = 2.7 \text{ kHz} \quad (7)$$

$$p_{cfb} = \frac{f_0 \cdot C_f}{C_t} = 4.4 \text{ MHz} \quad (8)$$

Where, with detector capacitance of 40 pF,  $C_t \approx 45$  pF. The closed-loop bandwidth (-3dB frequency) is evaluated by Equation 8, which is also the unity gain frequency of the charge feedback loop. The dominant pole (Equation 7) is around 2.7 kHz, and the non-dominant pole ( $p_2^*$ ) sits at a frequency around 50 MHz. The overall phase margin of the system is then given by (Equation

9).

$$PM = \tan^{-1}\left(\frac{p_2^*}{p_{cfb}}\right) = 85 \text{ degree} \quad (9)$$

## 5. Simulation results

The physical design of the CSA has been carried out using an inter-digitized layout for the large input transistor [12], using multiple contacts, frequent substrate contact, and guard rings to minimize the parasitic noise due to the resistive poly gate and distributed substrate resistance. Figure 3 shows the layout view of the designed CSA (415  $\mu\text{m}$  x 200  $\mu\text{m}$ ) as a part of the 16 channel pulse processing ASIC (5.6 mm x 5.2 mm) developed as FEE for Si-W calorimeter.

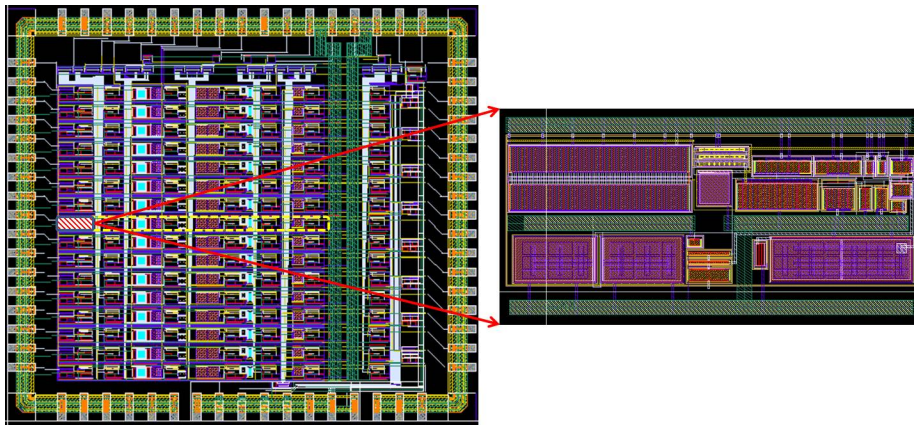


Figure 3: Layout view of the 16 channel pulse processing ASIC highlighting a single channel (yellow dotted) and CSA block (red hashed) along with a zoomed layout view of the CSA.

The simulations of the CSA were carried out with the silicon extracted view across all the design corners provided by the foundry. To inject a test charge in the simulation, a tail pulse (using an exponential voltage pulse) was used with a test (coupling) capacitor (0.8 pF to have the closed-loop voltage gain of 1) connected in series with the CSA input. The transient response at the CSA output is shown in Figure 4. The output dc point of the CSA is biased at 3.985 V and a linear behaviour of the CSA circuit can be seen up to a injected test

charge of  $\approx 2.8$  pC (corresponds to input voltage of 3.5 V into a 0.8 pF coupling capacitor).

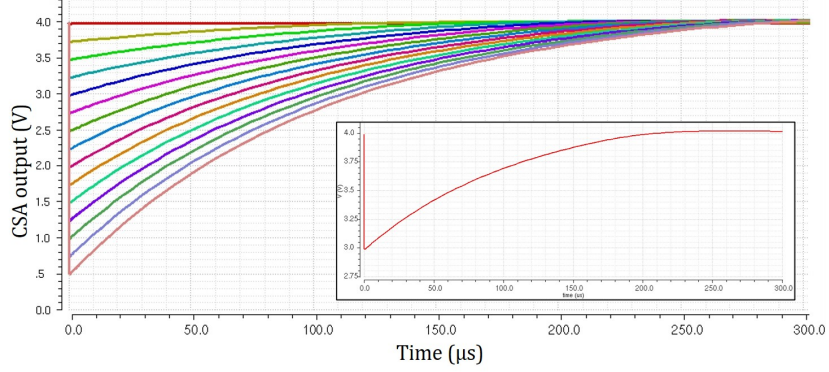


Figure 4: Transient response of the CSA with linear behaviour up to a test charge of 2.8 pC with a zoomed view in the inset showing response with 0.8 pC of input charge.

Table 3 summarizes the salient design features of the simulated CSA with a 40 pF detector capacitance ( $C_{det}$ ).

Sr. No	Parameter	Value
1.	dc Loop gain	83.73 dB
2.	Phase margin	86 degree
3.	Unity gain frequency	3.33 MHz
4.	Power consumption	2.3 mW
5.	ENC* ( $C_{det} = 0$ pF)	500 $e^-$
6.	Noise slope*	18 $e^-$ /pF
7.	Conversion gain	1.25 mV/fC
8.	Area	415 $\mu\text{m}$ x 200 $\mu\text{m}$
9.	Technology	0.35 $\mu\text{m}$ CMOS
10.	Supply	+5V, GND

\* when followed by a CR-RC<sup>2</sup> filter of 1.2  $\mu\text{s}$  peaking time

## 6. Test Results

As a part of a bigger FEE ASIC, the CSA was fabricated in a  $0.35\ \mu\text{m}$  CMOS technology and packaged in CLCC 68. The FEE ASIC consists of 16 pulse processing channels, where each channel consists of CSA, semi-gaussian pulse shaper, track & hold and gain stage. For diagnostic and calibration purposes, all the individual stage output of a particular channel was taken out to the package pins. The fabricated CSA has been functionally tested utilizing the calibration channel in the packaged ASIC in the laboratory. The linearity of the wide swing CSA has been measured by observing the output response on the oscilloscope with increasing input voltage pulse in series with a coupling capacitor (to inject charge) and plotted in Figure 5. The linear response of the CSA is satisfactory with an Integral Non Linearity better (INL) than  $\pm 0.4\%$  up to  $2.6\ \text{pC}$  of input charge (corresponding to an output swing of  $3.3\ \text{V}$ ). The measured conversion/charge gain is  $\approx 1.3\ \text{mV/fC}$ , while the ENC and noise slope shows a higher value of  $820\ \text{e}^-$  and  $25\ \text{e}^-/\text{pF}$  respectively from that achieved in the simulation. This results in a dynamic range of  $79\ \text{dB}$ . The cross-talk measured at the final output of the FEE ASIC is  $\sim 0.6\%$ . Table 4 summarizes the test results of the CSA.

Table 4: Performance summary of the CSA

Sr. No	Parameter	Value
1.	ENC* ( $C_{det} = 0\ \text{pF}$ )	$820\ \text{e}^-$
2.	Noise slope*	$25\ \text{e}^-/\text{pF}$
3.	INL	better than $\pm 0.4\%$ up to $2.6\ \text{pC}$
4.	Dynamic range	$79\ \text{dB}$
5.	Conversion gain	$1.3\ \text{mV/fC}$
6.	Cross-talk**	$0.6\%$

\* when followed by a CR-RC<sup>2</sup> filter of  $1.2\ \mu\text{s}$  peaking time

\*\* Measured at the final output of the FEE ASIC

The ASIC has been validated at the SPS beamline, CERN as FEE readout for the prototype forward calorimeter (FOCAL) [19], a proposed electromag-

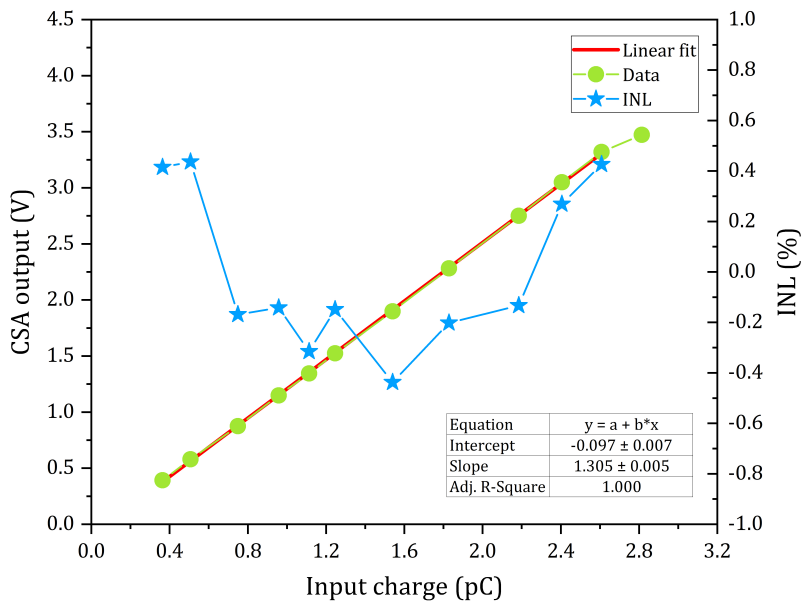


Figure 5: The linear response of the CSA.

netic calorimeter as part of the ALICE upgrade. The response of the prototype calorimeter was linear up to incident energy of 90 GeV for an electron beam validating the wide swing FEE. The MIP response, measured with a 120 GeV of pion beam, is shown in Figure 6, which signifies the low noise performance of the ASIC. These results, as depicted in Figure 5 and Figure 6, validate the wide dynamic range CSA, of this paper, as the first stage of the FEE ASIC.

## 7. Conclusion

A wide swing CSA has been designed in a  $0.35 \mu\text{m}$  CMOS technology, fabricated, and tested. The architecture of the CSA is based on a folded cascode amplifier as the input stage and wide swing current mirrors as the load. The CSA, designed with a reasonably low power budget of 2.3 mW, has shown a linear response up to  $\approx 2.6 \text{ pC}$  of input charge with a dynamic range of 79

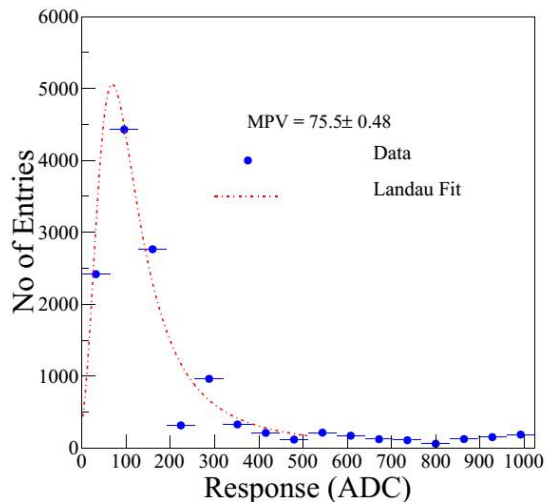


Figure 6: Minimum ionizing particle (MIP) response of a silicon pixel of the prototype FOCAL, facing the beam and readout by the FEE ASIC. The data for MIP particle is fitted with a landau distribution and resulted in 75 ADC counts as the most probable value (MPV) of energy loss (with a calibration factor of 15 used during analysis, corresponds to  $\approx 5$  mV) as expected.

dB. The design has been fabricated as a part of a 16 channel pulse processing FEE ASIC. The ASIC was successfully validated at the SPS beamline, CERN, as a FEE readout for the prototype FOCAL detector, using a 120 GeV pion beam and up to 90 GeV of an electron beam. For an anticipated input signal of positive polarity in the target application for a known detector biasing scheme, this design has achieved an enlarged negative output swing by biasing towards one supply rail and utilizing the voltage range towards the other supply rail. Similarly, for the opposite polarity (negative) of a large input signal, the same design architecture reported in this paper can be utilized using the complementary types of transistors (shown in Appendix B). Moreover, the combination of the wide swing CSA of this paper and the ADC+ToT [10] technique can result in FEE with an even higher dynamic range (shown in Appendix C).

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## Appendix A. The CSA and the silicon detector

The generalized circuit configuration of the CSA with silicon detector at the input and the output load is shown in Figure A.7. The total signal charge  $Q$  generated inside the detector (due to signal current  $I_{in}(t)$ ) will be distributed between the total input capacitance  $C_t$  ( $C_{det}+C_f+C_{gs1}+C_{gd1}$ ) [13] and the dynamic input impedance  $C_{inp}$  of the CSA. The dynamic input impedance of the CSA will be resistive and  $C_{inp} = 1/(\omega_0 \cdot C_f)$  [20], where  $\omega_0=2\pi f_0$  and  $f_0$  corresponds to the unity-gain bandwidth of the core amplifier with the output load. The expression for  $I_{csa}$ , the current getting integrated across the  $C_f$  can be written as,

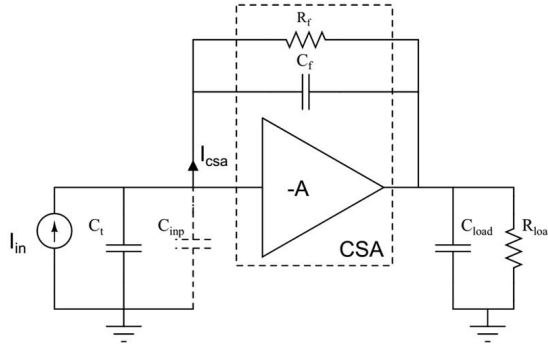


Figure A.7: Typical CSA and silicon detector configuration.

$$I_{csa}(s) = I_{in}(s) \cdot \frac{\frac{1}{sC_t}}{\frac{1}{sC_t} + \frac{1}{\omega_0 \cdot C_f}} = I_{in}(s) \cdot \frac{\omega_0 \cdot C_f}{sC_t + \omega_0 \cdot C_f} = I_{in}(s) \cdot \frac{1}{\tau_2} \cdot \frac{1}{s + 1/\tau_2} \quad (\text{A.1})$$

Where,  $\tau_2 = C_t / (\omega_0 \cdot C_f)$ . Now,

$$V_{out}(s) = I_{csa}(s) \cdot \frac{R_f}{1 + sC_f \cdot R_f} = I_{in}(s) \cdot \frac{1}{\tau_2} \cdot \frac{1}{s + \frac{1}{\tau_2}} \cdot \frac{1}{C_f} \cdot \frac{1}{s + \frac{1}{\tau_1}} \quad (\text{A.2})$$

Where,  $\tau_1 = R_f \cdot C_f$ . Rearranging,

$$\frac{V_{out}(s)}{I_{in}(s)} = \frac{1}{\tau_2} \cdot \frac{1}{s + \frac{1}{\tau_2}} \cdot \frac{1}{C_f} \cdot \frac{1}{s + \frac{1}{\tau_1}} \quad (\text{A.3})$$

Equation A.3 gives the transfer function of the closed-loop system involving the detector and the CSA. The transfer function involves two time constants ( $\tau_1$  and  $\tau_2$ ), one due to the feedback network ( $R_f$ ,  $C_f$ ) and the other due to the network involving  $C_f$ ,  $C_t$ , the core amplifier. Since the detector current can be approximated as a Dirac impulse with an integrated area of  $Q$ , the Laplace transform of  $I_{in}(t)$  is equal to  $Q$ . Hence, it can be written as,

$$V_{out}(s) = \frac{Q}{C_f \cdot \tau_2} \cdot \frac{1}{(s + \frac{1}{\tau_1}) \cdot (s + \frac{1}{\tau_2})} \quad (\text{A.4})$$

Taking the inverse Laplace transform,

$$V_{out}(t) = \frac{Q \cdot \tau_1}{C_f \cdot (\tau_1 - \tau_2)} \cdot [e^{-\frac{t}{\tau_1}} - e^{-\frac{t}{\tau_2}}] \quad (\text{A.5})$$

The expression of Equation A.5 is the general form of the time-domain response of the CSA output, where  $A_Q = 1/C_f$  is the charge gain of the CSA.  $\tau_1$  and  $\tau_2$  are the time constants associated with the two poles  $p_{rcf}$  and  $p_{cfb}$ . The value of the pole  $p_{cfb} (= (\omega_0 \cdot C_f) / (2\pi \cdot C_t))$  happens to be equal to the unity gain frequency of the charge feedback loop. So, to ensure stability, the high-frequency poles of the core amplifier ( $p_2^*$ ) need to be designed away from  $p_{cfb}$ . Equation A.5 shows the fall time is determined by the feedback resistor and capacitor ( $R_f \cdot C_f$ ), while the rise time is inversely proportional to the product of  $f_0$  and  $C_f$  and directly proportional to  $C_t$ .



## Appendix B. Wide swing CSA for the opposite polarity of an input signal

Using the same architecture as shown in section 2, the design of CSA can be modified to accommodate a large negative swing of the input signal. All the transistors of Figure 1b need to be changed to their complementary type respectively. Figure B.8a shows a simplified schematic of the same. The linear performance of the circuit has been plotted in Figure B.8b.

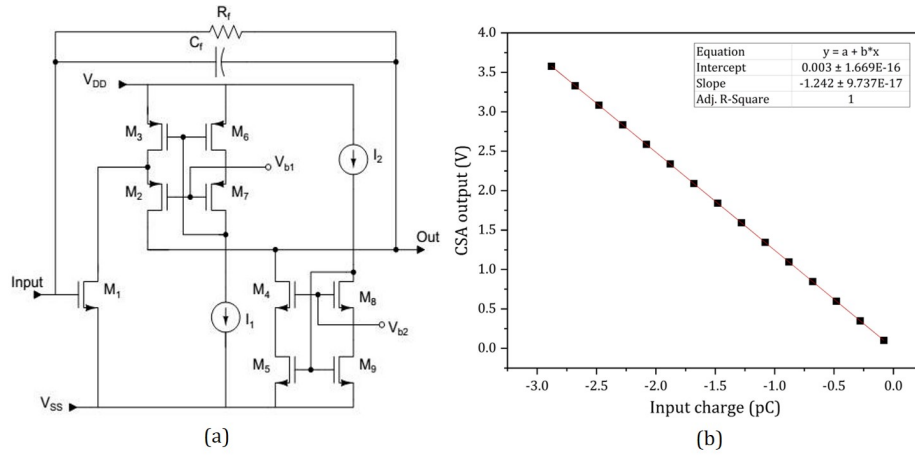


Figure B.8: The simplified schematic of the wide swing CSA for a negative input signal.

## Appendix C. Wide swing CSA with ToT to further improve the dynamic range

As a proof-of-concept of the dynamic range enhancement technique with the combination of the ToT scheme and the conventional pulse amplitude analysis using ADC, the designed CSA of this paper has been simulated with a much larger amplitude of the input signal than the original linear range of 2.6 pC. Figure C.9 shows the transient response of the CSA with a parametric sweep of the input signal from low to very high amplitude.

Time over threshold pulse width has been measured from Figure C.9 by keeping a threshold voltage of 2V (where the CSA output gets saturated over

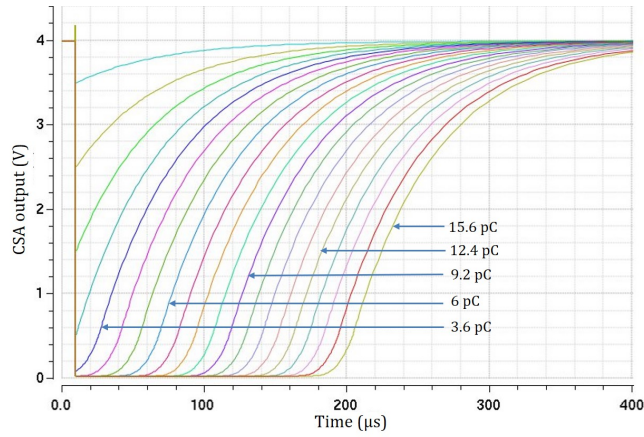


Figure C.9: Transient response of the CSA with gradually increasing input signal; The falling edge of the transient response can be seen to be proportionally spaced in time once the CSA output pulse height is saturated.

3.5V) and plotted in Figure C.10. It can be interpreted that the linear operating range of the CSA is enhanced up to more than 15 pC with reasonable linearity.

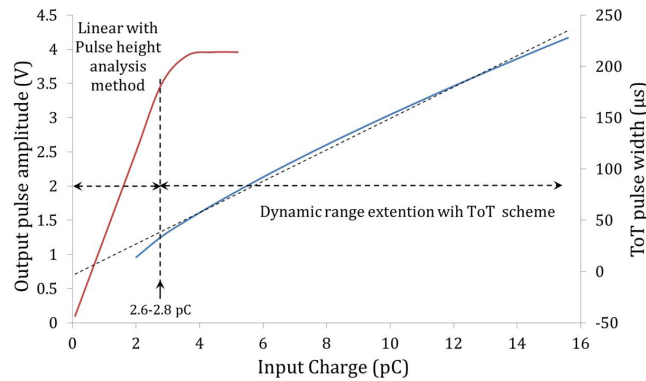


Figure C.10: Dynamic range enhancement of the CSA with a combination of pulse amplitude analysis and ToT scheme. It can be seen that up to an input signal of 2.6-2.8 pC, the pulse amplitude (red line) of the CSA output is proportional whereas, with a higher input signal, the time over threshold pulse width (blue line) is shown proportional behaviour.

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