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MAPS for the Upstream Tracker in LHCb Upgrade II

Yiming Li, on behalf of the LHCb UT Upgrade II team

Institute of High Energy Physics, Chinese Academy of Sciences, China

A R T I C L E   I N F O

A B S T R A C T

Upstream Tracker is a new tracking detector for LHCb Upgrade I to start operation in Run3 of LHC. In light of the plan of LHCb Upgrade II, simulation studies show that the current detector cannot operate due to the high occupancy and data rate. A first preliminary design is proposed to replace the Upstream Tracker with CMOS based detector, and available technology for future R&D are considered.

1. Upstream tracker in LHCb upgrade I

As a forward spectrometer designed for heavy flavour physics at the Large Hadron Collider (LHC), LHCb [1] has successfully operated since 2010 and produced high quality data enabling a plethora of important physics results. It is currently undergoing a major upgrade, named Upgrade I, aiming for a five-fold increase in the instantaneous luminosity to 2×10^{33} cm^{-2} s^{-1} [2]. This requires a complete removal of the hardware trigger allowing readout of the whole detector at 40 MHz. Most subsystems including all tracking detectors will be replaced. The new tracking system consists of a Vertex Locator (VELO) [3] enclosing the interaction region, an Upstream Tracker (UT) and a Scintillating Fibre Tracker (SciFi) which are located upstream and downstream of the bending magnet respectively [4].

Fast track reconstruction is a key element in the full software trigger scheme after Upgrade I, for which UT plays a crucial role by speeding up the match between VELO and SciFi segments and by reducing the ghost rate. It also helps to improve the momentum resolution of tracks with low p_T, and to ensure efficient reconstruction of long-lived particles which decays outside VELO such as K_S and Λ.

The layout of the current UT system is shown in Fig. 1. It consists of four planes of silicon strip detectors, with strips aligned along vertical direction (y), or tilted by stereo angles of $\pm 5°$. Note that this allows precise reconstruction in the bending plane (xz). UT uses four different types of silicon strip sensors, shown in the bottom of Fig. 1, featuring finer pitch and shorter strip length in the inner regions. The innermost part expects a maximum radiation fluence up to 5×10^{14} n_{eq}/cm^2. Each sensor is read out by 4 or 8 dedicated ASIC chips called SALT [5]. A sensor and its ASICs are mounted on hybrid flex to form a module. Modules are mounted on both sides of a stave to allow overlap between each other in y direction. Staves contain cooling tube for CO_2 embedded in foam core and CFRP face sheets. Both ends of staves are connected to periphery electronics providing various functionalities such as data formatting, timing distribution, control and optical conversion. Most components of UT have been shipped to CERN and preparation for the installation is ongoing.
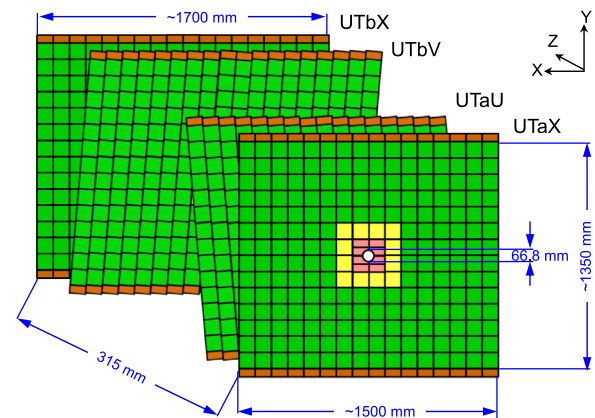
Sensor	A	B	C	D
Type	p-in-n	n-in-p	n-in-p	n-in-p
Thickness(μm)	320	250	250	250
Pitch (μm)	187.5	93.5	93.5	93.5
Length (mm)	~100	~100	~50	~50
Strips/sensor	512	1024	1024	1024
SALTs/sensor	4	8	8	8
Numbers	888	48	16	16

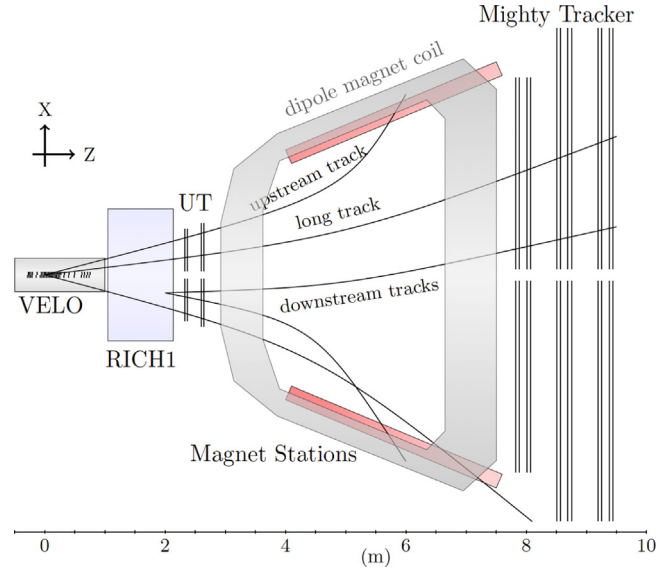**Fig. 1.** UT for LHCb Upgrade I.

E-mail address: liyiming@ihep.ac.cn.

Fig. 2. Sketch of tracking system in Upgrade II.

2. Upgrade II challenges

By the end of Run 4 around 2030, LHCb will have accumulated $50\,\text{fb}^{-1}$ with many subsystems reaching end of lifetime. To fully exploit the High-Luminosity LHC [6] potential in flavour physics, the LHCb collaboration proposes another major detector upgrade, Upgrade II. The goal is to enable the detector to operate at luminosity as high as $1.5 \times 10^{34}\,\text{cm}^{-2}\,\text{s}^{-1}$, so that an integrated luminosity of $300\,\text{fb}^{-1}$ will be achieved in the lifetime of LHC.

Upgrade II imposes more challenges for the whole detector in particular the tracking system. The pile-up, average number of interactions per bunch crossing, will increase from 5 after Upgrade I to around 40 after Upgrade II. Track multiplicity will be much higher, which makes track reconstruction more difficult and more time-consuming. In addition radiation damage will be more severe for most detectors. Efficient tracking is still crucial for the all-software trigger. Physics benchmarks requires excellent resolutions on track momentum and impact parameter, a tracking efficiency for long tracks over 95% with minimal ghost rate, without reducing current geometrical acceptance or adding more material budget.

Given the requirements mentioned above, the tracking system for Upgrade II has to be redesigned (Fig. 2). VELO is exploring new sensor technologies, and will add timing information to disentangle different interactions in the same bunch crossing (BX). A new detector inside the magnet, called Magnet Station, is proposed to extend acceptance of low momentum tracks. The inner part of SciFi will be replaced with silicon pixel detectors for better radiation hardness as well as finer segmentation and spatial resolution, forming so called Mighty Tracker.

Simulation is performed at Upgrade II condition ($\sqrt{s} = 14$ TeV, $\mathcal{L} = 1.5 \times 10^{34}\,\text{cm}^{-2}\,\text{s}^{-1}$) to examine the challenges for the current UT design. In the simulation, pp collisions are generated using PYTHIA [7,8] with a specific LHCb configuration [9]. Minimum-bias events are generated without requiring any specific physics signature. Decays of unstable particles are described by EVTGEN [10], in which final-state radiation is generated using PHOTOS [11]. The interaction of the generated particles with the detector, and its response, are implemented using the GEANT4 toolkit [12,13] as described in Ref. [14]. The full tracking system as after Upgrade I is assumed. The hitmap at the first plane per beam–beam colliding bunch in pp programme is shown in Fig. 3(a), and the hit density as a function of radius in the same plane is shown in Fig. 3(b). The average density per BX is 5.9 hits/cm^2/BX in colliding bunch crossings, as a result the occupancy in the innermost region will be so high (up to $\sim 10\%$) that UT performance will be compromised.
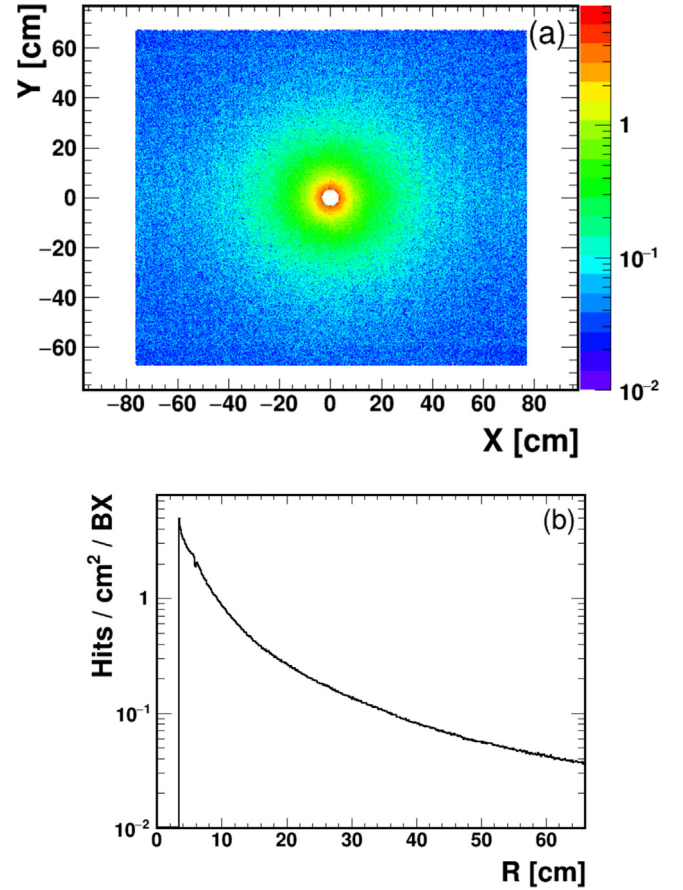

Fig. 3. The hitmap (above) and mean UT hit density (below) per BX at the first plane per beam–beam colliding bunch in the $p-p$ programme.

Similar study is performed for PbPb programme. The hit density per BX is roughly halved compared with the pp case, with a lower colliding rate. However, the maximum hit density in a central PbPb event could reach 52.5 hits/cm^2, resulting in 2.4 hits/strip in the innermost strip ($93.5\,\mu\text{m} \times 5$ cm) of the current UT design. In order to distinguish different hits a higher granularity is necessary.

Chip

Reticle size
~ 20.2×21.4 mm²

Pixel
Orientation
50×150 µm²

Stave

36 modules, ~1355 mm

Module

Plane

36 modules, ~1355 mm
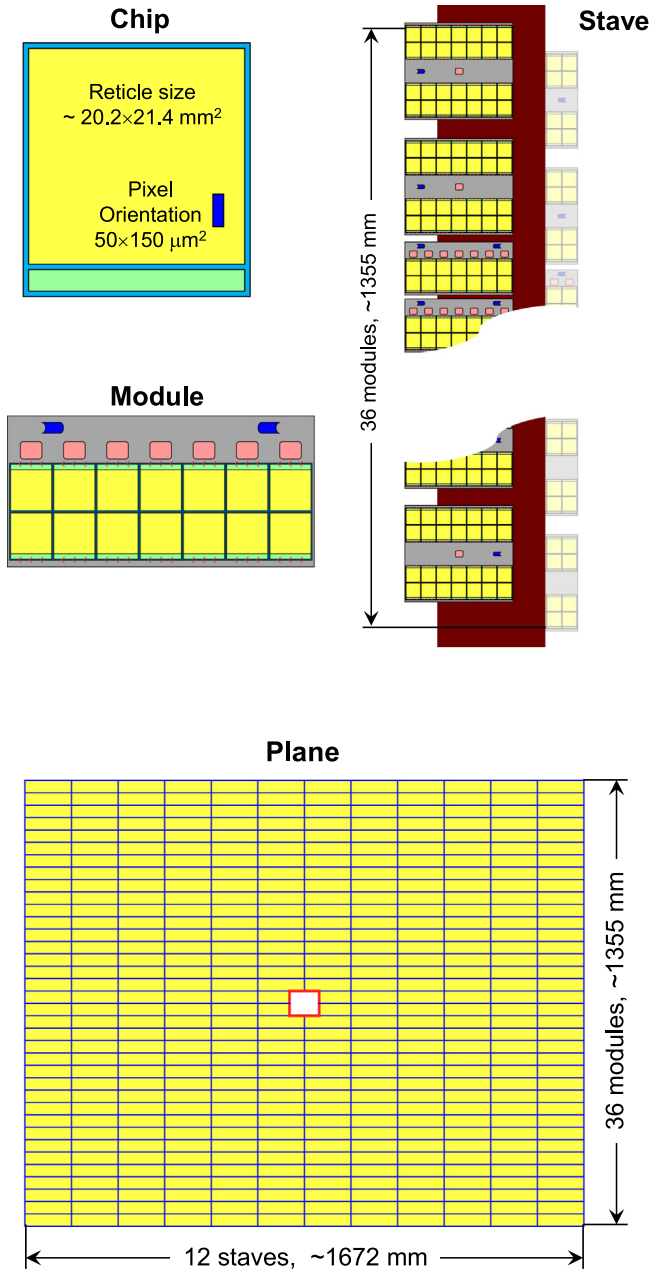
12 staves, ~1672 mm

Fig. 4. A possible system configuration of UT using HVCMOS in Upgrade II. The upper part shows a single chip, a module and a stave, where a yellow box corresponds to a chip. The bottom part shows a full plane, where a yellow box corresponds to a module.

36 modules

12 staves

Ring	5	4	3	2	1
e-links / chip	1	1	1	1-3	2-7
Gbps / e-link	0.32	0.64	1.28	1.28	1.28
lpGBT / module	0.5	1	2	7	14/10
Num of modules	1312	240	80	64	32
Num of lpGPTs	656	240	160	448	384

Fig. 5. Allocation of lpGBT.

Furthermore, UT is designed for a luminosity of 2×10^{33} cm^{-2} s^{-1}, and can handle data rate 1.5 times higher. However, the peak luminosity for Upgrade II will be increase by a factor of 7.5, too high for the readout electronics to cope with. The expected radiation fluence for the inner part will reach 3×10^{15} n_{eq}/cm^2, and the sensors of UT may not function properly by then.

In summary, a new UT system is mandatory to meet the challenging requirements in Run 5 and beyond.

3. MAPS for UT in upgrade II

The high hit density in UT calls for use of silicon pixel detectors for high granularity and better resolution. Monolithic Active Pixel Sensors (MAPS) is a promising technology for large area pixel detectors, cost-effective benefiting from mature CMOS processes. Both Mighty Tracker and UT envisage use of CMOS with similar requirements, and the R&D in sensor technology will be carried in common for the two detectors.

To achieve depletion in CMOS pixels, two approaches are considered either with small-electrode and low-voltage (LV-CMOS) [15] or with large-electrode and high-voltage (HV-CMOS) [16]. The LV-CMOS has a small sensor capacitance, resulting lower noise and less power budget, however to achieve desired radiation hardness modification in process has to be made. The HV-CMOS implements electronics inside charge collection well, allowing a high (50–100 V) bias applied and intrinsically radiation hard. The sensor capacitance in HV-CMOS is higher, hence a larger noise and more power consumption.

R&D for LHCb has mostly focused in HV-CMOS, building on developments for Mu3e [17] and possible ATLAS Pixel upgrade [18]. The 180 nm CMOS process demonstrates good intrinsic radiation hardness, and a pixel size of 50×150 µm² is possible. The ATLASPix3 sensor can achieve a time resolution of 5 ns, with a power consumption around 140 mW/cm². Ideally the time resolution should be reduced to 3–4 ns to distinguish between the 25 ns bunches. The required fluence (3×10^{15} n_{eq}/cm²) in the innermost part of UT is at the high end of what was achieved by ATLASPix3, so further sensor candidate must demonstrate the ability to sustain it.

A possible system configuration of UT upgrade using HV-CMOS is shown in Fig. 4. The layout using LV-CMOS would be similar. The system contains four planes, each with 12 staves. A chip with reticle size of 20.2×21.4 mm², and pixel size of 50×150 µm² is assumed. Fourteen chips in a 7×2 array are interconnected to form a module. For LV-CMOS the chip is larger, typically 35×35 mm², with a smaller pixel size of 30×30 µm². A module can be formed with an array of

4×2 chips for a similar stave width. A total of 36 modules are mounted alternatively on both sides of a bare stave similar as the way of stave construction in Upgrade I.

UT in Upgrade II is expecting a total data rate of approximately 6.8 Tbps, with the hottest chip at 9.0 Gbps. The radiation tolerant ASIC of lpGBT, common to HL-LHC applications, will be used for data concentration and transmission. The module configuration is optimised for efficient use of lpGBT chips. The allocation of lpGBT with different bandwidths of 1.28, 0.64 and 0.32 Gbps bandwidth is shown in Fig. 5.

In addition to the R&D programme foreseen on the technology, detailed studies are planned in the future to define the system design. This include momentum resolution combining with other tracking detectors, optimisation of number and layout of the planes, assessment of material budget, the timing performance, just to name a few.

4. Summary

The Upstream Tracker is being built for the imminent Run 3 as part of LHCb Upgrade I. However simulation studies show that the current design will not work under Upgrade II condition. Upgrade of UT using CMOS MAPS is foreseen, with HV-CMOS or LV-CMOS options. Common development will be carried out on sensor technology for UT and MT. A system design for UT with CMOS is proposed, while more studies are required to define the details.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgement

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