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Conception et caractérisation de capteurs CMOS pour détecteur pixel en physique des particules

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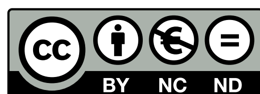

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Résumé

L'expérience ATLAS commencera à fonctionner avec l'accélérateur LHC à haute luminosité (HL-LHC) en 2026 pour augmenter la probabilité de nouvelles découvertes. Afin de faire face aux exigences d'ATLAS en termes d'intensite du rayonnement, de vitesse de lecture et de granularité au HL-LHC, le remplacement de l'actuel ATLAS Inner Tracker (ITk) est nécessaire. La technologie du détecteur de pixels monolithiques en "depleted" CMOS a été une des options envisagées pour la couche externe du detecteur pixel d'ATLAS mis a niveau et est une technologie à fort potentiel pour les futurs détecteurs a pixels. Cette thèse porte sur la mise en œuvre de nouvelles conceptions dans la "depleted" CMOS et son application dans le cadre de la mise à niveau de ATLAS. Le capteur monolithique basé sur la "depleted" CMOS technology offre de nombreux avantages, tels qu'un temps de production réduit, un budget de matériau réduit et un coût inférieur par rapport au détecteur a pixels hybride traditionnel.

Au sein de la collaboration ATLAS HV / HR, plusieurs prototypes ont été développés utilisant différentes depleted CMOS technologies, par exemple, LFoundry (LF) 150 nm, TowerJazz (TJ) à 180 nm et austriamicrosystems AG (AMS) à 180 nm. Ces prototypes sont étudiés pour la collecte de charges, l'influence de l'électronique sur la détection dans cette technologie intégrée, mais aussi par rapport au rayonnement. Réduire les dispositifs rend les circuits intégrés plus sensibles aux erreurs logicielles normalement causées par les particules alpha ou neutrons. Ces événements d'attaque par radiation qui entraînent des bouleversements minimes sont désignés sous le nom Single Event Upset (SEU), qui deviennent préoccupants pour un fonctionnement fiable du circuit. Plusieurs puces de test dans les technologies AMS, TowerJazz et LFoundry avec différentes structures tolérantes au SEU ont été prototypées et testées. Les structures tolérantes au SEU ont été conçues avec des simulations électroniques appropriées à l'aide d'outils de conception assistée par ordinateur (CAO) afin d'étudier la sensibilité de la charge injectée pour perturber un état de la mémoire. En outre, ces structures ont été rendues plus tolérantes à l' "Upset" en effectuant des layouts spéciaux pour SEU-hard. Les trois prototypes conçus étaient entièrement fonctionnels et ont été caractérisés au laboratoire. La puce tolérante AMS SEU a également été exposée à des protons de 24 GeV au synchrotron à protons du CERN pour mesurer la section transversale de SEU. Pour la mise à niveau ATLAS ITk Phase-II Pixel, l'un des principaux défis est une distribution d'énergie efficace et de faible masse vers les modules de détection d'alimentation. Un schéma d'alimentation alternatif appelé schéma d'alimentation série est prévu pour le futur détecteur Inner Tracker (ITk) de l'expérience ATLAS. Pour répondre aux exigences de l'expérience ATLAS concernant l'environnement d'une couche pixélisée dans un environnement de collisionneur à rayonnement élevé, de nouveaux développements avec des

capteurs "depleted" CMOS ont été développés dans le régulateur Shunt-LDO et la polarisation de capteur conçus dans la technologie d'imagerie CMOS TowerJazz 0,18 μm modifiée . Le régulateur proposé a une structure modulaire qui permet une meilleure gestion de l'énergie et une meilleure dissipation de la chaleur. Les régulateurs sont également tenus de travailler dans un système parallèle de redondance en cas de panne de courant. De plus, dans le processus modifié TowerJazz, deux niveaux de tension différents sont utilisés pour la "depletion" du capteur. Les tensions de polarisation sont générées en utilisant un circuit de pompe à charge négative.

En plus de participer aux nouvelles conceptions du la "depleted" CMOS, je me suis impliqué dans la caractérisation IC de ces prototypes en laboratoire, ainsi que dans plusieurs campagnes d'irradiation au synchrotron à protons du CERN.

Mots clés : Détecteurs de suivi de particules, électronique résistante aux rayonnements, Depleted CMOS sensors, alimentation en série, régulateur Shunt-LDO, pompe de charge, perturbations à événement unique.

Abstract

The ATLAS experiment will start operating at the High Luminosity LHC accelerator (HL-LHC) in 2026 to increase the probability of new discoveries. To cope with the ATLAS requirements in terms of radiation hardness, readout speed, and granularity at the HL-LHC, the replacement of the present ATLAS Inner Tracker (ITk) is needed. Depleted CMOS monolithic pixel detector technology has been one of the options considered for the outer layer of an upgraded ATLAS pixel detector and is a high potential technology for future pixel detectors. This thesis focused on the implementation of new designs in the depleted CMOS, and its application in the ATLAS upgrade framework. A monolithic sensor based on depleted CMOS technology offers various advantages such as less production time, lower material budget and lower cost in contrast to the traditional hybrid pixel detector.

Within the ATLAS HV/HR collaboration, several prototypes have been developed using different depleted CMOS technologies, for instance, LFoundry (LF) 150 nm, TowerJazz (TJ) 180 nm and austriamicrosystems AG (AMS) 180 nm. These prototypes are studied for charge collection, the influence of electronics on the sensing part in this integrated technology, but also versus radiation. Scaling down the devices makes integrated circuits susceptible to soft errors normally caused by alpha particle or neutron hits. These events of radiation strike resulting in bit upsets are referred to as Single Event Upsets (SEU), which become of concern for reliable circuit operation. Several test-chips in AMS, TowerJazz and LFoundry technologies with different SEU tolerant structures have been prototyped and tested. The SEU tolerant structures were designed with appropriate electronics simulations using Computer Aided Design (CAD) tools in order to study the sensitivity of injected charge to upset a memory state. Furthermore, these structures were made more tolerant to the upset by doing special SEU-hard layouts. All three prototypes which were designed were fully functional and were characterized in the laboratory. The AMS SEU tolerant chip was also exposed to 24 GeV protons at Proton Synchrotron in CERN to measure the SEU cross-section.

For the ATLAS ITk Phase-II Pixel upgrade one of the main challenges is a low mass, efficient power distribution to power detector modules. An alternative powering scheme named Serial Powering scheme is foreseen for the future Inner Tracker (ITk) detector of the ATLAS experiment. To meet the requirements of the ATLAS experiment to the environment of a pixelated layer in a high radiation collider environment, new developments with depleted CMOS sensors have been made in Shunt-LDO regulator and sensor biasing which are designed in modified TowerJazz 180 nm CMOS imaging technology. The proposed regulator has a modular structure that allows better power management and heat dissipation.

Regulators are also required to work in a parallel scheme for redundancy in case of power failure. Moreover, in the TowerJazz modified process, two different voltage levels are used for the purpose of sensor depletion. The bias voltages are generated by using a negative charge pump circuit.

Beyond participating in the new designs of the depleted CMOS, I was involved in the IC characterization of these prototypes in the laboratory, as well as multiple irradiation campaigns at Proton Synchrotron in CERN. While exposing the prototypes under the proton beam, the main focus was the investigation of the irradiation hardness. TID and NIEL effects on the electronics and sensor could be performed by characterization of the front-end : measuring the pre-amplifier amplitude, threshold scans, TDAC tuning, leakage current, etc.

Keywords : Particle tracking detectors, Radiation-hard electronics, Depleted CMOS sensor, Serial Powering, Shunt-LDO regulator, Charge Pump, Single Event Upsets.

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Introduction

The Large Hadron Collider (LHC) of the "European Organization for Nuclear Research" (CERN, Geneva, Switzerland) is the largest, highest energy particle accelerator in the world and is designed to probe the structure of matter to the smallest scales. To probe the elementary particles and interactions, it collides protons together at speed close to the speed of light. The fundamental structure of matter as we know it today is described as the Standard Model. According to this theory, all known matter around us is made of elementary particles (fermions) that are divided into two types called quarks and leptons. But the Standard Model is incomplete, as it cannot not explain the hierarchy problem, the nature of the dark matter, the matter/antimatter asymmetry... These mechanisms have been tried to be explained by extensions to the Standard Model generically termed as "Beyond the Standard Model".

The validation of the Higgs boson theory was one of the main goals of ATLAS and CMS experiments. After discovering a new particle at the LHC with a mass of $125.09 \pm 0.21(stat.) \pm 0.11(syst.)$ GeV, candidate to be the Standard Model Higgs boson, it also opened the path to deeper studies of this new particle as well as searches for new particles. To discover new particles, the LHC gradually increases its luminosity, which enables the physicists to access processes and decay channels that are more rare. This increase in the luminosity is known as High-Luminosity LHC (HL-LHC) where the number of collisions per unit time is roughly increased by a factor of 10. To handle the ATLAS requirements in terms of radiation hardness, readout speed and granularity at the HL-LHC, the replacement of the present ATLAS tracker is needed. The ATLAS Inner Tracker pixel detector will be made of a silicon-based 5-layer cylinder with endcaps. Pixel detectors often rely on a hybrid pixel concept, where the electronic read-out chip used to treat the information is physically separated from the sensor, used to detect particles. Both parts are connected together by the use of bump-bonds using flip-chip bonding technique. Hybrid pixel is the main candidate technology for the ATLAS pixel detector upgrade since it has proven to be radiation hard mainly because of its principle (sensor and the read out chip are on separate entities).

New developments are foreseen to cope with the more difficult environment of the future HL-LHC, both for the sensor and for the front-end electronics. Complementary Metal Oxide Semiconductor (CMOS) with minimun feature size of 65 nm is targeted to be the front-end electronics technology fulfill the HL-LHC requirements and will be described in chapter 2. As the radiation level is low in the fifth layer [a] with respect to the inner layers, it is possible to use depleted

a. Still, of order 0.8 MGy and 1.5×10^{15} n_{eq}/cm^2 (Dose expected for electronics and sensor for around ten years).

CMOS sensors in this environment. This technology integrates the sensing part together with the electronics on a single layer. There are various advantages of this technology such as a reduction in the costs, less production time and allows designing smaller size pixels while having a rather strong signal and high tolerance to radiation. This thesis work investigates depleted CMOS monolithic technology in the framework of the design of an upgraded ATLAS detector, but it should be noted that this work can be also applied out of the ATLAS ITk upgrade context.

In chapter 1, description of LHC, a brief overview on the physics requirements of the ATLAS detector and its upgrades are presented. In chapter 2, pixel detector technologies and pixel module for ITk are described. Device physics and radiation effects in the silicon are discussed in chapter 3. In chapter 4, design simulations and characterizations of the LFoundry 150 nm prototypes with respect to radiation in a high radiation environment are discussed. The main test results are given and the behaviour of different prototypes under irradiation are studied. In chapter 5, several mitigating techniques are discussed for Single Event Upset (SEU). We then study and present different prototypes of SEU-hard cells in different technologies. Chapter 6 contains the motivation for Serial Powering, and the Serial Powering concept, and then we describe the specificities of the implementation of Serial Powering with depleted CMOS sensors.

1. The LHC, ATLAS upgrades

1.1. Large Hadron Collider

The Large Hadron Collider (LHC) [1] is the world's largest and most powerful hadron accelerator. It is built underground at a 100 m depth near Geneva, Switzerland. It is placed in a 27 km circumference tunnel, lying across the border between France and Switzerland. The construction of LHC started in 1998 and its installation was finished in 2008. The LHC is designed to provide proton-proton (pp) collisions with a maximum proton single-beam energy of 7 TeV, for a 14 TeV maximum centre of mass energy. The LHC was operating (shutdown from December 2018) at a peak luminosity of 1×10^{-34} cm^{-2} s^{-1}, with the combined intensity of 1.15×10^{11} protons per bunch, crossing the experiments after every 25 ns.

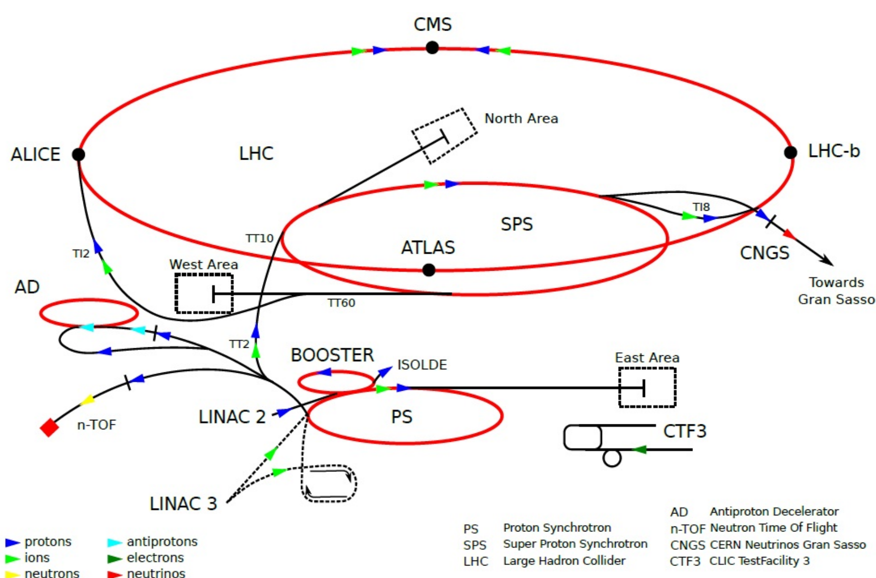


Figure 1.1. – The LHC Accelerator with all experiments.

The whole CERN accelerator complex, shown in figure 1.1, comprises not only the LHC ring and other accelerators, but also four detectors (ALICE [2], ATLAS [3], CMS [4] and LHCb [5]). The general purpose of these four detectors are:

1. ATLAS and CMS: studying Standard Model and beyond.
2. LHCb: studying b-physics and CP-violation.
3. ALICE: heavy ion physics.

The validation of the Higgs boson theory was one of the main goals of ATLAS and CMS experiments [6]. The Higgs boson particle is part of the standard model. It gives their mass to other particles. The confirmation of its existence in 2013 was an outstanding achievement of the ATLAS [7] and CMS experiments [8]: only possible because of the large amount of data, the performances of the detectors and the long and complex analysis.

Colliders must have high luminosity for the collection of large statical samples which are required for precise measurements. In LHC collisions, the number of events generated per second is given by:

$$N_{event} = L \cdot \sigma_{event} \tag{1.1}$$

where σ_{event} is the cross-section for the process under study, and L is the integrated luminosity of the accelerator. Instantaneous luminosity can be defined as the number of particles colliding per second, per effective area of the colliding beam.

$$L = \frac{n_1 \cdot n_2 \cdot k \cdot f}{4\pi \cdot \sigma} \tag{1.2}$$

where n_i is the number of particles per bunch, f is the revolution frequency, k is the bunches per beam, σ is the effective cross-section area of the beam.

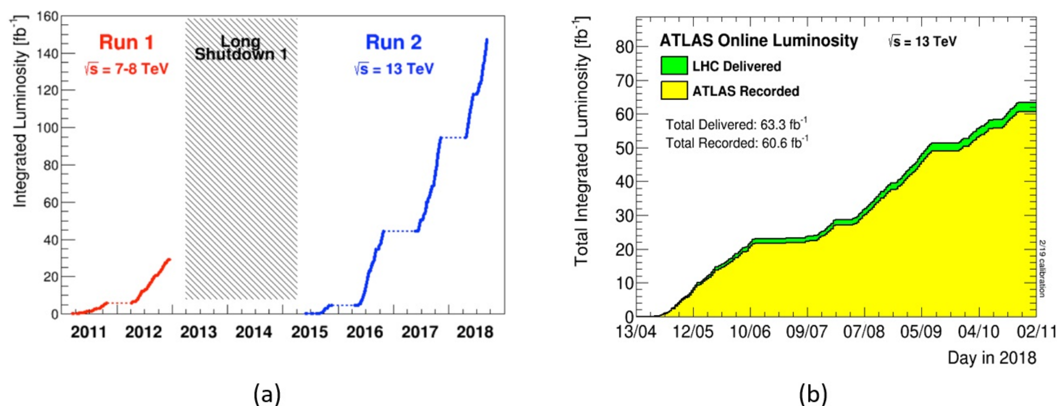


Figure 1.2. – (a) Integrated luminosity Run-1 and Run-2 [9]. (b) Integrated luminosity in 2018 [10].

The LHC started operating on November 23, 2009 at an energy of 450 GeV, which was further increased to 3.5 TeV in 2010. The collision energy reached 8 TeV, in the center of mass, in 2012 (end of Run-1). A cumulative luminosity versus time delivered to ATLAS experiment for Run-1 and Run-2 period is shown

in figure 1.2(a). Run-2 period with 13 TeV collision energy has started in 2015 and ended in 2018. The figure 1.2(b) shows the cumulative luminosity for the year 2018.

1.2. The ATLAS experiment

The ATLAS experiment is one of the detectors installed at the LHC. One of the major usage of this detector is to examine the Higgs-mechanism and explore new physics. Section 1.2.1 gives a brief overview on the physics requirements. Section 1.2.2 describes the physics requirements and the layout of ATLAS detector. In section 1.2.3, we give a description of the ATLAS upgrades.

1.2.1. Physics requirements

The physics program of the ATLAS experiment was designed to allow high precision tests of QCD, electroweak interactions and flavour physics at the LHC. The search for the standard model Higgs boson has been hallmark in establishing the performance of the ATLAS experiment. The design of the ATLAS detector needed to fulfill the many requirements. Few of them are listed below:

- Large acceptance in pseudorapidity with full azimuthal angular coverage.
- High granularity to handle particle fluxes and to decrease the influence of overlapping events.
- Good charged particle momentum resolution and reconstruction efficiency capability for the inner detector.
- Good muon identification and momentum resolution.
- Sufficient background rejection to operate at an acceptable trigger rate for most physics experiments.
- The sensor and electronics should be fast, radiation hard for the duration of the entire experiment lifetime.
- Hardware trigger rates for desired physics come in at around 1 MHz.

1.2.2. ATLAS layout

The ATLAS detector is one of the multi-purpose detectors at the LHC. Its layout is shown in figure 1.3. The height and length of the ATLAS detector are 25 m and 44 m respectively. The total weight is approximately 7000 tons. The ATLAS detector is composed of a set of sub-detectors: an inner detector, an electromagnetic calorimeter, a hadronic calorimeter, a muon spectrometer and forward detectors. They will be presented later in this section with more details given for the inner detector.

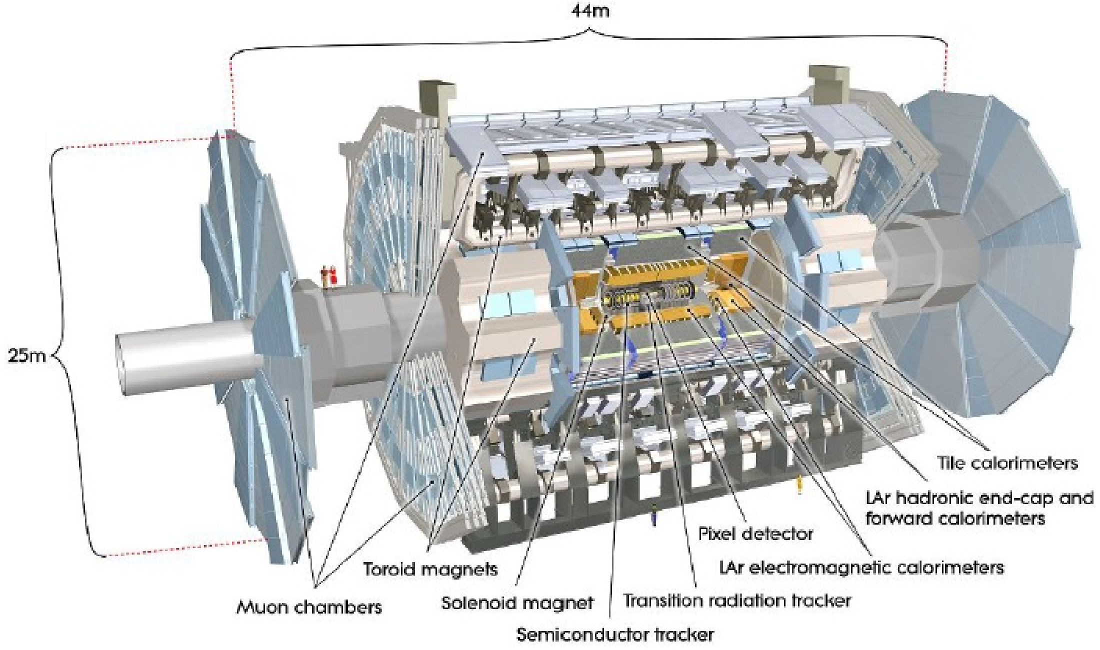


Figure 1.3. – Cut-away of the ATLAS experiment showing the various sub-detectors.

The coordinates of the ATLAS detector are determined by the right handed-system illustrated in figure 1.4. The +x direction pointing towards the center of the LHC ring, while the +y direction points are tilted sightly and pointing vertically upwards. The z direction corresponds to the path traversed by the beams, and the side-A is defined as the positive direction of the z-axis and the side-C is the negative direction of the z-axis.

Along with the Cartesian system, the cylinder coordinate system (r, ϕ, θ) is also used. Where r defines the radius from the beam axis in the x-y plane, ϕ is the azimuthal angle from x-axis in the transverse plane, and θ is the polar angle measured from z-axis. Rapidity y, can be defined as:

$$y = \frac{1}{2} ln \frac{E + p_z}{E - p_z} \tag{1.3}$$

where E is the energy of the particle and p_z is the z component of the particle momentum. If we assume the rest mass to be negligible, y becomes the pseudorapidity.

$$\eta = -\frac{1}{2} ln \left(tan \frac{\theta}{2} \right) \tag{1.4}$$

The ATLAS experiment is fundamentally a proton collider experiment due to

which it is not possible to measure the longitudinal energy of the initial colliding proton since in fact that the partonic initial energy is unknown and is parametrized by the Parton Distribution functions (PDF). The vectorial sum of particle momenta on the transverse plane is always conserved. In the x-y plane, the missing transverse momentum magnitude E_T^{miss} can be expressed as:

$$E_T^{miss} = \sqrt{(E_x^{miss})^2 + (E_y^{miss})^2} \tag{1.5}$$

This parameter E_T^{miss} is used in many analysis.

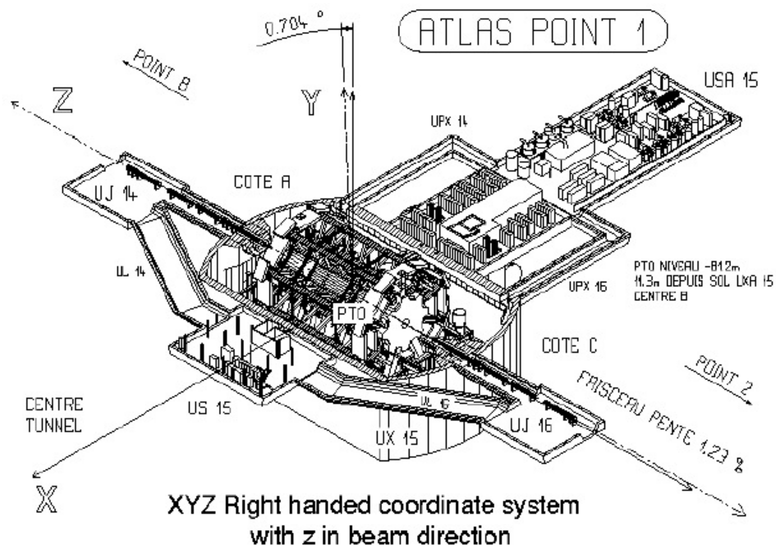


Figure 1.4. – ATLAS right-hand coordinate system.

1.2.2.1. Inner Detector

In the inner detector every 25 ns, nearly 100 particles emerge from the interaction point. The design of the inner detector allows it to function in such a harsh environment while sustaining a high track density. The inner detector shown in figure 1.5 is made up of:

1. The Pixel Detector
2. The Semiconductor Tracker
3. The Transition Radiation Tracker

Pixel Detector
The inner most part of the ATLAS experiment is the pixel detector. It is situated closest to the interaction point. To start with the detector system has three barrel

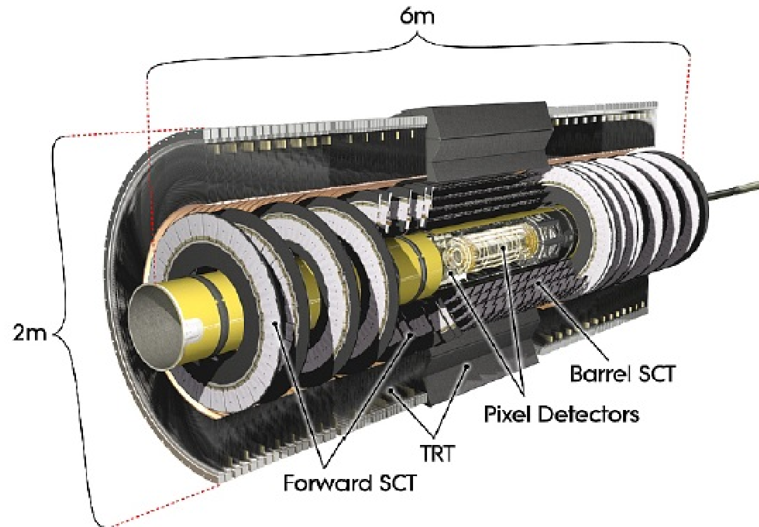


Figure 1.5. – Cut-away of the inner detector.

layers and two end caps of three pixel disks each of about 5, 9 and 12 cm radii as illustrated in figure 1.6(a). Among all the sub-detectors in the ATLAS experiment, the pixel detector should have the highest tolerance to radiation damage (up to a TID of 250 MRad). In 2014, an additional Insertable B-layer (IBL) [11] was added to improve ATLAS performance (see section 1.2.3).

The 3 layers pixel detector has a total of 1744 modules of which 1456 are in the barrel and 288 are installed in the disks. Figure 1.6(b) shows the schematics representation of the pixel module. This pixel module is based on the hybrid pixel detector concept (see section 2.2.1 for more details on this type of detector). Each module consists with the length of 62.4 mm and 21.4 mm wide, with a pixel size of 50 μm $\times$ 400 μm. Inside each module there are 46080 pixels, directly linked to 16 front-end chips for readout [3].

Semiconductor Tracker

The Semiconductor Tracker (SCT) is made up of silicon micro strips. It surrounds the pixel detector, as shown in figure 1.7. It has a barrel part which consists of 4 cylinders and 2 end-caps. Each end-cap has 9 disks with 4088 modules. The cylinders consist of 2112 detector units, the barrel modules [12] with a size of 6.36 cm $\times$ 6.40 cm. Figure 1.8 shows photograph and layout of a barrel SCT module. SCT sensors comprises of p-in-n type semiconductors. The thickness of the SCT wafer is 285 μm with silicon strips. The wafers are n-type semiconductors while the sensor strips are highly doped p-type semiconductors.

Transition Radiation Tracker

The Transition Radiation Tracker (TRT) is the outermost layer of the inner detector. As shown in figure 1.7 the TRT is placed between 55 cm and 108 cm radii with respect to the interaction point. The main function of the TRT is to

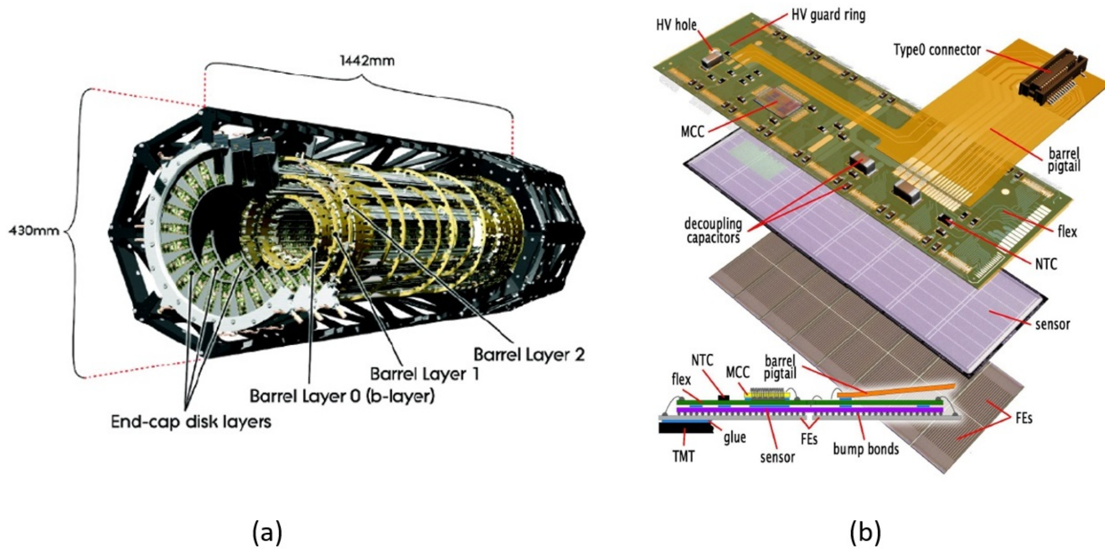


Figure 1.6. – (a) Side view of the pixel detector with 3 barrel layers and 3 disks in each endcap sides. (b) A schematics of barrel pixel module. FEs are the front-end chips which are bump bonded to the sensor.

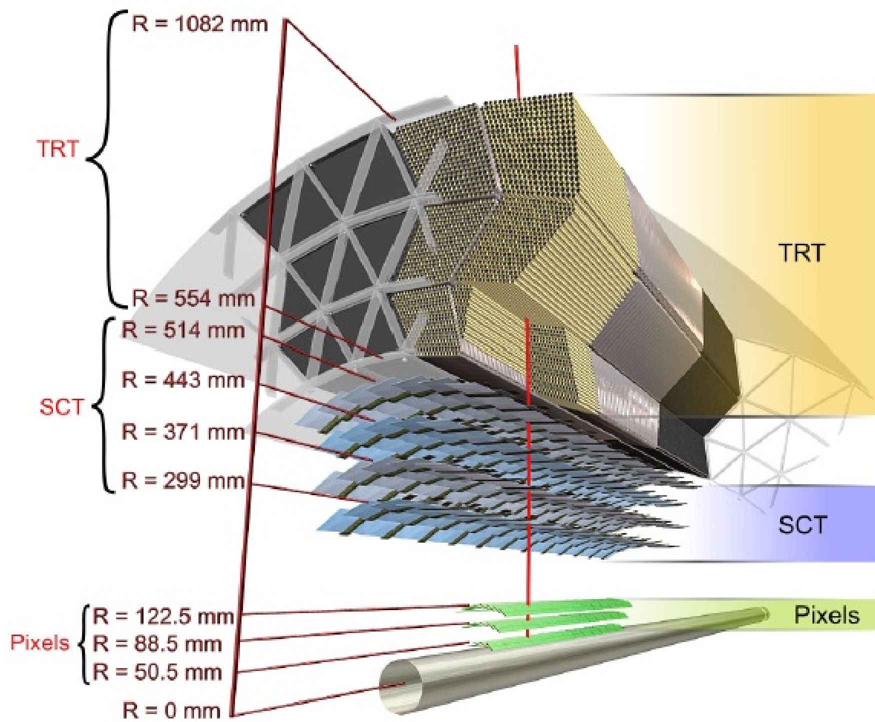
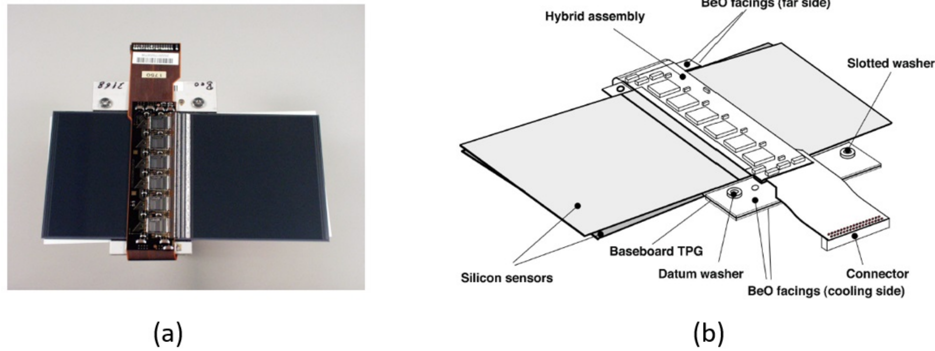


Figure 1.7. – Inner detector layout.



(a) (b)

Figure 1.8. – (a) Photograph of a barrel module [13].(b) Drawing of the same. The thermal pyrolytic graphite (TPG) base-board has a good thermal conductivity and is used to apply the bias voltage to the micro strip sensors.

allow continuous tracking along with electron identification by the detection of transition radiation X-ray photons. Straw tube gas chambers make up the TRT. In Run-1 the gas used was a mixture of Xenon, CO_2 and O_2. However, in Run-2 the gas Xenon was replaced by a mixture of Xenon and Argon.
The TRT is a polyimide drift (straw) tracker with the diameter of each straw equal to 4 mm. The wall of the straw tube is biased at -1.5 KV. 52544 straw tubes make up the barrel region to a total length of 1.5 m.

1.2.2.2. Calorimeters

The calorimeter system in ATLAS experiment consists of an electromagnetic [14] (EM) and hadronic calorimeter [15] as illustrated in figure 1.9. Accurate measurements of the energies of the particles and their positions is possible due to the fine granularity of the EM calorimeter. The electromagnetic calorimeter is a liquid Argon (LAr) sampling calorimeter and the end-caps of the hadronic calorimeter use liquid Argon has a detection medium. The barrel part of the hadronic calorimeter surrounding the EM calorimeter consists of iron tiles with scintillators to allow measurements of charge particles. Usually, equivalent depth in radiation and interaction lengths for electromagnetic and hadronic showers are provided by the calorimeters and reduces punch-through into the muon system.

1.2.2.3. Muon Spectrometer

The outermost detector of the ATLAS experiment is the muon spectrometer toroidal superconducting magnets [16]. Its function is to measure the momentum of muons that exit the calorimeter. As shown in figure 1.10, the muon spectrometer has four types of chambers, namely: monitored drift tubes (MDT), cathode

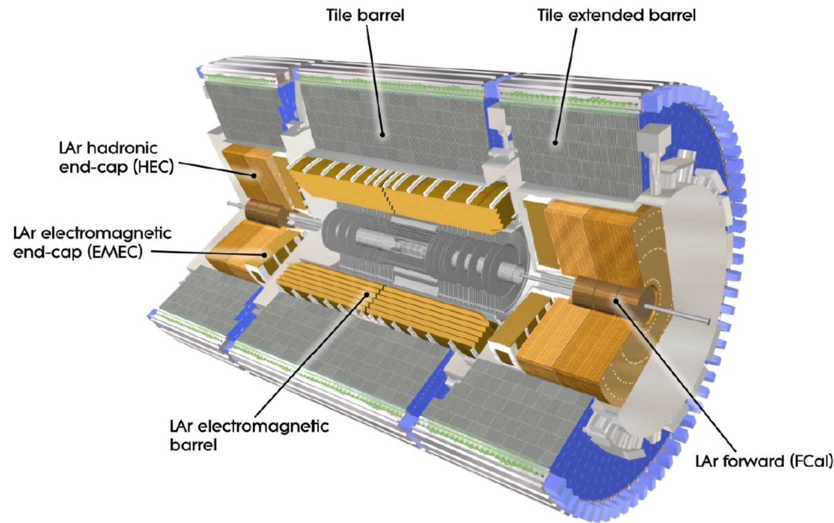


Figure 1.9. – Cut-away view of the ATLAS calorimeter system.

strip chambers (CSC), resistive plate chambers (RPC), and thin gap chambers (TGC).

The aim of this detector is to measure the momentum of high P_T muons which is an important information for the triggering system. The barrel region has 3 cylindrical layers for the measurement of muon tracks, while the end-cap regions of the muon spectrometer has 3 layers of chambers installed perpendicularly to the beam axis.

1.2.2.4. Forward detectors

Three smaller detector systems [17] occupy the forward regions of the ATLAS experiment as illustrated in figure 1.11. The aim of the forward detector is to detect the p-p scattering in the forward direction which allows measurements of the instantaneous and integrated luminosity. Luminosity measurement using Cerenkov Integrating Detector (LUCID) is a first detector, which is composed of two modules located at 17 m from the interaction point. Zero-Degree Calorimeter (ZDC) is the second detector and plays an important role in the determination of centrality of heavy-ion collisions. ALFA (Absolute Luminosity For ATLAS) is the third detector, which monitors absolute luminosity by elastic scattering at small angles.

1.2.3. ATLAS upgrades

The ATLAS collaboration planned to use time offered by the LHC Shut Downs to enhance the detection performances of the ATLAS experiment while replacing

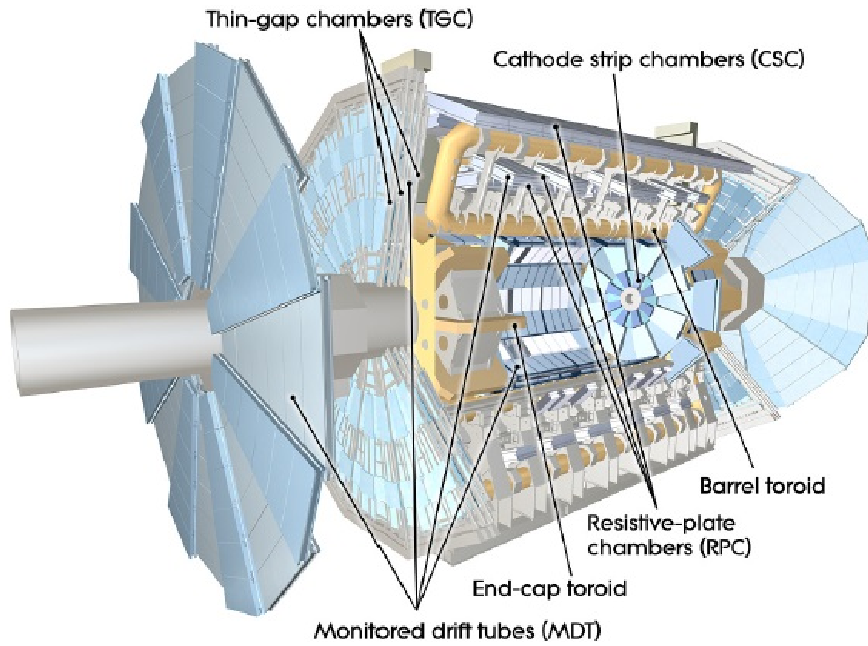


Figure 1.10. – Overview of the ATLAS muon system.

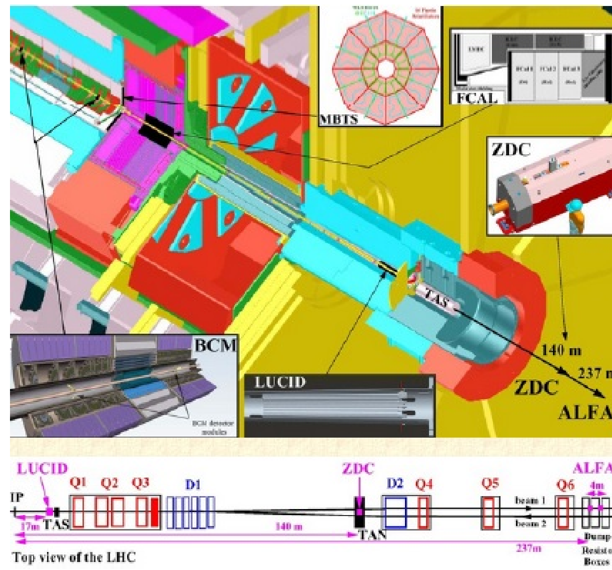


Figure 1.11. – Overview of the forward detectors of ATLAS.

damaged detectors. In the last few years the whole ATLAS experiment has been upgraded several times, however in this section only the upgrades of the pixel detector will be discussed. The schedule for Long Shut Downs is shown in figure 1.12. The collision energy needs to be increased up to 14 TeV in order to explore new physics opportunities, to characterize Higgs boson properties and search for new particles in the Standard Model.

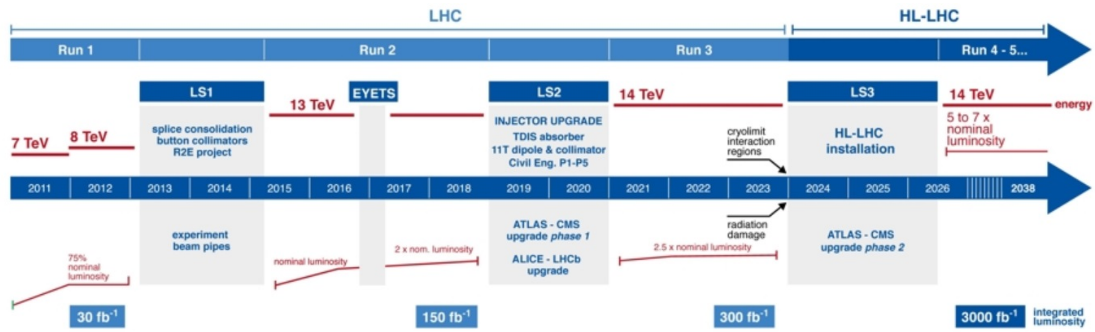


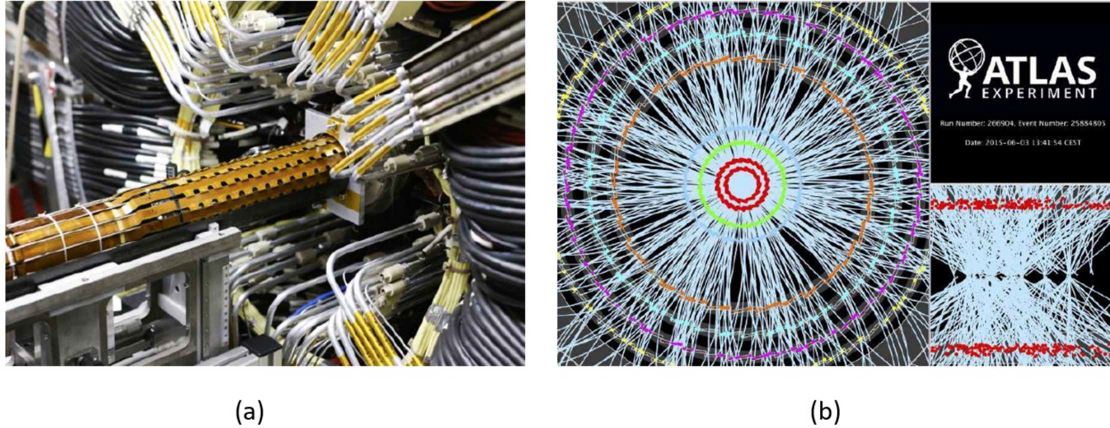
Figure 1.12. – Schedule of LHC Runs and Long Shut Downs.

In order to function with the increased number of pile-up interactions reached for the Run-2 and reduce radiation damage to the other pixel layers, a new layer called Insertable B-layer was added inside the pixel detector during the Long Shut Down 1 (LS1). A photograph of installation of IBL is shown in figure1.13(a). The coverage of the IBL is $\eta < 2.58$. It was directly installed on the beam pipe at a main radius of 33.25 mm. The size of a pixel in the IBL is 50 μm $\times$ 250 μm. A display of collision event with IBL recorded in June 2015 is illustrated in figure 1.13(b). The reasons for installing IBL were:

1. It improved the tracking efficiency and b-tagging capability of the ATLAS experiment.
2. It induced the development of a new readout IC termed FE-I4 to improve the detection capability in high hit rates condition.
3. It was installed closest to the interaction point which allowed precise primary vertexing performance.
4. Redundancy in the case of B-layer failure.

Not much changes to the pixel detector were carried out during the Long Shut Down 2 (LS2). However, this Shut Down gave an opportunity to install new opto-boards and upgrade the online firmware and software.

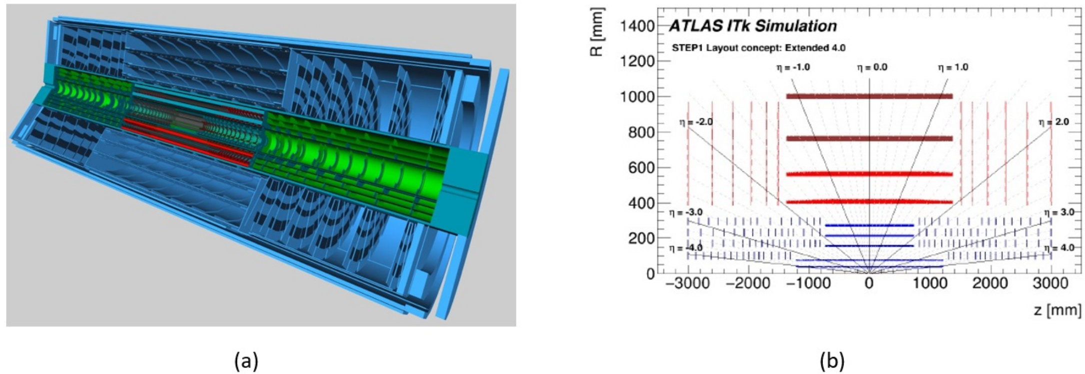
In Phase-II upgrade (2024-2025, LS3), ATLAS tracking system will be replaced by an all-silicon-detector tracker called Inner Tracker (ITk). The upgraded detector should handle a high luminosity of 7.5×10^{34} cm^{-2} s^{-1} and an increase



(a) (b)

Figure 1.13. – (a) Installation of IBL. (b) A display of collision event after the IBL insertion [18]. Red color illustrates the IBL.

in the number of events per collision from 25 to 200. In order to perform the usual inner detector tasks, the ITk needs to have new high radiation hardness and high bandwidth readout electronics and sensors. A display of the overall ATLAS Phase-II tracker ITk is illustrated in figure 1.14(a). The preliminary layout of the ITk includes 4 strip barrel layers supplemented with 2×6 end-cap disks and 5 pixel barrel layers as shown in figure 1.14(b). In the ITk, the strip part will cover a total area of about 165 m^2 with about 60 million channels. It is expected from the new layout to have pseudorapidity coverage of $\eta \leq 4$.



(a) (b)

Figure 1.14. – (a) Display of the ATLAS Phase-II ITk [19]. (b) Schematic layout of the ITk for the HL-LHC phase of ATLAS [19].

The upgraded pixel detector will be instrumental since it will consist of new readout electronics and sensor technologies which are able to withstand high radiation and occupancy environment of the HL-LHC. A new read out chip with a pixel size of 50 μm $\times$ 50 μm is developed in the 65 nm CMOS technology within the RD53 collaboration [20]. The pixel matrix consists of 400×192

pixels. There are two separate power domains for the chip: analog (VDDA) and digital (VDDD). More details on this readout chip (based on hybrid detector concept) is given in section 2.2.1. It will be used in all layers of the ITk pixel detector.

The detection of particles in the pixel detector is performed by silicon sensors. In the hybrid pixel detector, optimal sensor designs for the different pixel layers are to be chosen carefully. The sensor should be able to withstand large amount of non-ionizing and ionizing particle radiation damage. The expected maximum fluence for the inner and outer layers of the pixel detector is 1×10^{16} n_{eq}/cm^2 and 1.5×10^{15} n_{eq}/cm^2 respectively. Three types of sensors are currently being investigated for that purpose: 3D, planar and depleted CMOS sensors. In 3D sensors, the distance between the column electrodes is decoupled from the device thickness and can be chosen to be significantly smaller than the thickness of the standard planar sensors. Planar pixel sensors are the baseline option considered from second to fifth layer for the ITk Pixel Detector. The n-in-p technology has been chosen because it is a single sided process, simplifying the product flow with respect to the n-in-n technology. Depleted CMOS sensors are a cost-effective alternative with respect to traditional planar sensors if full size prototypes can be demonstrated to be radiation hard up to the level needed for fifth layer of the ITk. Various studies investigating radiation hardness improvements are described in [21] [22] [23]. It is also important to optimize the thickness of the sensor (it also defines the E-Field strength at the maximum bias voltage...) as this would reduce the cluster size at high pseudorapidities. This will consequently improve the resolution of tracks and data handling.

The HV/HR CMOS technologies [24] are the most recent family of detectors with advantages such as low-cost, thin and radiation-tolerant detectors with a high time resolution. This technology was proposed for the ATLAS Phase-II upgrade for the pixel detector. The most probable option was to use depleted CMOS sensors for the outermost layer (L4) which is situated within 30 cm from the interaction point. The R&D on the depleted CMOS sensors in ATLAS started in 2011, with many prototypes have been designed and characterized for radiation tolerance and efficiency. Chapter 2 discusses the ATLAS pixel detector technologies and pixel module for ITk. Chapter 3 deals with the device physics and radiation effects in the silicon. Chapter 4 shows the simulations and characterization of the LFoundry 150 nm CMOS technology prototypes. Chapter 5 describes the developments towards radiation tolerant memories in HV/HR CMOS process. Chapter 6 gives a motivation for Serial Powering and describes the developments in monolithic CMOS sensors for Serial Powering scheme. This PhD work is done in the context of depleted CMOS sensors.

2. ATLAS pixel detector technologies and pixel module for ITk

The HL-LHC is an upgraded version of the LHC, which will start from 2026 for about 10 years. During this tenure, it aims to accumulate a total data set of up to 3000 fb^{-1}. As discussed in section 1.2.3, the new all silicon tracker named ITk will consist of two subsystems with several layers of silicon particle detectors: a pixel detector will be composed of five silicon pixel layers and a strip detector with outer layers surrounding the pixel detector. In section 2.1, we give a description of the ATLAS ITk pixel detector project. Section 2.2 gives an overview of silicon pixel detectors.

2.1. ATLAS ITk Pixel Detector project

2.1.1. Motivation towards ITk

The current ATLAS Inner Tracking Detector was designed for $\sim$ 10 years with an expected peak luminosity to be approximately 2×10^{34} cm^{-2} s^{-1}. It was very difficult to predict the total luminosities integrated during the Phase-I. The elements placed inside the Inner Detector were designed to withstand the radiation fluences during the run time before the Phase-II upgrade. Present Inner Detector will not be able to meet the requirements that will be part of the physics program for phase-II upgrade due to the limitations which are listed below.

Radiation Damage
The current pixel detector was designed to withstand the radiation damage that is equivalent to an integrated luminosity of 630 fb^{-1} for b-layer and 112 fb^{-1} for outer layers. The designed radiation hard sensors and electronics are not suitable for the operation much beyond this level. Therefore, an upgraded pixel detector is required to meet the requirements.

Limitations from Detector Occupancy
Since the average proton-proton interactions will be around 200 per bunch crossing, the SCT will not be able to resolve close by tracks in the core of high p_T jets. The efficiency of the pattern recognition and track-finding will be comprised by the confusion due to additional hits without compensating the increase in granularity. This results in an increase in the rate of fake tracks.

Track Trigger

A trigger system is using simple criteria to rapidly decide whether or not to keep an event from a given bunch-crossing for later study, and only a small fraction of the total can be recorded due to the limitations in data storage capacity and rates. One of the main challenges in ATLAS at HL-LHC will be the performance of the trigger system. New inner detector electronics should be capable to accept higher L1 rate up to 1 MHz. High level track trigger need to be improved at HL-LHC. Moreover increase in the latency is not compatible with the old chips.

After the long shutdown of the LHC machine in 2022, the ATLAS experiment will start with the first physics data taking around the middle of 2026 and 10 more years of operation are planned. In 2026, the HL-LHC will be able to deliver a very high peak instantaneous luminosity which is 5-7 times higher when compared to the present value. At this ultimate luminosity (7.5×10^{34} cm^{-2} s^{-1}), an average of approximately 200 inelastic proton-proton interactions per beam crossing is being considered. Tracking coverage until η of four is only possible through an upgraded system of silicon barrel layers and disks (Strips) or rings (Pixels). To meet the requirements of a charged particle tracking detector, the biggest challenge is the design of a new all silicon tracker. The new inner tracker (ITk) should be capable to cope with the increase of approximately a factor of ten in the integrated radiation dose.

2.1.2. Description of the Pixel Detector Layout

Various layouts for the pixel detector were studied in order to extend η coverage. The two best layout candidates were namely Inclined and Extended. Based on the long barrel staves, the two layouts (Inclined and Extended) are used to push the material at the end of the barrel service. The inclination of the sensors in the forward part of the barrel layers for this layout is the main difference between the two concepts. The layout shown in this section is based on "Inclined Layout" and illustrated in figure 2.1. The new detector design also combines the precision central tracking in the presence of 200 pile-up events with the extended tracking coverage to a pseudorapidity of four. A pixel detector will be composed of five silicon pixel layers and a Strip Detector with outer layers surrounding a Pixel Detector. The two innermost layers of the upgraded pixel detector will be replaced due to the harsh radiation environment expected for the HL-LHC. The Inner Support Tube (IST) is used to separate the two innermost layers from the outer three layers, that facilitates a replacement of the inner layers. A total of thirteen hits for $\eta < 2.6$ is provided by the combination of both strip and pixel detectors.

Two new design ideas for the upgraded pixel detector have been implemented. First is based on the inclined barrel stave design, where the flat barrel stave is increased in length with inclined modules. This results in the shifting of the

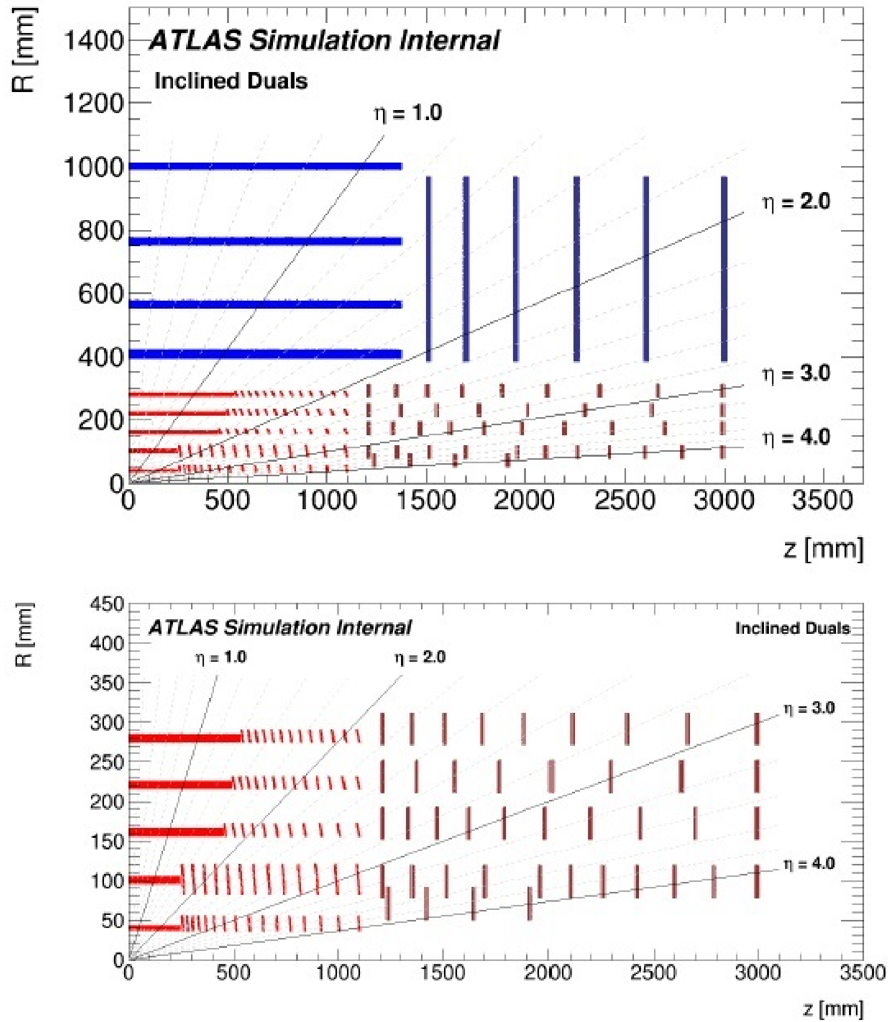


Figure 2.1. – Top: A schematic layout view of the ITk Inclined Duals layout for the Phase-II with the pixel layout. Bottom: A zoom view of the Pixel Detector. The interaction point is on the horizontal axis. The radius measured from the interaction point is shown on the vertical axis [19].

end-of-stave material out in z-direction. Another new design is the end-cap ring system, where layers of the pixel rings extend the coverage in z-direction and allow routing of the service separately along with each ring layer. In order to keep the hit counts stable as a function of η, it is possible by increasing the number of pixel rings in the layer which allows additional hits to be added. To achieve good tracking performance with extended coverage until η of four, it is important to have the inclined stave design for the inner barrel layers. As a consequence, it allows two or more hits in Layer 0 close to the interaction point. Furthermore, the impact parameter and vertex resolution can be improved by having the first hit close to the beam pipe.

2.1.3. Key requirements for the ITk design

To achieve good tracking performance over the lifetime of Phase-II, it is foreseen to replace the inner two layers of the pixel detector as mentioned in section 1.2.3. In order to have good radiation tolerance, the replaceable part of the pixel detector is designed for the total luminosity of up to 2000 fb^{-1}. This means that the devices installed in Layer 0 must be radiation hard up to a dose of 1 GRad (with safety factor 1.5). The new pixel detector will be designed with five silicon layers with less inactive material in the tracking volume. To deliver high track reconstruction and a low rate of fake tracks, the ITk is designed with efficient pattern recognition and track reconstruction. At the beginning of the HL-LHC operation, a single Level-0 trigger (L0) with an average frequency of 1 MHz and a maximum latency of 10 μs will be used to read out the data. The Pixel Detector will send the data to a fast track reconstruction process that will deliver track parameters as the input to the High-Level Trigger process (HLT). This trigger architecture is called "L0-only". This is considered as the baseline for the ATLAS experiment. An alternative trigger architecture is also considered and is called Level-1 (L1) or "L0-L1". In this scheme, an additional level of the trigger is used. The L0 will be operating at a maximum frequency of 4 MHz and a maximum latency to 10 μs. The Level-1 trigger will be operating at a maximum frequency of 800 kHz and a maximum latency of 35 μs. Level-0 and Level-1 triggered schemes are illustrated in figure 2.2 for the complete detector.

Level-0 trigger will be used to read full ITk. Different strategies will be employed in the different ITk sub-detectors for the Level-1 scheme. Inside the Strip Detector, 10% of the modules belonging to the Region of Interest (RoI) identified as a part of the L0 decision will support L0 read-out at a frequency of 4 MHz. Following this, full readout is carried with L1. The three outer pixel layers will be readout at a frequency 4 MHz and two inner layers will be read-out with a frequency of 1 MHz [19]. According to the Level-1 scheme, it requires more output bandwidth which results in more data cables. More details about this strategy is explained in [19].

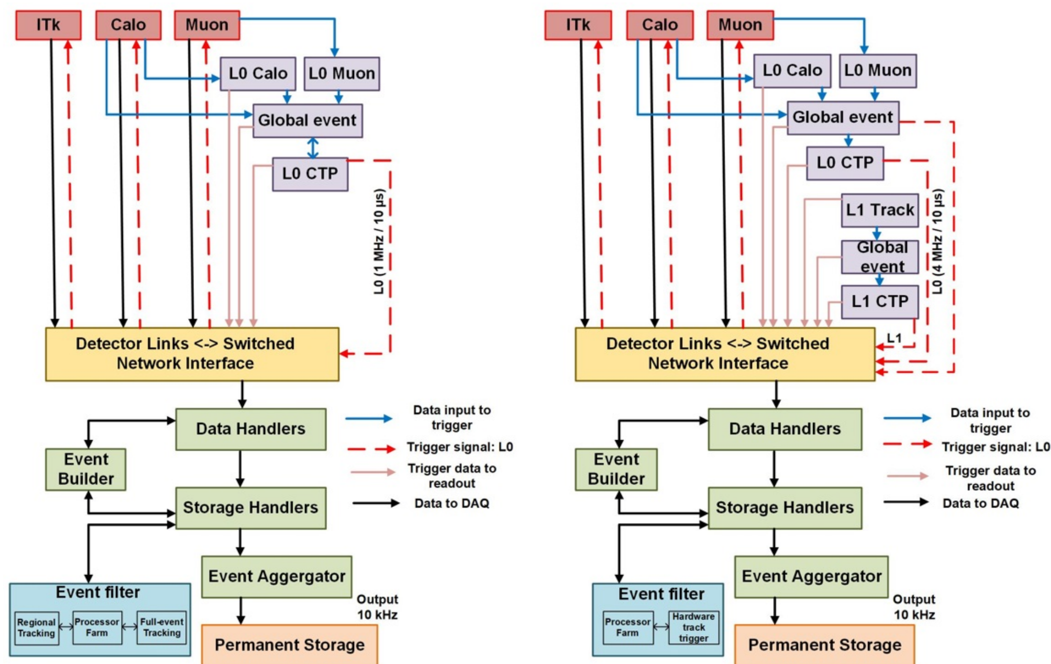


Figure 2.2. – Block representation of the ATLAS Phase-II trigger scheme. Left: with one trigger level: Level-0 (L0). Right: with two trigger levels: Level-0 (L0) and Level-1 (L1) [19].

2.2. Silicon pixel detectors

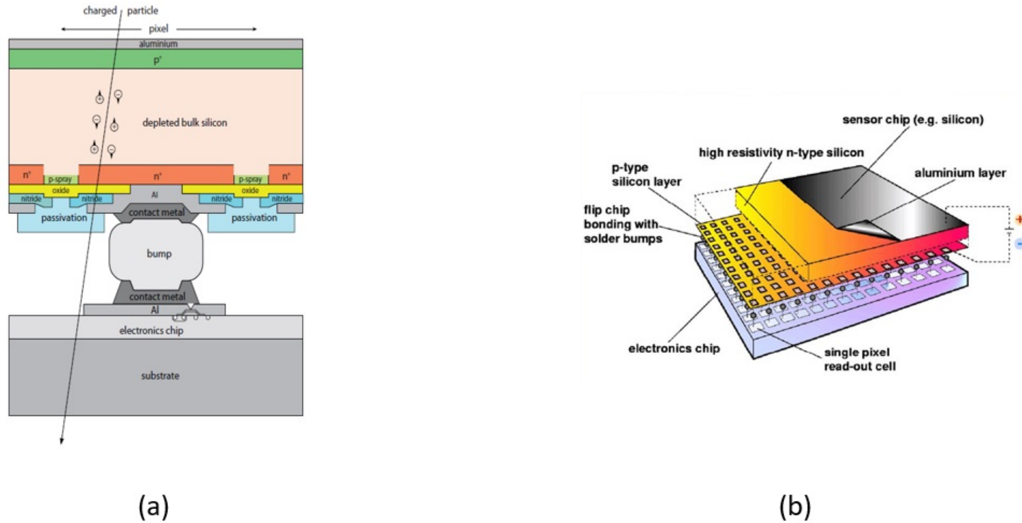
Solid state semiconductor materials such as silicon are used for tracking detectors in a high radiation environment under a strong magnetic field, such as at the Large Hadron Collider (LHC) experiments. In order to collect the charge from the ionization, the sensors are reversed biased and fully depleted (explained in section 3.3). For the ATLAS Phase-II run, two different silicon pixel detector concepts were studied and are described in the next two sections (2.2.1 and 2.2.2).

2.2.1. Hybrid pixel detectors in ATLAS ITk

Tracking and vertexing are possible in LHC radiation intense environment with the help of hybrid pixel detectors. They are radiation hard and the only viable concept to cope with the rate and radiation environment. Hence for tracking, three experiments at LHC (ATLAS, CMS and ALICE) have installed hybrid pixel detectors.

In a hybrid pixel detector concept, two separate layers are used to detect the particles and signal formation. The particles are detected by the sensor (first layer) and the readout chip (second layer) processes the signals recorded in

the sensor. A sketch of the cross-section of a hybrid pixel cell is illustrated in figure 2.3(a). Both these layers are connected together with indium or solder bump-bonding technologies as shown in figure 2.3(b). Fine pitch bump bonding is implemented to connect each pixel in the sensor to the readout chip. In this concept, independent developments towards readout chips and sensors



(a) (b)

Figure 2.3. – (a) Cross-section of a hybrid pixel cell [25]. (b) Schematic of a full hybrid pixel detector bonded to each other by means of bump contacts [25].

are made, however, the interconnection process requires significant financial expenses.

When an energetic charged particle passes through the sensor, it frees electrons and holes (ionization). Under the influence of an applied electric field, these charges move in the depleted region, inducing a signal on the pixel electrodes. The electronics inside the readout chip first convert the charge into an electrical signal by using a charge sensitive amplifier and then use discriminators for the digitalization process. There are various advantages of using hybrid pixel detectors as the sensor especially withstand the irradiation because of improvement due to the smaller 3D electrode distance and the readout chip can deal high hit rates (MHz/mm^2). From the studies, hybrid pixels are proven radiation hard up to 1×10^{16} n$_{eq}$/cm^2 [22].

The hybrid pixel detector is the baseline solution for the ITk pixel detector. To implement ITk modules, there are some additional improvements when compared to the current modules. Some of the improvements are listed below:

1. To improve the intrinsic resolution and two tracks separation, the pixel size has been reduced to 50 μm $\times$ 50 μm or 25 μm $\times$ 100 μm.
2. Various front-end architectures are studied and designed for lower threshold.

3. Additional features in the readout architecture to deal with hit rate and also the radiation tolerance has been increased to 1×10^{16} n_{eq}/cm^2.
4. To handle the data with high hit rates in the innermost layers, the output bandwidth of the system has been increased to 5.12 Gb/s per front-end chip.
5. To reduce the cost and fabrication time, the size of the module has been increased.
6. To reduce power losses in the cables and also the material budget, a new powering scheme: Serial Powering [26] [27] will be adopted in the tracker.

The limitations to the current readout chip [28], in particular the radiation hardness and its ability to cope up with high hit rates have led the developments in 65 nm feature size CMOS technology. The chosen front-end chip size will be 20 mm $\times$ 21 mm with 153,600 pixels. The chip will consist of around 500 M transistors. The pixel size will be 50 μm$\times$50 μm. The front-end chip is designed and carried out within the framework of the RD53 collaboration [20] by the joint group of people from ATLAS and CMS experiments. A large scale prototype called RD53A with the size of 2 cm $\times$ 1.18 cm was fabricated in TSMC 65 nm technology in 2017.

The RD53A readout chip consists of three different types of front-end amplifier designs and two different readout architectures. The objective to implement different structures was to compare the performance of different designs before and after the irradiation and select the best solutions for the final design. The three front-end architectures are: synchronous, linear, differential front-end. Figure 2.4 shows the layout view of the RD53A integrated circuit. The RD53A readout chip is described in detail in [29].

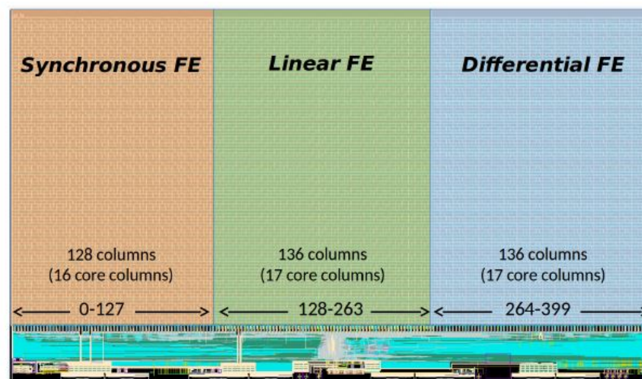


Figure 2.4. – Layout-view of the RD53A integrated circuit.

In addition, the RD53A chip is also robust with respect to local ionization effects known as Single Event Upsets (SEU). This effect temporarily affects the

functionality of the chip. Several prototypes have been designed with different architectures in order to study the behaviour of memory. The triple modular redundancy architecture is proved to be SEU tolerant for this application but it is difficult to use for the memories holding the configuration inside the pixel because of the space constraints [30]. During the data taking, the system is designed to allow for a refresh rate of 10 Hz (these memory cells). More details have been explicitly described in [30].

2.2.2. CMOS monolithic Pixel Detectors

In monolithic pixel detectors, the sensitive volume, and readout circuitry are combined on a single entity. Integrating the sensor and the electronics on a single entity is one of the biggest challenges in building such a type of detector. In high energy physics, monolithic pixel detectors provide various advantages such as less production time, lower manufacturing costs, less complexity, etc. A sketch of a monolithic pixel detector concept is illustrated in figure 2.5. The electronics and sensor are placed on a single substrate. There are two mechanisms that exist to collect charge generated in silicon by ionizing radiation: one is diffusion and other is drift. The monolithic pixel detectors collect the signal charge by diffusion which makes them very sensitive to the radiation damage (since it takes more time and hence increases the probability of signal charge to be captured by defects or traps), therefore results in the low signal collection. The application for monolithic pixel detectors is very limited in high energy physics since it was installed in two experiments: Belle-II [31] and STAR [32]. During the construction of Large Hadron Collider, monolithic detectors were not ready, they might be used for some other upgrades and pave the way to low power and very light inner detectors.

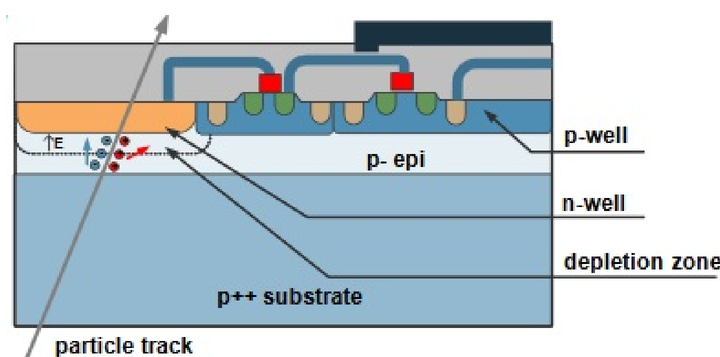


Figure 2.5. – Cross-section of monolithic pixel detector [33].

Monolithic active pixel sensors have already matured enough to be used as high precision tracking and vertexing devices in high energy physics experiments. Developments on monolithic active pixel sensors for the LHC started in

2011 with the design and characterization of small-scale prototypes [34]. This R&D led to the implementation of monolithic pixel detectors inside the ALICE experiment [34]. This was only possible because of the process changes in the monolithic sensor with the foundry, which enabled the charge collection by the drift mechanism [35]. A brief overview of the monolithic modified TowerJazz process is given in section 6.1. A cross-section of both the monolithic pixel sensors is shown in figure 2.6. In depleted CMOS sensors the charges are collected by drift during the ionization mechanism whereas in standard monolithic CMOS sensor, the charges are mainly collected by the diffusion process.

According to ATLAS specifications, the depleted CMOS monolithic technology should withstand the radiation in the outer layers, far enough from the interaction point. The expected radiation levels are 80 MRad Total Ionizing Dose (TID) and 1.5×10^{15} n_{eq}/cm^2 particle fluence. The goal is to achieve 50-100 μm of the depletion depth with a good signal and in-time charge collection.

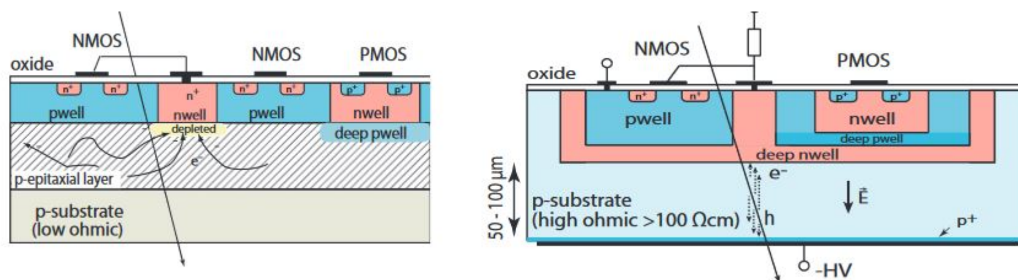


Figure 2.6. – A monolithic active pixel sensor (MAPS) with charge collection by diffusion process (left). DMAPS (Depleted MAPS) structure with charge collection by drift process (right) [25].

DMAPS detectors have various features and few of them are listed below:

1. High voltage technology [36] (> 100 V) increases the voltage handling capability and creates a depletion layer in the order of 40 μm-50 μm.
2. High resistivity wafers are also available from different foundries, which develops a depletion layer with only moderate bias voltages ($\approx$ 100 V).
3. Multiple nested wells are used in order to isolate transistors and shield deep well.

In DMAPS there are two different approaches. In the first approach, the entire CMOS electronics is placed inside the deep n-well which acts as a charge collecting electrode [37], as shown in figure 2.7(a). This is known as large collecting electrode approach. It provides good charge collection properties with a shorter travel distance, which results in smaller trapping possibilities after irradiation [33]. There are few drawbacks in this approach as it suffers from large inter-well capacitances, leading to larger noise values, more power consumption, and

slower timing when compared to the small collecting electrode approach. In the second approach, as shown in figure 2.7(b), the electronics is placed 2-4 μm far from the n-well collection electrode [38]. This is known as the small collecting electrode approach. Since the detector capacitor has implications on the noise, power and timing of the signal [39]. Due to low capacitance (5 fF), it provides excellent noise, power and timing performance. However, radiation tolerance is one of the major concerns since the drift distances of the signal charges are longer.

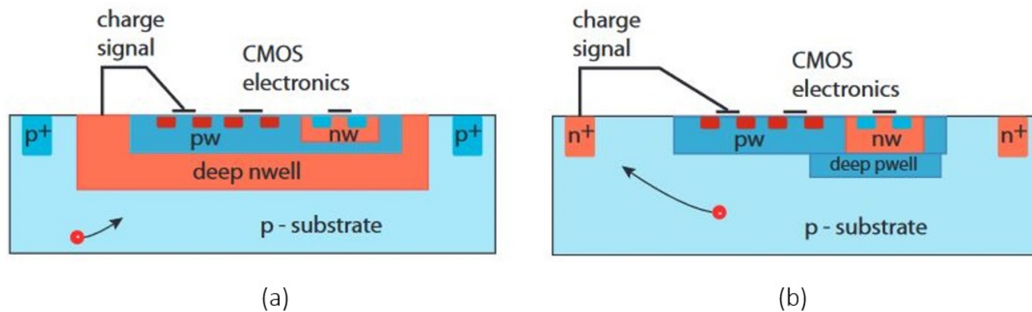


Figure 2.7. – (a) Cross-section of large collecting electrode approach. (b) Cross-section of small collecting electrode approach.

The CMOS community works on depleted CMOS monolithic sensors within the ATLAS collaboration and prototyped different ICs with three different foundries. The developments were carried out in three different foundries that were considered for the outermost pixel layer (Layer 4) of the ATLAS experiment namely: AMS 180 nm, LFoundry 150 nm and TowerJazz 180 nm technology. The AMS 180 nm and LFoundry 150 nm CMOS technology is based on the large collecting electrode approach, whereas the TowerJazz 180 nm technology is based on the small collecting electrode approach.

2.2.2.1. AMS 180 nm technology

There are several versions submitted in the AMS 180 nm technology. The first version ATLASpix-1 had a total size of 1 cm $\times$ 2 cm which was submitted to the foundry in January 2017 to show the viability of this technology. The reticle of the ATLASpix-1 chip [40] is shown in figure 2.8(a). There are three different pixel designs (M2, Simple and IsoSimple) and two different (triggered and column drain) readout architectures [41] implemented inside this chip. The pixel matrix M2 has a pixel size of 60 μm $\times$ 50 μm and uses a triggered readout architecture. Simple and IsoSimple matrices have pixel size of 140 μm $\times$ 40 μm and use column-drain readout architecture, which was used in the FE-I3 readout chip [42]. An additional isolation p-well is used for IsoSimple matrix. The ATLASpix-1 chip was fully functional after receiving from the foundry. Before the

radiation, the chip showed mean detection efficiency above 99.3 % [43]. The chip was afterwards irradiated to neutrons and protons up to 2×10^{15} n_{eq}/cm^2 and 100 MRad respectively. The mean detection efficiency was above 98 %. The irradiation results are summarized in [44]. The second version ATLASpix-2 was submitted to the foundry in August 2018. This prototype has a pixel matrix of 24 × 36 pixels with a pixel size of 128 μm × 50 μm. A Single Event Upset (SEU) tolerant test-chip was also submitted with the ATLASpix-2 chip, dedicatedly designed for Single Event Effect (SEE) tests. A detailed description on the design and measurements of the SEU test-chip is described in section 5.2 and section 5.2.6 respectively. The third version ATLASpix-3 was submitted to the foundry in April 2019 with improvements of the previous version and a shunt-LDO regulator [45].

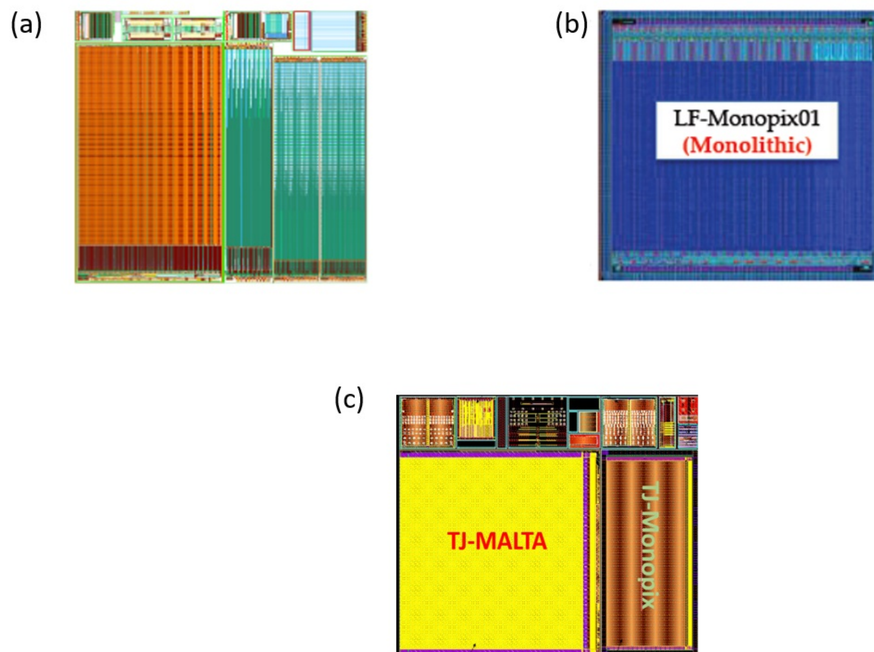


Figure 2.8. – (a) ATLASpix chip produced in AMS 180 nm. (b) LF-Monopix01 chip produced in LF 150 nm. (c) TowerJazz chip produced in TowerJazz 180 nm.

2.2.2.2. LFoundry 150 nm technology

Next technology based on a large collecting electrode approach is LFoundry 150 nm CMOS technology. The recent prototype in LFoundry: LF-Monopix01 [46] with a total size of 1 cm × 1 cm was submitted to the foundry in August 2017. It was produced on a high-resistivity (> 2 kΩcm) p-type substrate. The reticle of LF-Monopix01 is shown in figure 2.8(b), which has the pixel matrix

of 129 × 36 pixels with a pixel size of 250 μm × 50 μm [46]. There are nine different pixel designs with a column-drain readout architecture implemented inside this chip (discussed in chapter 4). Seven pixel designs have readout logic inside the pixel and the other two pixel designs have readout logic inside the periphery. The wafers were successfully thinned from 700 μm to 200 μm because an improvement in charge collection for irradiated thinned samples was seen from previous e-TCT studies [47]. The LF-Monopix01 chip was characterized in the laboratory and also under irradiation. The chip was irradiated to neutrons and protons up to 1 × 10^{15} n_{eq}/cm^2 and 160 MRad respectively. It turned out that high resistivity wafers up to 2 kΩcm and high voltage $<$150 V is needed for good performance after irradiation. The mean detection efficiency is above 98% after the fluence of 1 × 10^{15} n_{eq}/cm^2. The detailed measurements are discussed in [48] [49].

2.2.2.3. TowerJazz 180 nm technology

Two prototypes: TJ-MALTA [50] and TJ-Monopix [51] in a modified TowerJazz 180 nm CMOS technology are shown in figure 2.8(c) is based on a small collecting electrode approach. Both prototypes were produced on a high-resistivity p^+ type substrate in 2017. The TJ-MALTA chip (pixel pitch 36.4 μm × 36.4 μm) consists of eight different pixel designs with a asynchronous readout architecture, whereas TJ-Monopix chip (pixel pitch 36.4 μm × 40 μm) consists of four different pixel designs with synchronous readout architecture, well known as the column drain architecture. After receiving the prototypes in early 2018, the chips were fully functional and showed promising results with a mean detection efficiency of 97% before irradiation. Afterwards they were irradiated to neutrons up to 1 × 10^{15} n_{eq}/cm^2 and the value of mean detection efficiency was reduced to 70% [48]. A Technology Computer-Assisted Design (TCAD) simulation study was done to improve the mean detection efficiency and it led to making further changes in the TowerJazz process [52]. A new prototype named mini-MALTA with new process modifications was submitted to the foundry in August 2018. The chip was tested at DESY and ELSA (Bonn) test beams in March 2019, and then irradiated by protons in April 2019. From the test beam measurements, it turned out that the mean detection efficiency of the mini-MALTA TowerJazz chip was around 98 % at a fluence of 1 × 10^{15} n_{eq}/cm^2. The beam tests that show full efficiency of the whole chip up to 1 × 10^{15} n_{eq}/cm^2 and 70 MRad will be presented in [53]. Design activity was therefore started also on serial power, further described in chapter 6, for the TowerJazz 180 nm CMOS sensor.

In the last 4 years, many design groups were working on the CMOS depleted monolithic active pixels and developments carried out by the author in different technologies are described in chapters 4, 5, 6.

3. Device Physics and Radiation effects

3.1. Semiconductor fundamentals

Insulators are opposite of conductors because electrons in the insulators are closely and tightly bound to atoms by ionic bonds preventing such flow. In semicondutor matrials because of crystalline structure, valence electrons are shared between atoms. This sharing of valence electrons is called covalent bonding. In covalent bonding, it is very difficult for materials to move their electrons into the conduction band. At absolute 0 K, semiconductors behave like insulators. When the temperature increases, the resistivity of semiconductors decrease and thus the conductivity increases. Semiconductors are a different class of elements which have the conductivity between a conductor and an insulator. For electronics devices, mainly three types of semiconductors are used namely Germanium (Ge), Silicon (Si) and Gallium Arsenide (GaAs). Silicon and germanium are most commonly used for the sensor applications. At present and after the phase-II upgrade, the inner tracker of ATLAS will be made from silicon detectors only. In this section the different properties of silicon are briefly introduced.

3.1.1. Carrier Concentration

Semiconductors can be classified into two categories: intrinsic and extrinsic. A piece of semiconductor is called intrinsic if it is not doped with some other material. The number of free electrons can be calculated as the product of the density of states in the conduction band N(E) and of the Fermi function F(E) [54]:

$$n = \int_{E_c=0}^{E_{top}=\infty} N(E)F(E)dE, \tag{3.1}$$

where E_c is the lower bound in the conduction band, E_{top} is the top of the conduction band and E is the energy. The total density of states in the conduction band can be calculated as [54]:

$$N(E) = 4\pi\left(\frac{2m_n}{h^2}\right)^{2/3} E^{1/2}, \tag{3.2}$$

where m_n is the effective mass of the electrons and h is the Planck's constant.

The Fermi function (see figure 3.1) is given by [55]:

$$F(E) = \frac{1}{1 \, + \, e^{\frac{E-E_c}{kT}}}, \tag{3.3}$$

where E_c is the energy at the lower bound of the conduction band, since kT at room temperature is only 0.026 eV, for very low energies below 3 kT the Fermi function F(E) can be approximated by:

$$F(E) \approx e^{-\frac{E-E_c}{kT}}, \tag{3.4}$$

The concentration of free electrons and holes at a temperature T can be calculated as:

$$n = 2\Big(\frac{2\pi m_n kT}{h^2}\Big)^{3/2} e^{-\frac{E_C-E_F}{kT}} = N_C \cdot e^{-\frac{E_C-E_F}{kT}}, \tag{3.5}$$

$$p = 2\Big(\frac{2\pi m_p kT}{h^2}\Big)^{3/2} e^{-\frac{E_F-E_V}{kT}} = N_V \cdot e^{-\frac{E_F-E_V}{kT}}, \tag{3.6}$$

where n(p) is the concentration of electrons (holes) and m_n (m_p) is the effective mass of electrons (holes). N_C and N_V are the state densities in the conduction and valence band respectively. The corresponding values of theses states are 2.8×10^{19} cm^{-3} and 1.4×10^{19} cm^{-3} [56].

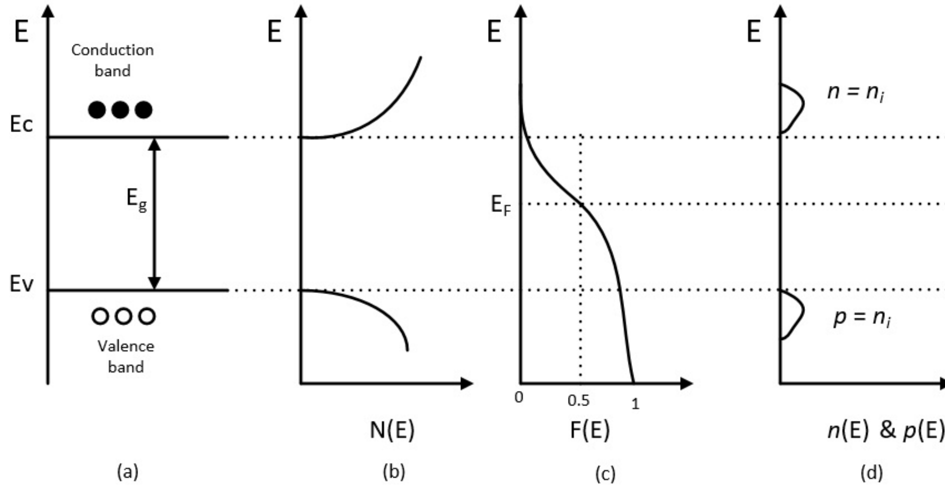


Figure 3.1. – Intrinsic semiconductor: (a) Band diagram. (b) density of states. (c) Fermi function. (d) carrier density.

At equilibrium for a particular material and temperature, the product of electrons and holes density is constant.

$$n \cdot p = n_i^2 = N_C \cdot e^{-\frac{E_C - E_F}{kT}} \times N_V \cdot e^{-\frac{E_F - E_V}{kT}} \tag{3.7}$$

$$n \cdot p = n_i^2 = N_C N_V \cdot e^{-\frac{E_g}{kT}} \tag{3.8}$$

The difference $E_C - E_V$ is known as energy gap E_g. At T=300 K, the intrinsic carrier concentration in silicon is given by:

$$n_i = 1.45 \times 10^{10}\ cm^{-3} \tag{3.9}$$

and the intrinsic Fermi level can be calculated as:

$$E_i = \frac{E_C\ +\ E_V}{2}\ +\ \frac{3}{4} kTln\left(\frac{m_n}{m_p}\right) \approx \frac{E_C\ +\ E_V}{2} \tag{3.10}$$

As the second term in the above equation is only 0.01 eV at room temperature and can be neglected.
A piece of silicon material is called extrinsic if some impurities are added to the material. The elements used to dope silicon are either from group III (e.g. boron) or from the group V (e.g. antimony, arsenic, and phosphorus) of the periodic table. For example, phosphorus is from group V and has an additional electron in its outermost shell which can be easily released as a free electron in the silicon lattice. Therefore, elements such as phosphorus are called as "donors" and the silicon doped with group V elements is said to be n-type. The holes are majority carriers and the electrons are minority carriers. Similarly when a silicon is doped with Boron from group III, which has one electron less than silicon in its outermost shell it can easily trap an electron from the silicon. Such elements from this group are known as "acceptors" and the silicon doped with group III elements is called p-type. The concentration of electrons as majority carriers is much higher than the concentration of the holes which are the minority carriers. A sketch in figure 3.2 shows a silicon lattice as intrinsic, n-type material and p-type material. The doping process leads to a shallow energy level in the forbidden energy of the band gap. In case of a p-type material, if the concentration of electrons is n and the acceptor doping concentration is N_A, the Fermi level is shifted towards the valence band (shown in figure 3.3) as:

$$E_F = E_i\ -\ kT\ ln\left(\frac{N_A}{n_i}\right) \tag{3.11}$$

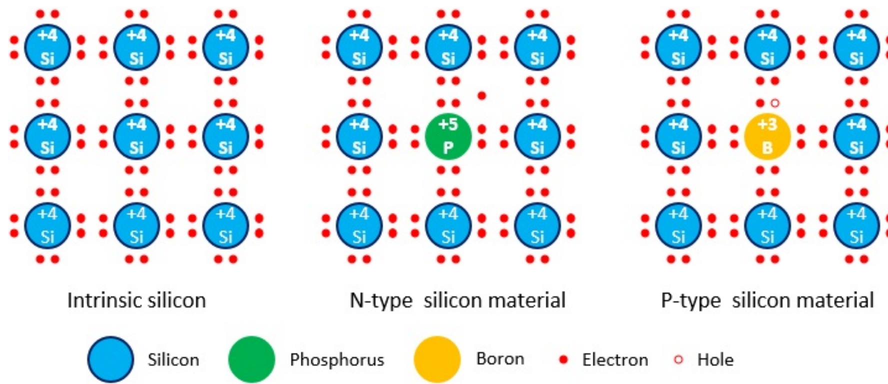


Figure 3.2. – Silicon doping profile with phosphorus and boron atoms.

Conversely, in case of a n-type material, if the concentration of electrons is p and the donor doping concentration is N_D, the Fermi level is shifted towards the conduction band as:

$$E_F = E_i \; + \; kT \; ln\left(\frac{N_D}{n_i}\right) \tag{3.12}$$

In practice, when a semiconductor is doped, it contains both donors and acceptors but in most cases only one dominates. If this is the case then effective doping is used which is the difference between acceptor and donor concentration.

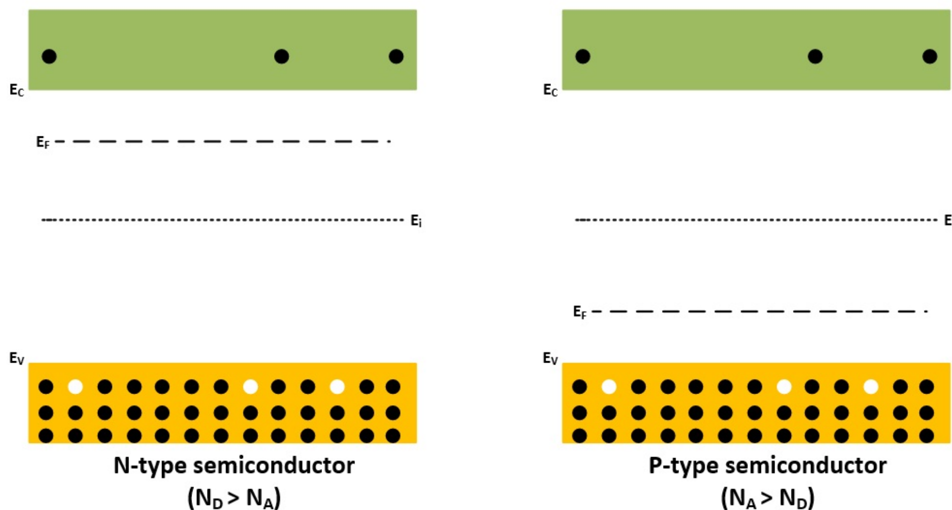


Figure 3.3. – Position of Fermi level for n-type and p-type semiconductor.

Position of Fermi Energy Level

The position of the Fermi energy level for n and p-type material is sketched in figure 3.1. It is noticed that at T=300 K the Fermi energy level is a function of donor concentration (n-type silicon) or a function of acceptor concentration (p-type silicon). Figure 3.4 shows a plot comparing the position of Fermi level in both cases and depending on the dopant concentration.

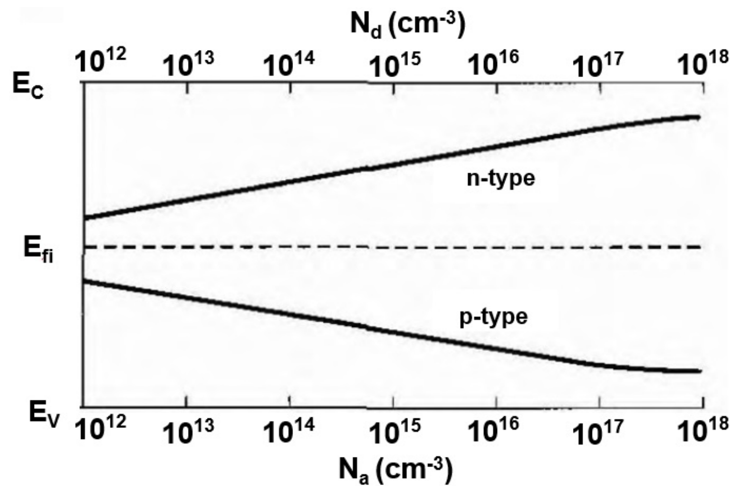


Figure 3.4. – Position of Fermi level versus doping concentrations [57].

The intrinsic carrier concentration is a strong function of temperature, as seen from the plot in figure 3.5 which shows the variation of the position of the Fermi level with varying the temperature. As the temperature increases, the intrinsic carrier concentration also increases and the Fermi level moves closer to the intrinsic Fermi level. At high temperature, the material starts to degrade and begins to lose its extrinsic characteristics. This leads to a transformation towards an intrinsic semiconductor.

3.1.2. Carrier Lifetime

In general, the electrons in the conduction band of a semiconductor will recombine with the holes in the valence band. This recombination mechanism can happen in two ways: direct recombination and indirect recombination. In direct recombination process, electrons fall directly from the conduction band to empty states (holes) in the valence band. During this transition, there will be energy lost by an electron by emission of a photon. The probability of a recombination process is constant in time. At a time t, the decay rate of electrons is proportional to the number of remaining electrons and the number of holes. Therefore, the net

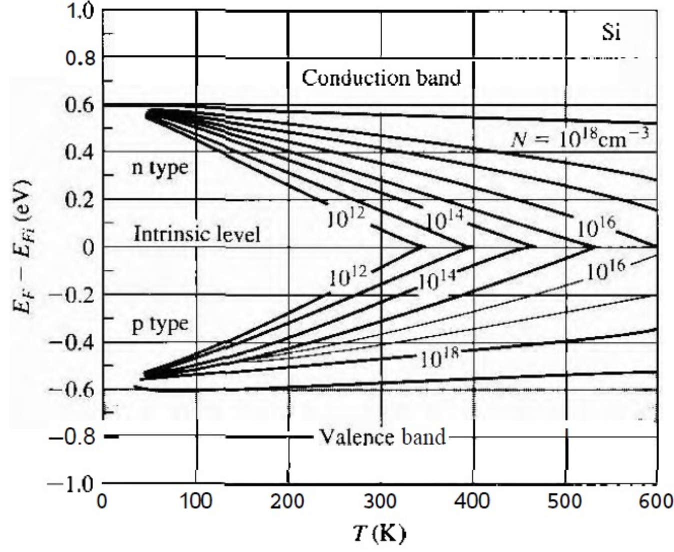


Figure 3.5. – Position of Fermi level versus temperature at various doping concentrations [57].

rate of change in electron concentration of the conduction band can be calculated as [57]:

$$\frac{dn(t)}{dt} = \alpha_r n_i^2 - \alpha_r n(t)p(t) \tag{3.13}$$

where $\alpha_r n_i^2$ is the thermal generation rate and $\alpha_r n(t)p(t)$ is the recombination rate. Now let us assume that there is an excitation which leads to an increase in the number of electron-hole pairs. Suppose the electron concentration (Δn) and hole concentration (Δp) are equal. Then after the recombination at time t=t_1 the instantaneous concentrations of excess carriers $\delta n(t)$ and $\delta p(t)$ are also equal. Therefore calculating the net total concentration in terms of the equilibrium with n_0 and p_0 as:

$$\frac{d\delta n(t)}{dt} = \alpha_r n_i^2 - \alpha_r \Big[n_0 + \delta n(t)\Big]\Big[p_0 + \delta p(t)\Big] \tag{3.14}$$

$$\frac{d\delta n(t)}{dt} = -\alpha_r \Big[(n_0 + p_0)\delta n(t) + \delta n^2(t)\Big] \tag{3.15}$$

Solving this non-linear equation is not that easy, so we need to take some assumptions such as $\delta\, n\, ^2(t)$ can be neglected and also the material is an extrinsic semiconductor which makes us to neglect the term representing the equilibrium minority charge carriers. For example, if the material is p-type then the equation becomes:

$$\frac{d\delta n(t)}{dt} = -\alpha_r p_0 \delta n(t) \tag{3.16}$$

The solution of above expression is an exponential decay from the original excess carrier concentration Δn:

$$\delta n(t) = \Delta n \cdot e^{-\alpha_r p_0 t} = \Delta n \cdot e^{-t/\tau_n} \tag{3.17}$$

In a p-type semiconductor, the excess electrons will recombine with a decay constant of $\tau_n = 1/\alpha_r p_0$ is called the recombination lifetime. The above calculation is made in terms of the minority carriers, thus τ_n is also called the minority carrier life-time.

3.1.3. The p-n semiconductor diode

A device called p-n diode is created by joining an n-type and a p -type material together. As we will discuss in this section, when this diode is reversely biased it can be used as the basic sensor element.

3.1.3.1. Structure of p-n diode and thermal equilibrium

If one p-type region is joined with one n-type region then a new structure is formed called p-n junction which is sketched in figure 3.6. The interface of these two regions is known as a metallurgical junction.

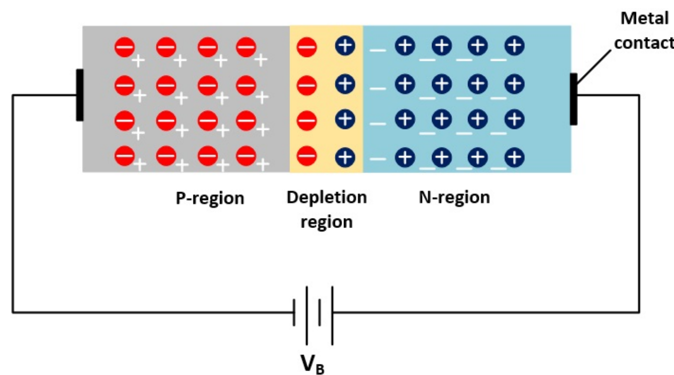


Figure 3.6. – A simplified view of p-n semiconductor junction.

To start with, let us consider there is no external bias provided, i.e $V_B = 0$. The majority charge carriers in the n-region "electrons" will start to diffuse towards

the p-region due to the concentration gradient, whereas, the majority charge carriers in the p-region holes will move towards the n-region. The majority charge carriers recombine together, and leave behind in the n-region an area of positively charger ions, and similarly in the p-region an area of negative charged ions. When the electrons diffuse from the n-region they leave positively charged ions and similarly when holes diffuse from the p-region they leave negative charged ions. These ions will induce an electric field near the metallurgical junction which results in a voltage difference. This voltage difference due to the remaining ion charges is known as the built-in voltage V_{bi}. This region with the positive and negative immobile ions is called the depletion zone (also called "space charge region"). In thermal equilibrium, no current is produced by this voltage since both diffusion and drift current cancel each other. There is then only one constant Fermi level E_F which is then constant throughout the junction, as illustrated in figure 3.7. For an abrupt pn junction the built-in voltage can be calculated as [58]:

$$V_{bi} = \frac{kT}{e} ln\left(\frac{n_{0,n}\, p_{0,p}}{n_i^2}\right) \approx V_T\ ln\left(\frac{N_D \cdot N_A}{n_i^2}\right) \tag{3.18}$$

Where $n_{0,n}$ is the electron concentration in the n-region and $p_{0,p}$ is the hole concentration in the p-region. V_T is known as the thermal voltage with the value of 26 mV at room temperature.

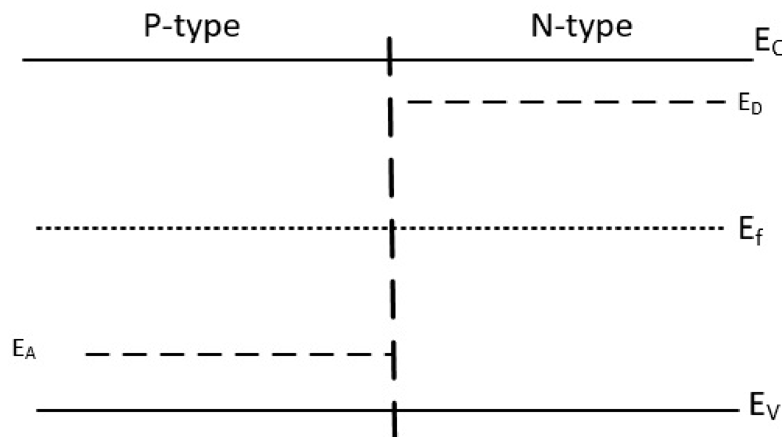


Figure 3.7. – Energy band diagram of p-n junction under no bias at 0K.

3.1.3.2. Reverse bias applied to p-n diode

A junction is reversed bias if an external voltage V_B is applied to the p-n diode such that the negative terminal of the supply is connected to the p-region and the positive terminal of the supply to the n-region as sketched in figure 3.6. In this configuration, the Fermi energy level will no longer be constant throughout

the p-n junction, as seen in figure 3.8. Because of this bias, the holes (majority charge carriers) in the p-region will be attracted towards the negative terminal and the electrons (majority charge carriers) in the n-region will also get attracted towards positive terminal of V_B.

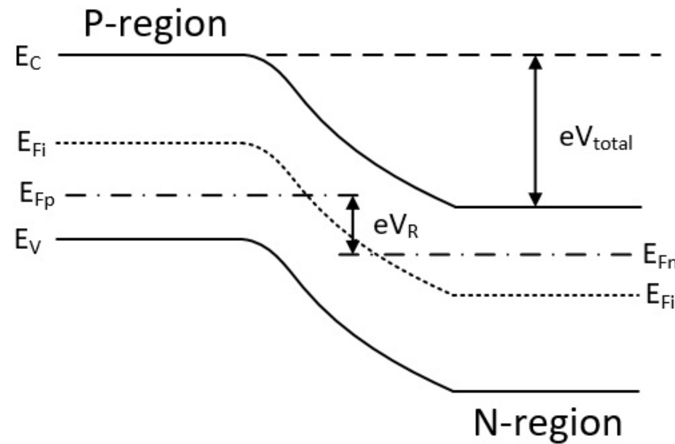


Figure 3.8. – Energy band diagram of pn junction under reverse bias.

This mechanism results in an increase in the size of the depletion region. The width of the depletion region and the electric field in the depletion region can be calculated by solving the one-dimensional Poisson equation. Taking some assumption, and the total depletion region width is obtained by:

$$W = x_n + x_p = \sqrt{\frac{2\varepsilon_0\varepsilon_{si}}{e}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V + V_{bi})} \tag{3.19}$$

where V is the externally applied. W is the total width of the depletion region, and x_n and x_p are the part of the depletion zone in the n- and p-region respectively.
The built-in voltage is nearly 0.6 V, which is very small as compared to a typical operating voltages for a reversed bias diode used as a detector, and can be neglected. In this case, the depletion zone is grown in the p-type material and the depletion region can be approximated as:

$$W \approx x_p \approx \sqrt{\frac{2\varepsilon_0\varepsilon_{si}}{e \cdot N_D}V} \tag{3.20}$$

$$W \propto \sqrt{\rho \cdot V} \tag{3.21}$$

The electric field reaches its maximum value and can be calculated as:

$$E_{max} = \frac{2V}{W} \approx \sqrt{\frac{2e \cdot N_D}{\varepsilon_0 \varepsilon_{si}} V} \tag{3.22}$$

In the case of reverse bias, in the absence of radiation, there is always a leakage current or dark current inside the p-n diode due to two components. The first is the diffusion gradient which involves movement of free carriers from the undepleted region to the space charge region. The second component which is more dominating is thermal generation at generation-recombination centres near the device surface and in the depletion region. The leakage current per unit area in the space charge region can be approximated as:

$$J_{vol} \approx -e\frac{n_i}{\tau_g} W \approx -e\frac{n_i}{\tau_g}\sqrt{\frac{2\varepsilon_0 \varepsilon_{si}}{e \cdot N_D} V} \tag{3.23}$$

where J_{vol} is generation current per unit area, τ_g is the carrier lifetime and n_i is the intrinsic carrier concentration. As seen previously temperature plays a vital role. Here the leakage current increases with the increase in the temperature. The relation can be described by [58]:

$$J_{vol} \propto T^2 e^{-E_g(T)/2kT} \tag{3.24}$$

For silicon, the volume current gets double for every 8K increase in the temperature.

3.2. Interaction of particles with matter

Charged particles lose part of their energy through elastic collisions with electrons when passing through the sensor material. The mean energy loss of a heavy charged particle per unit path length (is also known as "stopping power") is described analytically with the Bethe-Bloch formula [59] [60] which has been derived from quantum mechanics in the 1930s.

$$-\left\langle \frac{dE}{dx} \right\rangle = \frac{4\pi r_e^2 c^2 N_A z^2 Z}{A\beta^2} \times \left[\frac{1}{2} ln \frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} - \beta^2 + ...\right] \tag{3.25}$$

where
D is the classical electron radius ;
m_e is the electron mass ;
Z is the atomic number of the material ;
A is the atomic number of the material ;

N_A is the Avogadro's number with 6.022×10^{23} mol^{-1} ;
I is the mean excitation potential ;
ρ is the density of the material ;
z is the charge of a incident particle ;
c is the speed of light ;
β= v/c is the velocity of the incident particle in units of the speed of light ;
γ (Lorentz factor)= $(\sqrt{1-\beta^2})^{-1}$

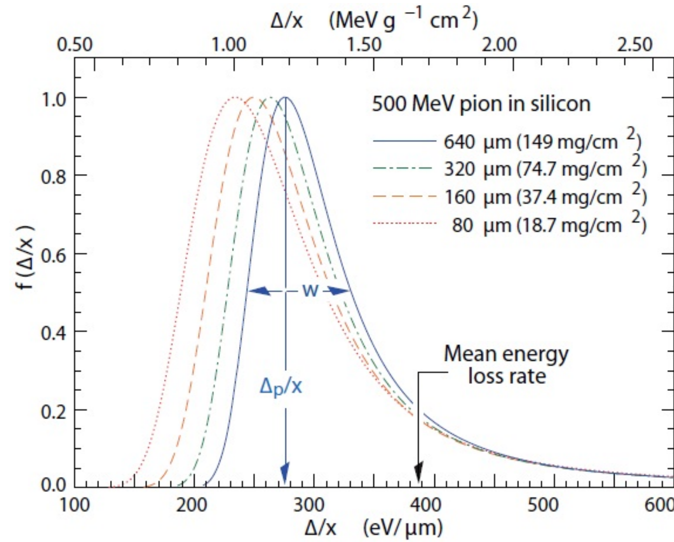


Figure 3.9. – Straggling functions f(Δ/x) in silicon for 500 MeV pions, normalized to unity at the most probable value. [61]

Figure 3.9 shows this variation in the distrubition with different thickness of silicon detectors. The peak in the distribution defines the most probable energy loss. The average value of this distribution is higher than the most probable value (MPV) due to the tail. During the ionization process, the electrons which gain very high energy from the interaction with the charged particle are knocked out of an atom. These electrons are called as δ-electrons or knock-on electrons.
To calculate the MPV of the electon-hole pairs generated during the ionization process in a thin silicon sensors is described by [62]:

$$Q_{MPV} = \frac{d}{\mu m}\left(53q_e + 4.5q_e\, ln\left(\frac{d}{\mu m}\right)\right) \tag{3.26}$$

where q_e is the charge of an electron, d is the thickness of the sensor. Hence with the equation shown above, a minimum ionizing particle (MIP) striking a silicon sensor of typical thickness of 250 μm most likely deposits a charge equal to 3.1 fC.

3.3. Detection principle and signal formation in a sensor

To read out the generated electron-hole pairs during the ionization process, a high field is usually applied to the sensor electrodes so that these charge carriers are separated. The positive charge carriers drift towards the negative potential and conversely the negative charge carriers drift towards the positive potential. A cross-sectional view of a depleted sensor diode in which a passing particle trigger the with ionization process is sketched in figure 3.10. Due to the movement of two different sort of charge carriers, instantaneously a current flows on each end. The Ramo's theorem [63] provides an analytical expression of the induced current which is given as:

$$i = -q \, \vec{E_w} \cdot \vec{v} \tag{3.27}$$

where i is the instantaneous current, q is the charge, v is the drift velocity and E_w is the weighting field.

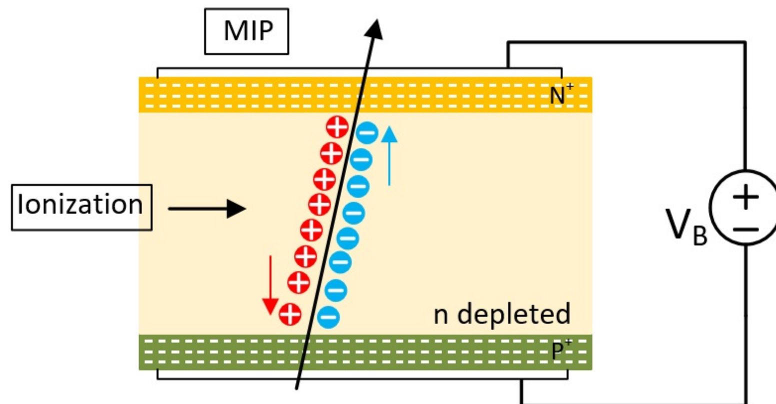


Figure 3.10. – Cross-section of a depleted sensor diode in which a passing particle electron-hole pairs.

If the applied voltage V_B is strong enough, a full depleted region might be formed due to the reverse biasing of the p-n junction. If this voltage is so large that it extends the depletion region over the whole sensor thickness then we called it as full depletion voltage V_{full} and is expressed as [58]:

$$V_{full} = \frac{eN_D d^2}{2\varepsilon_0 \varepsilon_{si}}$$

where e is the elementary charge, N_D is the dopant concentration of the silicon substrate, d is the sensor thickness and ε_{si} is the relative permittivity constant in silicon. Depending on the sensor, the value of the reverse bias voltage V_B varies

from about 20 V to nearly 1000 V. A sensor operates in over-depletion situation if the applied bias voltage is larger than the full depletion voltage magnitude. The depleted silicon sensor acts like a parallel-plate capacitor and the value of the capacitance is estimated using the formula:

$$C_{dep} = \frac{2\varepsilon_0 \varepsilon_{si} A}{d} \tag{3.28}$$

where A is the area of the sensor.
Usually, the diffusion process and new thermally generated charge carriers lead to a current flow through the depleted sensor diode which is known as leakage current. The value of the sensor leakage current can be estimated as [59]:

$$I_{leakage} = -eAd\frac{n_i}{\tau_g} \tag{3.29}$$

where n_i is the intrinsic carrier concentration and τ_g is the life time of thermally generated carriers. In particular, when a silicon sensor is exposed to irradiation, the carrier life time of the carriers are reduced and hence there is an increase in the leakage current. This is furthermore described in section 3.5

3.4. Sensor Segmentation

To know the exact position information of the hit, the sensor electrodes are segmented. Figure 3.11 on the left shows a structure of single ended strip detector. This kind of electrode arrangement usually provides information in one dimension only. Moreover, the binary readout with the segmented pitch p mostly drives the spatial resolution. With a uniform hit probability, and a hit position between two strips, the normalized probability distribution function f is expressed as:

$$\int_{-p/2}^{p/2} f(x)dx = 1 \tag{3.30}$$

which gives f= 1/p. Then the resolution which is calculated as RMS deviation is calculated as:

$$\Delta x = \sqrt{\frac{1}{p}\int_{-p/2}^{p/2} x^2 dx} = \frac{p}{\sqrt{12}} \tag{3.31}$$

Furthermore, the charge is shared between several strips and the spatial resolution can be improved by measuring the signal magnitude read on each strip. A custom made read-out integrated circuit is built, which is used to read out the signals from the sensor. This chip is placed close to the detector and connected

with wire-bonds going from the pads located on the detector to the readout chip. To have better spatial resolution the sensor can be segmented into 2 directions which gives information in two-dimensions. The structure of double-sided strip detector is on the right side in figure 3.11 on right side. In order with high data rate, the double sided strip detector suffers from hit ambiguities.

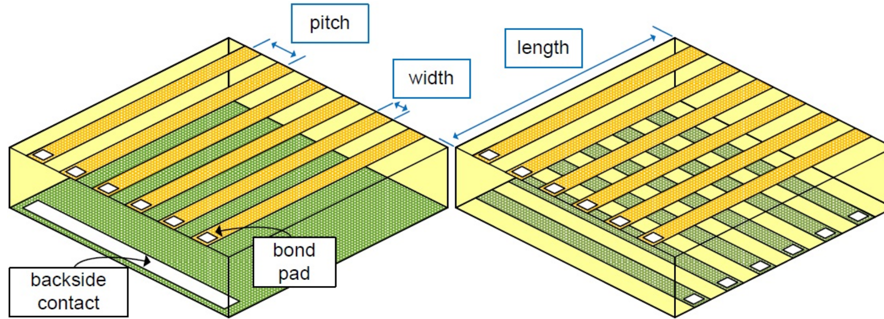


Figure 3.11. – Structure of single-ended and double-sided strip detector.

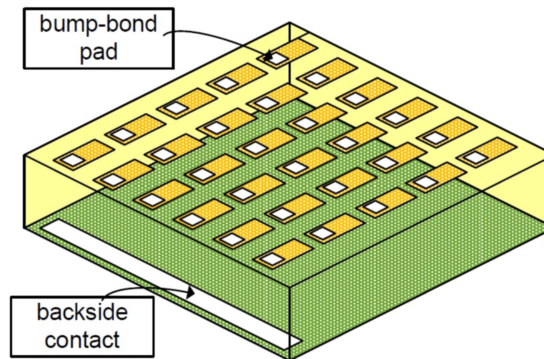


Figure 3.12. – Structure of pixelated sensor.

Figure 3.12 shows a pixelated sensor structure. Pixel segmentation provides two-dimensional information with good spatial resolution and no ghost hit ambiguities when compared to double-sided strip detectors. Lower detector capacitance and low leakage current is a result of the small area of sensor segments. In the case of a pixelated sensor, detector capacitance is dominated by fringing capacitances to adjacent sensor segments. An important advantage of the small pixel area is a reduced hit occupancy when compared to double-sided strip detectors. Therefore, in a high hit rate environment like ATLAS experiment, the pixel detector is the only operational sensor geometry for the innermost detector layers. However, as there is a strong increase in the number of readout channels, this type of detector imposes additional constraints on readout electronics and require an additional integration step. In a hybrid pixel detector concept as shown in figure 3.13, the readout chip is placed on top of the sensor and the size

of each readout channel has to match exactly the size of the sensor pixel. Each sensor pixel is connected to the corresponding channel of the readout chip by flip-chip and bump-bonding technique.

In a monolithic pixel detector concept, the readout chip and the sensor is placed on a single die. This concept offers various advantages such as no hybridization is required, reduced material budget, low cost and in the case of the processes we consider later in this work, considerable depleted regions in high resistive substrates, fast charge collection by drift, multiple wells for shielding, etc...

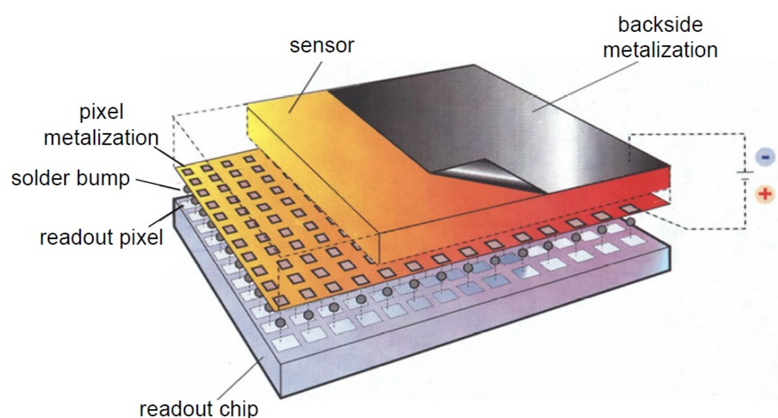


Figure 3.13. – Schematic view of a hybrid pixel detector.

3.5. Radiation effects in Semiconductors

Pixel detectors used as tracking devices are placed very close to the interaction point in high energy experiments. They are therefore exposed to very intense irradiation which damages the sensors and the electronics. The consequences of radiation in silicon can be of three sorts: bulk damage, surface damage and single-event effects (SEE). Bulk and surface damages changes the properties of the material and can lead to increase of the dark current, change of effective doping concentration, charge trapping and increase in full depletion voltage. In this section, radiation effects are described briefly.

3.5.1. Bulk damage

When a neutron or a high-energy charged particle strikes silicon atoms, they move from their original positions and create interstitials I and vacancies V (Frenkel pair) as shown in figure 3.14. Usually, the incoming particle has a

very high energy which creates much more complex configurations such as di-vacancies V_2 and triple-vacancies V_3. These vacancy complexes produce crystal imperfections which lead to the formation of additional energy levels.

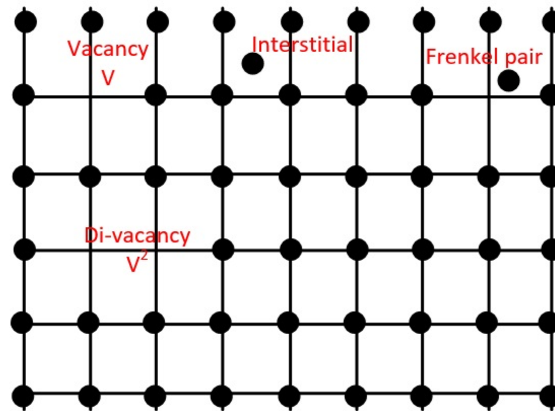


Figure 3.14. – Atomic displacements in the silicon lattice caused by the interactions of incidence particles

The new energy levels can be classified as shallow and deep trap levels. These trap levels change the electric properties of the material. The electronics nature of radiation-induced shallow trap mostly compensates for donors and act as acceptors. This leads to an increase in the absolute effective doping concentration. As a consequence material from a low doped n-type silicon might change to a p-type silicon. This phenomenon is known as "type inversion". In figure 3.15 the variation of effective doping density versus normalized fluence [a] is shown. The effective doping density decreases with a fluence up to 2-5 $\cdot$ 10^{12} cm^{-2}. After this value, type inversion phenomenon takes place and then effective doping increases linearly with the fluence [64] [65].

On top of the change in effective doping, another effect of radiation if the formation of more recombination-generation channels are formed due to deep traps which lead to decrease of the carrier life time and an increase in the thermal generation rate. As a consequence this results in signal degradation and increase in the leakage current.

A minimum recoil energy E_d of about 25 eV [67] can knock out a single silicon atom from its lattice site. If the value of the recoil energy is less than 25 eV then it will lead to lattice vibrations only. For electrons, about 260 keV energy is required to make such a collision and due to a higher mass, protons and neutrons require about 190 eV of energy to cause bulk damage. If the energy of the primary knocked-out atom is more than 130 keV, they are capable of removing other atoms locally. This phenomenon is referred to as defect clusters. Simula-

a. It is the number of particles which cross a unit of area.

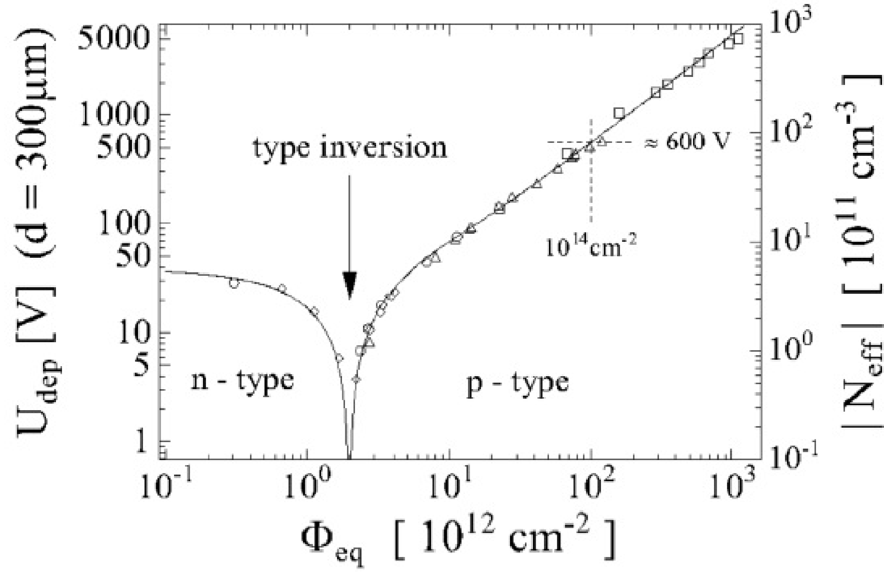


Figure 3.15. – Variation in the full depletion voltage of a silicon sensor and effective doping concentration as a function of normalized fluence [66].

tion results show that the inner diameter of these clusters is around 10 nm and it is surrounded by a 200 nm wide area which has a lower defect density [68].

To achieve good approximation, the damage in bulk radiation of silicon is linearly proportional to the non-ionizing energy deposited by energetic nuclear recoils and to the particle flux. The hypothesis of the Non-Ionizing Energy Loss (NIEL) [69], defines the bulk damage cross section by [70]:

$$D(E_p) = \sum_{n=i} \sigma(E_p) \int_{E_{Rmin}}^{E_{Rmax}} f_i \ (E_p, E_R) \ P(E_R) \ dE_R \qquad (3.32)$$

where all the possible interaction are considered in the sum, E_R is the energy of the recoiling nucleus, the function f_i describes the distribution of the recoil atom, and the function $P(E_R)$ [71] is the Lindhard partition function of the energy loss in non ionizing processes. The total displacement damage per volume is:

$$T_{dam} = N.t_{exp} \int_0^{\infty} \phi(E_p) \ D(E_p) \ dE_p \qquad (3.33)$$

where t_{exp} is exposure time, $\phi(E_p)$ is the differential particle flux, and N is the number of silicon atoms per unit volume.

Figure 3.16 shows the displacement damage cross-section in silicon for protons, neutrons, pions and electrons. To characterize the displacement damage caused by different particles with different energies, we take NIEL value which

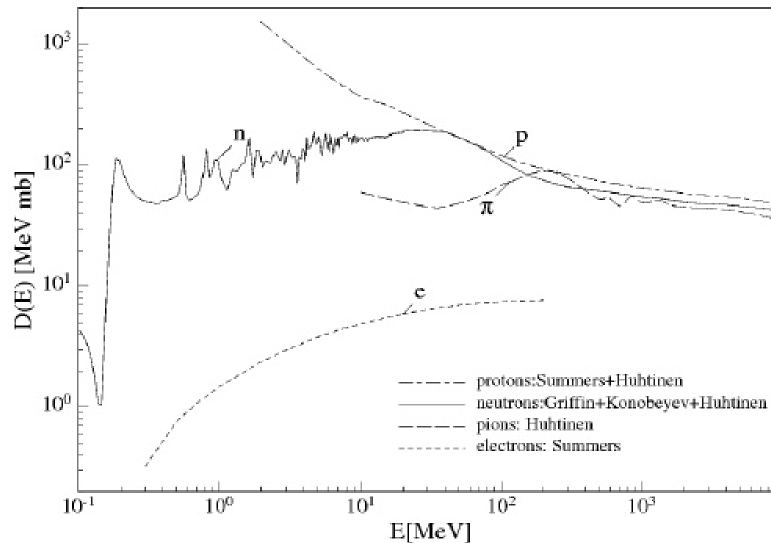


Figure 3.16. – Displacement damage cross-section in silicon for various particles [72] [73] [74].

is usually scaled by referring to the equivalent fluence of 1 MeV neutrons. Different NIEL value is calculated with different particles having same energy. For instance, a 200 MeV proton has roughly the same NIEL as an 1 MeV neutron.

3.5.2. Surface damage

In a CMOS silicon process, MOS transistors are more sensitive to ionization compared to bulk damage. This surface damage depends on the total energy of ionizing radiation absorbed in SiO_2, and is characterized by what is called Total-Ionizing-Dose (TID). The common unit to quantify the ionization damage is "rad". In a MKS system, the unit Gray is employed which is equal to 100 rad. When an energetic ionizing particle strikes on the transistor it produces defects in the oxide, and also on the interface between silicon-oxide. In 1964, the first study on TID degradation on MOS devices at the Naval Research Laboratory (NRL) was performed [75].

Figure 3.17 illustrates the band diagram showing the transport and trapping of holes in the oxide. Many publications [76] [77] [78] have described the different processes in detail. We briefly describe the four processes below.

Oxide Traps

Ionizing radiation causes creation of electron-hole pairs in the oxide layer. Assuming a positive bias is applied to the gate, the electrons are quickly collected at the gate electrode due to their high mobility in the oxide ($\mu_{n,oxide}$=20 cm^2/Vs) at room temperature. However, the holes move very slowly towards the Si/SiO_2 in-

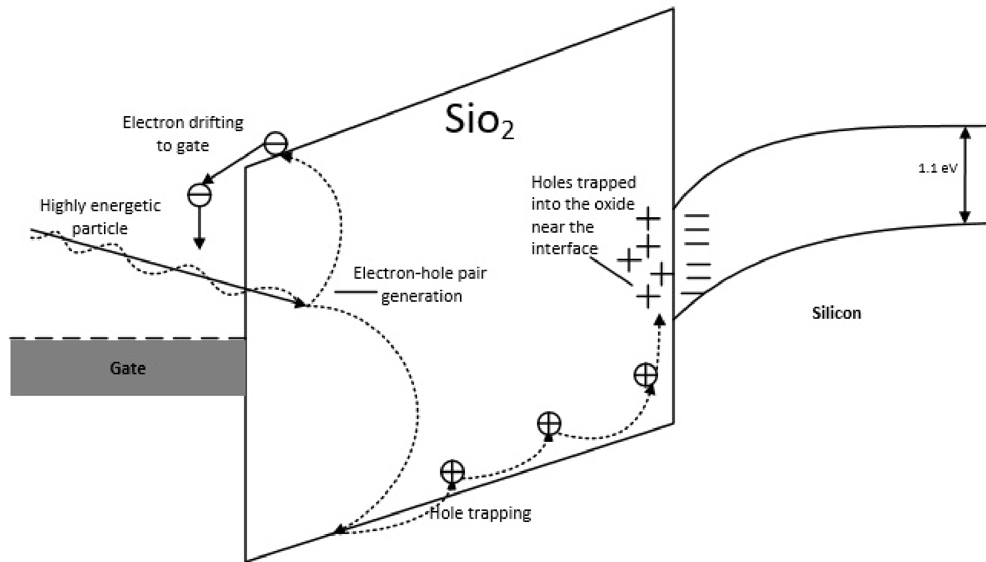


Figure 3.17. – Band diagram showing the transport and trapping of holes in the oxide of NMOS transistor.

terface due to very low mobility in the oxide ($\mu_{p,oxide}$=2 × 10^{-5} cm^2/Vs) at room temperature. As the holes moves towards the vicinity of the Si-SiO_2 interface, it causes a distortion of the local potential field of the SiO_2 lattice. This local distortion makes the hole traps become deeper. The holes captured in these deep traps cannot move further. During the irradiation, the deep trap centers will collect the holes which gives rise to a fixed positive oxide charge Q_{ox}. These deep trap centers are also identified to be the point defects in the SiO_2 structure with a oxygen vacancy. The density of positive oxide trapped charges depends on parameters such as oxide quality and electric field. The non-trapped holes will recombine with electrons coming from the silicon after reaching the interface. Moreover, the electrons might tunnel from the silicon surface into the oxide and recombine with trapped holes [79]. The trapped positive charges at the interface leads to a generation of parasitic negatively charged channels which eventually change the electrical properties of a transistor. In a n-channel transistor, the threshold voltage is lowered due to positive oxide charge since it attracts more electrons to form the silicon inversion. Conversely, in a p-channel transistor the absolute threshold voltage is increased, i.e V_T is more negative. Recent studies [80] [81] [82] have shown a severe effect on the threshold shift as seen in the case of NMOS transistor. These threshold voltage shifts are a big concern in analog circuitry and also change the switching times in digital circuitry. Even worse, transistor can become always on or always off with no possibility to switch them any more.

Interface Traps

Ionizing radiation also creates additional interface traps which are caused by liberation of protons from the hole (h^+). These traps are found in the silicon energy gap as shown in figure 3.18. They act as additional acceptor or donor states. Previous work showed [83] [84] that if the Fermi level is present above the trap energy level, the trap "accepts" an electron from the silicon. This makes the interface trap to be negatively charged. Therefore, for an NMOS transistor, the interface traps are predominantly negatively charged which results in positive threshold-voltage shifts. Conversely, traps in the lower portion of the band gap are predominately donors. If the Fermi level is present below the trap energy level, the trap "accepts" an electron from the silicon. This makes the interface trap to be positively charged. Therefore, for an PMOS transistor, the interface traps are predominantly positively charged which results in negative threshold-voltage shifts. For a NMOS transistor, the generation of fixed positive oxide traps is faster than interface traps. At higher TID levels, slower build up of interface traps gives rise to the so-called rebound in the evolution of the electrical parameters. The degradation in the threshold and drain current of the 65 nm TSMC MOS devices as shown in the figure 3.19. Additionally, the increased density in the interface states also results in the flicker noise of MOS transistors.

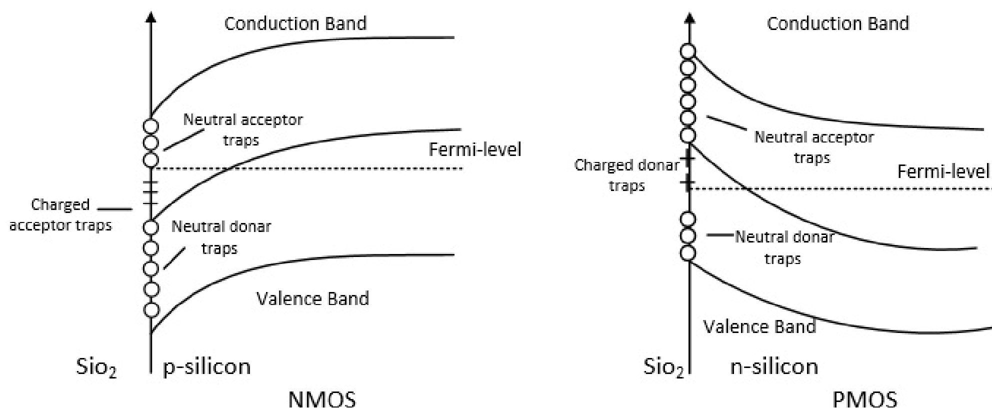


Figure 3.18. – Band diagram showing the behavior of interface states for NMOS and PMOS transistor.

In modern deep sub-micrometer technology, scaling down of a device usually tends to make it more radiation tolerant. The reason is the reduction of the number of trapped charges due to the fact that the oxide thickness becomes thinner when scaling down. Furthermore, shallow-trench isolation (STI) is the most advanced technique used for field oxide for device isolation in modern IC fabrication. When considering TID effects, the radiation-induced oxide traps and interface traps build-up along or near the STI side-wall which results in leakage

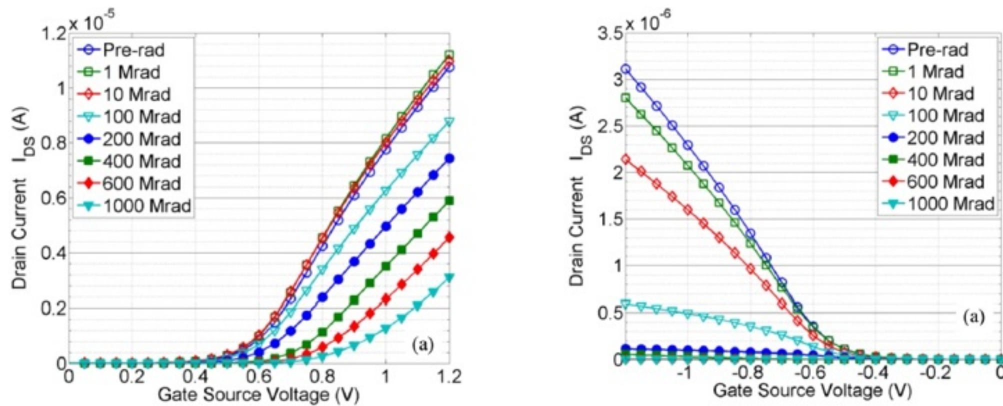


Figure 3.19. – NMOS $I_{DS}(V_{GS})$ characteristics (left) and PMOS $I_{DS}(V_{GS})$ characteristics (right). DC performance of n and p-channel transistors are presented in 65 nm bulk CMOS devices was investigated using 10 keV X-rays. Measurements were taken at room temperature up to 1 Grad [82].

paths. These leakage paths degrades the performance and increases the static power dissipation after the irradiation. In 65 nm technology [82], 400 nm thick STI field oxide is placed to isolate one device from the other. To overcome drawbacks, special design techniques can also be applied to increase the radiation tolerance of the electronics. Two major used techniques are P+-type guard rings, creating isolation between the wells and the enclosed gate NMOS transistor layout. The usage of guard rings and ELTs strategy eliminates the parasitic leakage paths between the adjacent devices.

3.5.3. Single-Event Effects

Single Event Effect (SEE) is a phenomenon induced by the striking of a highly-ionizing particles in electronic chips which leads to change in the memory state. These are also referred as soft-errors. An explanation for the Single Event Upset (SEU) meachnism was first proposed in 1962 by J.T. Wallmark and S.M. Marcus. Moreover, the first observation of SEE on earth was in 1978 [85].

3.5.3.1. Single-Event Latch-up (SEL)

The most serious reliability concern in integrated circuit is known as Latch-up. In the silicon bulk, a parasitic thyristor is formed by the parasitic junction structure as sketched in figure 3.20. This mechanism can be mitigated by some layout techniques and process modification [86]. An energetic charged particle

that would pass through the CMOS device depositing charges in the parasitic thyristor could lead to a positive current loop. Due to the positive feedback loop, the current inside the device increases very sharply and breaks the device. This phenomenon is known as "Single Event Latch-up" (SEL). Since many years, SEL has been studied mainly with heavy ions [87] and also with neutrons irradiation [88].

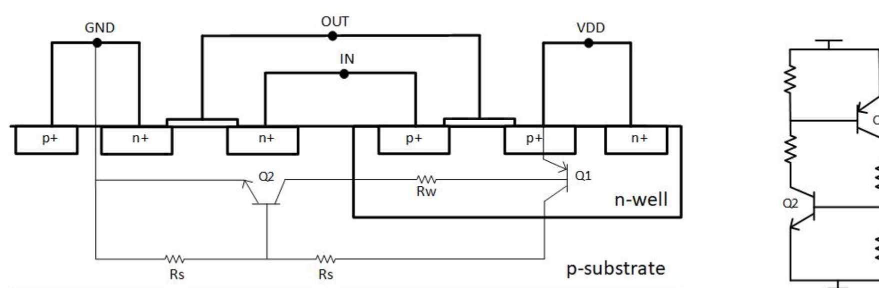


Figure 3.20. – Cross-section of a CMOS inverter in a bulk silicon technology with PNPN parasitics thyristor (left) and its schematic structure (right)

3.5.3.2. Single-Event Upset (SEU)

A high energy charged particle or highly ionizing particles produces a track of ionization with electron-hole pairs when passing through the device as sketched in figure 3.21. A cylindrical track of electron hole pairs is inversely proportional to substrate doping. When applying an electric field, the electron-hole pairs are quickly separated as they drift in opposite directions and are collected. Charge moving to a sensitive node (drain of a MOS transistor) is equivalent to current flow through that node. This charge collection is a drift process which might be completed in few nanoseconds followed by a much slower diffusion process shown in figure 3.21. The total collected charge is calculated by the integral over time of current.

The magnitude of the collected charge in a sensitive load depends on a complex combination of factors like the size of the device, biasing of the various circuit nodes, substrate structure and device doping [89]. However, two main factors play an important role: type of the incident particle, and its energy and trajectory in the vicinity of the sensitive node. The collected charge modifies the value stored at the node only if it exceeds a particular threshold called critical charge, $Q_{crit.}$. However, the sensitivity of SEU increases with the scaling down of the technology since the critical charge is proportional to the node capacitance and to the supply voltage, two quantities that have a tendency to go down in magnitude when going to smaller feature sizes. This means that less charge is needed to induce an SEU. The value of the critical charge can be obtained from simulations.

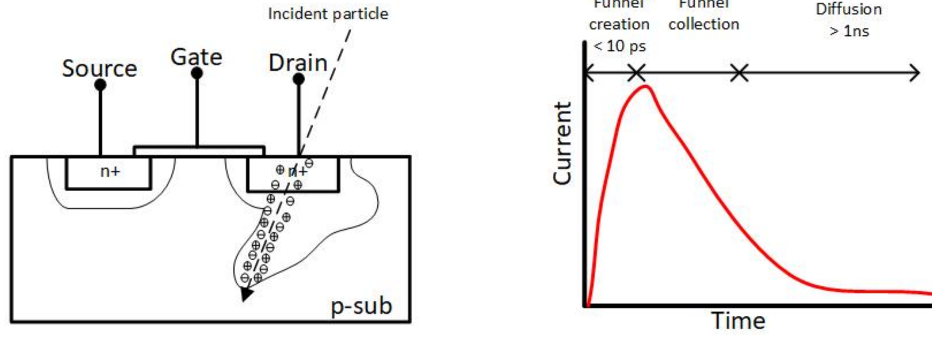


Figure 3.21. – Energetic particle strikes on drain of the transistor and funnelling (left) and resulting a current pulse (right).

The amount of energy deposited by a charged particle per unit of length can be expressed in terms of linear energy transfer (LET). In silicon, 3.6 eV of energy is required to create a single electron-hole pair. In SEU studies, LET is used as stopping power (dE/dx). This incremental energy dE is measured in MeV and material thickness is usually measured in the units of mg/cm^2. LET has units of MeV/cm^2/mg. The plot in figure 3.22 shows the stopping power of a proton, α particle and magnesium ion in silicon. As seen from the plot, except at low energies, higher the charge on the ion the higher is the stopping power. The magnesium ion produces more ionization per unit length compared to α particle and proton. The deposited charge can be expressed through the formula.

$$Q_{dep} = \frac{q\rho L_f LET}{E_{eh}} \tag{3.34}$$

Where $q = 1.602 \times 10^{-19}$ C, L_f is the funnel length which is length of the region involved in the charge collection and ρ is the density of the traversed material with the units mg/cm^3). The size of the funnel length is in the order of 1-3 μm. The value of LET is determined by the atomic number of the material traversed and is inversely proportional to the energy of incident particle.

LET measurements can be determined by exposing a device to an ion beam. By knowing the LET value we could calculate the upset rate in the real application radiation environment. The value obtained from the experiment is the number of errors N per number of particle of a certain energy deposited. It is then easy to compute the cross-section of a memory which can be expressed as:

$$\sigma = \frac{N}{\phi \cdot cos\theta} \tag{3.35}$$

where θ is the beam angle with respect to the Device Under Test and ϕ is the

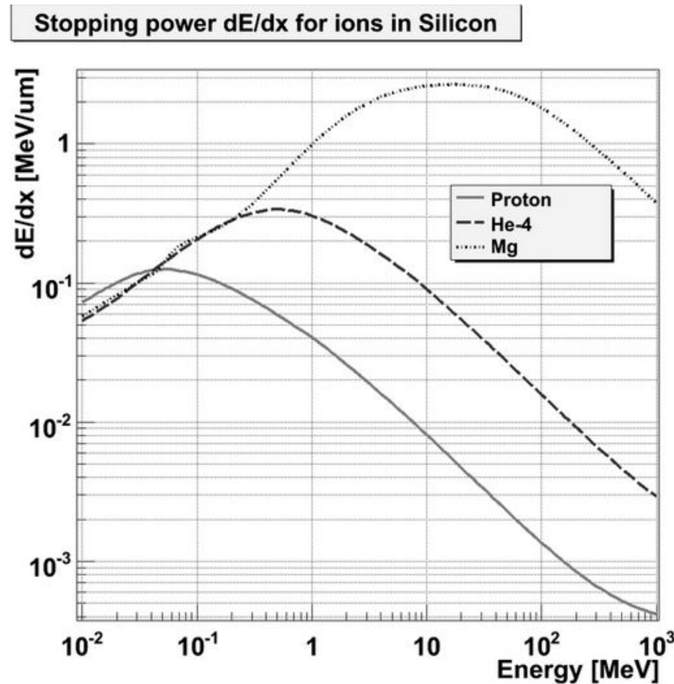


Figure 3.22. – Stopping power for various ions in silicon versus kinetic ion energy [90].

particle flux. The cross-section can be given as a value which is expressed in units of cm^2.

Figure 3.23 shows the cross-section versus LET plot for bandgap voltage reference circuit. It can be seen that the cross-section curve is saturated when the LET of the particle is above 50-60 $MeV \cdot cm^2/g$.

3.5.3.3. Critical charge simulations

It is very important to study the circuit response to a single-event upset mechanism and this is usually done using a circuit simulator (for example, by SPICE or one of its various commercial versions). An SEU is usually modelled by using a current source with an exponential time profile to inject the charge into the node of interest. Figure 3.24(a) shows a standard SRAM cell with an injected current on node Q. Figure 3.24(b) illustrates the current pulse generated during the ionization process. The total injected charge can be calculated by doing the integral of the current. By doing a parametric simulation, we could predict the critical charge Q_{Crit} for an upset. To simplify the simulations, a triangular shape current pulse is very often injected with a very fast rising time (1 pico-second), slow fall time (5 nano-second) and very small pulse width (100 femto-seconds). While designing a SEU robust architecture, the critical charge parameter is used to compare the different architectures and strategies.

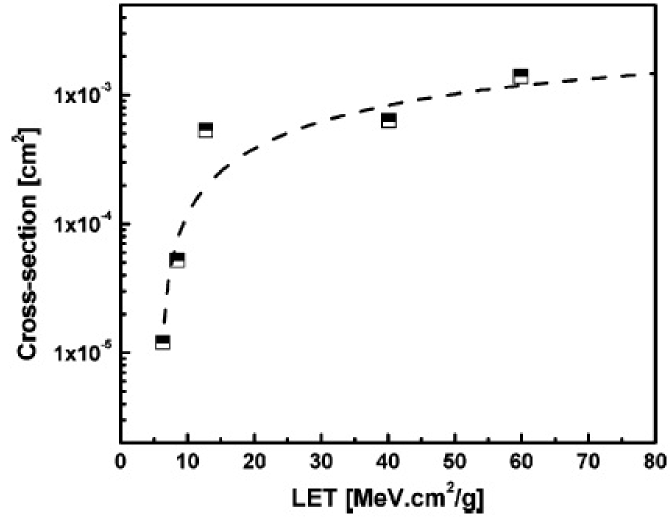


Figure 3.23. – Experimental cross-section versus LET of the LM236 bandgap voltage reference when exposed to heavy ion [91].

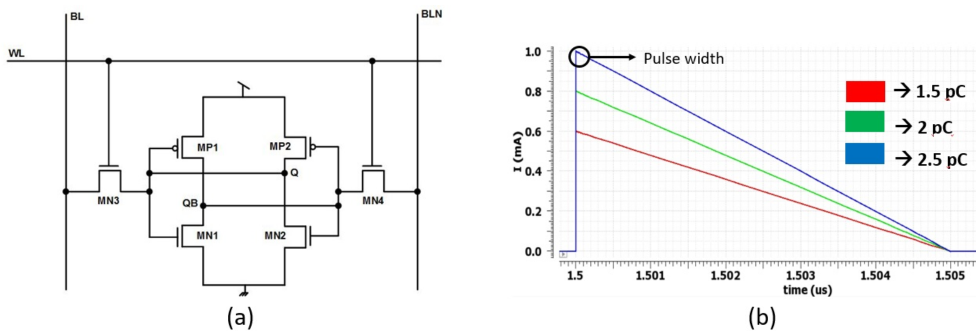


Figure 3.24. – (a) Single-event upset simulation with charge injection of a standard SRAM cell. (b) Injected current curves with corresponding collected charge.

3.5.3.4. Single-Event Transient

Single events can cause one or more glitches to occur in digital and analog circuit. This is called as single-event transients (SETs). Dealing with SETs which are caused after an interaction of a heavy ion or high-energy proton with a sensitive device of an electronic circuit has proven to be very complex. Ion induced electron–hole pairs can lead to current spikes that propagate through the integrated circuit and making it difficult to operate with a specific circuit configuration [92] [93]. SETs can be limited by doubling the logic function itself, since a variation in the value of one input does not always affect the output. This lowers the probability of a SET causing an error, but it's usually balanced by the fact that a single node often influences more than one output. In chapter 5, we will discuss some of the ways to mitigate the SET effects in the electronic circuits in more detail.

4. Simulations and test results from LFoundry 150 nm prototypes

In the past five years, a variety of prototypes in LFoundry 150 nm have been designed and fabricated within the ATLAS HV-CMOS pixel collaboration. In 2015, the first prototype called CCPD-LF (Capacitive Coupled Pixel Detector) was designed in collaboration with the University of Bonn and Karlsruhe Institute of Technology (KIT). After that, two more prototypes, namely LF-CPIX and LF-Monopix, have been produced in collaboration with the University of Bonn and IRFU [a]-CEA. One of the author's primary goal was to study and understand the LFoundry front-end. In this chapter we discuss few design features along with simulation results and measurements for both most recent prototypes.

4.1. LF-CPIX Prototype

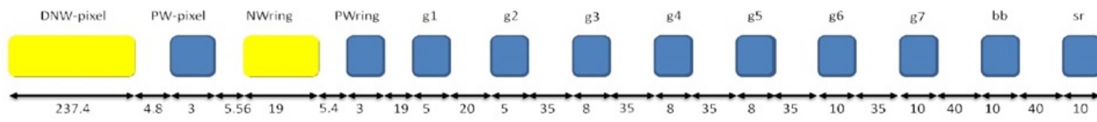
Based on the previous results from the prototype CCPD-LF (5 mm $\times$ 5 mm), a new large size demonstrator chip, namely LF-CPIX chip [94], was submitted in March 2016. The prototype was manufactured on a high resistivity wafer with 2 kΩcm. This chip was designed to have better features such as a larger matrix (10 mm $\times$ 10 mm), less threshold dispersion, higher breakdown voltage, etc. The pixel size is 250 μm $\times$ 50 μm which is compatible with the FE-I4 ATLAS pixel readout chip.

4.1.1. Chip design

There are two versions (V1 and V2) of LF-CPIX chip produced. The difference between them is the guard ring structure. LF-CPIX V1 uses a strategy with the guard-rings as sketched in figure 4.1. The number of guard rings (9) is equal to CCPD-LF one. The distance between the end of the depletion area and the cutting edge (inactive distance) is over 300 μm [95]. Whereas in LF-CPIX V2, the number of guard rings have been optimized trying to increase the breakdown voltage and decrease the dead area. The implemented guard ring strategy for LF-CPIX V2 is illustrated in figure 4.1. Compared to LF-CPIX V1, the distance between the end of the depletion area and the cutting edge (inactive distance) is also reduced to 100 μm. The figure 4.2 shows the floorplan for LF-CPIX chip. There are mainly three pixel sub-arrays: Passive pixels, AnaDig pixels and Ana pixels. There are about 1872 total pixels in the upper part of the matrix which are called "passive pixels". Each passive pixel consists of a charge collection diode and test signal

a. Institute of research into the fundamental laws of the Universe, Paris.

Version 1: Similar to CCPD_LF chip



Version 2: Reduced the number and spacing of the guard rings.

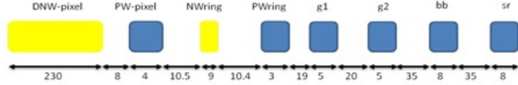


Figure 4.1. – The guard ring layout for version 1 and version 2 of LF-CPIX chip. All the distances are expressed in μm.

injection circuitry. On the left side, the second type of sub-array called "AnaDig pixels" is placed. It consists of 1908 pixels. AnaDig pixels is made up of two different types of Charge Sensitive Amplifier (CSA) namely: NMOS CSA and PMOS CSA. On the right side of LF-CPIX chip, the third type of sub-array called "Ana pixels" is placed. It consists of 1908 pixels. In Ana pixels, CMOS CSA is implemented. Moreover, two more flavours (analog saturated and analog linear pixels) are also implemented in this sub-array.

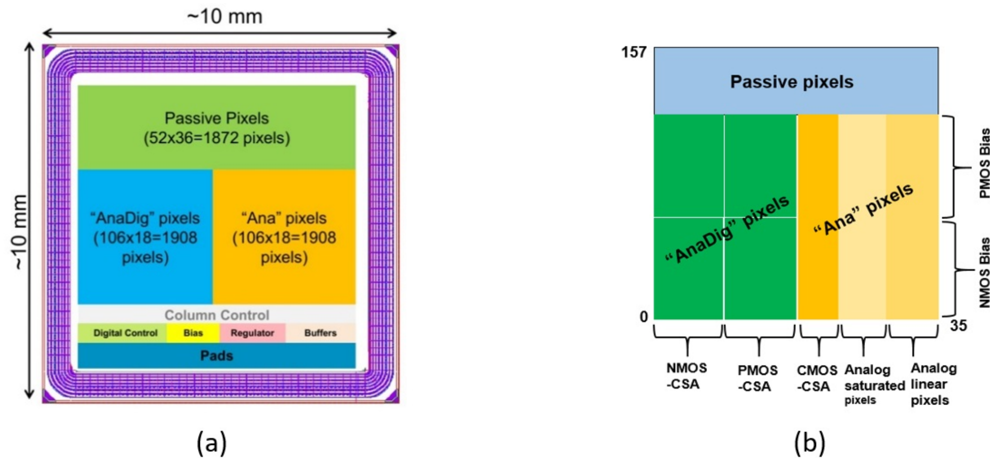


Figure 4.2. – LF-CPIX chip floorplan.

The simplified block diagram of the pixel electronics inside the LF-CPIX demonstrator is sketched in figure 4.3. The signal processing starts from the pre-amplifier and is AC coupled to the sensing diode. A PMOS transistor is used as coupling capacitor in this case. The pre-amplifier is used as an integrator which converts the charge to voltage signal. The output of the pre-amplifier drives the next stage which is a source follower. The output voltage signal of the source follower is filtered by a baseline restoration stage and then sent to a discrimi-

nator with the threshold voltage which is tuned by a 4-bit trim pixel DAC. In the "AnaDig pixels" sub-array, there are two kinds of pre-amplifier with folded cascode topology. The discriminator used in CCPD-LF is optimized to reduce the dispersion and time walk. A new kind of pre-amplifier with CMOS input is implemented inside "Ana pixels" sub-array. The analog pixels in this sub-array (analog linear and analog saturated) are simpler than digital pixels with reduced in-pixel electronics. The idea is to generate an analog saturated pulse compatible with the input of the FE-I4.

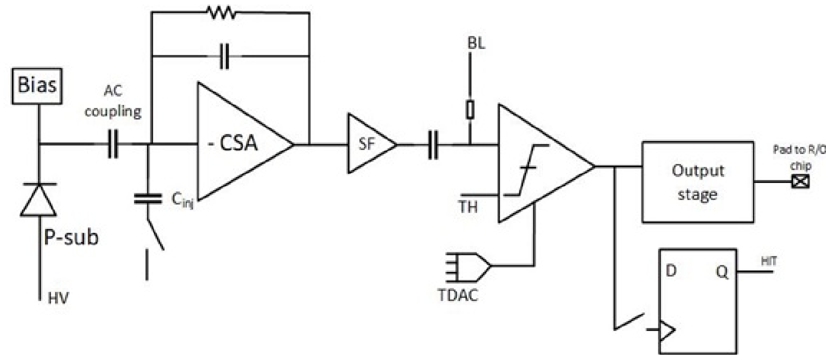


Figure 4.3. – Simplified block diagram of the pixel electronics inside the LF-CPIX demonstrator.

The comparator consists of three main blocks: a discriminator, signal stretching circuit and output stage. The discriminator is composed of a differential transistors pair which compares the pre-amplifier signal to the threshold. The signal stretching circuit allows enlarging the output signal. With the output stage, the amplitude of the output signal can be tuned.
The Deep N-Well (as shown in figure 2.7) acts as a charge collecting electrode. The bias scheme for charge collection diodes have been implemented in two different ways. The schemes are PMOS-based current source bias and a diode-connected NMOS transistor bias as illustrated in figure 4.4. The upper half and lower half of the pixel matrix uses PMOS and NMOS transistor biasing scheme respectively. The idea is to compare these two schemes and implement the best in the next iteration.
A global shift register is used to configure (and read out in stand-alone mode) all pixels. Along with the pixel sub-arrays, voltage and current DACs, two buffers for monitoring purposes are also implemented. An on-chip regulator has been designed to generate the adjustable supply voltage for the CMOS input pre-amplifier. The total size of this regulator is 155 μm $\times$ 50 μm. All these blocks are placed at the bottom of the chip and 85% of the area is occupied by the pixel matrix. The chip uses 46 pads, which are placed at the bottom. The core of the chip is powered with a supply of 1.8 V. The size of the LF-CPIX chip is 1 cm $\times$ 1 cm and the layout is shown in figure 4.5.

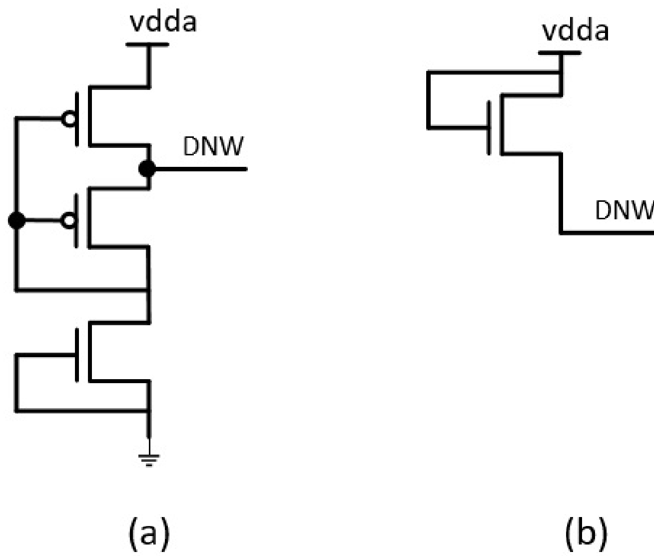


Figure 4.4. – Charge collection diode bias schemes: (a) PMOS based current source. (b) diode-connected NMOS-transistor.

Figure 4.5. – Layout of the LF-CPIX demonstrator.

4.2. Front-end analysis

The LF-CPIX demonstrator has a pixel matrix with different front-end designs. The front-end is equipped with a pre-amplifier and a discriminator. The pre-amplifier consists of a Charge Sensitive Amplifier (CSA) with a feedback network as illustrated in figure 4.6. The feedback circuit consists of a capacitor and a resistor in parallel configuration. One of the major design criteria of CSA is its capability to quickly integrate the total charge onto the feedback capacitor. The response speed is hence inversely proportional to the Gain Bandwidth product (GBW) of the CSA, therefore for high speed applications we require very large GBW. For our application, the topology used to design a CSA is a folded cascode amplifier where input bias current in the first branch is very important since it determines the transconductance g_m of the input transistor. Moreover, an increase in the input bias current also reduces the equivalent noise charge (ENC). The feedback capacitance C_f realizes the charge gain ($1/C_f$). The value of the feedback capacitor used in the design is 5 fF. Since linear resistors are usually very large, a NMOS transistor is used and acts as a feedback resistor to reset the voltage signal. In other terms, the feedback capacitance is discharged by the resistive feedback. The total size of the pre-amplifier and discriminator is 60 μm $\times$ 15 μm and 40 μm $\times$ 15 μm respectively.

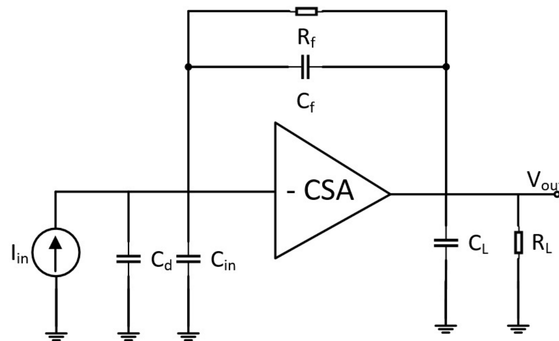


Figure 4.6. – Charge feedback configuration of CSA

Let us assume that the core amplifier has a transconductance of g_m and an output impedance equal to $R_L \parallel C_L$. Under the assumption of $C_{in} \gg C_f$, $g_m R_f \gg 1$ and $g_m R_L \gg 1$, the transfer function in the frequency domain can be expressed as [96]:

$$\frac{V_{out}(s)}{I_{in}(s)} = -\frac{g_m}{s^2 C_t [C_f + C_L] + s g_m C_f + g_m G_f} \tag{4.1}$$

where the two poles are:

$$p_1 = \frac{1}{2\pi\tau_1} = \frac{1}{2\pi R_f C_f} \tag{4.2}$$

$$p_2 = \frac{1}{2\pi\tau_2} = \frac{g_m C_f}{C_t[C_L + C_f]} \tag{4.3}$$

The first pole is determined by the product of feedback network components and the second pole is the result of the capacitive feedback. The time constant $R_f C_f$ also determines the reset time of the CSA.
The time domain response $V_{out}(t)$ can be calculated by the inverse Laplace transformation of equation 4.1. The response for a negative delta current pulse $I_{in}(s)$ can be approximated as the Dirac-impulse with an integrated area of Q. The output signal in the time domain is expressed as:

$$V_{out}(t) = \frac{Q\tau_1}{C_f[\tau_1 - \tau_2]}[e^{-t/\tau_1} - e^{-t/\tau_2}] \tag{4.4}$$

The output signal rise time, which is independent from the input charge, is calculated:

$$t_r = 2.2\tau_2 = \frac{2.2C_t}{2\pi GBW C_f} \tag{4.5}$$

From the equation 4.5, it is seen that for a fast response a large GBW is required. To achieve large GBW, there is an increase in power dissipation. The feedback resistance R_f represents the small-signal equivalent resistance of the feedback network. Since the feedback transistor is biased with a very low current of 800 pA, it operates in weak inversion. Therefore the equivalent resistance for all subarrays is 30 MΩ. Using a feedback capacitance C_f = 5fF, the time constant is given by:

$$\tau_f = R_f C_f \approx 150ns \tag{4.6}$$

Figure 4.7 shows the different CSA's designed in the front-end of the pixel. All three different input folded cascode amplifiers are designed to consume 14 μA bias current. The pre-amplifer can be made operational and non-operational by an "enable" analog switch. A separated power supply called Vddapre is designed for PMOS input pre-amplifier. Biasing of pre-amplifier is done in order to avoid the noise-pulses injection from the main power line (vdda). Furthermore, the supply voltage for CMOS input pre-amplifier is also generated with the regulator.

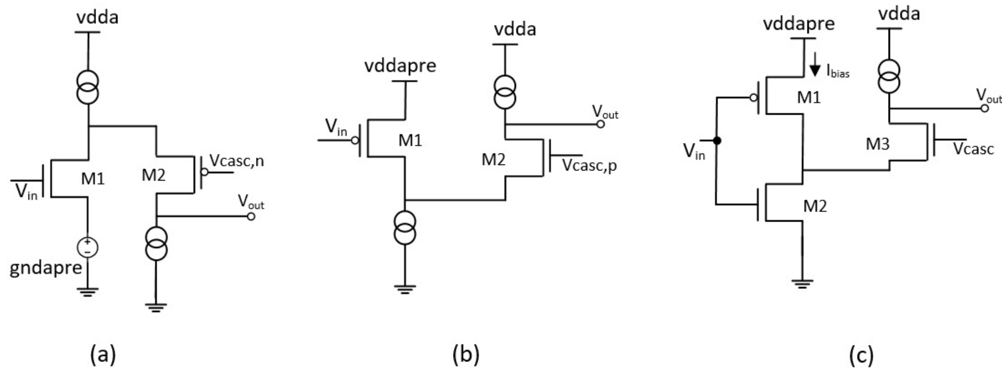


Figure 4.7. – Different pre-amplifiers implemented inside the LF-CPIX demonstrator. (a) NMOS input folded cascode. (b) PMOS input folded cascode. (c) CMOS input folded cascode.

This linear voltage regulator is used to provide the bias current in the main branch of the CMOS pre-amplifier. The idea of using a new design is based on different concept [97]. In this concept, the total transconductance for the given bias current is: $g_m(total) = g_m(PMOS) + g_m(NMOS)$. This improves the speed and noise performance for a given bias current. The detailed design is discussed in [98].

4.2.1. Simulation results

Linearity of PMOS input pre-amplifier design

Linearity simulations have been performed for three different pixel matrices: NMOS, PMOS and CMOS input pre-amplifers. Inside each pixel (of figure 4.3) there is an injection capacitor with a value of 2 fF. The value of the injected input charge is determined by applying a test voltage pulse. Table 4.1 shows different current and voltage values used for designing the three pixel matrices. The transient response of the pre-amplifier is shown in figure 4.8, obtained by varying the charge from 1ke- to 20ke-. The simulated gain value for this design is 18 μV/e-. The linearity response of the PMOS input pre-amplifier at different process corners (to simulate process variations) is shown in figure 4.9.

The gain of this design is calculated from the linearity response which is represented by a blue curve called "`Out_BL`" in figure 4.10. The blue curve shows a constant behaviour up to a charge of 20ke-. The red curve represents the slope of the maximum threshold voltage for which a hit is recorded at a particular charge. These two curves correspond to simulation results. An exponential increase can be seen after a charge of 12ke-. The blue dots represents the measurement response in the voltage gain by increasing the injected charge.

Such plot is given at different process corners in figure 4.11. From these si-

Parameters	PMOS-CSA	NMOS-CSA	CMOS-CSA
Pre-amplifier Current	14 μA	14 μA	14 μA
Pre-amplifier Load Current	250 nA	250 nA	250 nA
Source Follower	1.5 μA	1.5 μA	1 μA
Feed back Current	800 nA	800 nA	800 nA
VDDAPRE	1.5 V	-	-
VDDA	1.5 V	1.8 V	1.8 V
VCASC	1 V	520 mV	700 mV
Baseline voltage	750 mV	750 mV	750 mV

Table 4.1. – Design voltage and current values for PMOS, NMOS, CMOS CSAs.

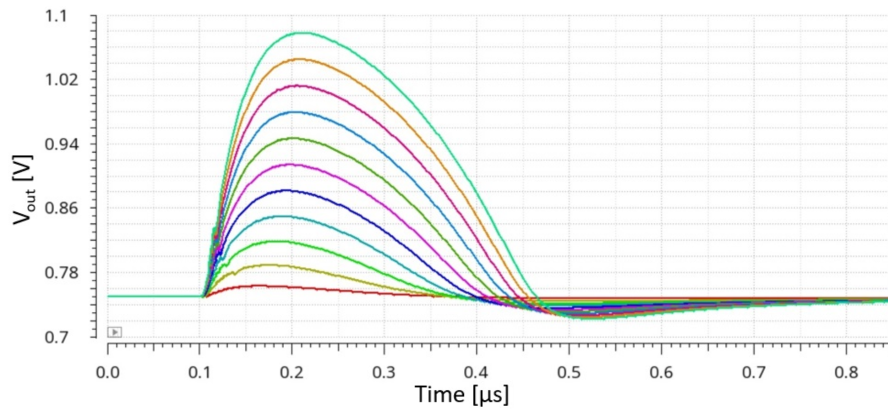


Figure 4.8. – Simulated transient response of PMOS input pre-amplifier for different number of injected electrons.

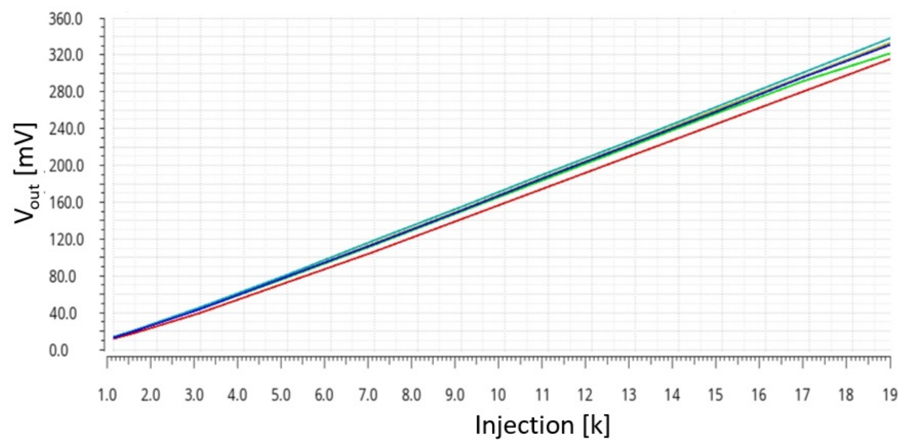


Figure 4.9. – Simulated output response of the PMOS input pre-amplifier at different process corners.

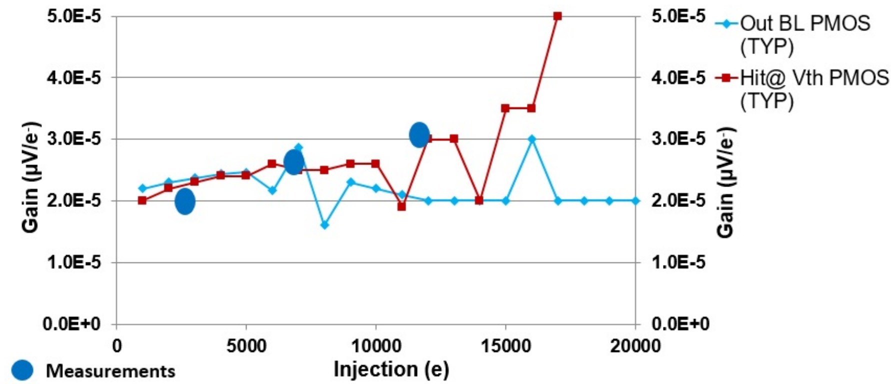


Figure 4.10. – Simulated linearity response of the PMOS input pre-amplifier at nominal process.

mulations, two points are noticed. Firstly, the red line is always above the blue line, which means that a hit is still recorded for slightly larger value of the threshold. Secondly, for Fast-Slow (FS) and Slow-Slow (SS) process corners, there is an exponential increase in the slope of the maximum threshold voltage around an injected charge of 14ke-. At both these corners, PMOS transistor effect is observed. Therefore, we could conclude that in this front-end design, there is an effect (sensitive) of the PMOS transistor in the process corners.

Linearity of NMOS input pre-amplifier design

The transient response of the pre-amplifier is shown in figure 4.12, obtained by varying the charge from 1ke- to 20ke-. Simulated output response of the NMOS input pre-amplifier is shown in figure 4.13.

The gain of NMOS pre-amplifier (blue curve) with variation in the injected charge is shown on figure 4.14. The simulated gain value for this design is 17 μV/e-. The blue curve shows a constant behaviour up to a charge of 20ke- . Here also, the red curve represents the slope of the maximum threshold voltage for which a hit is recorded at a particular charge. There is an exponential increase in the red curve after a charge of 18ke-. The linearity response of the NMOS input pre-amplifier at different process corners is shown in figure 4.15.

From these simulations, we can see that there is an exponential increase for the red curve around an injected charge of 14ke- for Fast-Slow (FS) and Slow-Slow (SS) process corners. At both these corners, there is a effect of PMOS transistor. The red dots represents the measurement response in the voltage gain. We could see that the measured gain is constant with the increase in the injected charge.

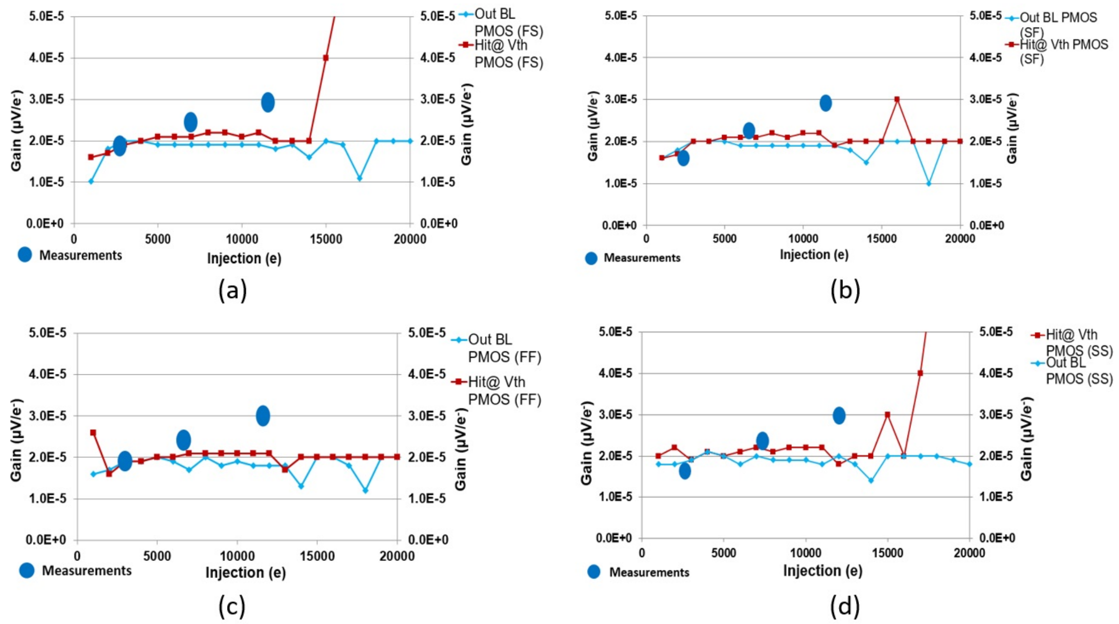


Figure 4.11. – Simulated linearity response of the PMOS input pre-amplifier at different process corners. (a) Fast-Slow, (b) Slow-Fast, (c) Fast-Fast, (d) (Slow-Slow).

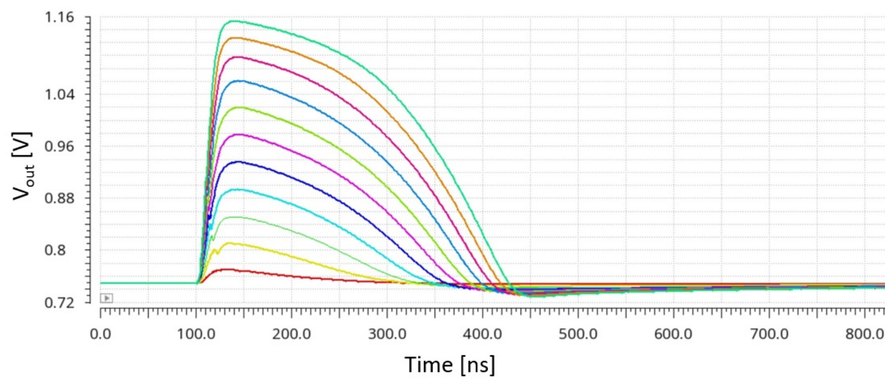


Figure 4.12. – Simulated transient response of NMOS input pre-amplifier for different injected charges (1ke- to 20ke-).

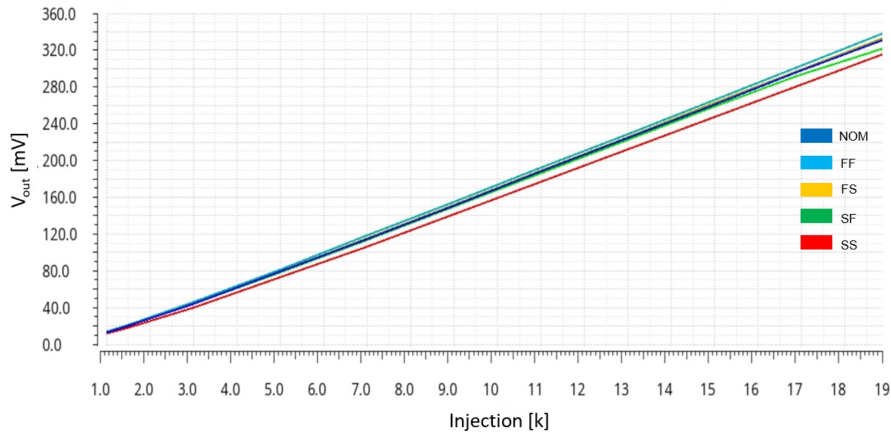


Figure 4.13. – Simulated output response of the NMOS input pre-amplifier.

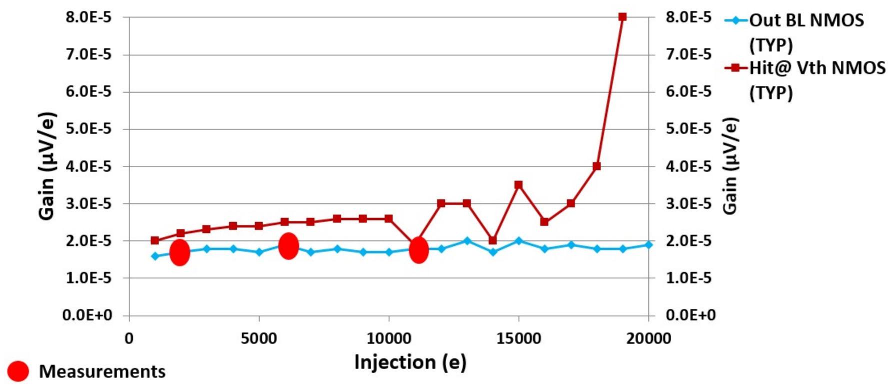


Figure 4.14. – Simulated linearity response of the NMOS input pre-amplifier at nominal process.

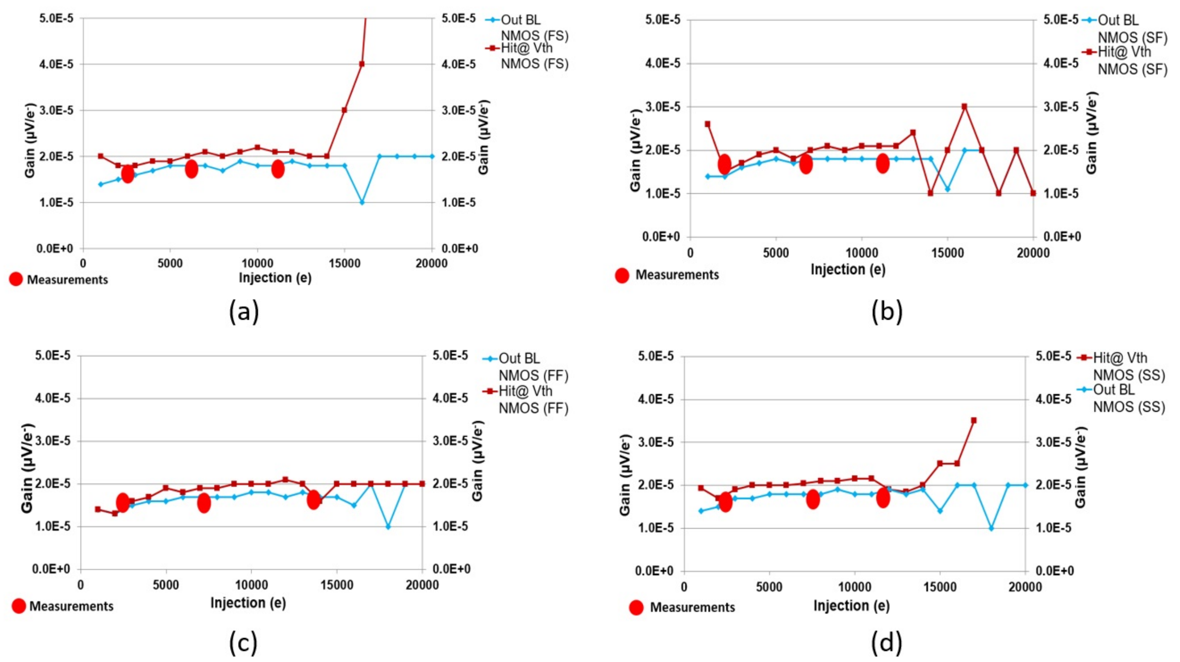


Figure 4.15. – Simulated linearity response of the NMOS input pre-amplifier at different process corners.

Linearity of CMOS input pre-amplifier design

Similarly to PMOS and NMOS, the output response of the CMOS pre-amplifier is shown in figure 4.16, obtained by varying the charge from 1ke- to 20ke-. The linearity response of the CMOS input pre-amplifier at nominal process is shown in figure 4.17.

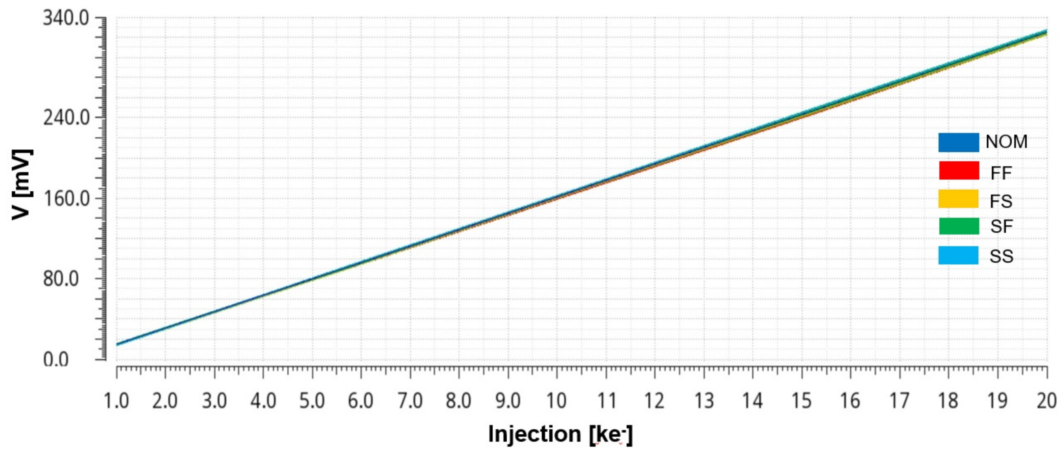


Figure 4.16. – Simulated response of CMOS input pre-amplifier for different injected charges (1ke- to 20ke-).

The gain of CMOS pre-amplifier (blue curve) as the function of the injected charge is shown in figure 4.17. From this plot, a stable behaviour can be seen from both blue and red curves up to an injected charge of 20ke-.

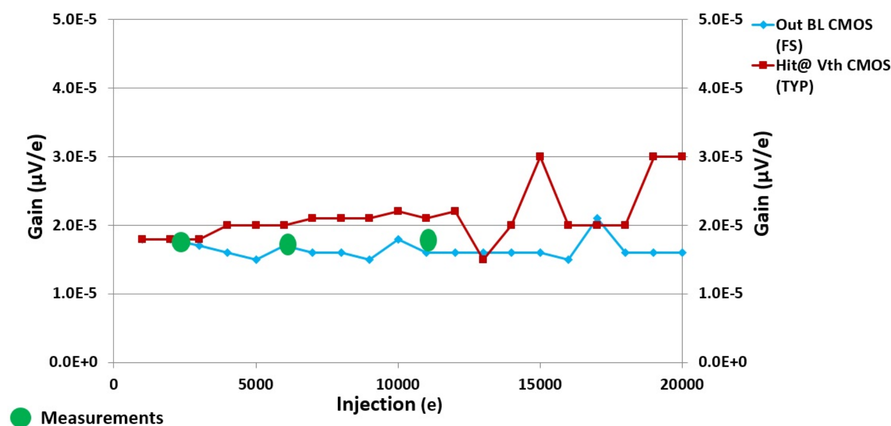


Figure 4.17. – Simulated linearity response of the NMOS input pre-amplifier at nominal process.

In this design also, there is an exponential increase in the red line after an injected charge of 14ke- for Fast-Slow (FS) and Slow-Slow (SS) process corners

(figure 4.18). The green dots represent the measurement response in the voltage gain. We could also see that the measured gain value in this design is constant up to a charge of 20ke-. This design is robust when compared to PMOS input pre-amplifier.

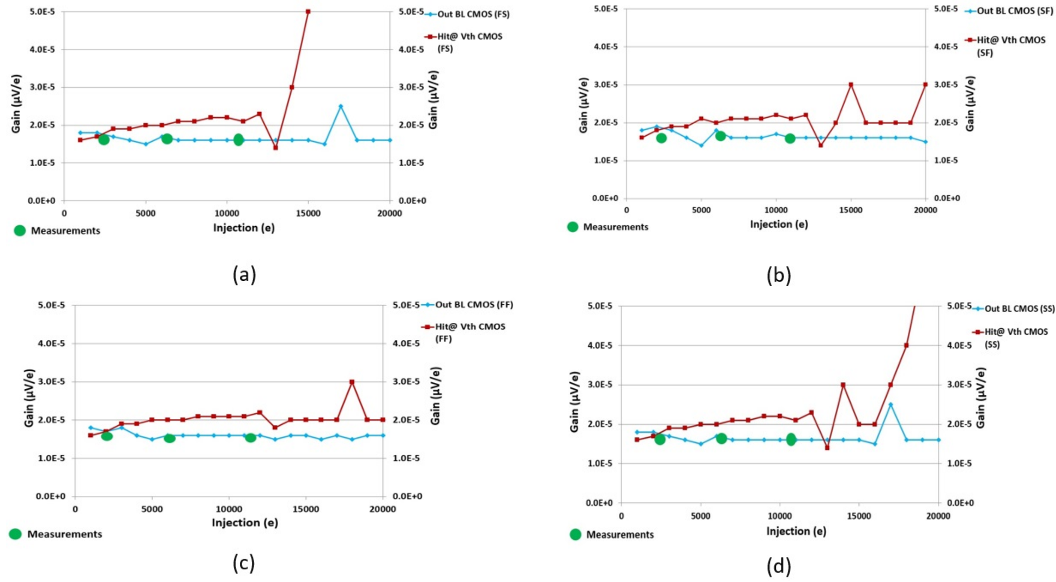


Figure 4.18. – Simulated linearity response of the CMOS input pre-amplifier at different process corners.

4.3. Digital Block Functioning

The bias block placed at the bottom of the chip is used to provide all the biasing to the circuits. It contains 13 6-bit DACs. At the output of each DAC, some current mirrors divide the current value to provide the adequate range of current for each bias. A sketch of LF-CPIX pixel architecture with supplies and biases is shown in figure 4.19. The default values for the global DACs is shown in table 4.2. The power supply for analog (vdda) and digital domains (vddd) is 1.8 V.

The digital cell matrix is used to configure and read the chip. A sketch of digital matrix is illustrated in the figure 4.20. It contains shift registers which transfer configuration bits to global DACs and pixel matrix controlled by two load signals : LdDac and LdPix. There are in total five control signals shown in table 4.3.

Data is given to the input pad "SIN". It moves through the shift register at the frequency of CKConf clock and is read out through pad "SOUT". When "SR-EN" is logic 0, the information shifts through pixels. The loading and reading of data

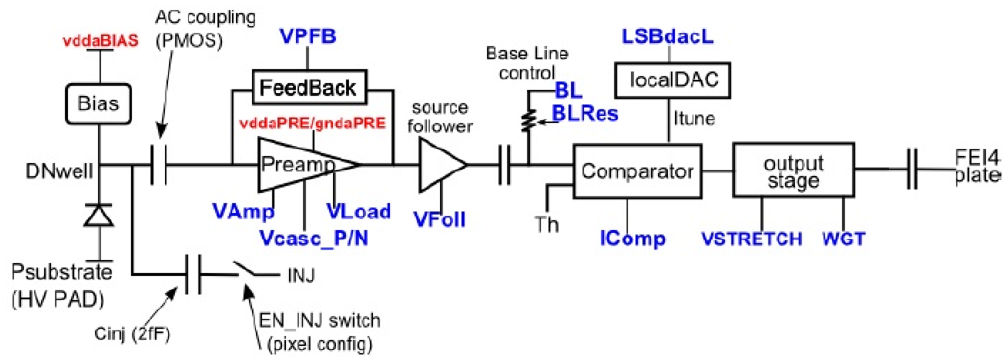


Figure 4.19. – LF-CPIX pixel architecture (supplies in red, biases in blue).

Table 4.2. – Default values for the global DACs inside the LF-CPIX chip.

DACG	Name	Function	Typical value
1	BLRes	R value of the filter	28
2	VAmp	Current of the pre-amplifier	26
3	VPFB	Feedback resistance value	47
4	VFoll	Current of source follower	12
5	VLoad	Bias of pre-amplifier load	11
6	IComp	Current to comparator	24
7	VSTRETCH	Current for width of comparator	5
8	IBOTA	Current for OTA	20
9	IBCS	Current of CS amplifier(anasaturated pixels)	23
10	WGT	Current for amplitude of the pixel output	32
11	LSBdacL	Current of LSB of the local DAC	32
12	LSBdacL2	Current of LSB of the local DAC	32
13	IBCS2	Current of CS amplifier	23

Signal name	**function**
CKConf	Shift register clock
LdDAC,	Load the global DACs latches from the Shift Register
SR_EN	Enable the "HIT" reading or the data loading on each pixel
RESET	Reset of the Global Shift register
LdPix	Load the pixel configuration from the Shift Register

Table 4.3. – Control signals in shift register

is done when CkConf is set to logic 1. Once the shift register is loaded, the two load signals LdDAC and LdPix can be used to store the data in corresponding latches. When "SR-EN" is set to logic 1, the hit signal of the pixel is sent to the matrix shift register. Finally to read this data, "SR-EN" is set to logic 0.

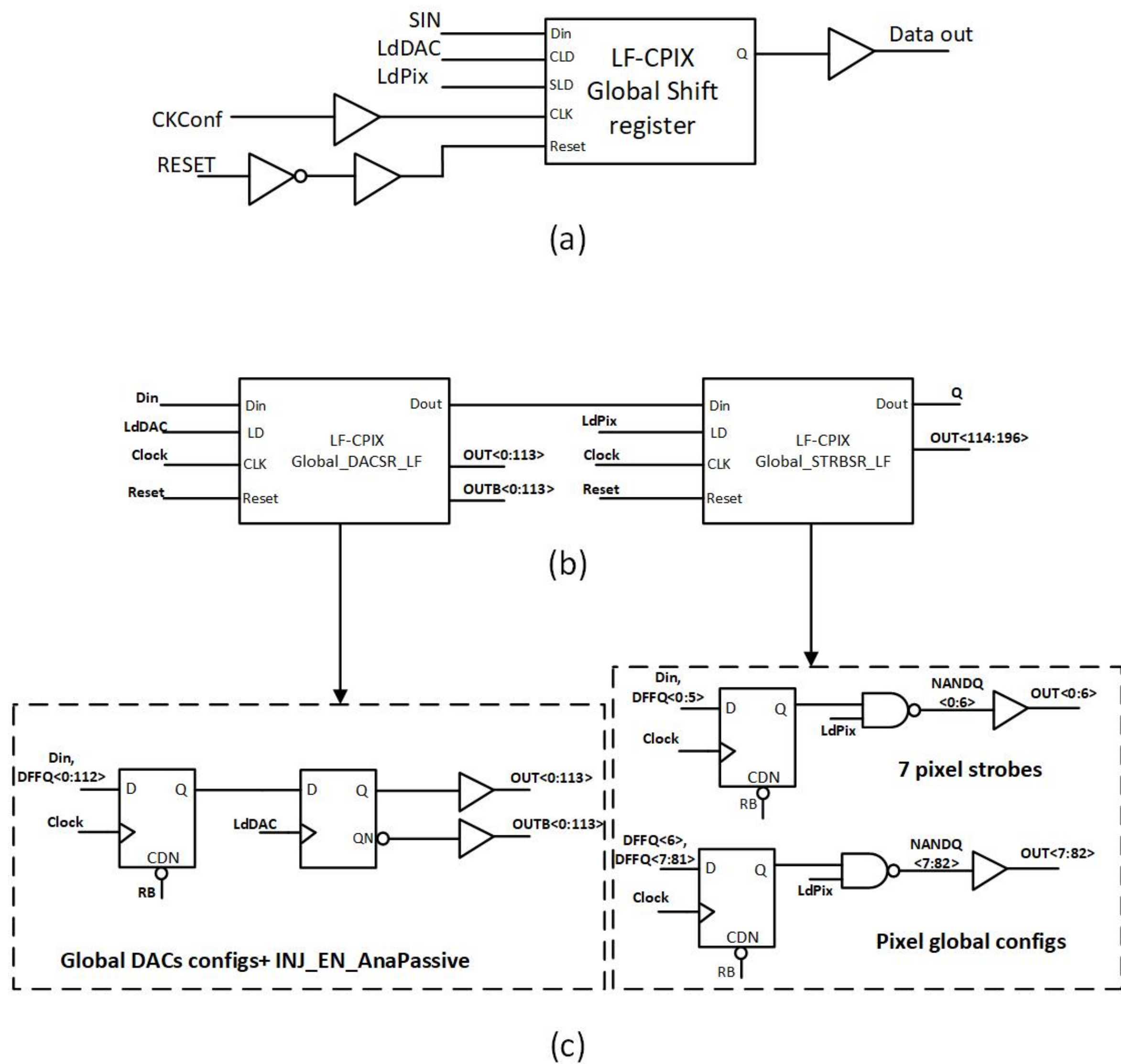


Figure 4.20. – (a) Block diagram of digital matrix. (b) Block diagram of global shift register. (c) Schematic of global shift register.

4.4. Characterization of LF-CPIX prototype

Test results of LF-CPIX (V1 and V2) prototypes are discussed here. At first the laboratory setup (4.4.1) and results (4.4.2) are presented. The next two sections (4.4.3 and 4.4.4) are dedicated to irradiation test performed on few samples.

4.4.1. Experimental setup

To characterize the LF-CPIX prototype in a standalone mode, a test setup was developed in the laboratory. A typical setup construction to test a prototype in laboratory is sketched in figure 4.21. The hardware consists of three boards : multi I/O board based on the compact USBpix system [99], GPAC board (Generic Purpose Analog Card) and DUT (Device Under Test). The multi I/O board includes a free programmable Xilinx Spartan3 FPGA, SRAM Memory, USB2.0 Interface and a 8051 microcontroller with I2C and SPI functionality. The microcontroller provides an easy to use interface to the FPGA. Especially the configuration for the FPGA can be accomplished via USB download so that no additional (JTAG or other) interface to the FPGA is required. The programming mode provided by the micro-controller is called slave parallel programming. More information on this FPGA configuration can be found in [99].

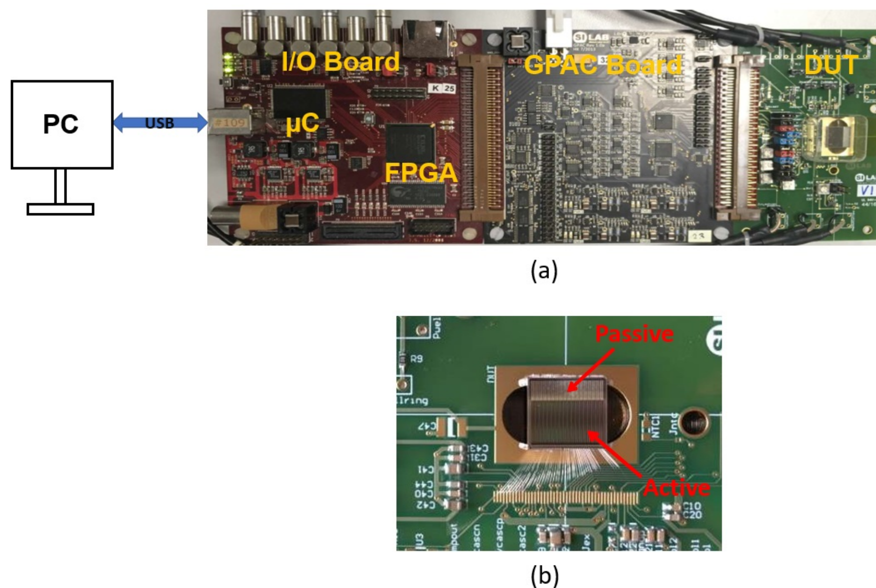


Figure 4.21. – (a) LF-CPIX test setup system composed of PCB board, the GPAC board with voltage regulators, DACs and signal level adaption, multi I/O board with FPGA, microprocessor with USB interface. (b) LF-CPIX demonstrator on a PCB board.

The GPAC extends the digital IO capabilities of the I/O card by analog blocks

(power supplies, voltage and current sources, fast ADC, etc.), programmable level LV-CMOS, and LVDS digital IOs. The LF-CPIX prototype is powered and configured with the GPAC card (external power supplies are not used). A robust plug system is used to establish a connection between the adapter board and the multi I/O board with USB interface for communication with a PC. The complete test setup is controlled by a python software package which implements an application programming interface (API). The API covers low-level and high-level functions. Low level functions are typically chip readout and configuration. High level functions are like the execution of parametrized threshold scans and data fitting algorithms.

4.4.2. Laboratory measurements

LF-CPIX V1 and V2 samples were received in the Q4 of 2016. The boards were extensively tested in laboratory to verify the functionality, and to evaluate the performances. First of all, two boards from both the versions were selected to perform I-V measurements. The results for LF-CPIX V1 and V2, at room temperature, are shown in figure 4.22. The leakage current for all the boards is around 10-15 nA before the breakdown voltage. The breakdown voltages of LF-CPIX V1 and V2 are around -130 V and -220 V respectively. From these measurements, we could conclude that the implemented guard ring strategy for LF-CPIX V2 was successful. From the previous studies, moreover the depletion depth of LF-CPIX V2 was estimated more than 70 μm at 150 V of high voltage by edge-TCT, a technique that consists of shining very fast infra-red laser pulses on the edge of a sensor [100].

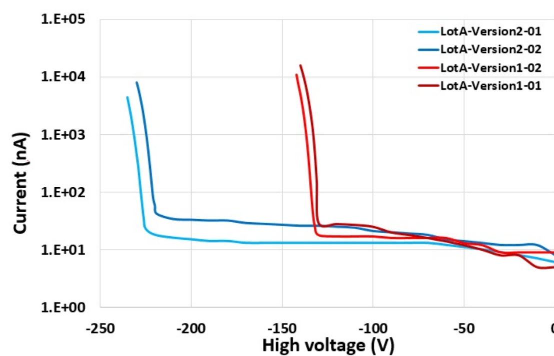


Figure 4.22. – I-V curve of LF-CPIX V1 and V2 chips.

An example of the real time monitoring of the clock, SIN and SOUT signals for LF-CPIX V1 and V2 is shown in figure 4.23.

Chip performance was first evaluated by using an external injection circuit. The designed value of the injection capacitor is 2 fF and by applying some voltage, the total injected charge is calculated. The plot in figure 4.24 shows the

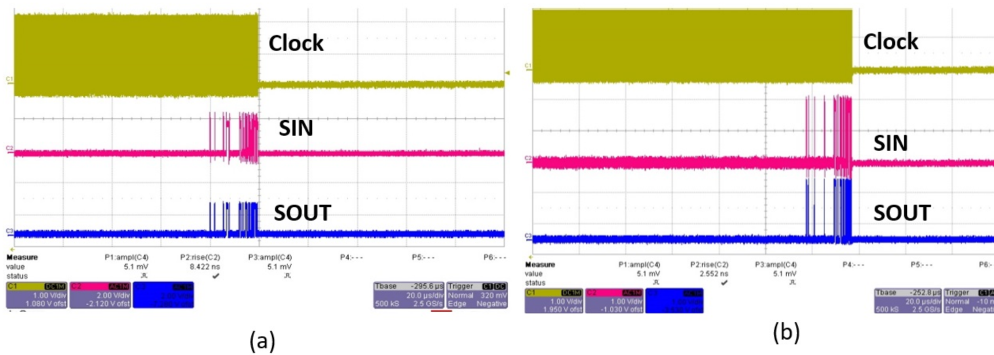


Figure 4.23. – Clock, SIN and SOUT signals monitored by oscilloscope for (a) LF-CPIX V1 (b) LF-CPIX V2.

response of the pre-amplifiers and discriminators for 1 V. The pixel performance was calculated by performing the threshold and injection scans. They consist in fixing one parameter (threshold or injection amplitude) and varying the other one from low to high value.

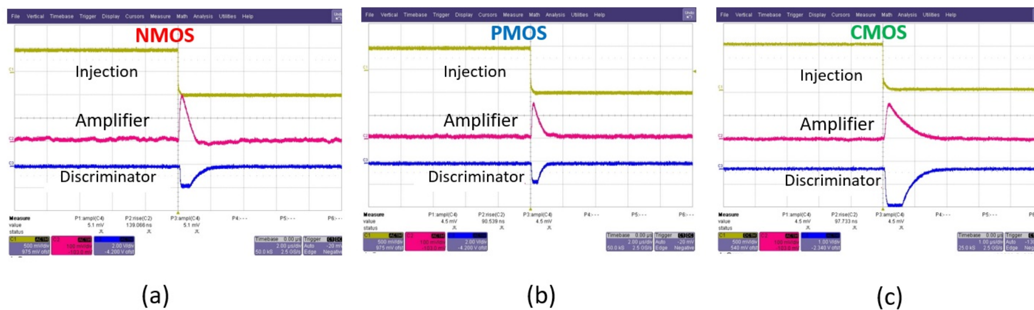


Figure 4.24. – Measured pre-amplifier and discriminator responses for 1 V of external injection. (a) NMOS input pre-amplifier (b) PMOS input pre-amplifier (c) CMOS input pre-amplifier

For the threshold scans, the baseline (BL) was always set at 0.75 V while the injective value was varied from 1 V to 0.75 V typically. The step size during this process was kept as 0.01 V. Typical result is the so-called S-curve (figure 4.25) which is obtained by firing occurance of the pixel, for which a fit can be applied. From this fit the amplitude of the pixel can be extracted. It corresponds to the 50% point of the S-curve. The gain values for the three pixel matrices was calculated by taking the ratio of the resulting voltage amplitude and injected charge. The gain mapping of three pixel matrices in LF-CPIX V1 and V2 is shown in figure 4.26 and figure 4.27 respectively. From these gain values, the PMOS matrix shows slightly higher gain when compared to other two matrices. While performing the gain measurements, we observed an increase in the gain value by

increasing the injection for PMOS matrix. Figure 4.28 shows the gain distribution for two injection voltages. There is an increase in the gain value by increasing the injection. This phenomena was already observed from the simulations described in section 4.2.1.

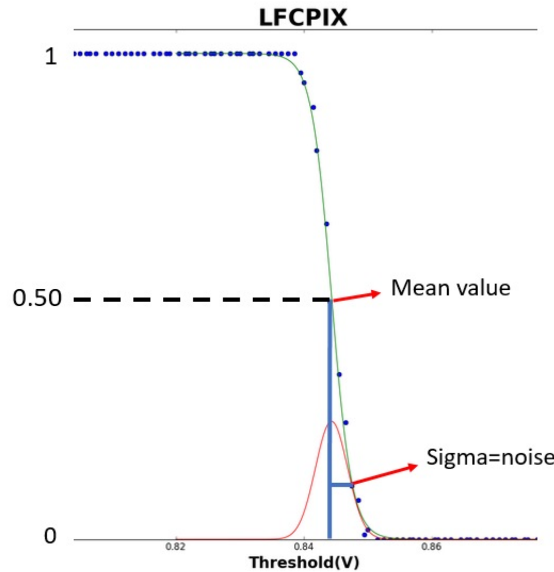


Figure 4.25. – S-curve for a single pixel with mean and sigma value.

After performing the threshold scan for both versions of LF-CPIX, the performance of the pixel was then evaluated using an injection scan. In this scan, the threshold (TH) is fixed at a default value (0.75 V) and injection value is varied from low to high. The injection value was varied from 0 V to 0.60 V with a set size of 0.01 V. The maximum injection value of 0.60 V corresponds to 7500 electrons. Initially, the scan was performed with TDAC = 7. Noise comparison for three pixel matrices is listed in table 4.4. The measured noise value for three pixel matrices were slightly lower than the simulated value. NMOS pixel matrix showed higher noise value when compared to other pixel matrices. Whereas, the PMOS pixel matrix showed the lowest noise. This behaviour is similar for both versions. The noise mapping and values from three pixel matrices are shown in figure 4.29. Figure 4.30 shows the Gaussian distribution which is obtained after performing the threshold scan and TDAC tuning for all three pixel matrices. The effective mean threshold value for the three pixel matrices is around 2500 electrons with a dispersion of 55 electrons. The value of the dispersion is quite encouraging since one of the main problems found regarding in-pixel electronics was a significant threshold dispersion of the discriminator in CCPD-LF [101]. Figure 4.31 shows the threshold map for three pixel matrices.

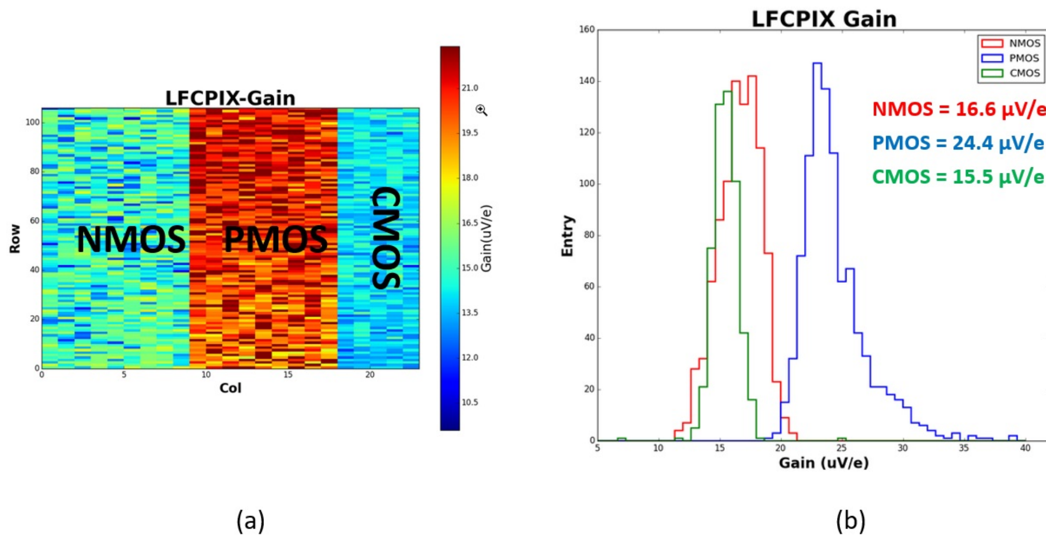


Figure 4.26. – Gain for LF-CPIX V1:(a) Gain mapping for all three pixel matrices. (b) Gain values from Gaussian distribution.

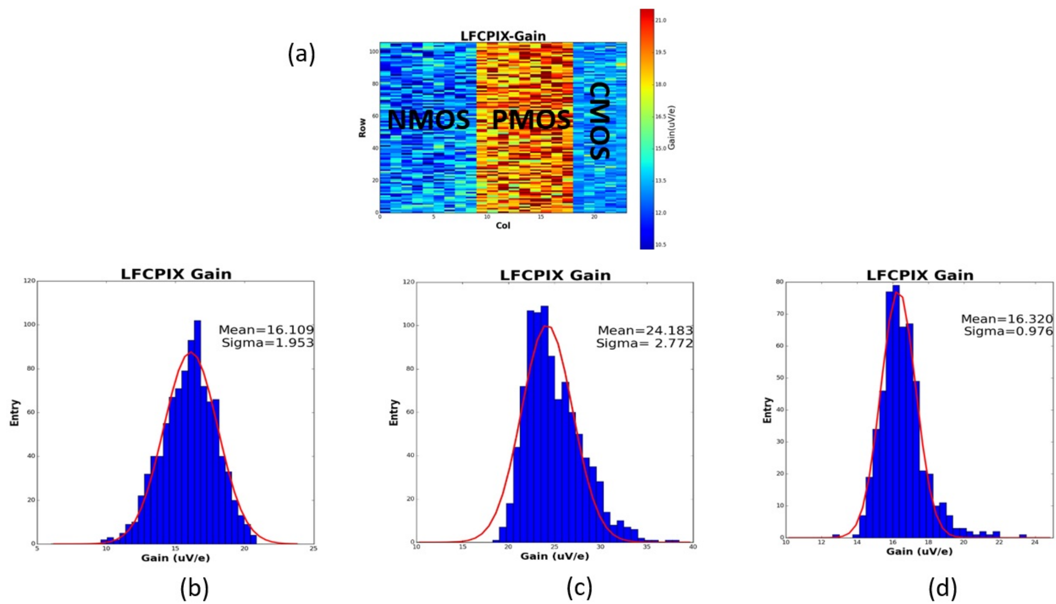


Figure 4.27. – Gain for LF-CPIX V2:(a) Gain mapping for all three pixel matrices. (b) (c) (d) Gain values of NMOS, PMOS and CMOS pixel matrices respectively from Gaussian distribution.

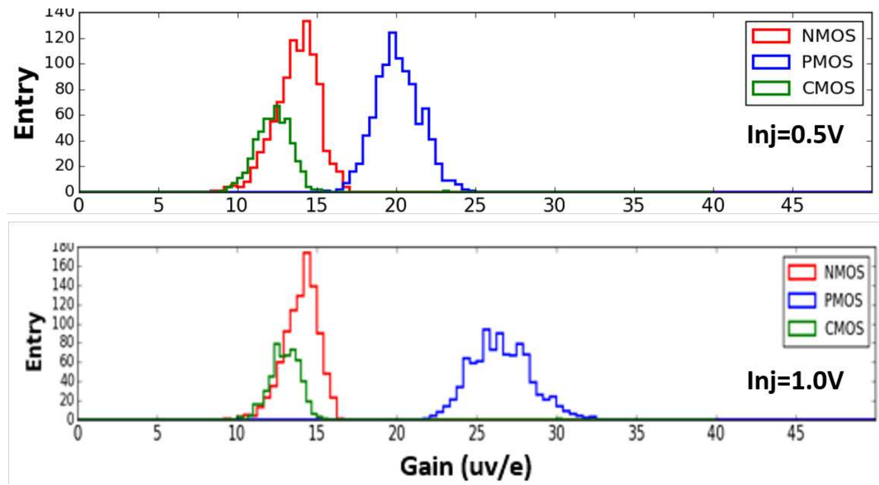


Figure 4.28. – Gain distribution for all three pixel matrices at different injection values. 0.5 V and 1.0 V grossly corresponds to the charges expected for 1 and 2 MIPs.

Pre-amplifier Noise	Simulated	Measured
PMOS	130e	102e
NMOS	149e	144e
CMOS	125e	104e

Table 4.4. – Noise comparison for PMOS, NMOS, CMOS CSAs.

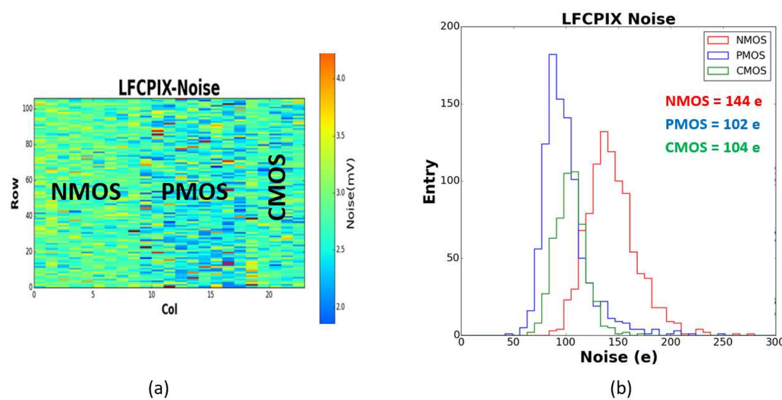


Figure 4.29. – (a) Noise mapping for all three pixel matrices of LF-CPIX V1. (b) Noise values from Gaussian distribution.

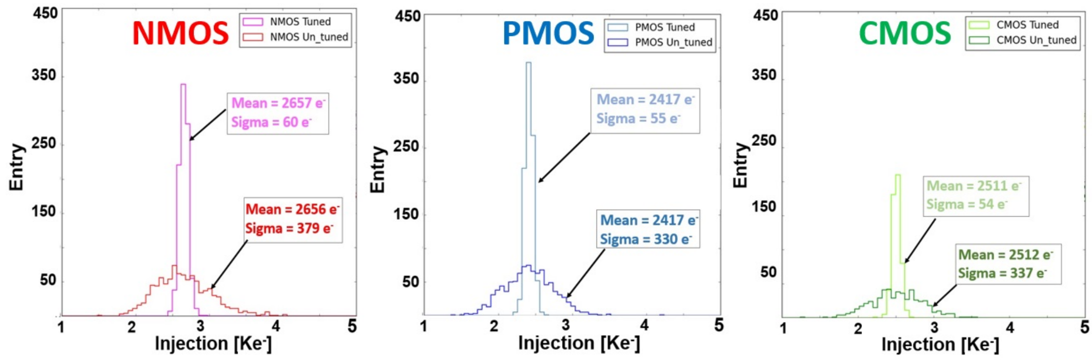


Figure 4.30. – Gaussian distribution of threshold scan before and after tuning for LF-CPIX V1. (a)NMOS pixel matrix. (b) PMOS pixel matrix. (c) CMOS pixel matrix.

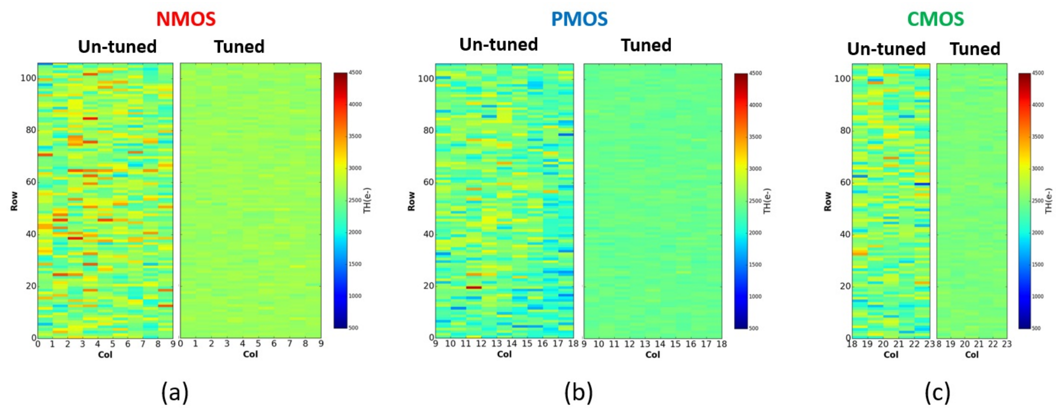


Figure 4.31. – Mapping of threshold scan before and after tuning for LF-CPIX V1. (a) NMOS pixel matrix. (b) PMOS pixel matrix. (c) CMOS pixel matrix.

4.4.3. Irradiation Test setup

After performing laboratory tests, few samples were selected for a beam test under protons at CERN: one LF-CPIX V1 with 750 μm sensor, two LF-CPIX V2 each with 250 μm and 750 μm. Two different thickness were selected in order to compare the performances among them. The planning and beam test setup phase started in May 2017.
The objective of this irradiation campaign was to reach the Total Ionising Dose (TID) of 150 MRad (since the requirement for layer 4 is 80 MRad) and measure the leakage current of the sensor versus dose, understand the behaviour of the analog part, compare the behaviour of different front-end designs, measure the power consumption of the chip versus dose, etc. This should be underlined that this was the first time that the LFoundry demonstrator chip was operated in "HL-LHC" like conditions.

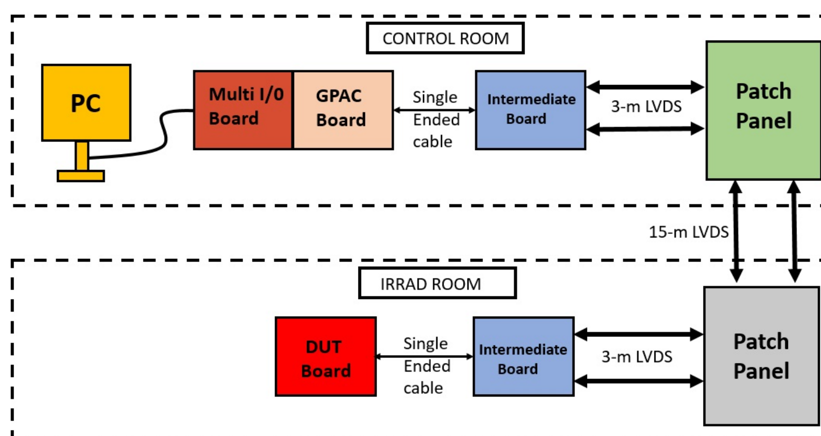


Figure 4.32. – A sketch of LF-CPIX test setup at CERN Proton Synchrotron (PS).

A sketch of the test setup is shown in figure 4.32. The samples were installed in zone 2 of IRRAD room inside the EAST hall building 157 at CERN [102]. This facility provides protons with a constant energy of 24 GeV. The setup was installed in two zones: the control room and IRRAD room. The set-up installed in the control room zone consisted of a laptop PC, a multi I/O board connected directly with GPAC board, a single ended cable connecting the intermediate board (converts single ended signals to LVDS signals), a 3-m LVDS cable connected to the control room patch panel. The set-up installed in the IRRAD zone consisted of the IRRAD room patch panel, an intermediate board which converts all the LVDS signals to single ended signals and a Device Under test (DUT). The distance between the control zone and IRRAD zone is 15 meters. The measurements were performed at room temperature (20°C). The duration of this irradiation campaign was about 19 days and the irradiation was paused 38 times so that measurements could be taken.

4.4.4. Irradiation test results

Analog front-end performance depends on the transistor characteristics, such as gate threshold voltage or other bias voltages. These characteristics will modify the performance of the transistor because of oxide charges build up near the interface between the silicon and silicon-oxide surface as discussed in chapter 3. Threshold scan was performed for 2 samples with different sensor thickness : LF-CPIX V2-01 (750 μm) and LF-CPIX V2-02 (250 μm). The mean threshold value for the pixel matrices was extracted from the threshold scan. Plots in figure 4.33 show the mean threshold value versus the dose for both chips. In LF-CPIX V2-01 board [b], the mean threshold value for NMOS flavor is stable with respect to dose, while for PMOS flavor, in the very beginning it decreases and later on becomes more stable. On the other hand for LF-CPIX V2-02 board, the mean threshold value for all three flavors show very stable behaviour up to 62 MRad. After 62 MRad, the chip was unresponsive because some shift registers were not getting configured properly and also the amplitude of the SOUT signal was decreased.

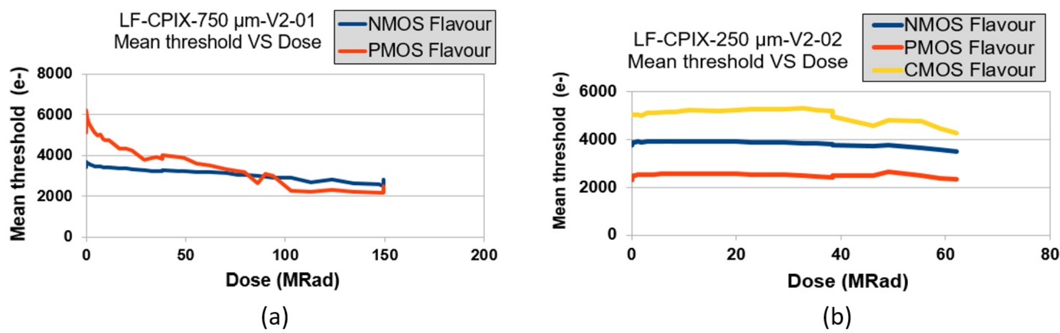


Figure 4.33. – Mean Threshold as a function of dose. (a) LF-CPIX V2-01 (with 750 μm sensor thickness) (b) LF-CPIX V2-02 (with 250 μm sensor thickness).

The dispersion of the threshold is also a very important component which is extracted after performing the threshold scan. As the TDAC tuning takes over 4 hours for the whole chip, it was not possible to pause and put the table out of the beam for such a long time. Hence, the TDAC tuning was performed in the beginning at 0 MRad and then the same values were used to perform threshold scan. For both samples, the dispersion was increasing as a function of the dose value and is shown in figure 4.34. The NMOS flavor showed very stable behaviour when compared to the other flavors. After 4 days of irradiation and reaching 38 MRad, it was decided to perform a new threshold scan plus TDAC tuning for further measurements. The TDAC tuning was performed with a global threshold value of 0.81 V instead of 0.79 V since it was not possible to get correct S-curves. The dispersion value decreased for all the flavors in both chips because

b. No response from the CMOS flavour due to some technical issue.

new TDAC values were loaded. After reaching a dose of 86 MRad for LF-CPIX V2-01 chip, some shift registers were not getting configured properly and also the amplitude of the SOUT signal decreased. Thereafter, the table was put out of the beam for nearly four hours, as a result the chip was functioning properly with correct S-curves and SOUT signal. After reaching a total dose of 150 MRad, the chip was retuned with all the global parameters and was functional. At 150 MRad, the mean threshold value for NMOS and PMOS flavours decreased by 26% and 22% respectively when compared to the initial values.

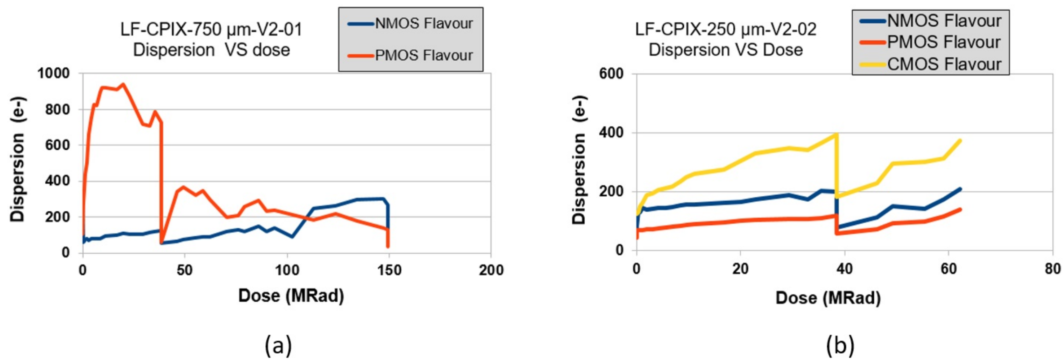


Figure 4.34. – Dispersion as a function of dose. (a) LF-CPIX V2-01 (with 750 μm sensor thickness) (b) LF-CPIX V2-02 (with 250 μm sensor thickness).

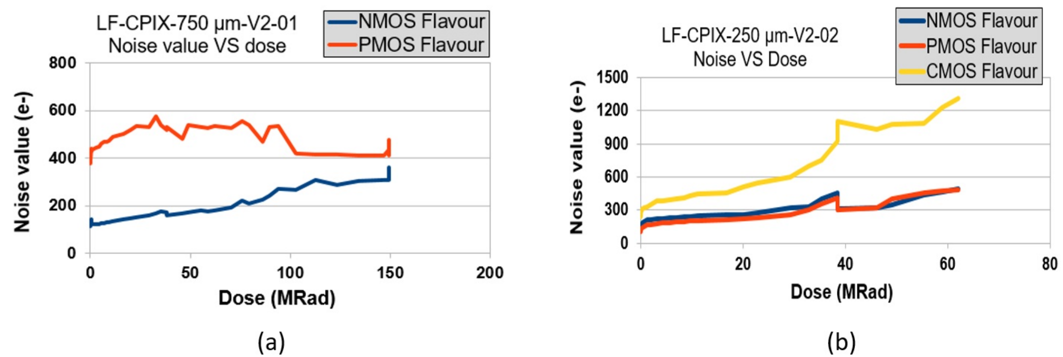


Figure 4.35. – Noise as a function of dose. (a) LF-CPIX V2-01 (with 750 μm sensor thickness) (b) LF-CPIX V2-02 (with 250 μm sensor thickness).

Figure 4.35 shows the noise variation versus dose for both samples. Noise for all the flavours was increasing with the dose because of increase in the leakage current. These noise values are still acceptable for NMOS and PMOS matrices. However, the noise for CMOS matrix was increasing at a higher rate when compared to the other matrices. At 150 MRad, the noise value for NMOS and PMOS matrices increased by 60% and 10% respectively when compared with the initial values. The noise measurements were performed again at low temperature

(-15°C), the values were decreased by more than 55% and were similar when compared to the values before irradiation.
Figure 4.36 shows the current consumption for analog and digital domains versus dose for both samples. For LF-CPIX V2-02 chip, an unusual behaviour in the current consumption was observed after 62 MRad because some shift registers were not configured properly and the amplitude of the SOUT was not correct.
Figure 4.37 shows the leakage current versus the applied voltage after 150 MRad. The red curve illustrates the leakage current at 20°C, whereas the green curve shows it around -15°C. The leakage current for both samples at low temperature is around 30 μA which is acceptable for our application.

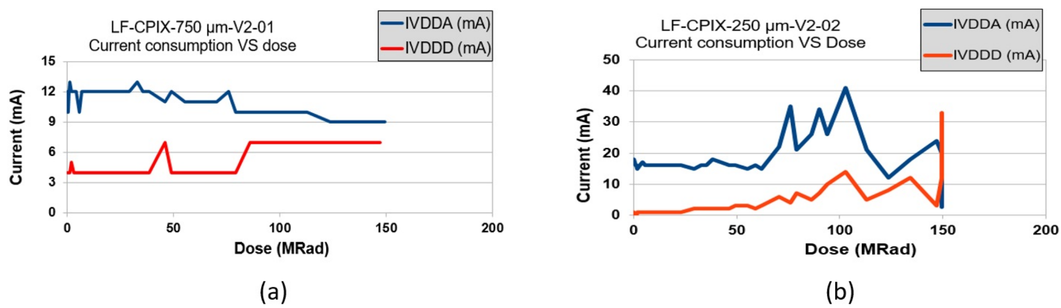


Figure 4.36. – Current consumption as a function of dose. (a) LF-CPIX V2-01 (with 750 μm sensor thickness) (b) LF-CPIX V2-02 (with 250 μm sensor thickness).

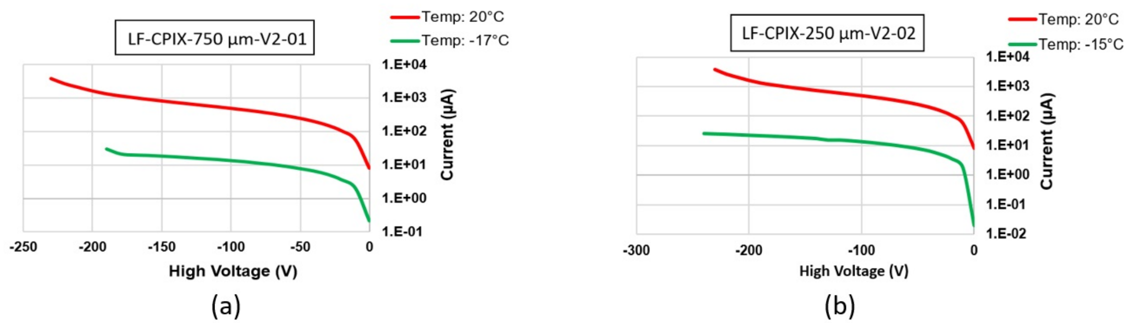


Figure 4.37. – Leakage current for two LF-CPIX samples irradiated up to 150 MRad at different temperature.

LF-CPIX demonstrator has shown very promising results after irradiating it up to a total ionising dose of 150 MRad. All three pixel matrices (NMOS, PMOS and CMOS CSAs) were functional. In terms of analog performances, threshold tunability and limited noise increase was seen after 150 MRad. Detailed characterization of LF-CPIX chip is described in [103].

4.5. LF-Monopix Chip

The first prototype LF-Monopix [46] has been developed based on monolithic pixel detector concepts as briefly introduced in section 2.2.2. It is also the first monolithic prototype implemented in the LFoundry aimed for dedicated pixelated layer of the ATLAS experiment. This design has significant inputs from its predecessor LF-CPIX chip discussed in section 4.1. The floor-plan for LF-Monopix chip is sketched in figure 4.38(a). The LF-Monopix demonstrator has a pixel matrix with 129 columns and 36 rows. There are nine different pixel sub-arrays. Seven sub-arrays are made up of analog front-end and in pixel read out logic. They have different discriminator and CSA implementations. Whereas in order to reduce the cross talk, the remaining two pixel sub-arrays are made up of analog front-end with readout logic inside the periphery. Special techniques such as current steering logic and column bus readout through a current-limiting source follower have been used. The layout view for LF-Monopix chip is illustrated in figure 4.38(b).

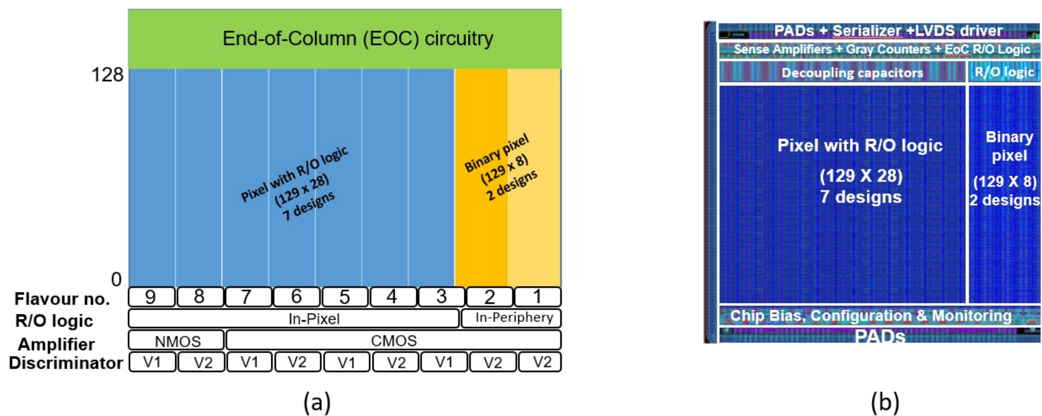


Figure 4.38. – (a) A sketch LF-Monopix chip with different flavors. (b) Layout view of LF-Monopix chip.

The readout logic is implemented inside the pixel for seven sub-arrays. A sketch of front-end design with readout logic is shown in figure 4.39. When the analog signal crosses its threshold voltage, a discriminator will fire and output holds until the analog pulse falls below the threshold. This leads to a digital signal at the output of the discriminator and the analog information can be obtained by measuring the width of digital signal (Time over Threshold). Two gray encoded time stamps, corresponding to the Leading Edge (LE) and Trailing Edge (TE) of the information, are stored in local in-pixel RAM memories. The pixel readout is arbitrated by a token propagation and the highest readout priority is given to the topmost pixel. A gray counter running at 40 MHz time stamp is distributed over the pixel matrix. The data is received at the end of each column

from the RAM sense amplifiers and sent to the DAQ system using a 160 Mbps serial link. The hit data is sent out immediately through the serial link off chip.

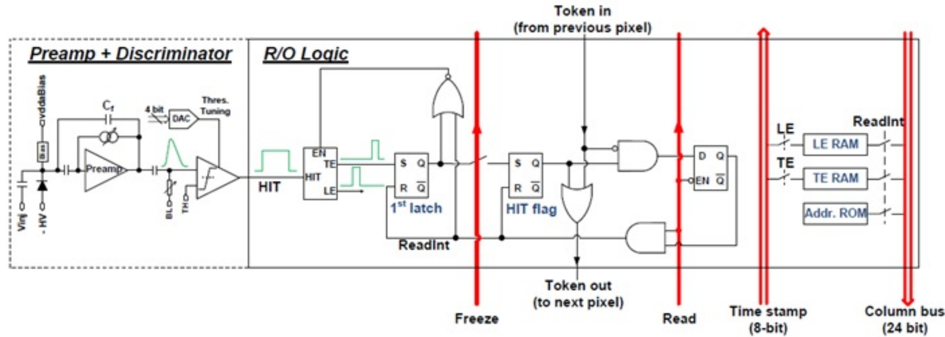


Figure 4.39. – A sketch of front-end design with readout logic for LF-Monopix chip.

4.6. Front-end Scheme

In LF-Monopix chip, there are various front-end designs. Two types of pre-amplifier designs are used namely: NMOS and CMOS CSA. The NMOS CSA has been designed and modified from LF-CPIX chip. Its schematic is shown in figure 4.40. The bias current in the first branch was increased from 14 μA to 17 μA which resulted in an increase in the transconductance and the gain. Concerning the CMOS CSA, no modifications were carried out from the previous version which was used in LF-CPIX chip. The bias current of 15 μA is used in this case.

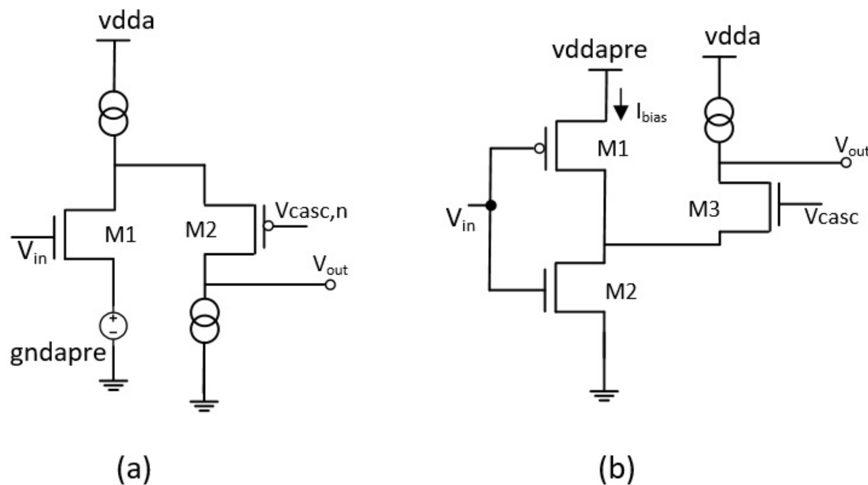


Figure 4.40. – A sketch of two front-end designs: (a) NMOS CSA. (b) CMOS CSA.

In this chip, two versions of discriminator have been implemented. The first version is the same discriminator design as in LF-CPIX chip (figure 4.41(a)). The second version (figure 4.41(b)) consists of a self-biased differential amplifier with bias current less than 4 μA and a CMOS inverter. The design is faster than V1 discriminator. The new discriminator V2 is sketched in figure 4.41(b).

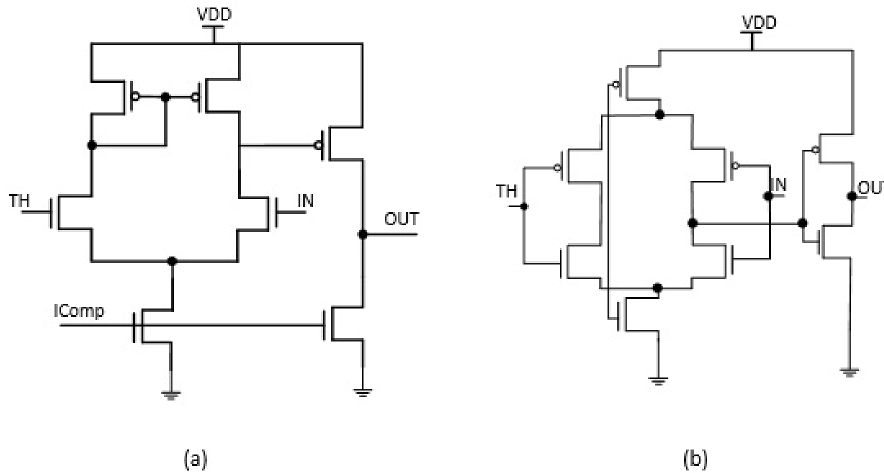


Figure 4.41. – A sketch of two versions of discriminator designs: (a) V1 Discriminator. (b) V2 discriminator with self bias scheme.

4.6.1. Simulation results

Linearity simulations have been performed for four different front-ends : NMOS CSA with discriminator V1 and V2, and CMOS CSA with discriminator V1 and V2.
Table 4.5 shows different current and voltage values used for designing NMOS and CMOS pixel matrices respectively. The linearity response of four different front-ends at different process corners is shown in figure 4.42. The injected charge was varied from 1ke- to 20ke- charge.

The gain of design is calculated from the linearity response which is represented by a blue curve called "Out_BL" in figure 4.43. The red curve represents the slope of the maximum threshold voltage for which a hit is recorded at a particular charge. There is an exponential increase in the red curve after 15ke- for NMOS and CMOS CSA with V2 discriminator (figure 4.43(b and d)). Concerning NMOS and CMOS CSA with V1 discriminator, it shows very stable behaviour up to an injected charge of 20ke-.

For NMOS and CMOS CSA with V1 discriminator, the simulated responses of "Out_BL" and slope of the maximum threshold voltage by varying the injected charge up to 20ke- at different process corners are shown in figures 4.44

Parameters	NMOS-CSA	CMOS-CSA
Pre-amplifier Current	17 μA	14 μA
Pre-amplifier Load Current	250 nA	250 nA
Source Follower	1.5 μA	1 μA
Feed back Current	400 nA	400 nA
VDDAPRE	-	1 V
VDDA	1.8 V	1.8 V
VCASC	520 mV	700 mV
Baseline voltage	750 mV	750 mV

Table 4.5. – Current and voltage values for NMOS and CMOS CSA with V1 and V2 discriminator.

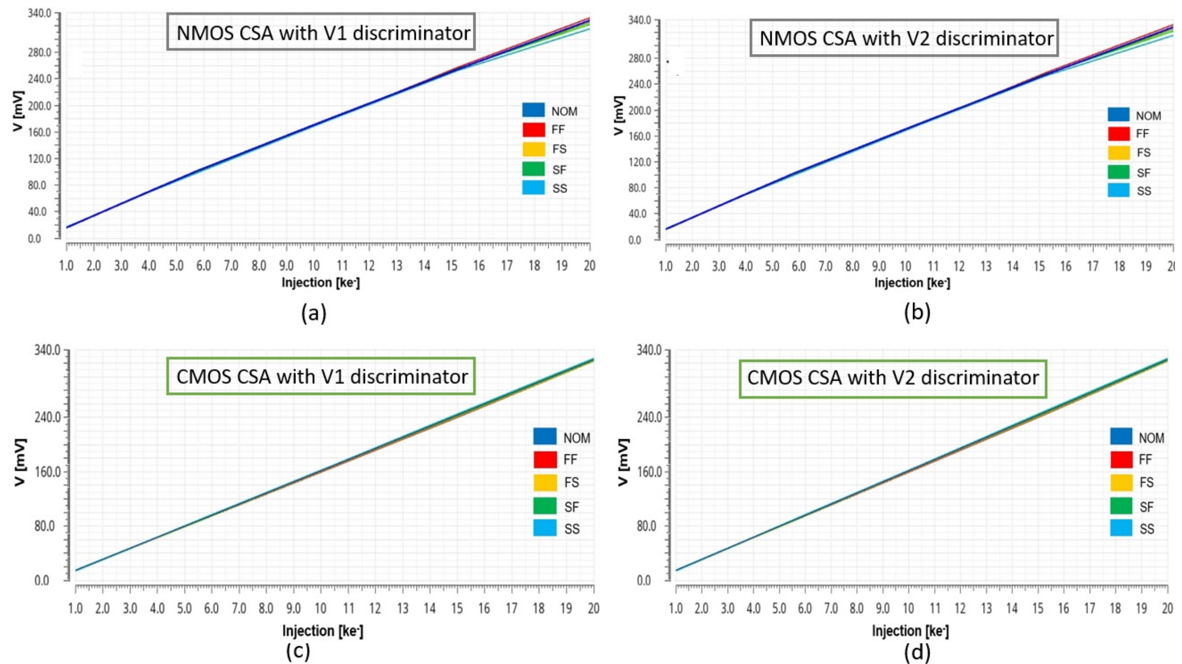


Figure 4.42. – Simulated output response of the front-ends. (a) NMOS CSA with V1 discriminator. (b) NMOS CSA with V2 discriminator. (c) CMOS CSA with V1 discriminator. (d) CMOS CSA with V2 discriminator.

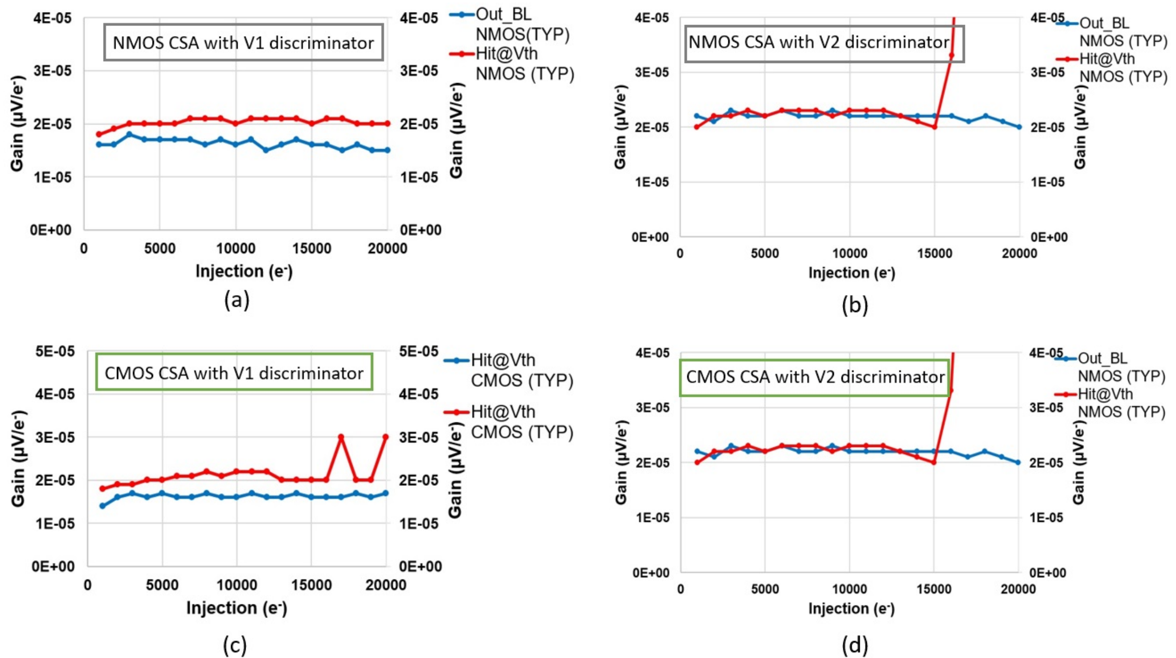


Figure 4.43. – Voltage gain of the front-ends. (a) NMOS CSA with V1 discriminator. (b) NMOS CSA with V2 discriminator. (c) CMOS CSA with V1 discriminator. (d) CMOS CSA with V2 discriminator.

and 4.45. From these simulations, except fast-slow (FS) corner, all other corners show a stable response up to 20ke-.

Linearity simulations were carried out for NMOS and CMOS CSA with V2 discriminator also. Figures 4.46 and 4.47 show the behaviour of "`Out_BL`" and slope of the maximum threshold voltage by varying the injected charge up to 20ke-. From these simulations, we see that for the fast-slow (FS) and fast-fast (FF) process corners, the V2 discriminator does not fire after 6ke- electrons. There is a NMOS effect in this new front-end design.

From these simulations we conclude that the new discriminator design is not robust in two corners (FS and FF). It means that NMOS transistors have lower threshold voltage than the typical model. Therefore after radiation, the threshold voltage of NMOS should decrease more. The NMOS Fast corner will show the effect of radiation on NMOS transistor. This design should be modified and made more robust in the next iteration of LF-Monopix chip.
The LF-Monopix chip was received from the foundry in Q1 of 2017. The chip was fully functional and characterized in the laboratory. The breakdown voltage of the LF-Monopix chip was around 280 V with the leakage current of 20 nA. 3 Samples were irradiated with protons at PS CERN in October 2018 for 10 days reaching a Total Ionizing Dose (TID) of 165 MRad. The LF-Monopix chip showed good performance under the beam. Characterization of LF-Monopix chip is described in [103].

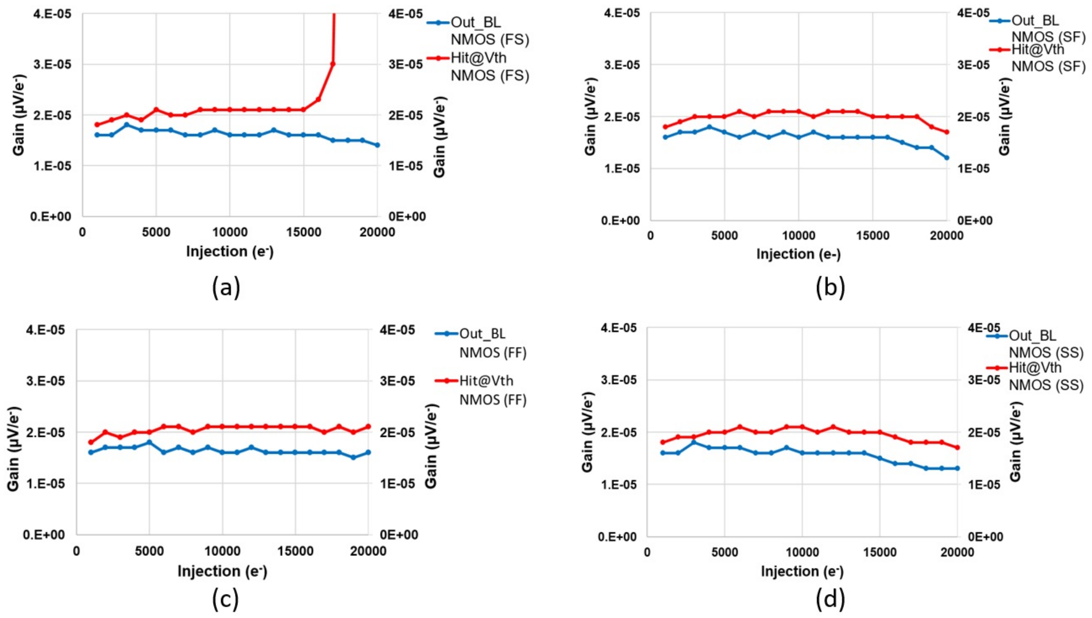


Figure 4.44. – Simulated linearity response of the NMOS CSA with V1 discriminator at different process corners.

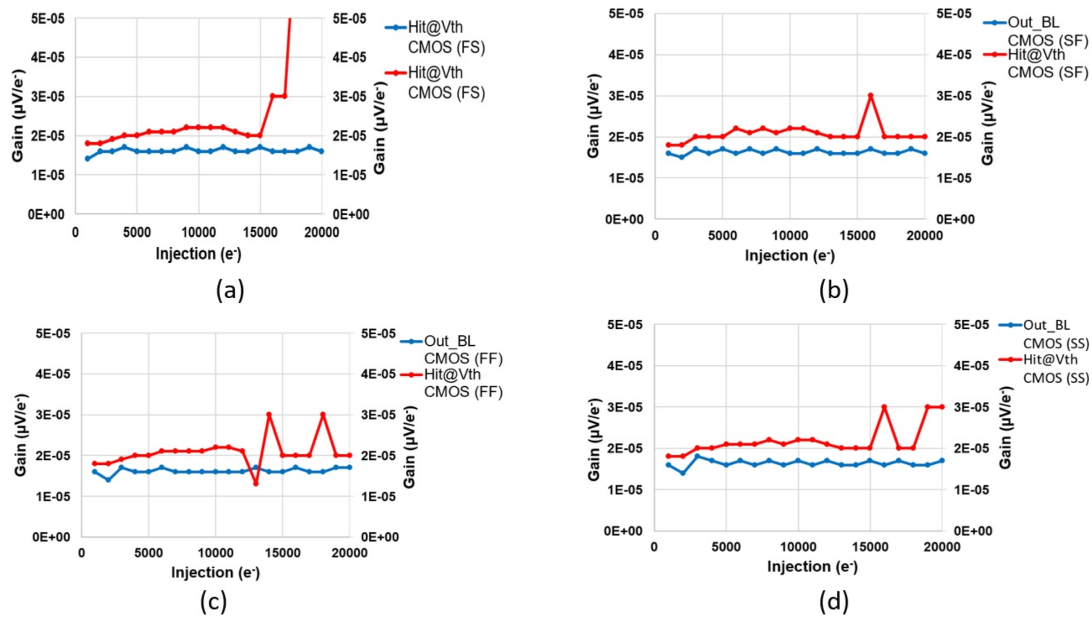


Figure 4.45. – Simulated linearity response of the CMOS CSA with V1 discriminator at different process corners.

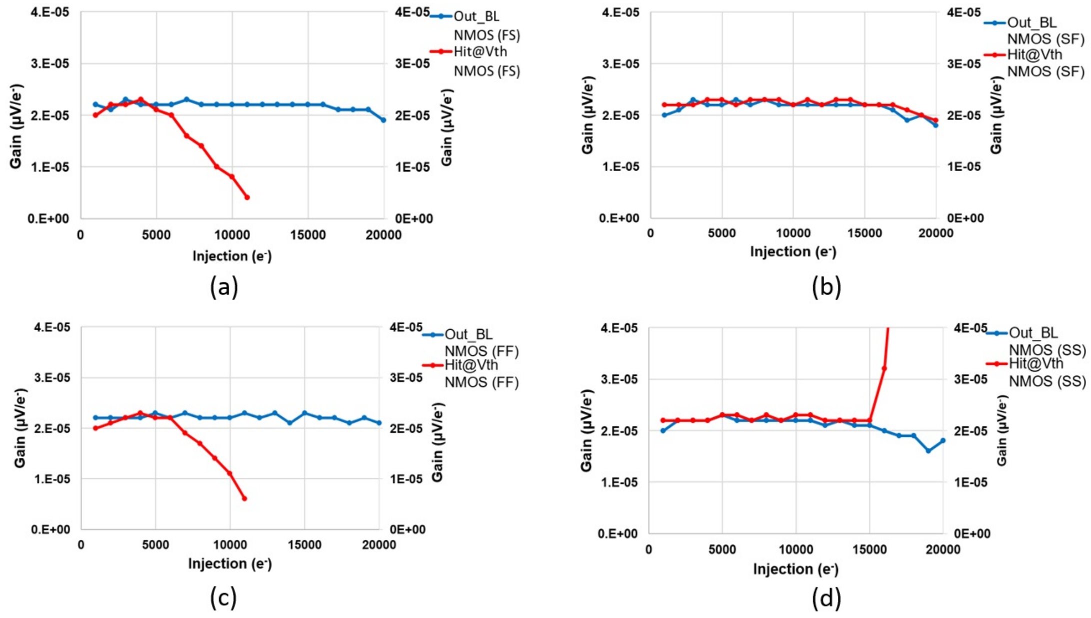


Figure 4.46. – Simulated linearity response of the NMOS CSA with V2 discriminator at different process corners.

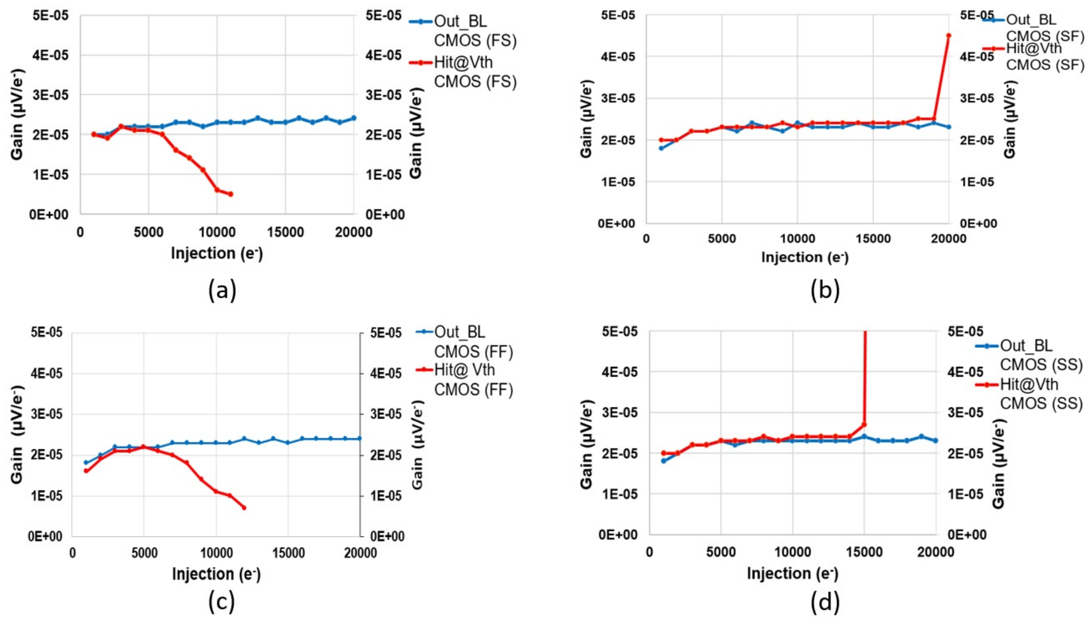


Figure 4.47. – Simulated linearity response of the CMOS CSA with V2 discriminator at different process corners.

4.7. Summary

Two prototypes, namely: LF-CPIX and LF-Monopix, have been developed to demonstrate their suitability as pixel detectors in the outer layers of the ATLAS pixel detector in the HL-LHC. The pixel design was studied for LF-CPIX and LF-Monopix within the framework of the ATLAS ITk upgrade. The prototypes have been fabricated using 150 nm CMOS LFoundry technology on high resistivity (> 2 kΩcm) wafers. The first prototype, LF-CPIX, was used for detailed characterization of the sensor and the analog readout of the depleted CMOS sensor. The second prototype, LF-Monopix, was based on a fully monolithic approach, including fast readout digital logic that handles the required hit rate.

Two LF-CPIX prototype versions were submitted to the foundry. LF-CPIX V1 uses the same number of guard rings as implemented for the CCPD-LF prototype, whereas in LF-CPIX V2, the number and spacing of guard rings have been optimized in order to increase the breakdown voltage and minimize the inactive area. The LF-CPIX prototype consists of three-pixel sub-arrays: passive, analog-digital, and analog. The lab measurements before irradiation were in agreement with the simulation in terms of analog outputs of all the three pixel matrices. For the three pixel matrices implemented, both the pre-amplifier and the discriminator were responsive up to TID of 150 MRad and NIEL of $2.7 \times 10^{15} n_{eq}$/cm^2. Limited degradations in the threshold dispersions and small shifts in the average threshold values were observed. Moreover, the noise performance showed a limited degradation for the NMOS pixel matrix, in particular when compared to PMOS and CMOS pixel matrices.

In LF-Monopix there were nine different pixel sub-arrays. Seven sub-arrays were made of analog front-end and in-pixel read out logic. The other two sub-arrays had read out logic implemented inside the periphery. The sub-arrays differ in discriminator and pre-amplifier implementations. Linearity simulations were carried out for different front-end designs. The simulation results indicated that the new discriminator design is not robust in two corners (FS and FF). This issue was addressed and mitigated for the next design thus making the design more robust in all corners.

5. Developments towards radiation tolerant memories in HV/HR CMOS process

In this chapter, the main developments and implementations of the SEU tolerant memories are discussed. Several prototypes in AMS, TowerJazz and LFoundry technologies have recently been developed by our group. This section starts with some mitigating techniques against SEUs. Design and test results for a SEU tolerant memory chip in AMS 180 nm will be discussed in section 5.2. In section 5.3, we will discuss the second prototype in TowerJazz 180 nm CMOS which was submitted in August 2018. Section 5.4 deals with a third prototype which was designed in LFoundry 150 nm CMOS and submitted to the foundry in January 2019. The AMS SEU tolerant chip was tested under the proton beam.

5.1. Mitigation of SEUs

In a high radiation environment like the ATLAS experiment, SEUs (introduced in section 3.5.3.2) are a major concern for integrated circuits. Three general classes of techniques can be used to protect the circuits from being upset, namely: process level, circuit level and system level techniques. On process level there are different ways to mitigate this issue, by using the Silicon on Insulator (SOI) process, or triple, or quad well processes. It is shown in [104] that the soft error rate could be also improved by using high threshold transistors. The major drawback of this technique is the fabrication cost.
On circuit level, hardening is achieved by designing the structures which can store the data in a redundant way. It is an attractive solution for the CMOS process since at lower cost the memory is tolerant to SEU. On a system level, the memory can be made tolerant by implementing techniques such as temporal sampling, triple modular redundancy. In this section, we will describe various design techniques to make the circuit tolerant to SEUs.

5.1.1. The Dual Interlocked Storage Cell (DICE)

A D-latch is used to store one bit of information. If the data in the input changes while the load signal is high, then the output will follow the input. In a standard D-latch, the information is stored only at 1 node. To make the design tolerant to SEU, some redundancy needs to be obtained in the cell. As seen in [105], to achieve redundancy, four inverters can be cascaded to form a double

SRAM cell as sketched in figure 5.1. But this structure does not give any protection as if a particle strikes on any one of the sensitive nodes (X1-X2-X3-X4), the error would propagate in a loop of the whole cell. The dual-interlocked cell (DICE) structure shown on figure 5.2 is more robust to SEU than the standard cells as error propagating path breaks between X1-X3 and data is recovered on node X3. In a DICE cell, the data is stored in 4 sensitive nodes (X1-X2-X3-X4). These nodes store the data as 2 pairs of complementary values. The data can be read or written into the cell by the access transistors which are controlled by the load signal.

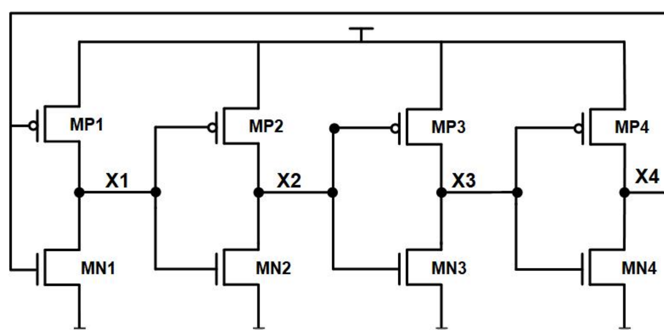


Figure 5.1. – Double SRAM structure. Access transistors are not shown.

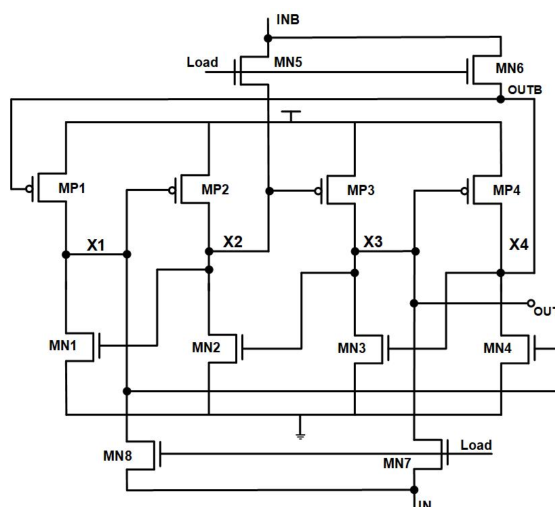


Figure 5.2. – Schematic of a DICE latch structure

To take an example, when the stored data is 0 then initially the cell stores 1010 on X1-X2-X3-X4 nodes, in particular X2 is low and X3 is high. If we assume a particle strikes on the node X2, the transistor MN1 is turned ON, forcing node X2 to to lose its stored value from 0 to 1. This will turn OFF transistor MP3. Transistor MN3 is also in OFF state due to the logic 0 stored at node X4. The

error at node X2 does not propagate since transistors MP3 and MN3 are in an OFF state. Therefore, X3 and X4 do not lose their value and the correct value is stored throughout the cell.
Once the node is exposed to a SEU it requires a certain amount of time for the initial state to be restored across the cell. This delay is termed as recovery time. Rising clock during the recovery time can store a wrong value into the memory cell. It should be noted that if two sensitive nodes of the cell storing the same data (X1-X3) or (X2-X4) collect charge at the same time, the DICE cell is likely to get upset. In practice, the probability of the occurrence of this event is made low by increasing the space between the two sensitive nodes of the same DICE cell [106]. Measurement studies [107] have demonstrated that DICE cell could be made more than 30 times more tolerant to SEU when compared to standard latch by employing the interleaved layout technique.
The DICE cell consisting of 12 transistors which occupy nearly twice the area, when compared to standard D-latch and burn twice more power. Indeed when working on hardened by design techniques, the SEU-hardness benefits need always to be counterbalanced against area needed by the cells in the first place, power restrictions in the second. Nevertheless, DICE is a powerful structure in terms of SEU-hardness and is suitable for being used as latches.

5.1.2. The Whitaker Cell

Another possible immune to SEU logical cell was developed by Whitaker [108]. The cell is sketched in figure 5.3 and has 4 memory nodes X1-X2-X3-X4 like a DICE cell. The cell is divided into two sections with a same type of transistor in each. The left section consists only of PMOS transistors and the right section consists only of NMOS transistors. The same information is stored in two sections, providing redundancy similar to the DICE cell.

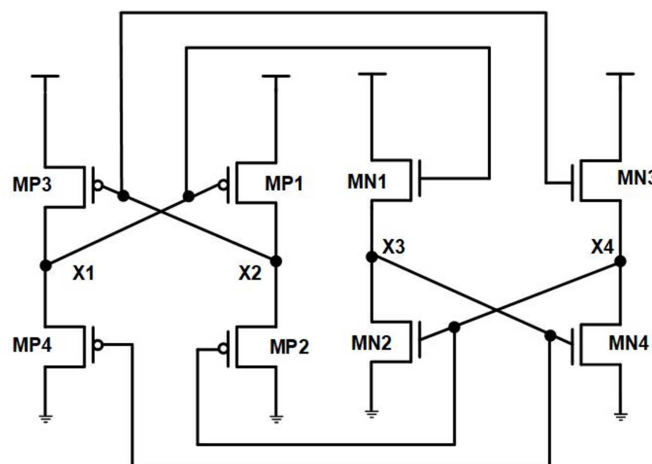


Figure 5.3. – Schematic of Whitaker latch structure. Access transistors not shown.

In this case, transistors MN1 and MN3 are designed to be weak compared to MN2 and MN4. Similarly, MP2 and MP4 are designed to be weak compared to MP1 and MP3. Let us assume node X1 stores 0, and a SEU triggers to 1 making MP1 turned OFF but node X2 will still remain 1 at 1. Any upset in the left section (consists only of PMOS transistors) of the schematic will keep all the PMOS transistors to be in OFF state. Only a transistor in the right section (consists only of NMOS transistors) will be turned ON by an upset in left section. The Whitaker cell consists of 16 transistors.
The main drawback of this cell is its very high static power dissipation due to degraded voltage levels and hence limits the number of cells in the design. To overcome this problem, an improved version of this design has been previously described by Liu [109]. In Liu's design, a complementary devices were inserted between the power supplies (VDD and VSS). With this modification, the DC paths are disconnected when the cell is not functional. However, this cell is not much attractive since it takes more area and power when compared to the DICE cell. Moreover, this cell is slower than a DICE cell due to the degraded logic levels.

5.1.3. The SRAM memory Cell

The conventional 6-T static random access memory (SRAM) is a static volatile memory which is used to store the data. The conventional structure of SRAM is less tolerant to SEU since it has two sensitive nodes Q and QB as sketched in figure 5.4. SRAM cell is widely used in space, terrestrial and other applications [110] [111] [112]. Recent studies [113] [114] have shown that it can be made very tolerant to SEU.

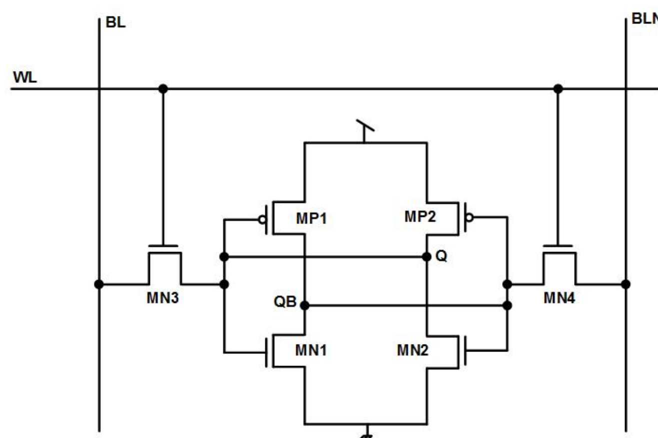


Figure 5.4. – Schematic of a SRAM memory cell.

Figure 5.5 shows the conventional 6-T SRAM memory cell with capacitor to enhance the SEU and SET tolerance. By adding this capacitor, the total node

capacitance on the sensitive node increases. This means more charge is needed to upset the value which is stored. The word line WL is used to drive the two NMOS transistors MN3 and MN4 which connect to bit line and negated bit line (BL/BLN) respectively. The size of the SRAM memory cell is mostly dominated by the capacitor "C" and also the value of the capacitor depends on the Q_{crit}.

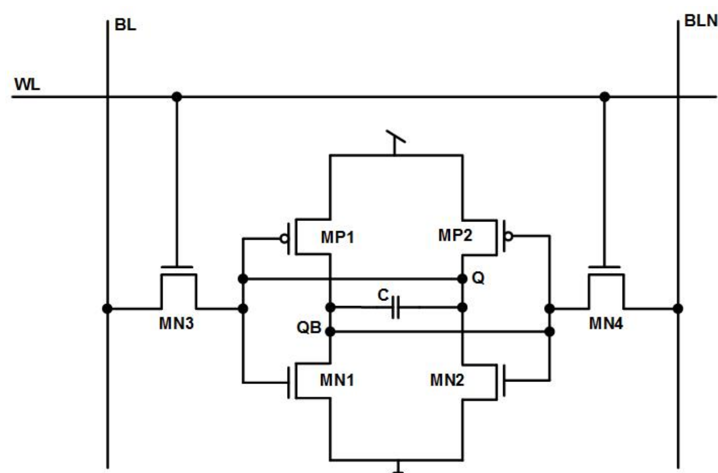


Figure 5.5. – Schematic of SRAM memory cell with capacitor.

The conventional SRAM structure was implemented inside the pixel of LF-MONOPIX 01 chip. From the simulations, the structure could withstand about 500 fC of charge before making an SEU. To make it more immune to SEU, (we targeted about 2.5 pC) the above stratgegy was not possible since it required a very large value of the capacitor. For application in high radiation environments, like the ATLAS experiment, this strategy is not suitable since the "cell area" is one of the most important constraint. To overcome this, a study was made on the design of the SEU tolerant SRAM cell in LFoundry which is discussed in section 5.4.2.8.

5.1.4. Triple Redundancy Logic (TRL)

The structures described until now are more resistant than standard SRAM and standard latch. The technique called Triple Redundancy Logic (TRL), was first developed in 1952 by Von Neumann with the purpose of enhancing reliability of an electronic system. Soon this concept was implemented in the field of microelectronics so that the IC is more tolerant to an ionizing particle. The block diagram of TRL technique is sketched in figure 5.6. In this technique, the latches are triplicated and their outputs are fed to a majority voter, and if the content of any of these latches is corrupted by a soft error, it is retained through the majority voting circuit. The basic principle of TRL has proven [115] to be tolerant to

the SEU.

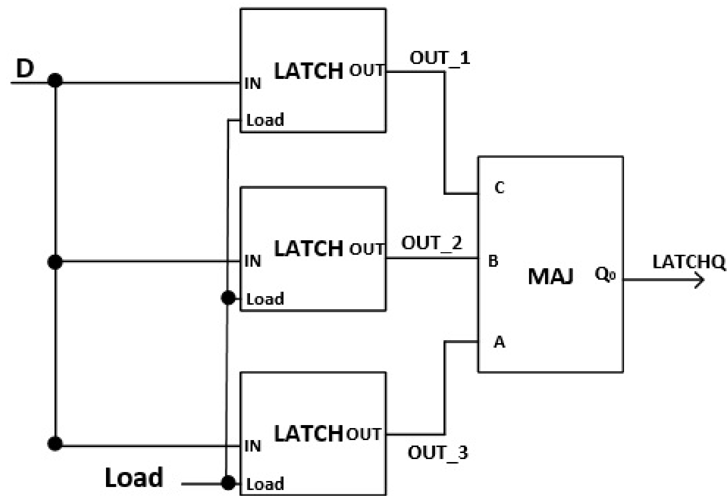


Figure 5.6. – Block diagram representation of Triple Redundancy Logic technique.

The TRL technique can be easily applied to a state machine and make a memory unit by synthesis. Many different versions of this technique have been implemented in CMOS technology. Few of these versions will be discussed in 5.2.2.

5.1.5. Temporal redundancy

The TRL technique is SEU tolerant only if output of one of the three latches is flipped as the data is sampled for all the three latches at same time. If in case, the output of two latches are flipped at the same time then definitely, the SEU will take place. This is the major drawback of this architecture. The architecture can be made more SEU tolerant if the data from the latches is sampled at different time intervals.
One of the another main technique is known as temporal redundancy. In other words, it means redundancy in the time domain. In this technique, multiple sampling of data is done at different time intervals which results in data redundancy. The major concern during this technique is that the data should be stable during the sampling mode.

The circuit sketched in figure 5.7(a) is a block diagram of temporal sampling latch with different clocks. It consists of three latches (A1, A2 and A3) with a majority cell (A4). The latches A1, A2 and A3 are controlled by clock A, clock B and clock C respectively. Clocks B and C are generated by delaying the clock A by ΔT and 2ΔT. The three latches operate in a parallel mechanism and form a temporal sampling stage of the circuit. An asynchronous voting scheme is per-

formed by the majority cell.

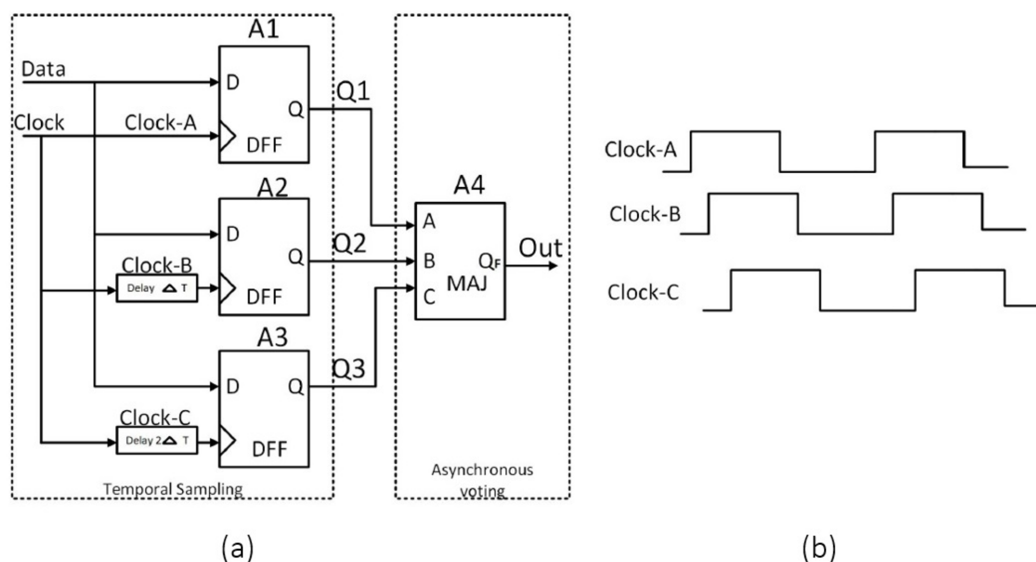


Figure 5.7. – (a) Temporal sampling latch technique. (b) Different clock intervals.

Figure 5.7(b) shows the master clock (clock A) with the other two clocks generated locally by adding buffers. This circuit performs in two modes : sample and hold mode. During the sample mode, the data at the input of the latches also appears at net Q1, Q2, Q3. Next in the hold mode, the data is stored in the latches till the next rising edge of the clocks. Depending on the outputs of the latches A1, A2 and A3 the majority cell releases the majority of the sampled data. This data acts as an input of the combinational block. The evaluated data from the combinational block should reach at the input of the proceeding latch before the rising edge of its clock to avoid set-up and hold timing violations.
Suppose if a highly energetic particle strikes at the input of the latches and creates a transient. This might propagate the wrong value at the output of the latch A1 only since A2 and A3 latches will be in hold mode. The majority cell ensures that the correct data value is asserted on the output node. In this way, we can make the structure immune to SEUs and this technique will be implemented in the next iteration of RD53 chip. However, the major drawback of this technique is that it is limited to low frequency operations.

5.2. Radiation tolerant Single Event Upset memories in AMS 180 nm CMOS

Within the HV-CMOS ATLAS collaboration [116], a first test chip containing SEU tolerant memories was produced in AMS aH18 CMOS process. The SEU test chip was submitted in the MPW submission with ATLASpix-2 chip in August 2017. The objective was to design different SEU structures and choose the best structure for the final ATLASpix-3 chip which is dedicated to the environment of a pixelated layer in a high radiation collider environment. The AMS SEU tolerant chip was exposed to 24 GeV protons at the Proton Synchrotron (PS) at CERN.

5.2.1. Architecture of SEU tolerant chip

The SEU tolerant memory chip consists of five different types of latches organized in six columns. Each column consists of 80 bits of latches which are connected in series. All memory latches can be accessed with shift registers based on flip-flop cells of the AMS aH18 standard library. Loading and shifting the bits into the latches is performed using a simple procedure. In the first phase, the data will be loaded into the shift register. Next, when the load signal goes from 0 to 1, the data will move from the shift register to the latch. Thereafter in the third phase, the read back signal allows the loading of data back from the latch to the shift register. Finally, in the last phase the information will propagate out of the chip by using the clock signal.

The block diagram of the architecture of this SEU tolerant chip is sketched in figure 5.8. The chip consists of two parts, the first part known as core which consists of six columns with six different latch structures. The second part consists of the demultiplexer block which helps in selecting a particular column to be enabled with various global signals (CLK, CLR, RB, Load, SIN). Moreover, all these global signals are buffered inside the chip.

5.2.1.1. SEU-CORE matrix

The SEU core matrix is sub-divided into six different columns with five different latch structures. The depth of the latches is 80 bits and they are controlled by global signals. The block diagram of the arrangement of the various structures is sketched in figure 5.9. The different structures implemented in the core are:

1. Column 1 : TRL with DICE latch.
2. Column 2 : TRL with standard latch.
3. Column 3 : SPLIT TRL with standard latch.

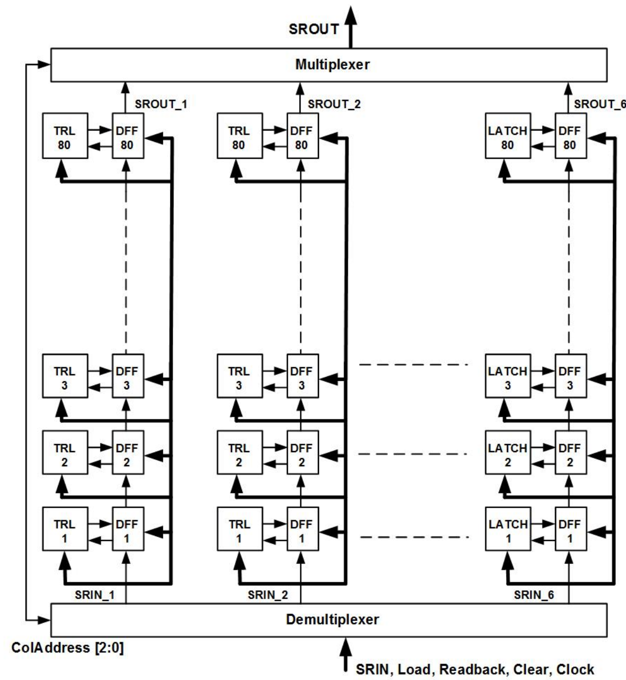


Figure 5.8. – Block diagram architecture of the SEU tolerant chip in AMS

4. Column 4 : SPLIT TRL with standard latch.
5. Column 5 : Standard latch.
6. Column 6 : DICE latch

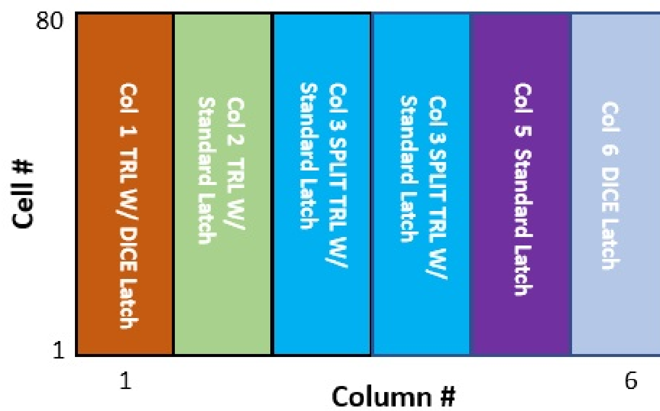


Figure 5.9. – Different structures inside the AMS SEU test chip

The main function of the demultiplexer is to select a particular column inside the core. The selection of these columns is done by the column address [2:0]

which is chosen with the help of decoder circuits. For every global signal there is an individual decoder implemented. The decoder block is designed using AND gates from the digital library. Table 5.1 shows the logic for column selection for the AMS SEU chip.

Table 5.1. – Logic for column selection inside the decoder block for SEU core.

In <2>	In <1>	In <0>	OUT
0	0	0	Not connected
0	0	1	OUT <6> column 6
0	1	0	OUT <5> column 5
0	1	1	OUT <4> column 4
1	0	0	OUT <3> column 3
1	0	1	OUT <2> column 2
1	1	0	OUT <1> column 1
1	1	1	Not connected

5.2.2. Design of SEU hard memory cells

A CMOS process has been adopted in order to satisfy the high level of integration requirement for an upgraded pixelated detector. In this section, we discuss a detailed description on the design with simulation results for the SEU tolerant memories.

5.2.2.1. Design of the standard latch

The standard latch structure is based on conventional transmission gates and other transistors. Figure 5.10 shows the block diagram of a 1-bit memory unit standard cell. The cell consists of 2 multiplexers, D-FF and standard latch. RegD is the input and is sent through the two multiplexers to the shift register and finally to the standard latch when the load signal is enabled. To avoid the problem of driving many inputs from a single output (fan-out problem), suitable blocks of the standard cells were selected from aH18 library. Figure 5.11 shows the layout of the standard cell unit. From previous experiences [30], we already know that this design is not SEU-hard enough, yet this design provides an important reference to compare and normalize the SEU cross-sections we get with other more SEU-tolerant structures. The design was simulated at different process corners, supply voltage variations, temperatures (PVT) with monte-carlo simulations.
The standard latch is shown on figure 5.12. The dimensions of the standard latch is 6 μm $\times$ 4 μm. This structure does not have any redundancy. The simulation result of 1-bit standard cell unit with the logic 0 is shown in figure 5.13(no injected charge). The data is loaded into the latch and then read back through

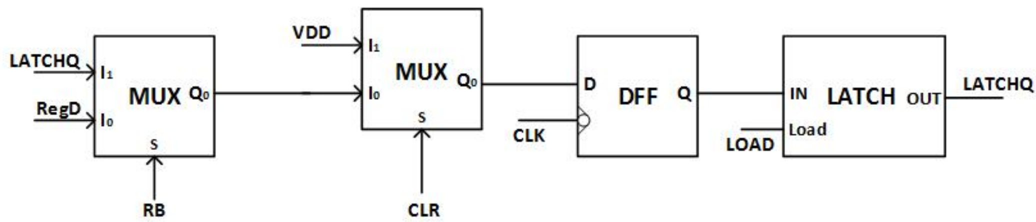


Figure 5.10. – Block diagram of the 1-bit standard cell unit.

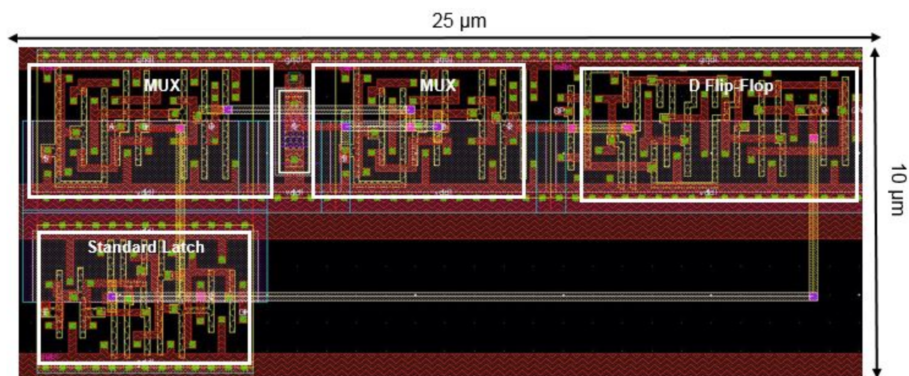
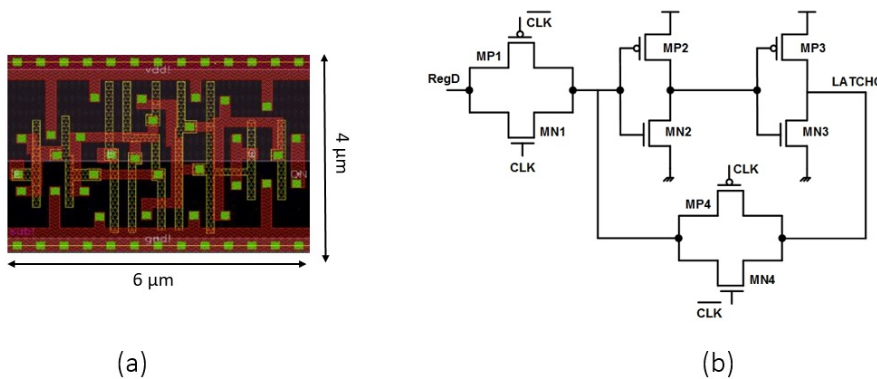


Figure 5.11. – Layout view of 1-bit standard cell unit.



(a) (b)

Figure 5.12. – (a) Layout of 1-bit standard latch. (b) Schematic view of 1-bit standard latch.

the shift register. From the simulations, a transient was noticed up to a charge of 350 fF. The latch undergoes a SEU if more than 350 fC is deposited. From this we could conclude that the Q_{crit} is around 350 fF for the standard latch. Figure 5.14 shows the layout of the 80-bits standard cell matrix. The dimensions of the DICE matrix is 300 μm $\times$ 130 μm. The whole matrix is inside the Deep NWELL.

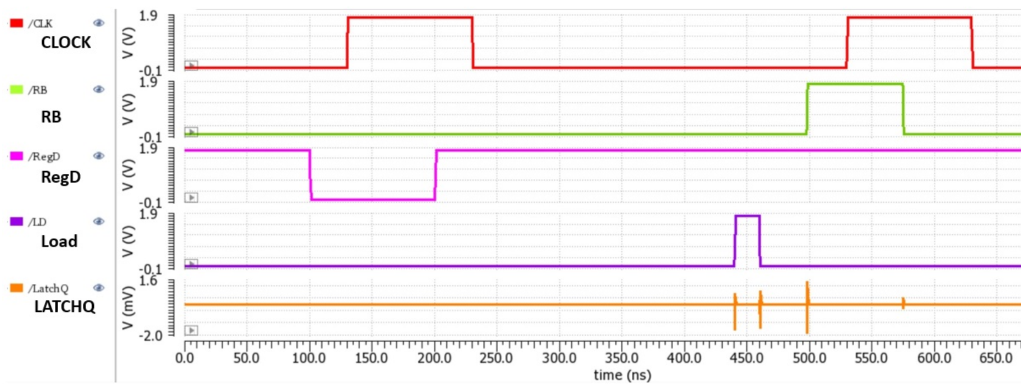


Figure 5.13. – Simulation 1-bit with standard cell for logic 0 as input.

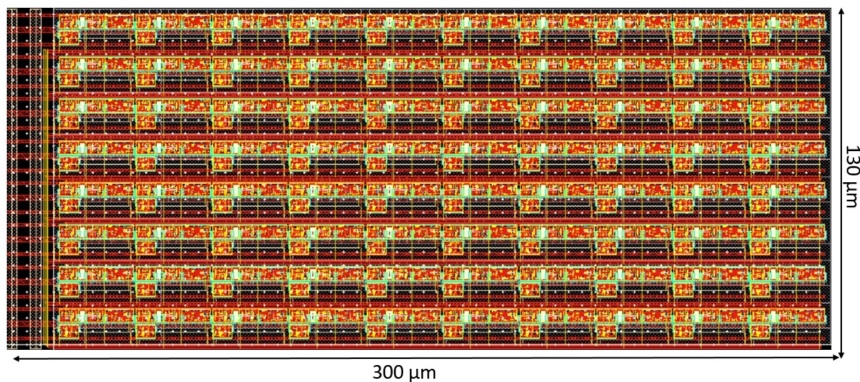


Figure 5.14. – Layout view of the 80-bits standard cell matrix.

5.2.2.2. Design of a DICE Cell unit

The schematic of the DICE latch is constructed by using the conventional two cross-coupled inverters as shown in figure 5.2. Figure 5.15 shows the block diagram of 1-bit DICE cell unit. It consists of 2 multiplexers, D-FF and the DICE cell itself. RegD is the input and is sent through the two multiplexers to the shift register (SR) and finally to the DICE latch. This operation is controlled by various global control signals. The input data would appear at the output of the DICE latch when the load signal is enabled. Figure 5.16 illustrates the layout of the 1-bit DICE cell unit as implemented in the chip discussed here. To avoid any fan-out problem at different process corners, suitable blocks of the standard cells were selected from aH18 library.

Logic 0 or 1

Suppose we would like to store logic 0 or 1 into the DICE latch. In the first clock the data would be stored into the D-FF and once the load signal goes high the data would be loaded into the DICE latch. After that the output of the DICE

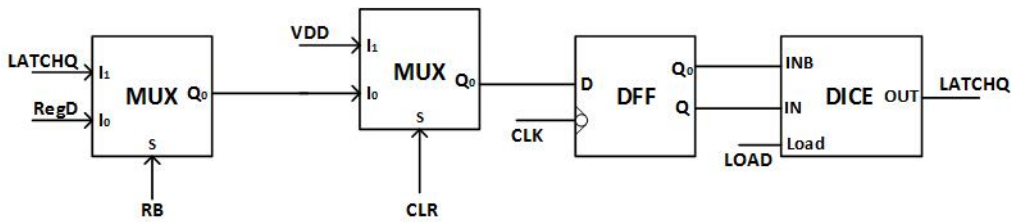


Figure 5.15. – Block diagram of 1-bit DICE cell unit.

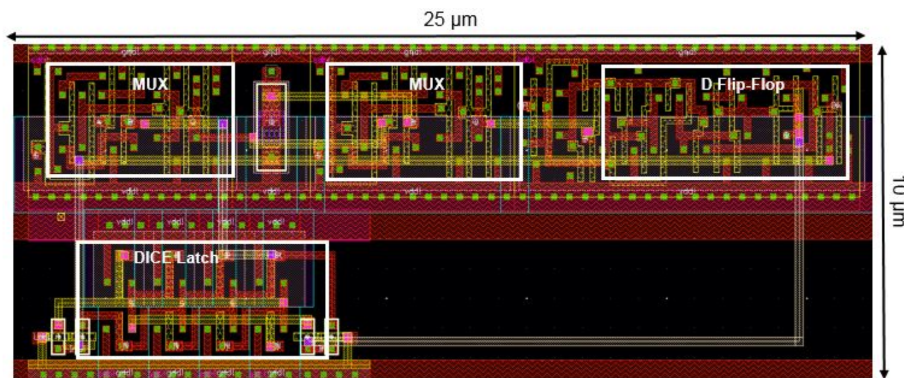


Figure 5.16. – Layout view of 1-bit DICE cell unit.

latch is given as one of the inputs of the multiplexer where it forms a feedback loop. When the read back (RB) signal goes high, the data is being read back. The simulation result of 1-bit DICE cell unit for logic 0 is shown in figure 5.17. From the plot we can see that first the input data (RegD) is loaded into the standard latch when the load signal is enabled. After loading the data we read back the loaded data through the D-FF by enabling the read back signal.

Figure 5.17. – Simulation of 1-bit with DICE cell unit for logic 0 as input.

Figure 5.18 (a)(b) shows the layout and schematic view of the DICE latch. There are 2 sensitive nodes which store the same logic state (X1-X3) or (X2-X4). In the SPICE simulation we have seen that when a very high charge of 2.5 pC was injected only on the node X1, the output of the DICE latch did not change because of the redundant structure. If the particle strikes on both the sensitive nodes at the same time then the value which was stored inside the latch would be flipped. As DICE latch is used as a memory inside the pixel, it should be compact because of the area constraints. In this case taking the area into consideration, if we inject a charge of 2.5 pC on X1 node and 20 fC on the X3 node simultaneously, the value flipped. In order to make the design more tolerant, the distance between the sensitive nodes (X1-X3) or (X2-X4) is increased in the layout. By increasing the distance between these two nodes, the latch is less sensitive to charge sharing effect and the probability for charges to be collected on these two sensitive nodes simultaneously is reduced. In our case, the separation between X1-X3 was taken to be 3.5 μm such that the DICE is made more tolerant and still is compact. Many bulk contacts were also added in order to make the memory cell immune to single event latch-up (SEL). In the end, the DICE latch was designed with a relatively compact size of 8.5 μm $\times$ 4 μm. The design was simulated at different process corners, supply voltage variations, temperatures (PVT) with monte carlo simulations as shown in table 5.2.

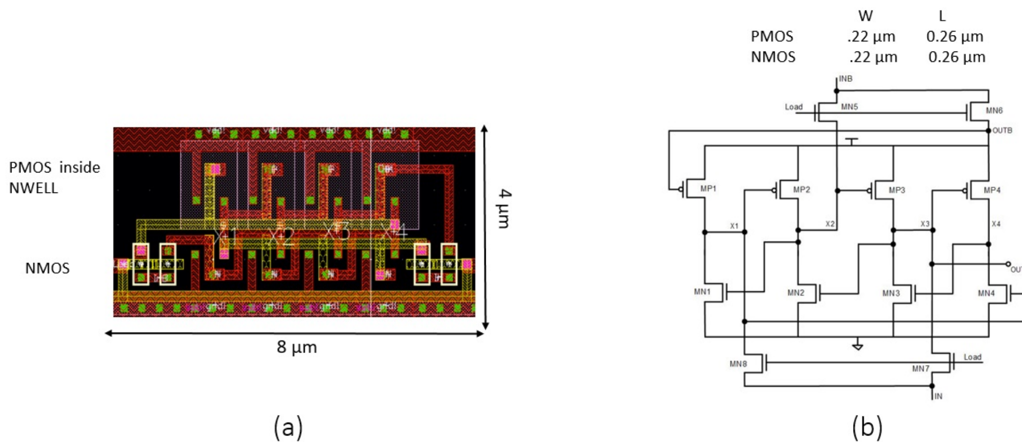


Figure 5.18. – (a) Layout of 1-bit DICE latch. (b) Schematic view of 1-bit DICE latch.

Figure 5.19 shows the layout of the 80-bits DICE cell unit. The dimensions of the DICE matrix is 340 μm $\times$ 130 μm. The whole matrix is inside the Deep NWELL.

Table 5.2. – Status with logic 0 and 1 at different process corners of the DICE cell.

Temp (°C)	TYP	FF	SS	FS	SF
-20	Yes	Yes	Yes	Yes	Yes
0	Yes	Yes	Yes	Yes	Yes
27	Yes	Yes	Yes	Yes	Yes
50	Yes	Yes	Yes	Yes	Yes
80	Yes	Yes	Yes	Yes	Yes

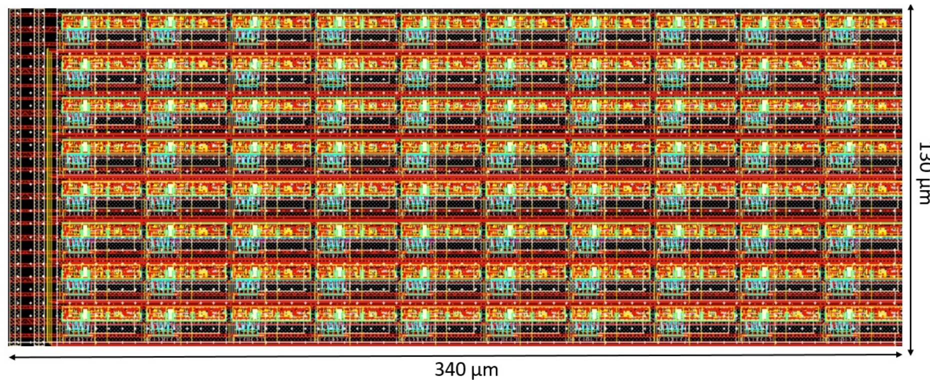


Figure 5.19. – Layout view of the 80-bits DICE cell matrix.

5.2.2.3. Triple Redundancy Logic (TRL) with standard latches

As discussed in 5.1.4, TRL is an another technique to make the memory more resistant to SEUs by triplication of the latches and the addition other logic blocks such as error correction and majority voting cell. If the content of any of these latches is corrupted by a soft error, it is filtered out through the majority voting circuit. This type of approach is very common in today's world as SEU is one of the major issues in HEP. In this TRL structure, the standard latches are triplicated and followed by a majority voting cell. The block diagram of this structure is shown in figure 5.20. This version is preferred compared to TRL with DICE

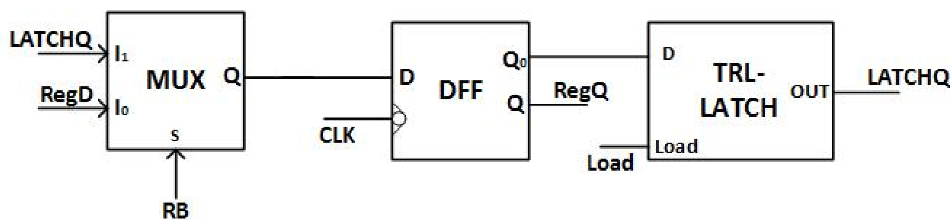


Figure 5.20. – Block diagram of the 1-bit Triple Redundancy Logic block with standard latches unit.

latches and is attractive for HEP applications. This is due to the fact that all the cells used in this structure are coming from the standard library and the structure can be synthesised by using automatic synthesis tools. The drawback of this structure is that it is not enough SEU tolerant when compared to TRL with DICE latch and also the area of the whole cell is more than three times of a single standard latch. In figure 5.20 the input data would first appear at the output of the D-FF at the first clock and once the load signal goes high, the data will be loaded into the TRL-latch cell. The data is finally read out through the shift register of the next clock. The layout of this whole unit is illustrated in figure 5.21 with the size of 55 μm $\times$ 10 μm. In order to make the structure more tolerant, the distance between the two sensitive nodes was increased to 7 μm in the layout. We expect to have a gain of around 200 when comparing to the standard latch because of the architecture of the latch [30]. Figure 5.22 shows the block diagram of the 1-bit Triple Redundancy Logic cell with standard latches, were the standard latches are triplicated and followed by a voting system. The simulation result for the logic 0 is shown in figure 5.23.

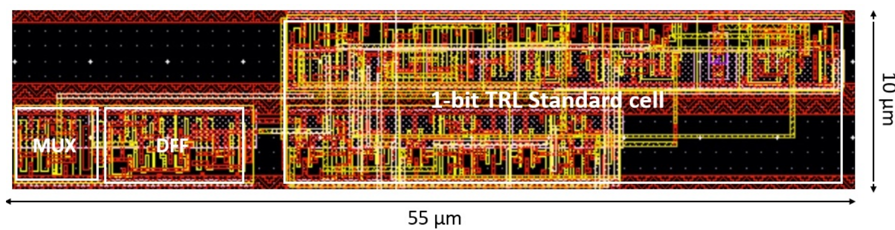


Figure 5.21. – Layout view of 1-bit Triple Redundancy Logic block with standard latches.

Figure 5.24 shows the layout of the 80-bits TRL cells with standard latches matrix. The dimensions of the DICE matrix is 640 μm $\times$ 130 μm. The whole matrix is inside the Deep NWELL.

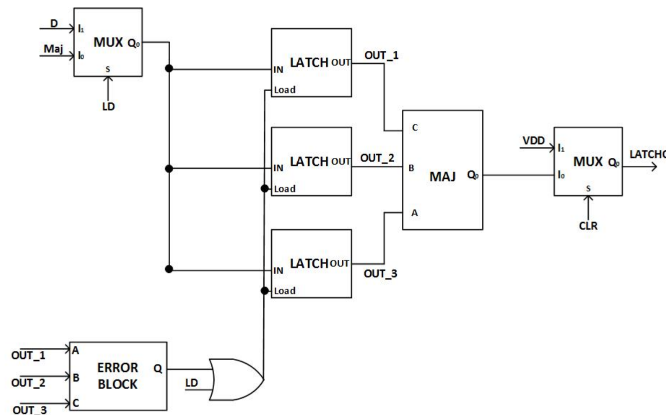


Figure 5.22. – Block diagram of 1-bit Triple Redundancy Logic cell (TRL) with standard latches.

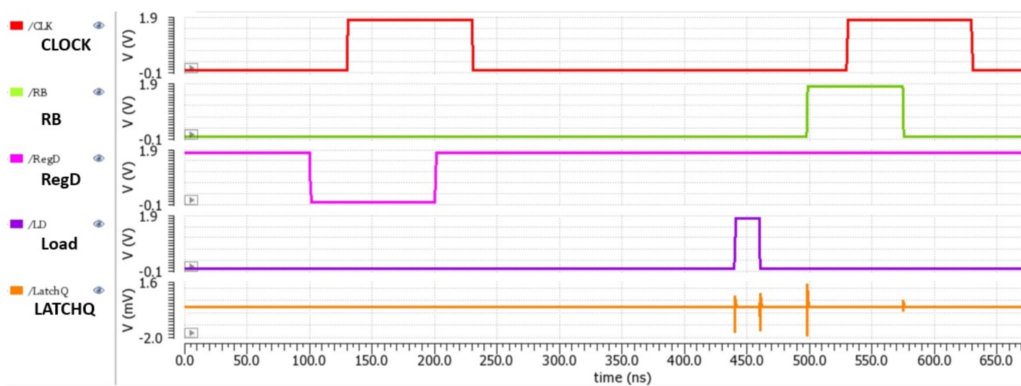


Figure 5.23. – Simulation of 1-bit with TRL cell with standard latches for logic 0 as input.

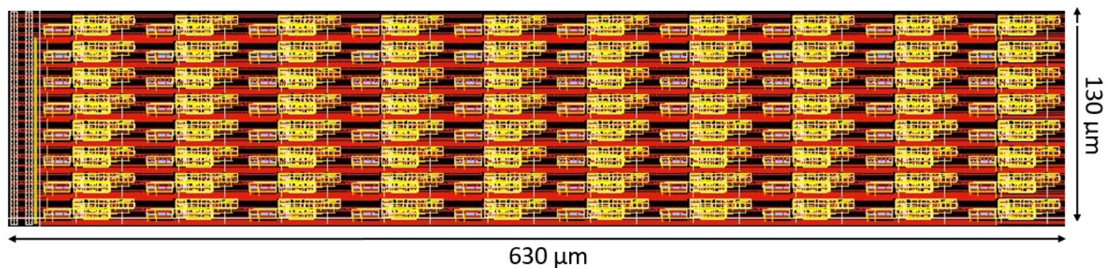


Figure 5.24. – Layout view of the 80-bits TRL with standard latches matrix.

5.2.2.4. Triple Redundancy Logic (TRL) with DICE latches

There are several versions of TRL structures implemented in this test chip. In this version, DICE latches are used instead of standard latches. The block diagram shown in figure 5.25 is of 1-bit TRL with DICE cells. It is made of 1 multiplexer block, D-FF and TRL block. The layout of this whole unit is illustrated in figure 5.26. The area of 1 bit TRL with DICE cells unit is 60 μm $\times$ 10 μm. However, it consumes a rather large area and can not be implemented inside the pixel. It can nevertheless be used in the chip periphery where it increases the SEU-hardness quite drastically.

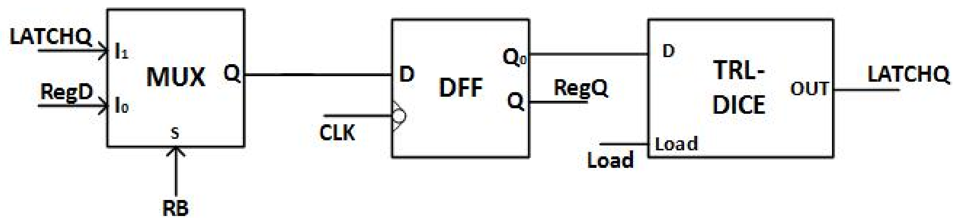


Figure 5.25. – Block diagram of 1-bit Triple Redundancy Logic block with DICE latches.

In figure 5.25 the input data would first appear at the output of the D-FF at the first clock and once the load signal goes high, the data will be loaded into the TRL-DICE cell. The data is finally read out through the shift register at the next clock edge. Figure 5.26 shows the layout of the TRL with DICE cells unit with the size of 60 μm $\times$ 10 μm. Figure 5.27 on the left illustrates the block dia-

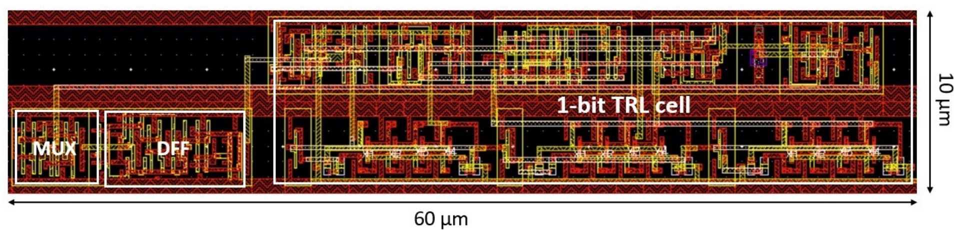


Figure 5.26. – Layout view of 1-bit Triple Redundancy Logic block with DICE latches cell.

gram of the 1-bit TRL DICE cell. The DICE latches is triplicated followed by the majority block. The three DICE latches output are input to the majority voting block. In this design we can see there is a feedback loop formed: the output of the three latches goes in the input to the majority as well as the input of the error block. Error block contains a self correction error block which is sketched in figure 5.27(b). In order to make the structure more tolerant, the distance between

the two sensitive nodes in the architecture was increased to 14μm. The size of the 1-bit TRL with DICE latches is 40 μm $\times$ 10 μm and the layout is shown in Figure 5.28. The simulation result of 1-bit with DICE cell unit for logic 0 is shown in figure 5.29.

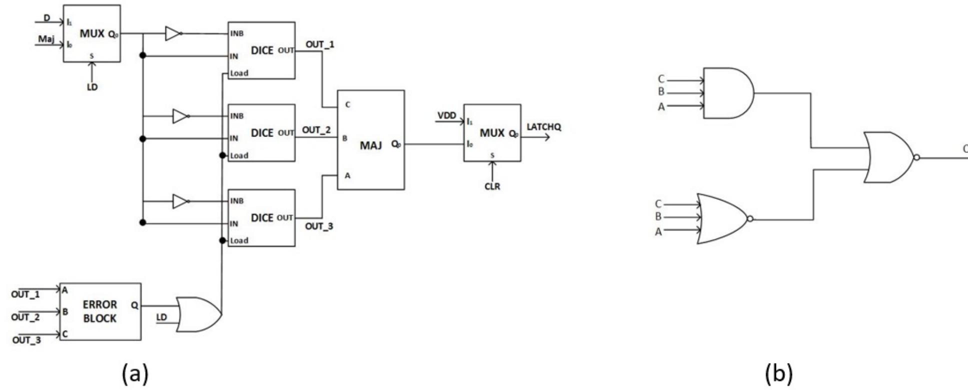


Figure 5.27. – (a) Block diagram of 1-bit Triple redundancy logic (TRL) cell with DICE latches. (b) Self correction error block.

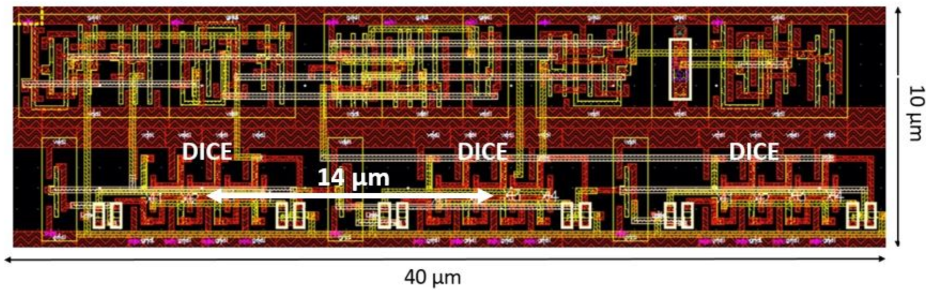


Figure 5.28. – Layout view of 1-bit Triple Redundancy Logic (TRL) cell with DICE latches.

Figure 5.30 shows the layout of the 80-bits TRL with DICE cells matrix. The dimensions of the DICE matrix is 640 μm $\times$ 130 μm. The whole matrix is inside the Deep NWELL. The design was simulated and verified at different process corners, supply voltage variations, temperatures (PVT) with monte carlo simulations.

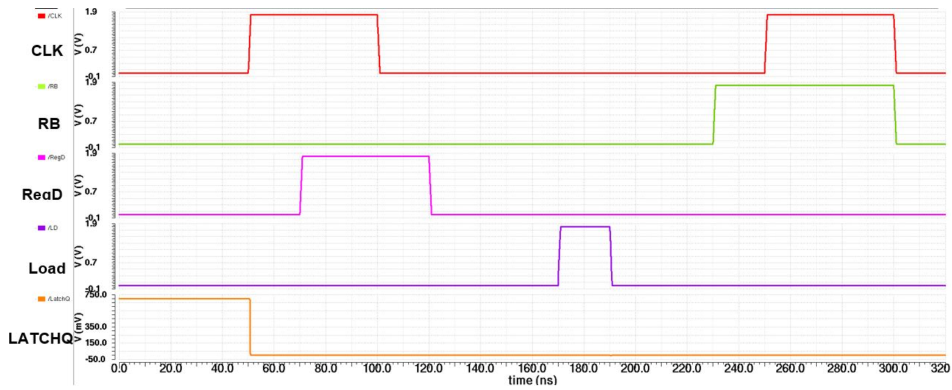


Figure 5.29. – Simulation 1-bit with DICE cell unit for logic 0 as input.

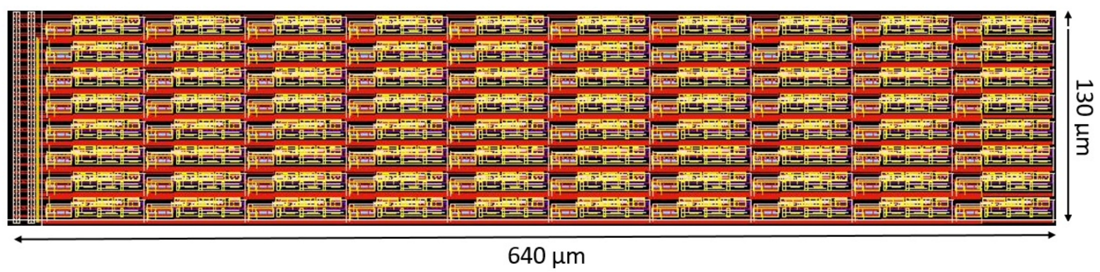


Figure 5.30. – Layout view of the 80-bits TRL with DICE cells matrix.

5.2.2.5. SPLIT Triple Redundancy Logic (TRL) with standard latches

This is the third TRL version structure implemented in the chip. This structure was first implemented few years ago in the framework of RD53 collaboration [20]. In a conventional 1- bit TRL with standard cells architecture, three standard latches are connected in parallel followed by the majority voter circuit. In SPLIT TRL technique, one of the three latches is placed further away in the other bit. This technique is known as SPLIT Triple Redundancy Logic (TRL). This technique is beneficial since it improves the SEU tolerance due to the increase in the separation of the sensitive nodes of the latch. The block diagram of this structure is sketched in figure 5.31. There is a total of five control signals at various levels similar to previous structures. At the rising edge of the first clock, input data RegD appears at the output of the latch 1 D-FF and input of the MUX in latch 2. At the rising edge of the second clock, the same data would appear at the output of the latch 2 D-FF. After a certain time period, the data will be latched into the TRL-SPLIT block. The layout view of 2-bits SPLIT Triple redundancy logic (TRL) with standard cells is shown in figure 5.32 with the size of 115 μm $\times$ 10 μm. The block diagram of SPLIT-TRL block is sketched in figure 5.33

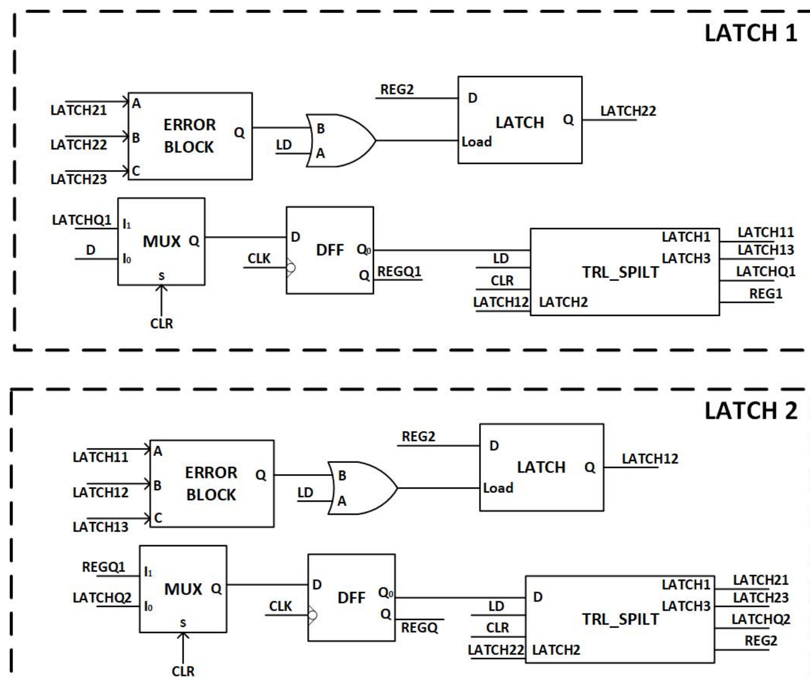


Figure 5.31. – Block diagram of 2-bits SPLIT Triple Redundancy Logic (TRL) cell with standard latches.

In this structure, two major changes in the design have been done. First, the separation between the sensitive nodes was increased by placing one of the latches far from the other two. Secondly, all three latches had three independent error

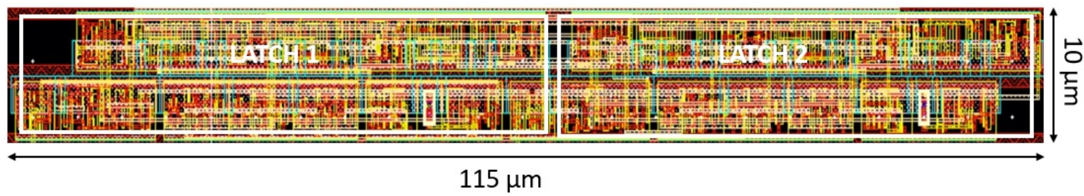


Figure 5.32. – Layout view of 2-bits SPLIT Triple Redundancy Logic (TRL) cell with standard latches.

block and load signal. It has been proven in the 65 nm process [30] that using independent load signals for latches increases the SEU tolerances. For this design, a gain of 4000 was measured when compared to a standard latch with the minimum distance between the two sensitive nodes has been increased to 50μm. This structure stores 2 bits in together which means 4 possible input patterns (00, 01, 10, 11) can be simulated to check the functionality of the latches. Figure 5.34 shows the simulated response with "01" as input.

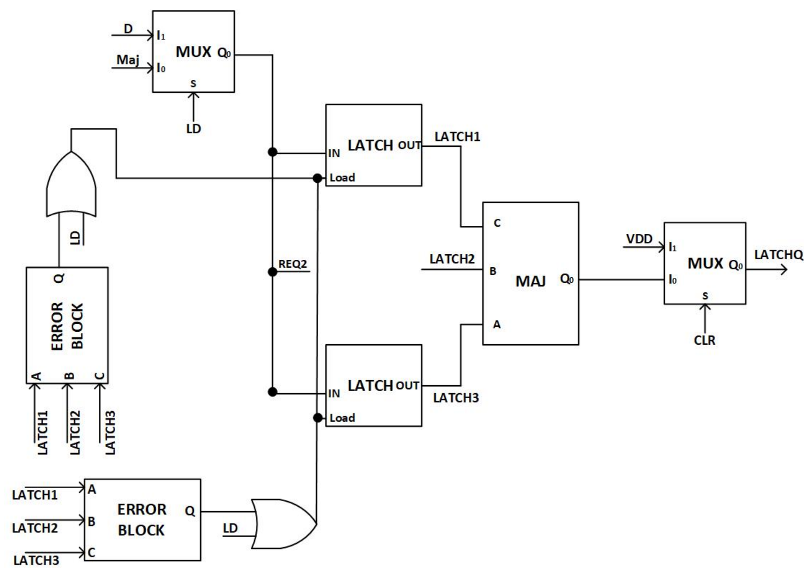


Figure 5.33. – Block diagram of 1-bit SPLIT Triple Redundancy Logic (TRL) cell with standard latches.

Figure 5.35 shows the layout of the 80-bits TRL with DICE cells matrix. The dimensions of the DICE matrix is 600 μm $\times$ 130 μm. The whole matrix is inside the Deep NWELL. The design was simulated and verified at different process corners, supply voltage variations, temperatures (PVT) with monte carlo simulations.

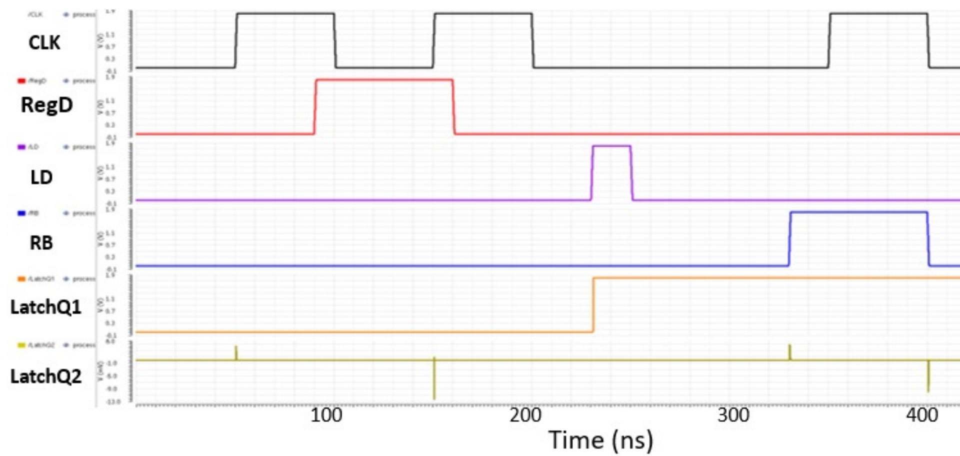


Figure 5.34. – Simulation of 2-bits SLIT-TRL with standard cells for logic 01 as input.

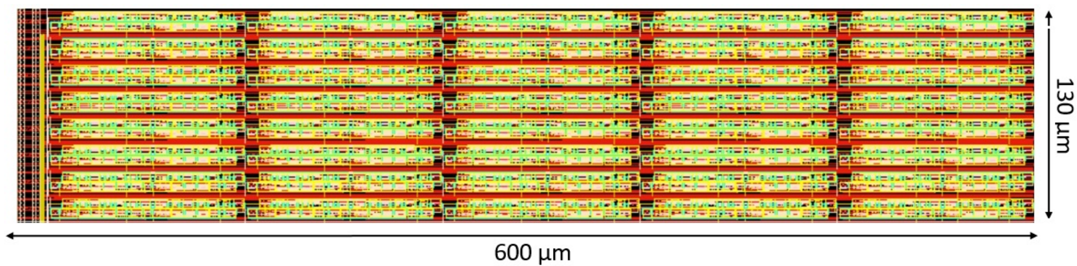


Figure 5.35. – Layout view of the 80-bits SPLIT-TRL with standard latches matrix.

5.2.3. ASIC layout

The AMS SEU tolerant test chip has been submitted to the foundry for fabrication in August 2017. It is designed in a CMOS 180 nm technology with a power supply of 1.8 V. The chip size is 1.3 mm $\times$ 1 mm and the layout is shown in figure 5.36. The chip contains 6 columns with 80 bits in each columns. 14 pads located at the bottom of the chip are used for communication and powering. These pads are listed in table 5.3.

Table 5.3. – AMS SEU tolerant test chip pads list.

Pad	Name	I/O	Function	Comments
1	VDDIO	Supply	1.8 V	ESD protection
2	GNDIO	Supply	0 V	ESD protection
3	VDD	Supply	1.8 V	Core supply
4	GND	Supply	0 V	Core Supply
5	CMD2	Input	Column selector	Select the column by decoder
6	CMD1	Input	Column selector	Select the column by decoder
7	CMD0	Input	Column selector	Select the column by decoder
8	RDBCK	Input	Readback	Latches data loading in shift register
9	CLK	Input	Clock	Clock to load shift register
10	LD	Input	Load	Data loading in latches
11	CLR	Input	Clear	Reset
12	SIN	Input	Data	Data input
13	SOUT	Output	Data	Data output
14	HV	HV	High voltage	Either connect to 0 V or -30 V

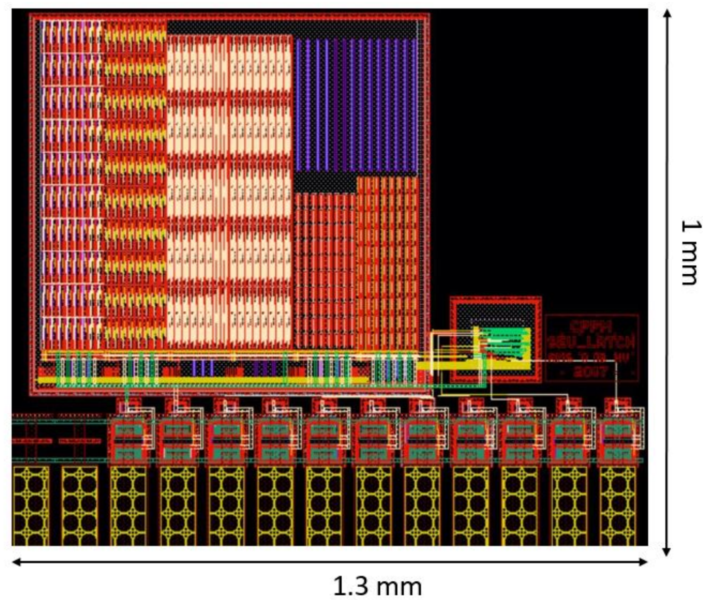


Figure 5.36. – AMS SEU tolerant test chip layout. Different SEU tolerant architectures implemented as shown in figure 5.9.

5.2.4. Test setup for AMS SEU tolerant chip

Laboratory tests of the AMS SEU tolerant chip were performed. As there were no major issues in the chip, a beam test at CERN Proton Synchrotron (PS) [117] was organized in October 2018.
To prepare the beam test, two samples (board no. 1 and board no. 2) out of five chips were selected for the irradiation under the proton beam. The samples were placed on the same table as 3 LF-Monopix chips and 2 RD53A chips. The main goal of this beam test was to study the AMS technology in terms of SEU, to measure and understand the cross-section for different structures which are implemented inside the chip.

5.2.4.1. Experimental setup

Irradiation tests for AMS SEU test chip were carried out at CERN PS facility. This facility provides protons with a constant energy of 24 GeV. The operation cycle of the PS accelerator defines the structure of the beam. The super-cycle period of the machine depends on the mode of operation. In a super-cycle there are several spills of particles and they are distributed to the experiments sharing the beam. More often, IRRAD3 beam line receives 1 to 4 spills per super-cycle. The duration of each spill is 400 ms and the intensity can be tuned. A secondary emission chamber (SEC) device which is placed inside the control room to monitor the proton beam intensity. Moreover, a much more precise value of the proton fluence is measured by irradiating thin foils of Aluminium (these Aluminum foils are given to radioprotection department so that we can know the actual value of the dose). During this irradiation campaign a mean fluence per spill of 149.4×10^9 protons/cm^2 was recorded. The layout of the facility is shown in figure 5.37. There are 3 different zones where samples can be placed for irradiation. Our samples were installed in zone 2.

Figure 5.38 illustrates the test set up used for SEU evaluation at CERN for the AMS chips. This set up consists of a laptop PC, motherboard which is produced by Annecy-le-Vieux Particle Physics Laboratory, a 20 m LVDS cable, translator board, a single ended cable and a Device Under Test (DUT). The motherboard is powered by a DC supply of 5 V. On this board there are 40 Transistor–Transistor Logic (TTL) signals, 32 LVDS signals (DB-37 connectors), 4 successive approximation ADC and 10 DACs. The test chip is controlled and read out by a DAQ system controlled by a laptop PC. The program is used to configure a Field Programmable Gate Array (FPGA) which generates the digital signals to control and read back the DUT. The software to control the IO signals is written in C++ code using Labwindows interface. A small microprocessor BeagleBone is mounted on the motherboard which acts as an interface between the computer and the board. To program a FPGA , a flexible Very High Speed Hardware Description Language

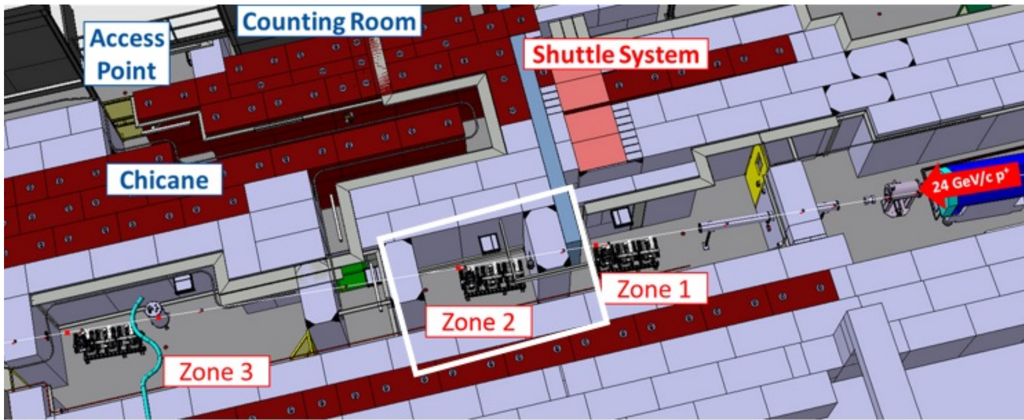


Figure 5.37. – Detailed layout of the IRRAD facility inside the EAST hall building 157 at CERN [117].

(VHDL) code is written. Few ICs on the motherboard are used to convert 5 V TTL signals into LVDS signals. These LVDS signals from the DB 37 connector, are transmitted through a 20 m cable which is connected to the translator board located in the irradiated zone. The translator board is powered by a regulator mounted on the board. The LVDS signals are converted into single-ended signals and transmitted through a 2-3 metres of flat cable to the Device Under Test.

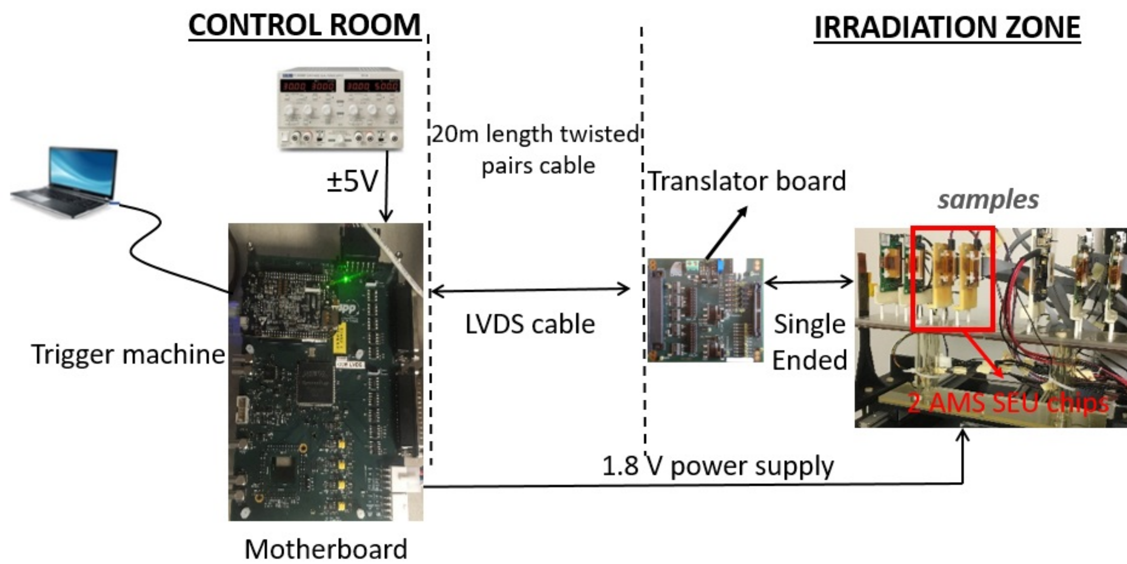


Figure 5.38. – Experimental setup for AMS SEU testchip at CERN.

5.2.5. Irradiation testing procedure

Testing with the proton beam was planned to characterize the SEU robustness of the chip and its internal structures. Protons were chosen for this test because it gives both TID and NIEL irradiation damages. For the testing of the AMS chip we followed the following procedure.

- When the beam will strike the SEU chip, a counter placed near the table will generate a short pulse.
- This pulse is connected to a psV4 connector on the motherboard which acts as a triggering pulse.
- After this, a readback operation is performed through the shift registers and latches.
- Once readback is done, again the data is loaded inside shift registers and latches. The operating frequency is 1 MHz.
- Same process repeats with the next beam.

Two kinds of bit-stream were used: all-1s stream and all-0s stream. These simple streams are easy to compare at high-speed on the test board.

5.2.6. Proton beam test results

5.2.6.1. SEU cross section

The main objective was to assess the SEU-hardness of each structure by measuring each structure's sensitivity to proton-induced SEUs in terms of a cross-section. The mean dose rate during this campaign was 2 MRad/hr. The plot of mean dose rate versus time is shown in figure 5.39. The value of cross-section is determined by using the formula shown in equation 3.35

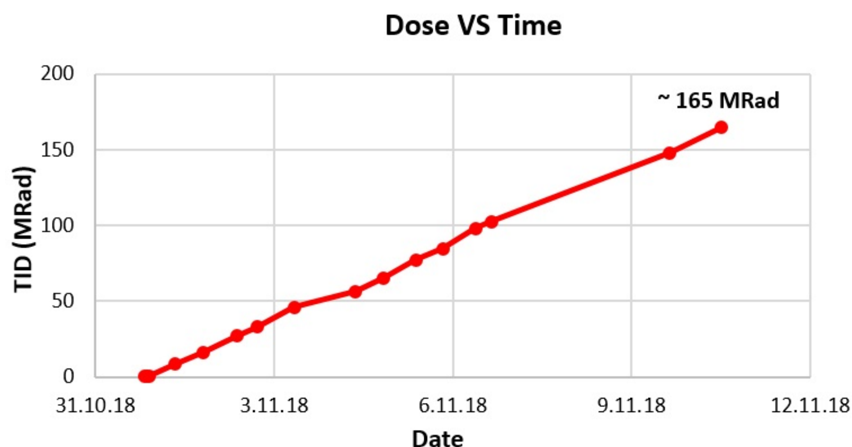
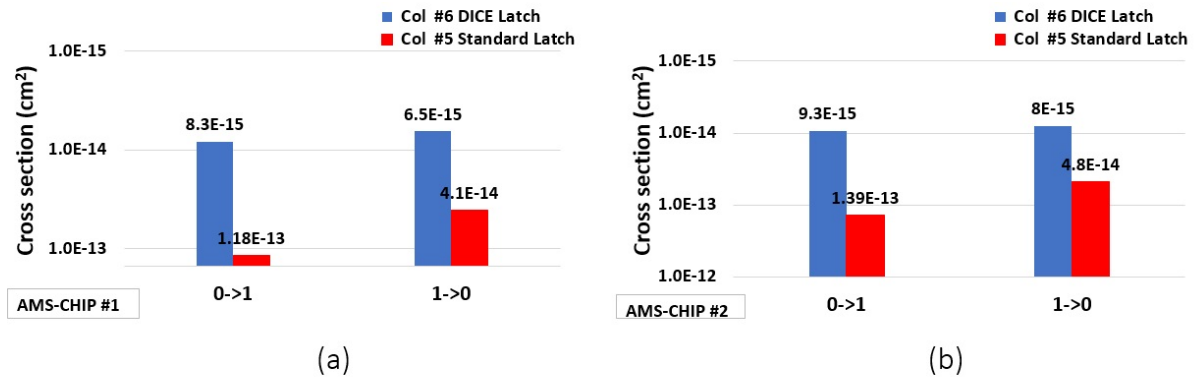


Figure 5.39. – Plot of mean dose rate versus time for the AMS SEU chip.

With the available statistics, the cross-section was calculated for all the structures implemented inside the chip. Figure 5.40 shows the cross-section plot for both chip 1 and chip 2. The DICE and standard latch have been tested with the bit-stream of all 0 and all 1. The cross-section of the proposed DICE latch is much lower than that of the standard latch. Furthermore, there is a difference of 35% in cross-section values for standard latch for both logic 0 and 1. Whereas, DICE latch is very homogeneous in this case. Figure 5.41 shows the plot of error rate [a]



(a) (b)

Figure 5.40. – Cross-section for all "0" and all "1" pattern for AMS chip 1 and chip 2.

per spill for both chip 1 and chip 2. The plot 5.40 shows that the proposed DICE latch is 15 times more SEU tolerant when compared to the standard latch. This is due to the structure and the separation of 2 sensitive nodes shown in the layout of DICE latch.
Table 5.4 shows the comparison on mean time between 2 upsets (MTBU) for standard and DICE latch, an order of magnitude difference seen for both the chips. The value of MTBU is calculated using equation 5.1.

$$MTBU = \frac{A}{\sigma \times Hit\ rate_{L4} \times Total\ bits} \tag{5.1}$$

where A is the size of the final AMS-CMOS chip, expected hit rate for fifth layer (L4) is 3.5×10^7 pr/sec/cm^2.

Figure 5.42(a)(b) shows the cross-section plot and figure 5.43(a)(b) shows the error rate plot of three TRL versions for both chip 1 and chip 2. The value of the cross-section for TRL with standard latch is around 4500 times higher when compared with other two versions. This behaviour is observed in both the chips. After getting these cross-section values, this has raised our suspicion of a design

a. Ratio of total number of errors to total number of spills.

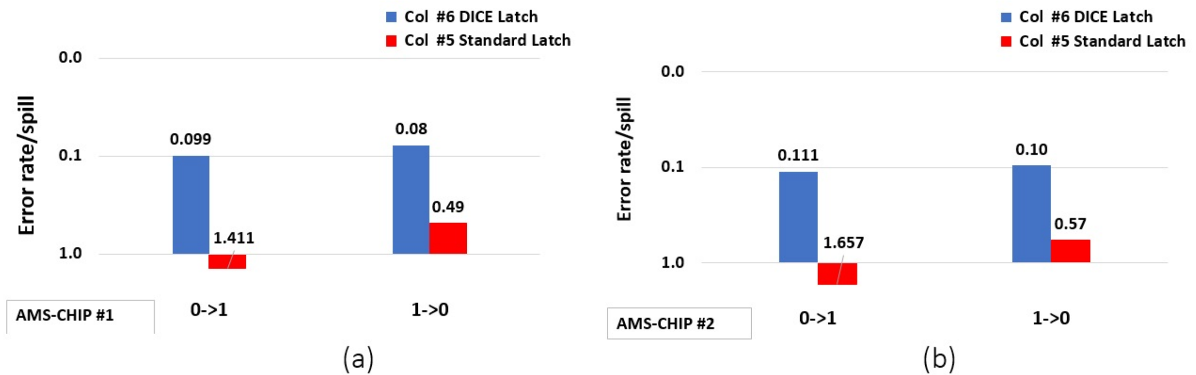


Figure 5.41. – Error rate per spill for all "0" and all "1" pattern for AMS chip 1 and chip 2.

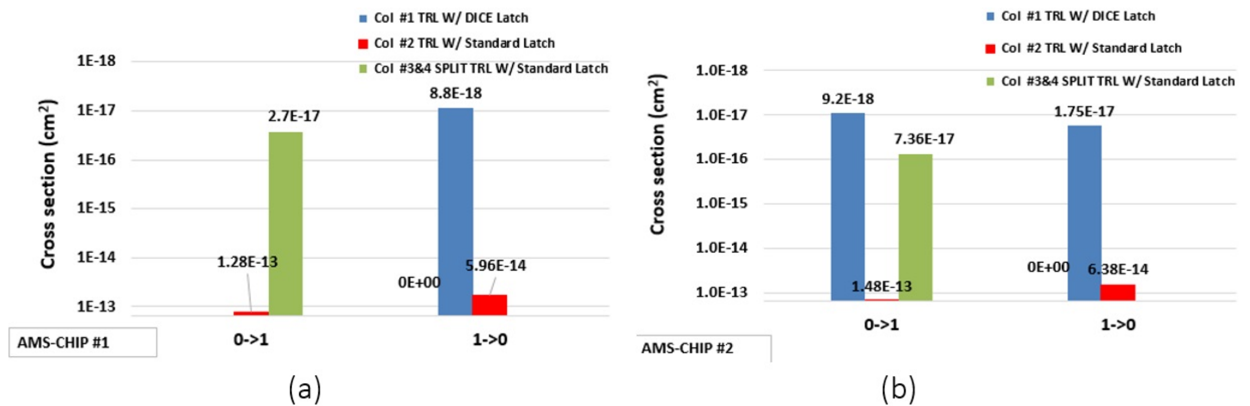
Table 5.4. – Comparison of mean time between two upsets for standard and DICE latch from AMS chip 1 and chip 2.

Structure	Estimated MTBU for chip 1	Estimated MTBU for chip 2
Standard Latch 0→1	3.4 sec	2.9 sec
Standard Latch 1→0	9.7 sec	8.3 sec
DICE Latch 0→1	48.1 sec	43.1 sec
DICE Latch 1→0	61 sec	49.7 sec

flaw. An explanation for the significant SEU rate observed on this structure is due to a schematic design. An inverter was missing after the first multiplexer in figure 5.2.2.3 which causes timing violations. This leads to change of input and the load signal for all three latches at the same time.

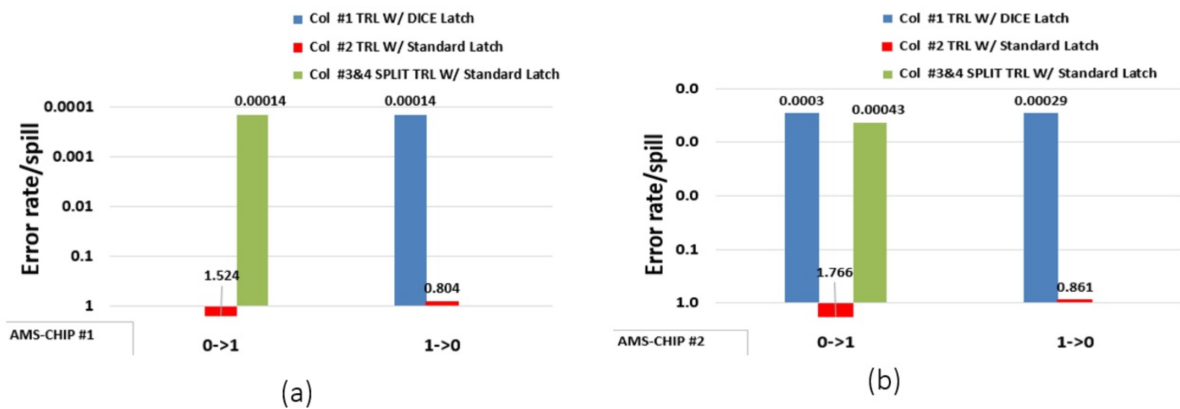
The other two structures, on the other hand, show good and stable performance under the beam. We could get very few errors (2-4) during whole campaign, which proves that the design is very robust to SEU.

The figure 5.43(a)(b) shows the plot for error rate per spill for TRL versions. From this we can see that TRL with DICE latches is very robust when compared to other two. Following these measurement results, SPLIT TRL with standard latch architecture can be implemented in the periphery for the final AMS CMOS-1 chip since and it would be only made of standard cells as it will be feasible from routing perspective. Table 5.5 shows the comparison on mean time between 2 upsets (MTBU) for all three TRL versions implemented inside the chip, an order of magnitude difference seen for both the chips. The value of MTBU is calculated using equation 5.1. Table 5.6 summaries the cross-section values and area for all the architectures implemented inside the AMS SEU test chip.



(a) (b)

Figure 5.42. – Cross-section for all "0" and all "1" pattern for TRL versions in AMS chip 1 and chip 2.



(a) (b)

Figure 5.43. – Error rate per spill for all "0" and all "1" pattern for TRL versions in AMS chip 1 and chip 2.

Figure 5.44 to figure 5.45 show the behaviour of every individual memory cell inside a 80 bit memory for different structures. These measurements are based on all "0" and all "1" pattern loaded to chip 1. From the figure 5.44 to figure 5.46, few things are common: firstly, we can see the number of errors inside the DICE latch are much less than standard latch and secondly, TRL with DICE latches and SPLIT with standard latches show positive results. Figure 5.47 and figure 5.48 illustrates the behaviour of each SEU tolerant structure for chip 2.

Table 5.5. – Comparison of mean time between two upsets for TRL versions from AMS chip 1 and chip 2.

Structure	Estimated MTBU for chip 1	Estimated MTBU for chip 2
TRL W/ DICE latch 0→1	-	12.1 hours
TRL W/DICE latch 1→0	12.7 hours	6.3 hours
SPLIT TRL W/ standard latch 0→1	4.1 hours	1.3 hours
SPLIT TRL W/ standard latch 1→0	-	-

Table 5.6. – SEU measurements for each architecture.

Cell	Area (μm^2)	$\sigma(0\to1)$	$\sigma(1\to0)$
Standard latch	24	1.39×10^{-13}	4.8×10^{-14}
DICE latch	34	9.3×10^{-15}	8×10^{-15}
TRL W/ standard latch	360	1.48×10^{-13}	6.3×10^{-14}
TRL W/ DICE latch	400	7.36×10^{-17}	0
SPLIT-TRL W/ standard latch	500	9.2×10^{-18}	1.75×10^{-17}

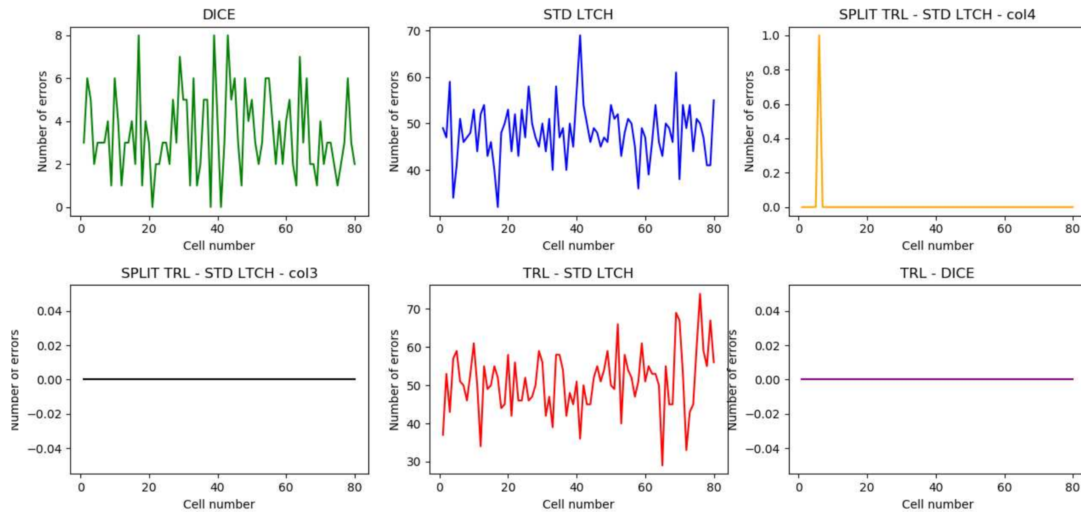


Figure 5.44. – Number of errors per cell for all "0" pattern inside the 80 bits latches from chip 1.

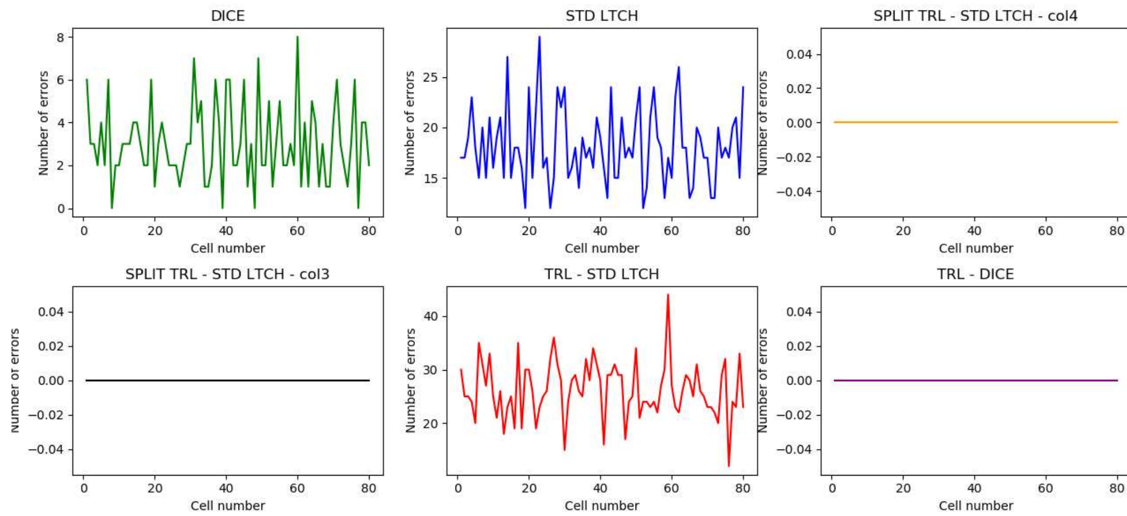


Figure 5.45. – Number of errors per cell for all "1" pattern inside the 80 bits latches from chip 1.

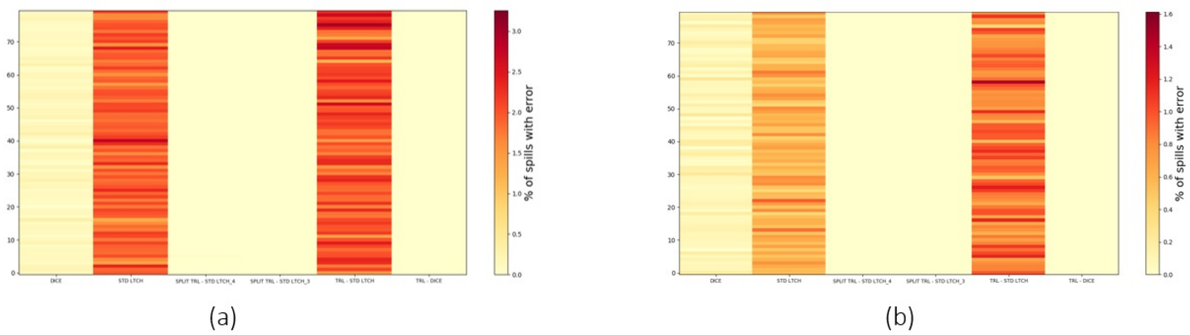


Figure 5.46. – 2-D map plot of number of spills (in percentage) with errors for all "0" and all "1" pattern for chip 1.

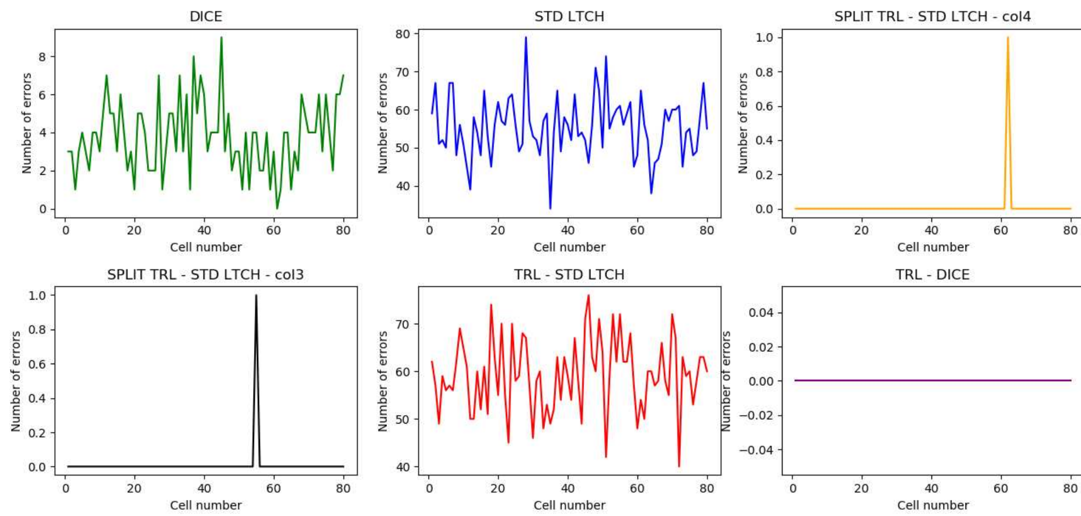


Figure 5.47. – Number of errors per cell for all "0" pattern inside the 80 bits latches from chip 2.

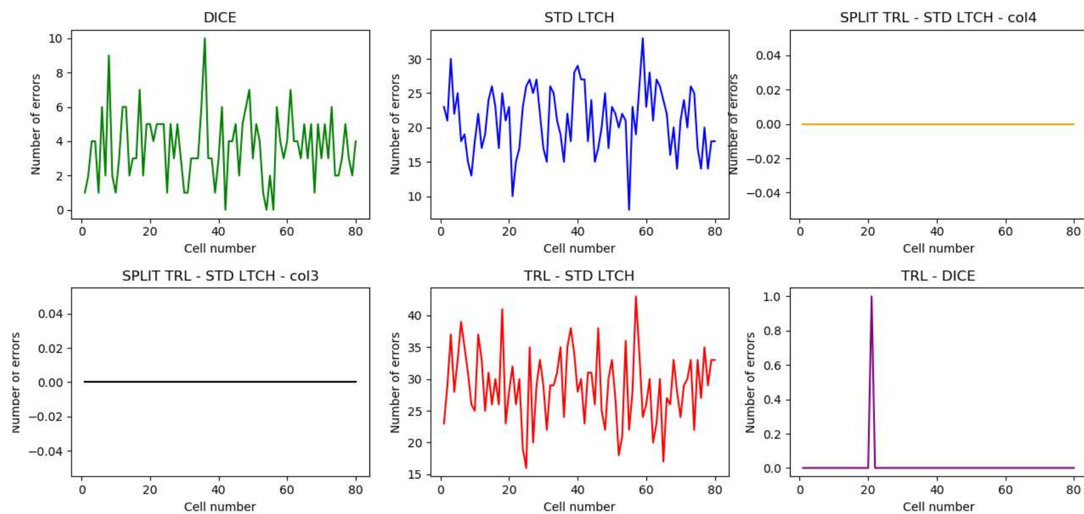


Figure 5.48. – Number of errors per cell for all "1" pattern inside the 80 bits latches from chip 2.

5.3. Radiation tolerant Single-Event Upset memories in TowerJazz 180 nm CMOS

Six different SEU tolerant structures were designed and fabricated in a modified TowerJazz 180 nm CMOS imaging technology. The SEU test chip was submitted in the MPW submission with other test chips in August 2018. The objective was to design different SEU structures and choose the best structure for the final TowerJazz chip and CMOS-1 chip which is dedicated to the environment of a pixelated layer in a high radiation collider environment.

5.3.1. Architecture of SEU tolerant chip

The architecture is similar to the architecture described in section 5.2. In this chip we have designed and implemented six different types of structures in six different columns. The chip is made of two parts, the first part known as core which consists of six columns with six different latch structures. The second part consists of the demultiplexer block which helps in selecting a particular column to be activated with various global signals (CLK, CLR, RB, Load, SRIN). The design of the demultiplexer is similar as implemented for AMS test-chip. The selection of these columns is also done in the same way by using the column address [2:0] which is chosen with the help of 3×8 decoder.

SEU-CORE matrix

The SEU core matrix is sub-divided into six different columns with six different structures of latches. The depth of the latches is 80 bits. The block diagram of various structures are sketched in figure 5.49. The different structures implemented in the core are :

1. Column 1 : TRL with DICE latch.
2. Column 2 : TRL with standard latch.
3. Column 3 : SPLIT TRL with standard latch.
4. Column 4 : SPLIT TRL with DICE latch.
5. Column 5 : Standard latch.
6. Column 6 : DICE latch.

5.3.2. Design of SEU hard memory cells in TowerJazz

In this section, a detailed description on the design with simulation results for the SEU tolerant memories in this technology will be discussed.

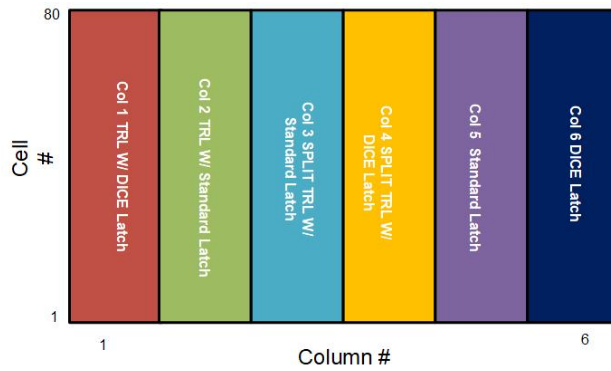


Figure 5.49. – Different structures inside the TowerJazz SEU tolerant test chip.

5.3.2.1. Design of a standard latch

The design of standard cell unit is similar to the design shown in figure 5.10. A standard latch used in standard cell unit is based on the transmission gates and other transistors discussed in section 5.2.2.1. To avoid any fan out issues, proper sized blocks were used from the TowerJazz standard library. The design and implementation of standard cell is very important since it gives the information about the radiation robustness of the technology.

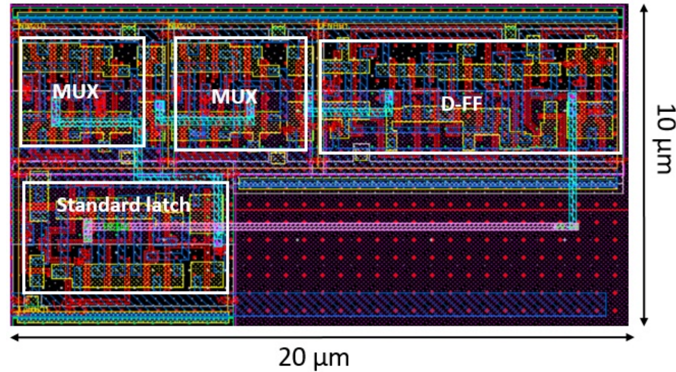


Figure 5.50. – Layout view of 1-bit standard cell unit.

In the simulation of the standard latch design, there was a transient noticed up to an injected charge of 550 fC on the input node. From the simulations, the Q_{crit} is around 550 fC which is larger than in AMS standard cell design. Figure 5.51 shows the simulation response of 1-bit standard cell for logic 0.

The layout view of the standard cell unit for 80 bit is shown in figure 5.52. The size of this matrix is 260 μm $\times$ 120 μm which is less than the layout shown in figure 5.14.

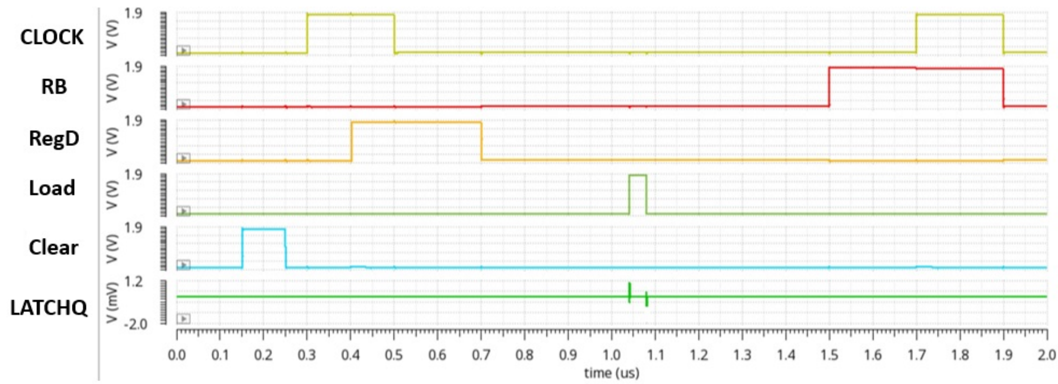


Figure 5.51. – Simulation of 1-bit with standard cell unit for logic 0 as input.

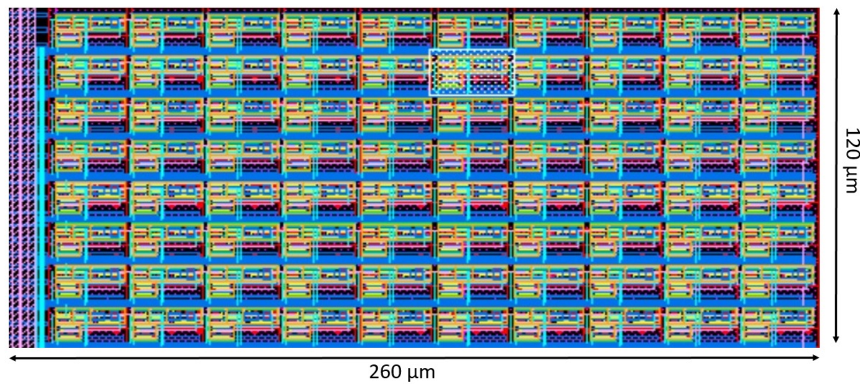


Figure 5.52. – Layout view of the 80 bits standard cell matrix.

5.3.2.2. Design of a DICE latch

The DICE cell was designed and implemented in the 6th column of the core-matrix. The goal was to design a robust and compact DICE cell in order to study the TowerJazz technology. The layout and schematic view of the DICE cell is illustrated in figure 5.53(a)(b) respectively. The size is 13.5 μm $\times$ 3.5 μm of the DICE cell. After studying and simulating the DICE cell at various process corners, it was concluded that it is better to design the cell slightly bigger so that there will be an increase in node capacitance. In this case, we injected a charge of 2.5 pC on X1 node. Whereas, to make it enough SEU tolerant we took the value of $Q_{crit.}$ to be 30 fC which is slightly higher than previous design in AMS technology. The design was furthermore made more tolerant to SEU by increasing the separation between the drains of the 2 NMOS transistors (MN1-MN3, MN2-MN4). The distance between them was increased from 3.5 μm to 5 μm when compared to AMS DICE cell. The switches (MN5-MN6, MN7-MN8) which are used to read and write in the DICE cell have been made slightly bigger

than other transistors used in the latch. The separation of these switches is also very important. This is because it was seen from the previous experience while making the FE-I4 chip that if there is a particle striking on the load signal then it may lead to SET. In this layout, these switches are placed in two ends with an increased distance of 14μm. A lot of bulk contacts are added so that the cell is immune to SEL and has a good performance under the beam. The design was simulated and verified at different process corners, supply voltages variations and different temperatures (PVT) with monte-carlo simulations.

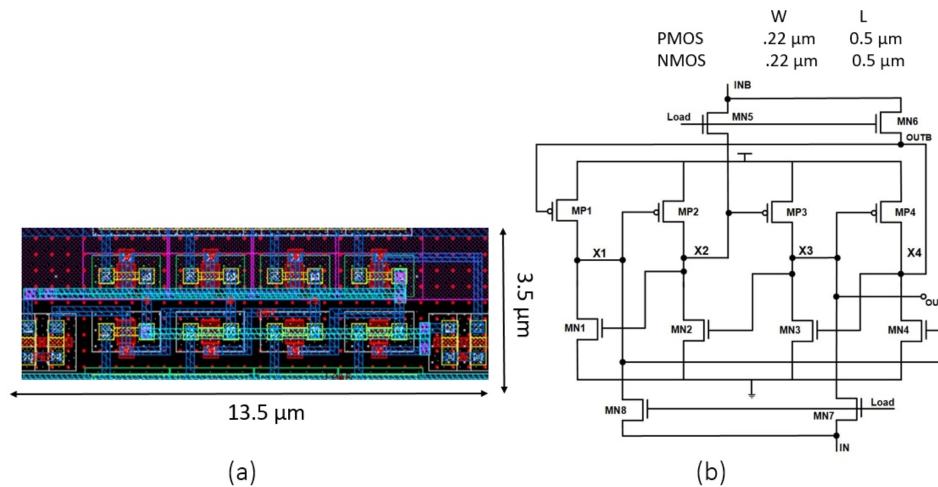


Figure 5.53. – (a) Layout of 1-bit DICE latch. (b) Schematic view of 1-bit DICE latch.

Figure 5.54 illustrates the layout of 1-bit DICE cell unit. The layout area of the whole DICE cell unit is 20 μm $\times$ 10 μm which is more compact to the previous layout as shown in figure 5.16.

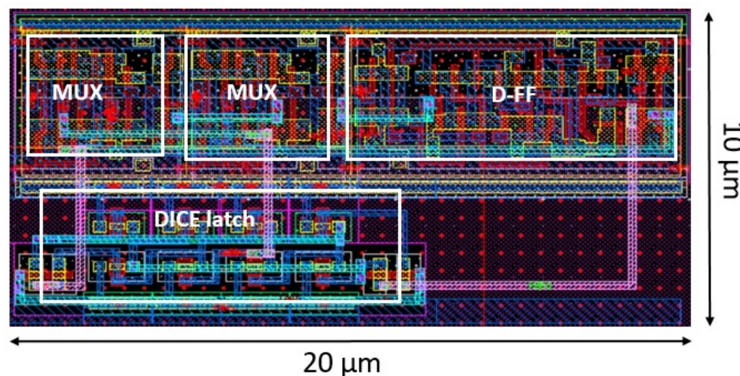


Figure 5.54. – Layout view of 1-bit DICE cell unit.

The simulation result of 1-bit DICE cell unit for logic 0 in TowerJazz technology is shown in figure 5.55.

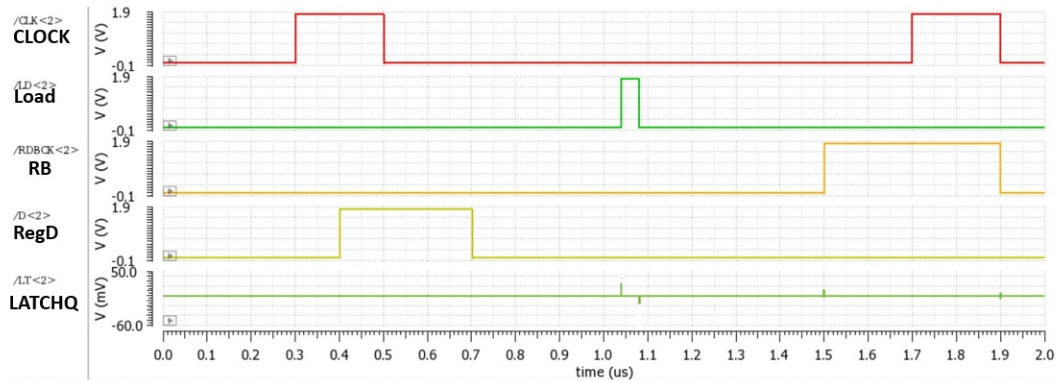


Figure 5.55. – Simulation of 1-bit with DICE cell unit for logic 0 as input.

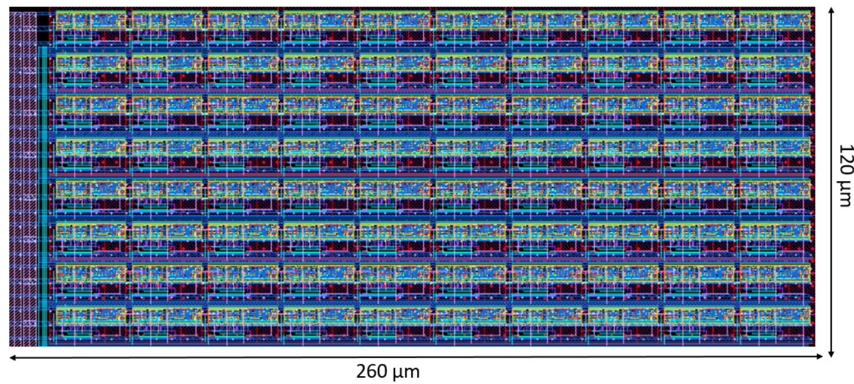


Figure 5.56. – Layout view of the 80 bits DICE cell matrix.

The figure 5.56 shows the layout view of the DICE matrix inside the Deep NWELL. The size of the matrix is 260 μm $\times$ 120 μm which is much more compact than the AMS layout as shown in figure 5.19.

5.3.2.3. Triple Redundancy Logic (TRL) with standard latches

TRL with standard cells is also implemented in the TowerJazz SEU chip as previously done for AMS test-chip. The block diagram of 1-bit TRL with standard cells unit is similar as for the AMS test-chip as sketched in figure 5.20. The internal block diagram of 1-bit TRL block also similar to the AMS test-chip as sketched in figure 5.22. The layout of the 1-bit TRL with standard cells unit block is shown

in figure 5.57. To make the structure more SEU tolerant, the distance between the two sensitive nodes was increased to 8.2 μm from 7 μm (previously used in AMS prototype) in the layout. Figure 5.58 shows the simulation response of 1-bit TRL with standard cells for logic 0. The figure 5.59 shows the layout view of the TRL with DICE cells matrix inside the Deep NWELL. The size of the matrix is 550 μm $\times$ 130 μm.

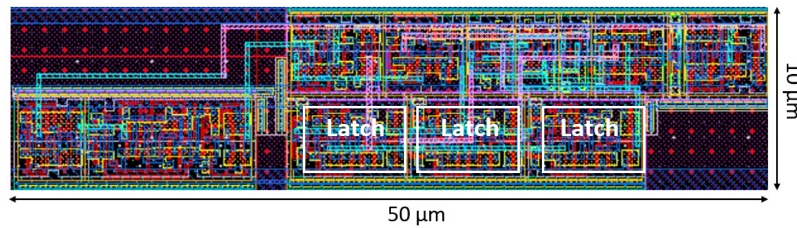


Figure 5.57. – Layout view of 1-bit Triple Redundancy Logic (TRL) with standard cells.

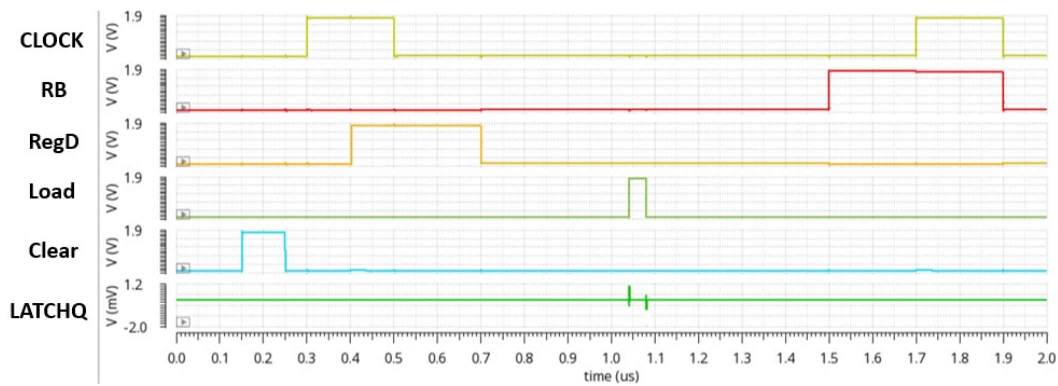


Figure 5.58. – Simulation of 1-bit Triple Redundancy Logic (TRL) with standard cells for logic 0 as input.

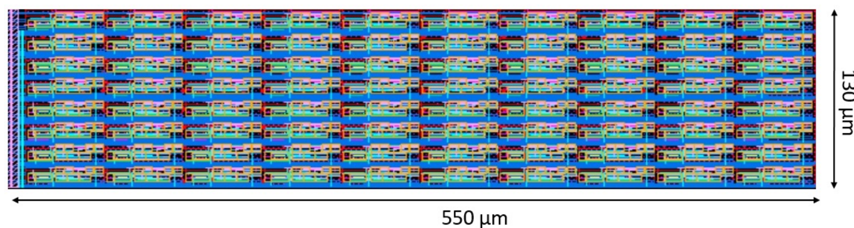


Figure 5.59. – Layout view of the 80 bits TRL with standard cell matrix.

5.3.2.4. Triple Redundancy Logic (TRL) with DICE latches

The basic implementation of this design has been described in section 5.2.2.4. After designing this structure in the AMS technology, it is implemented in column 4 of the TowerJazz SEU test chip. The block diagram of TRL with DICE cells is the same as on the figure 5.25. The size of 1-bit TRL with DICE cells in TowerJazz is 40 μm $\times$ 10 μm. In the layout, to make the memory more tolerant to SEU, the distance between the sensitive nodes have been increased to 15 μm from 14 μm which was previously used in the AMS test chip.

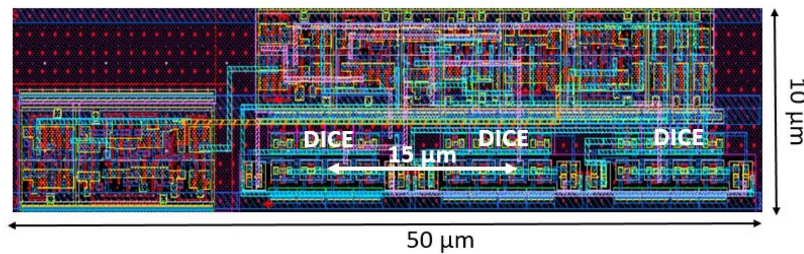


Figure 5.60. – Layout view of 1-bit Triple Redundancy Logic (TRL) with DICE latches.

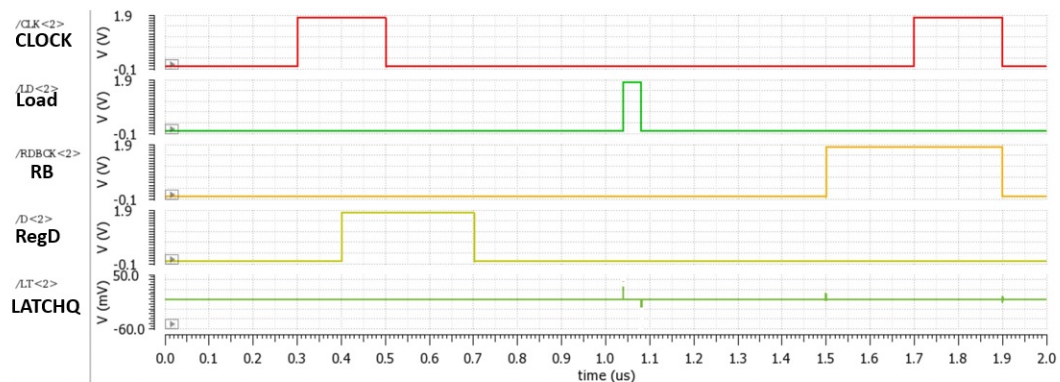


Figure 5.61. – Simulation of 1-bit Triple Redundancy Logic (TRL) with DICE latch for logic 0 as input.

Figure 5.61 shows the simulation response of 1-bit TRL DICE latch for logic 0. The figure 5.62 shows the layout view of the TRL with DICE latch matrix inside the Deep NWELL. The size of the matrix is 640 μm $\times$ 130 μm. The design was simulated and verified at different process corners, supply voltages variations and different temperatures (PVT) with monte-carlo simulations.

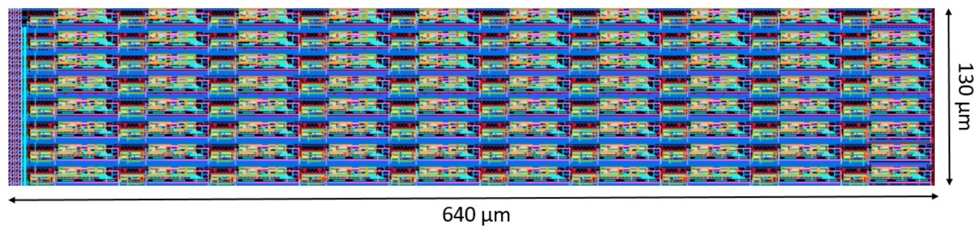


Figure 5.62. – Layout view of the 80 bits Triple Redundancy Logic (TRL) with DICE latch matrix.

5.3.2.5. SPLIT Triple Redundancy Logic (TRL) with standard latches

After implementing this structure previously in AMS, a similar study and implementation of this structure was also done in TowerJazz. The schematic of this structure is similarly as discussed in section 5.2.2.5. The idea is to increase the distance of the sensitive nodes by placing one standard latch far from the other latches. The layout view of 2 bits SPLIT TRL with standard cell is shown in figure 5.63. The size of this latch is 115 μm $\times$ 10 μm similar to the AMS prototype. The only difference comes in the layout, where the distance between the sensitive nodes have been increased to 65μm from 50μm while keeping the cell compact.

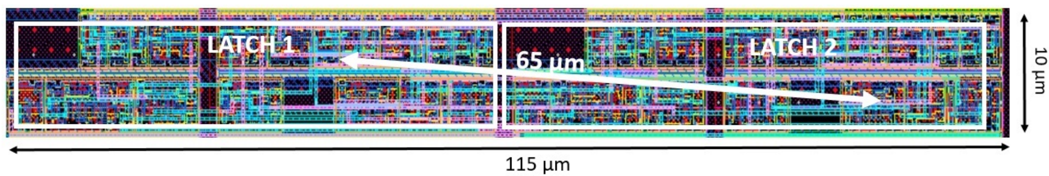


Figure 5.63. – Layout view of 2-bits SPLIT Triple Redundancy Logic (TRL) with standard latches.

The simulation response for logic "01" at the input is shown in figure 5.64. The layout view of 80 bits SPLIT TRL with DICE latches are shown in figure 5.65. The size of whole matrix is 640 μm $\times$ 130 μm.

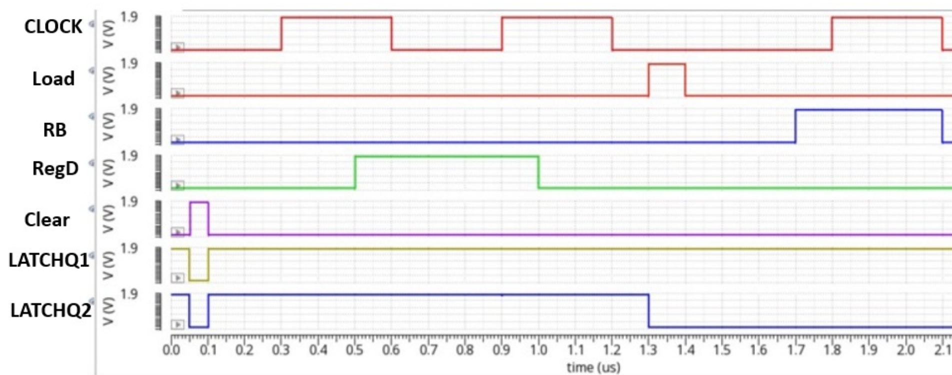


Figure 5.64. – Simulation of 2-bits SPLIT Triple Redundancy Logic (TRL) with standard latches for logic 01 as input.

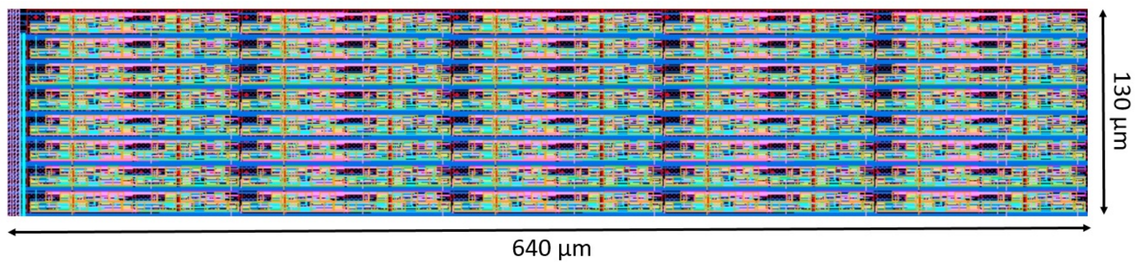


Figure 5.65. – Layout view of the 80-bits SPLIT Triple Redundancy Logic (TRL) with standard cells matrix.

5.3.2.6. SPLIT Triple Redundancy Logic (TRL) with DICE latches

This is the fourth version of TRL which is designed and implemented in the TowerJazz SEU chip. In a 1-bit SPLIT TRL version, one of DICE latch out of three latches is placed far from the other two. The block diagram of 2 bits-SPLIT TRL with latches in sketched in figure 5.66.

The function of this version is same as discussed in section 5.2.2.5. Figure 5.67 shows the schematic diagram of 1-bit SPLIT TRL with DICE latches. We know the DICE latch is more tolerant than the standard latch, therefore we expect this type of structure to be more tolerant to SEU when compared to SPLIT TRL with standard latch. Furthermore, to make it more tolerant by design, the separate load signals are used to trigger the respective DICE latch inside the memory. Figure 5.68 shows the layout of the 2 bit SPLIT TRL with DICE latches. The size of this latch is 125μm $\times$ 10μm with the separation of 65 μm between the two sensitive nodes.

The simulation response for logic "01" at the input is shown in figure 5.69. The layout view of 80 bits SPLIT TRL with DICE latches are shown in figure 5.70. The

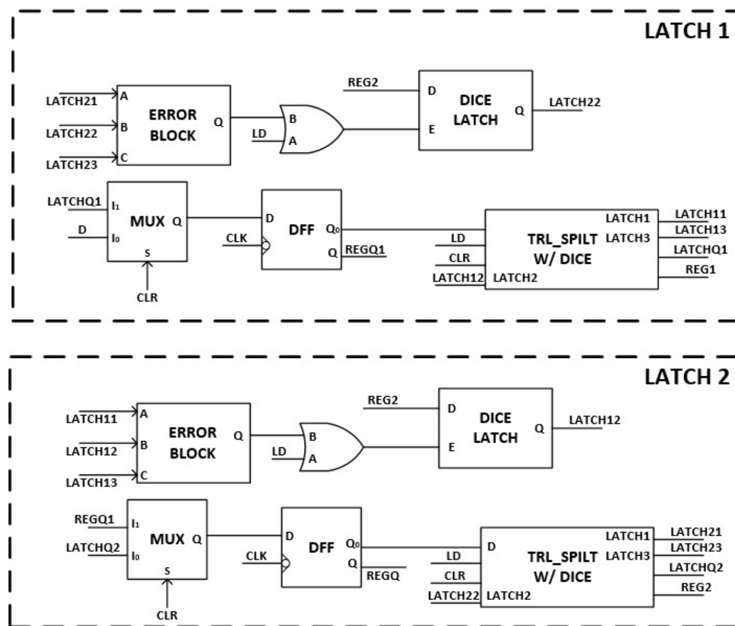


Figure 5.66. – Block diagram of 2 bits SPLIT Triple Redundancy Logic (TRL) with DICE latches.

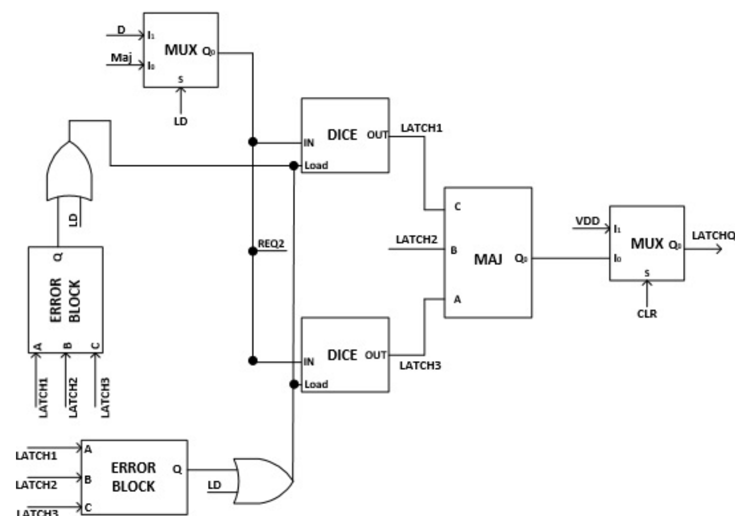


Figure 5.67. – Schematic diagram of 1-bit SPLIT Triple Redundancy Logic (TRL) with DICE latches.

size of whole matrix is 640 μm $\times$ 130 μm. The design was simulated and verified at different process corners, supply voltages variations and different temperatures (PVT) with monte-carlo simulations.

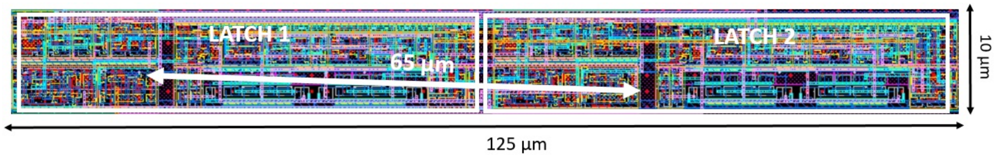


Figure 5.68. – Layout view of 2 bits SPLIT Triple Redundancy Logic (TRL) with DICE latches.

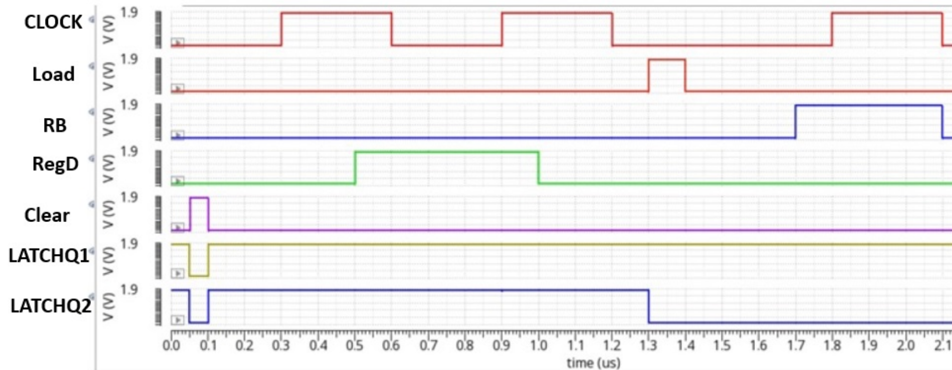


Figure 5.69. – Simulation of 2-bits SPLIT Triple Redundancy Logic (TRL) with DICE cells for logic 01 as input.

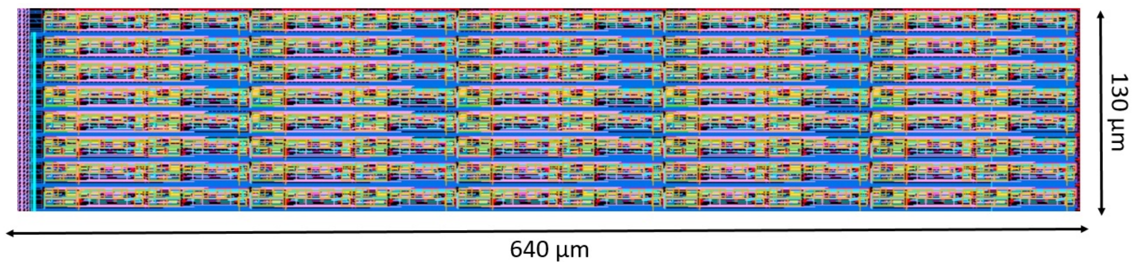


Figure 5.70. – Layout view of the 80-bits SPLIT Triple Redundancy Logic (TRL) with DICE cells.

5.3.3. ASIC layout

The TowerJazz SEU tolerant test chip has been submitted to the foundry for fabrication in a CMOS 180 nm technology in August 2018. The total chip size is 1 mm × 1.3 mm and the layout is shown in figure 5.71. The chip contains six columns with 80 bits in each column. There are in total 12 pads located inside the chip. These pads are listed in Table 5.7. The core is powered at 1.8 V.

Table 5.7. – TowerJazz SEU tolerant test chip pads list

Pad	Name	I/O	Function	Comments
1	VDD	Supply	1.8 V	Core supply
2	GND	Supply	0 V	Core Supply
3	CMD0	Input	Column selector	Select the column by decoder
4	CMD1	Input	Column selector	Select the column by decoder
5	CMD2	Input	Column selector	Select the column by decoder
6	SUB	Input	Readback	Connect to 0 V
7	CLR	Input	Clear	Reset
8	RB	Input	Readback	Latches data loading in shift register
9	SRIN	Input	Data	Data input
10	LD	Input	Load	Data loading in latches
11	CLK	Output	Clock	Clock to load shift register
12	SROUT	Output	Data	Data output

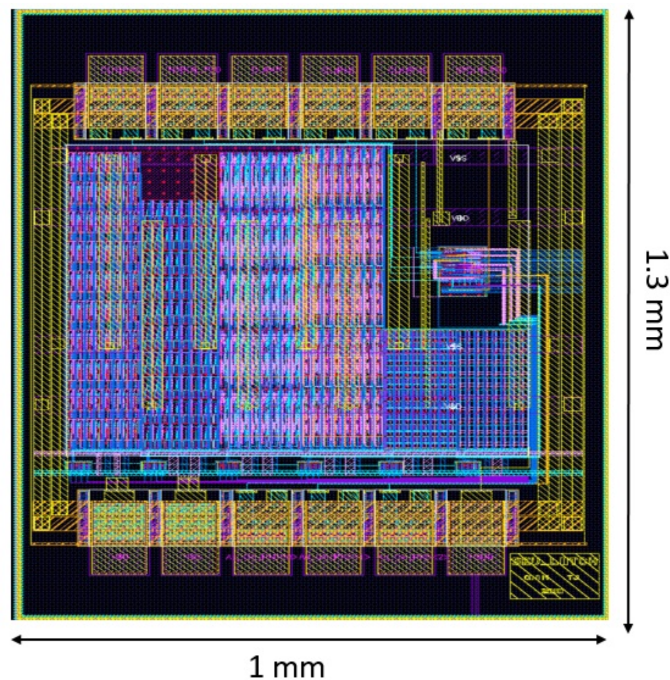


Figure 5.71. – TowerJazz SEU tolerant test chip layout. Different SEU tolerant architectures implemented as shown in figure 5.49.

5.3.4. Outlook

Five samples of the TowerJazz SEU tolerant test chip were received in February 2019. These samples were tested in the laboratory with three kinds of bit-stream: all-1s stream, all-0s stream, and "1010..-stream". All the columns in-

side the test chip were working correctly with different patterns. Two irradiation campaigns are planned in autumn of 2019 (after the time of writing of this document). The first campaign will take place at the University of Jyvaskyla for four days. The facility at the University of Jyvaskyla provides high penetration heavy-ion cocktail beams which are used for commercial services and academic research [118]. A second campaign is planned with protons and should take place at the KVI-Center for Advanced Radiation Technology (KVI-CART) [119] for one week. The primary energies of the proton are in the range of 40 to 190 MeV. After exposing the test chip at different facilities, cross-sections will be calculated for all the architectures and compared to the cross-sections results obtained with the AMS SEU tolerant test chip in AMS technology.

5.4. Radiation tolerant Single-Event Upset memories in LFoundry 150 nm CMOS

The experience gained from the two prototypes discussed in previous sections 5.2 and 5.3 has provided the guidelines to develop a new prototype in LFoundy 150 nm CMOS process. The complete design was motivated by two factors. Firstly, getting very promising test results under the proton beam from the AMS test-chip and secondly, as this technology is also considered for the environment of a pixelated layer in a high radiation collider environment. The design and optimization of SEU tolerant chip in LFoundry was the last part of this PhD work. In January 2019 the LFoundry SEU tolerant prototype, incorporating with different structures was submitted to the foundry for fabrication. This chapter describes in detail the design with simulation results.

5.4.1. Architecture of SEU tolerant chip

The architecture of SEU tolerant chip in LFoundry is almost similar to the architecture described in section 5.2.1. In this chip we have designed and implemented distinct structures in different columns. The chip consists of two parts, the first part known as core which consists of eight different structures. The second part consists of the demultiplexer block which helps in selecting a particular column to be enabled with various global signals (CLK, CLR, RB, Load, SIN). The design of the demultiplexer is similar as described for AMS and TowerJazz SEU test-chips but the logic to access columns have been changed. The selection of these columns is done with the help of 3×8 decoder block. Table 5.8 shows the column selection for different input combinations inside the decoder.

5.4.1.1. SEU-CORE matrix

The SEU core matrix is sub-divided into eight different columns with different structures of memories. The depth of each memory column is 80 bits and controlled by global signals. The block diagram of various structures are sketched in figure 5.72. There are two versions of the DICE latches and four versions of Triple Redundancy Logic inside the core matrix. The different structures implemented in the core are :

1. Column 1 : Standard latch.
2. Column 2 : DICE latch.
3. Column 3 : "Enhanced" DICE latch.
4. Column 4 : TRL with standard latch.
5. Column 5 : TRL with DICE latch.

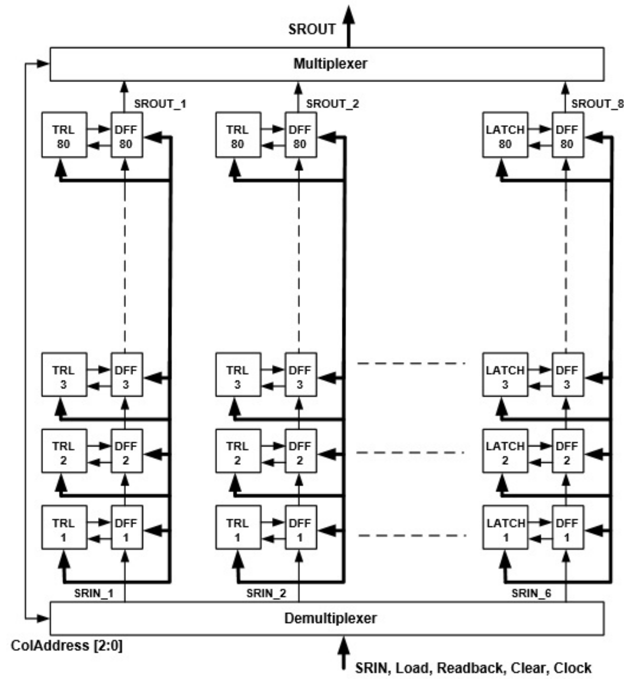


Figure 5.72. – Block diagram architecture of the SEU tolerant chip in LFoundry.

6. Column 6 : SPLIT TRL with standard latch.
7. Column 7 : SPLIT TRL with DICE latch.
8. Column 8 : Static Random Access Memory (SRAM)

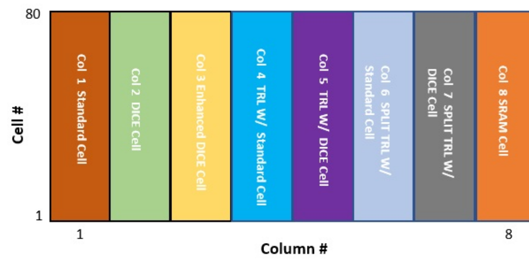


Figure 5.73. – Different structures inside the LFoundry SEU test chip.

Table 5.8. – Logic for column selection inside the decoder block for SEU core in LFoundry.

In <2>	In <1>	In <0>	OUT
0	0	0	OUT <1> column 1
0	0	1	OUT <2> column 2
0	1	0	OUT <3> column 3
0	1	1	OUT <4> column 4
1	0	0	OUT <5> column 5
1	0	1	OUT <6> column 6
1	1	0	OUT <7> column 7
1	1	1	OUT <8> column 8

5.4.2. Design of SEU hard memory cells in LFoundry

Eight different SEU tolerant structures were designed and fabricated in LFoundry 150 nm CMOS process. The objective was to design different SEU structures and choose the best structure for the final Lfoundry LF-CMOS chip. In this section, a detailed description of the design will be discussed along with the simulation results for SEU tolerant memories.

5.4.2.1. Design of a standard latch

A standard latch structure is based on the transmission gates and other transistors as discussed in section 5.2.2.1. To make the design more robust in all process corners, blocks with the minimum feature sizes of 150 nm have been selected from the standard library. The design and implementation of standard cell is very important since it tells about the radiation robustness of the technology. The figure 5.74 shows the layout of 1-bit standard cell unit. From the simulations, a transient was noticed with an injected charge of 1500 fC on the output node. The latch undergoes a SEU if more charge is injected. From this we could conclude that the Q_{crit} is around 1500 fC for the standard latch in this technology. This value gives an indication about the SEU robustness when compared to other two technologies discussed above. The Q_{crit} for AMS and TowerJazz standard latch is around 350 fC and 550 fC respectively.

The simulation result of 1-bit standard cell unit in LFoundry CMOS the logic 0 is shown in Figure 5.75. Figure 5.76 shows the layout of the 80-bits standard cell matrix. The size of this matrix is 300 μm $\times$ 130 μm.

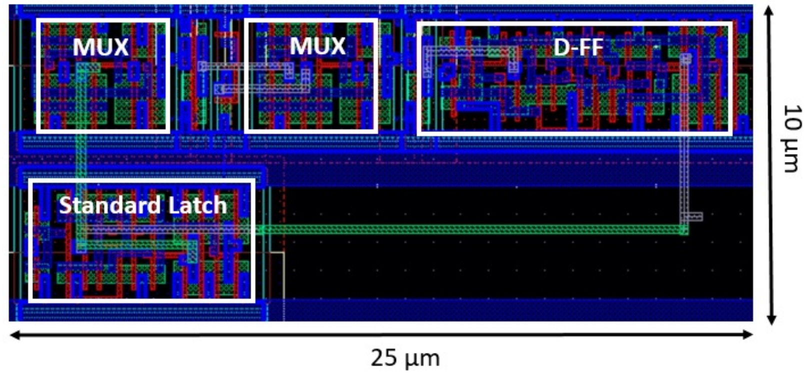


Figure 5.74. – Layout view of the 1-bit standard cell unit.

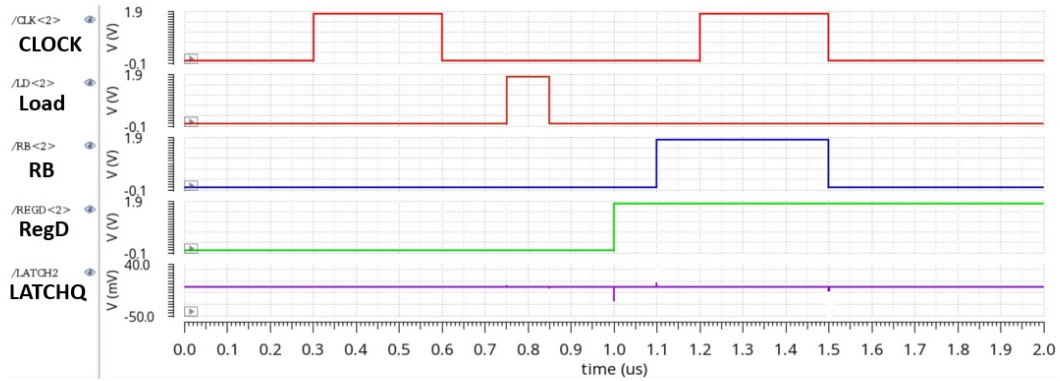


Figure 5.75. – Simulation 1-bit with standard cell unit for logic 0 as input.

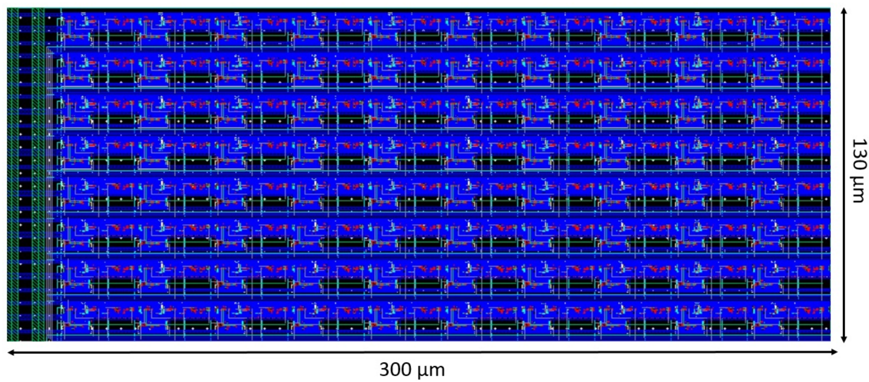


Figure 5.76. – Layout view of the 80-bits standard cell matrix.

5.4.2.2. Design of a DICE latch

The first version of DICE cell was designed and implemented in the 2nd column of the core-matrix. The goal was to design a robust and compact DICE cell in order to study the LFoundry technology. The layout and schematic view of the DICE cell is illustrated in figure 5.77(a)(b) respectively. The size of 1-bit DICE cell is 8 μm $\times$ 4 μm. Proper sizing of the transistors inside the DICE latch was made after studying and simulating the cell at various process corners. Whereas, to make it SEU tolerant we took the value of $Q_{crit.}$ equal to 30 fF. The distance between the two sensitive nodes was taken to be 2.5 μm. The switches (MN5-MN6, MN7-MN8) which are used to read and write in the DICE cell have the same size with the other transistors inside the latch. Figure 5.78 shows the layout of 1-bit DICE cell unit in LFoundry.

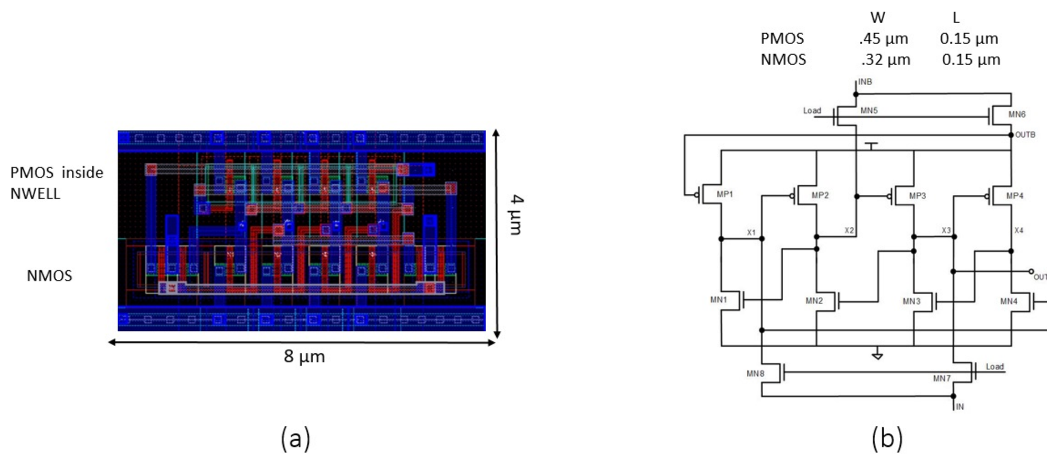


Figure 5.77. – (a) Layout view of 1-bit DICE latch. (b) Schematic view of 1-bit DICE latch.

The separation of these switches is also very important as discussed before. In the layout, the distance between the switches is kept around 7μm. Bulk contacts are added so that the cell is immune to SEL and have a good performance under the irradiation. The design was simulated and verified at different process corners, supply voltage variations and temperatures (PVT) with monte-carlo simulations.

The simulation result of 1-bit DICE latch unit in LFoundry CMOS with logic 0 is shown in figure 5.79.

Figure 5.80 shows the layout of the 80-bits DICE latch unit. The dimensions of the DICE matrix is 300 μm $\times$ 130 μm.

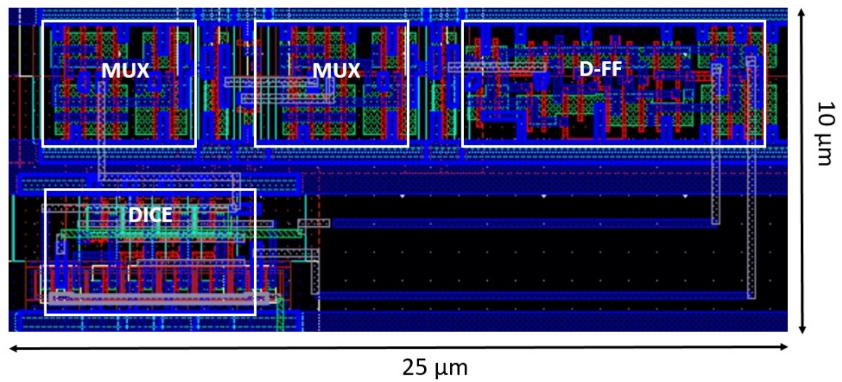


Figure 5.78. – Layout view of 1-bit DICE latch unit.

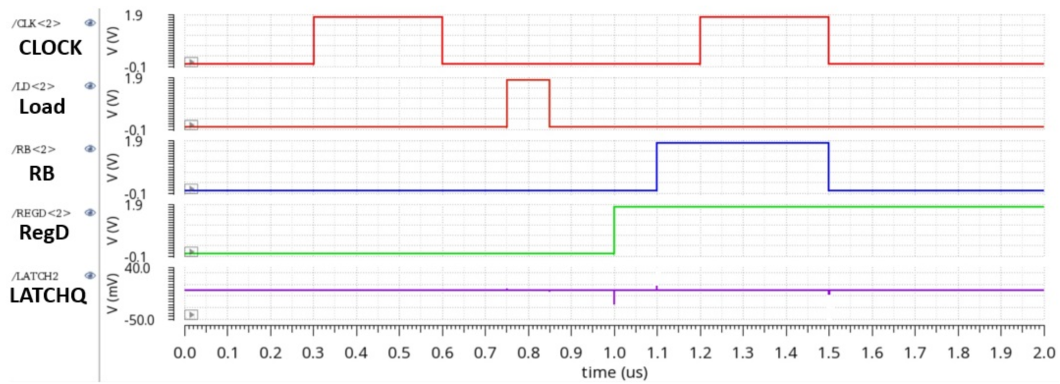


Figure 5.79. – Simulation of 1-bit DICE cell unit for logic 0 as input.

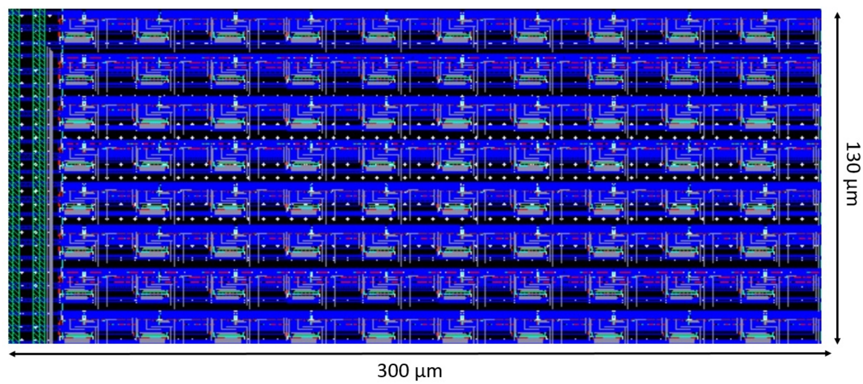


Figure 5.80. – Layout view of the 80-bits DICE cell matrix.

5.4.2.3. Design of "enhanced" DICE latch

This is the second version of the DICE latch implemented in the test-chip. The reason of implementing this version was to compare the performance with the first version of DICE and SRAM cell. In this version, the sizes of the transistors are kept same as in the first version with only difference is the distance between the two sensitive nodes was increased from 2.5 μm to 5.5 μm. Moreover, by increasing the distance, the separation between the switches are is also increased. The overall layout of this version is very compact with the size of 11 μm $\times$ 4 μm. Figure 5.81 shows the layout of 1-bit DICE cell unit with "enhanced" DICE latch.

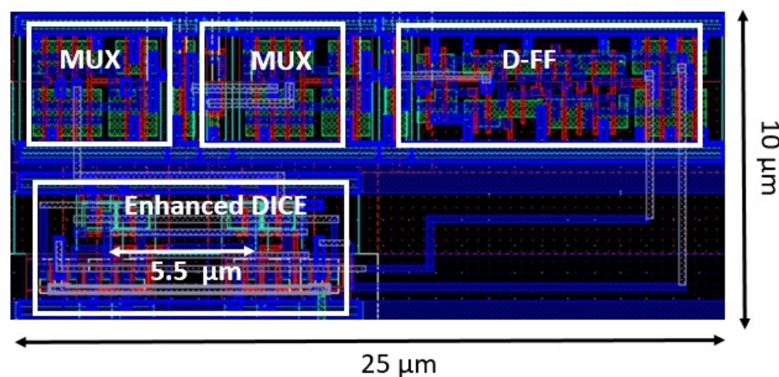


Figure 5.81. – Layout view of 1-bit DICE cell unit with "enhanced" DICE latch.

5.4.2.4. Triple Redundancy Logic (TRL) with standard latches

The first version of TRL is made with standard cells only, similar as implemented for AMS, TowerJazz technologies. This structure is placed in the 4th column inside the core matrix. The block diagram of 1-bit TRL with standard cells unit is sketched in figure 5.20. Inside the TRL-Latch block, three standard latches are connected in parallel and their output is fed as in input to the majority block as discussed in above section. To make the design more tolerant to SEU, triplication of load signals is done corresponding to the three standard latches. The internal block diagram of 1-bit TRL block is sketched in figure 5.82.

The distance between two sensitive nodes was kept around 9 μm. The size of the 1-bit TRL with standard cells is 40 μm $\times$ 10 μm and the layout is shown in Figure 5.83.

The simulation result of 1-bit TRL with standard cells for logic is shown in figure 5.84. The layout of the 80-bits TRL with standard latches unit is shown in Figure 5.85. The dimensions of the matrix is 600 μm $\times$ 130 μm. The whole matrix is inside the Deep NWELL.

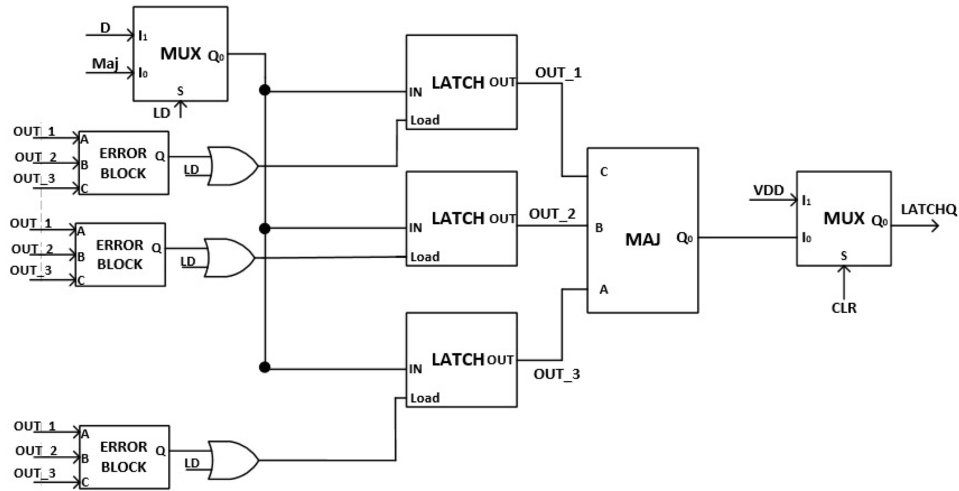


Figure 5.82. – Block diagram of 1-bit Triple Redundancy Logic (TRL) with standard latches.

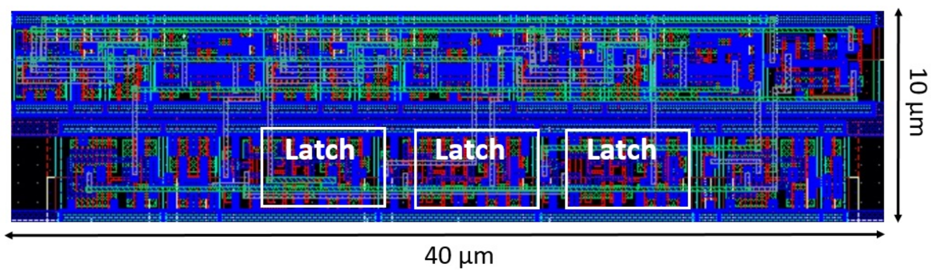


Figure 5.83. – Layout view of 1-bit Triple Redundancy Logic (TRL) with standard latches.

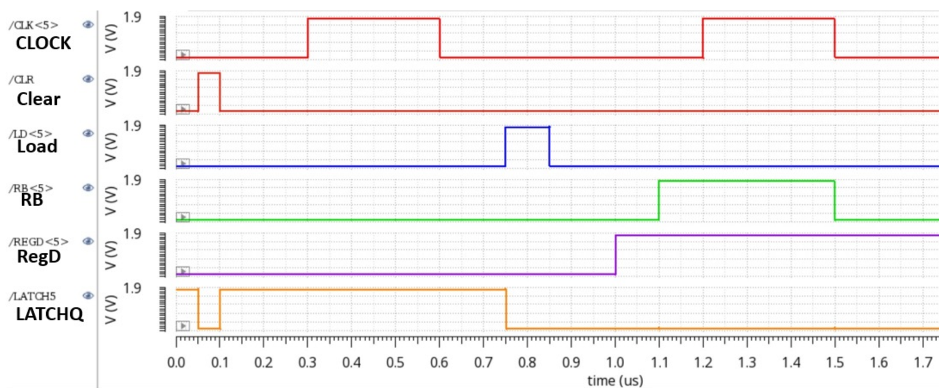


Figure 5.84. – Simulation result of 1-bit Triple Redundancy Logic (TRL) with standard latches for logic 0 as input.

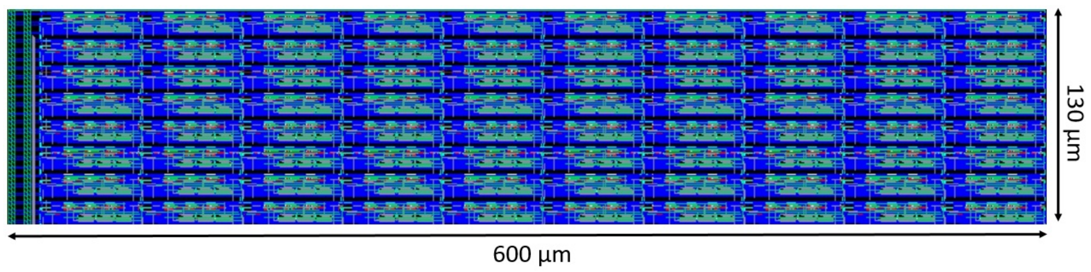


Figure 5.85. – Layout view of the 80-bits Triple Redundancy Logic (TRL) with standard latches matrix.

5.4.2.5. Triple Redundancy Logic (TRL) with DICE latches

TRL with DICE latches is implemented in this prototype as well. This structure is placed in the 5th column inside the core matrix. The block diagram of 1-bit TRL with DICE latches unit is shown in figure 5.25. Inside the TRL-DICE block, three DICE latches are connected in parallel and their output is fed as input to the majority block. To make the design more tolerant to SEU, three self correction error blocks is designed which means that DICE latches will be triggered with independent load signals. The block diagram of 1-bit TRL DICE latches is sketched in figure 5.86, keeping the same area as shown in the AMS test chip design. The distance between the two sensitive nodes was kept around 11 μm. The size of 1-bit TRL with DICE latches in LFoundry is 40 μm $\times$ 10 μm and the layout is shown in Figure 5.87.

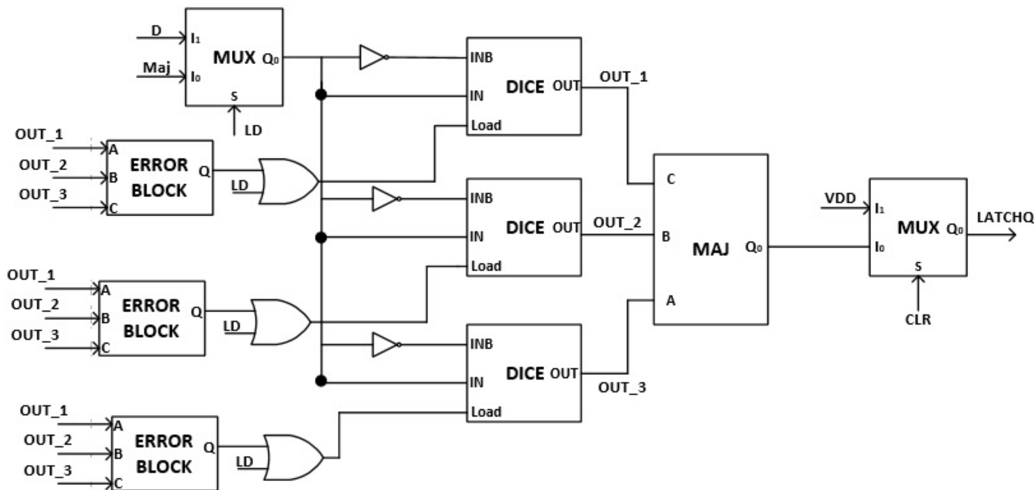


Figure 5.86. – Block diagram of 1-bit Triple Redundancy Logic (TRL) with DICE latches.

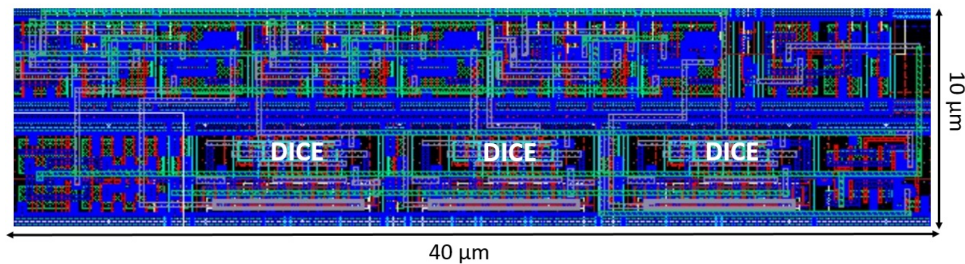


Figure 5.87. – Layout view of 1-bit Triple Redundancy Logic (TRL) with DICE latches.

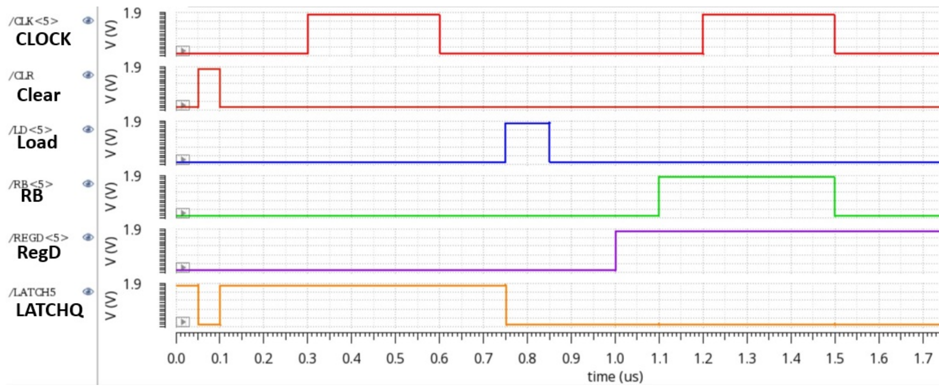


Figure 5.88. – Simulation result of 1-bit Triple Redundancy Logic (TRL) with DICE latch for logic 0 as input.

The simulation result of 1-bit TRL DICE latch unit for logic 0 is shown in figure 5.88. Figure 5.89 shows the layout of 80-bits TRL with DICE latch unit. The dimensions of the whole matrix is 600 μm $\times$ 130 μm.

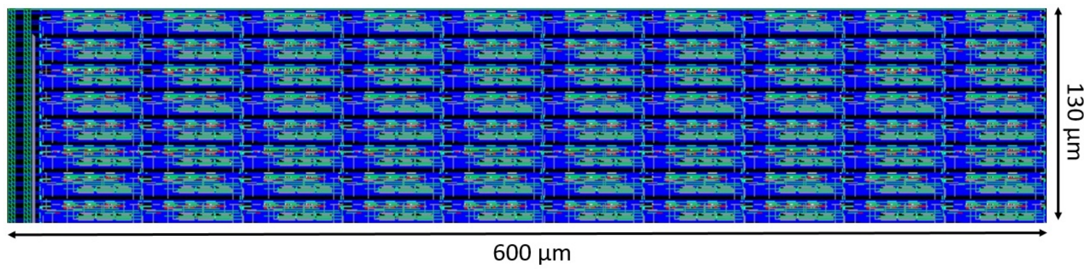


Figure 5.89. – Layout view of the 80-bits Triple Redundancy Logic (TRL) with DICE latches matrix.

5.4.2.6. SPLIT Triple Redundancy Logic (TRL) with standard latches

After implementing this structure previously in AMS and TowerJazz, a similar study and implementation of this structure was also done in LFoundry. The schematic of this structure is similarly as discussed in section 5.2.2.5. The idea is to increase the distance of the sensitive nodes by placing one standard latch far from the other latches. The layout view of 2 bits SPLIT TRL with standard cell is shown in figure 5.90. The size of this latch is similar to the AMS prototype. From the test results discussed in section 5.2.6, this architecture showed very encouraging performance.

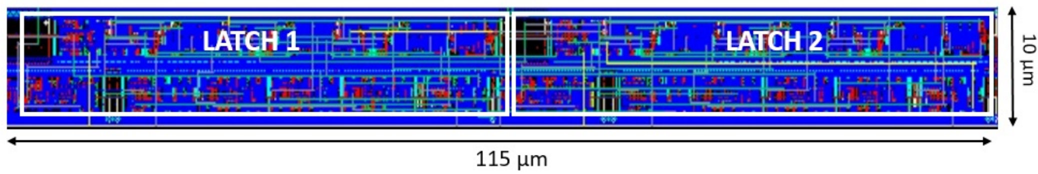


Figure 5.90. – Layout view of 2-bits SPLIT Triple Redundancy Logic (TRL) with standard cells.

The simulation response for logic "01" at the input is shown in figure 5.91. The layout view of the 80 bits SPLIT TRL with standard latches is shown in figure 5.92. The size of whole matrix is 600 μm $\times$ 130 μm.

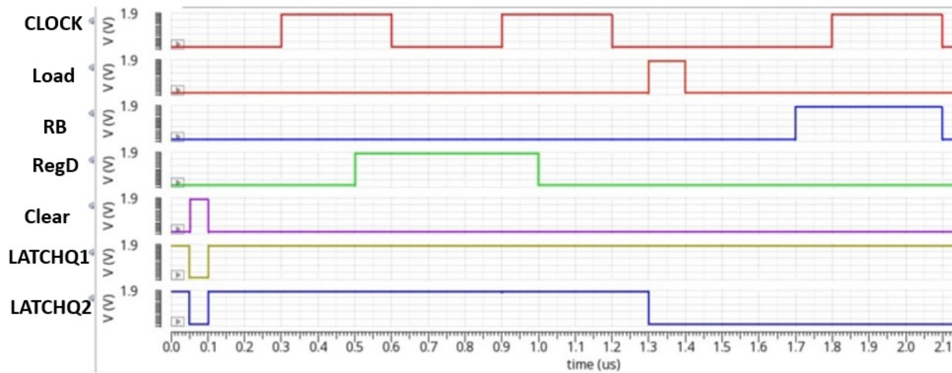


Figure 5.91. – Simulation of 2-bits SPLIT-TRL with standard cells for logic 01 as input.

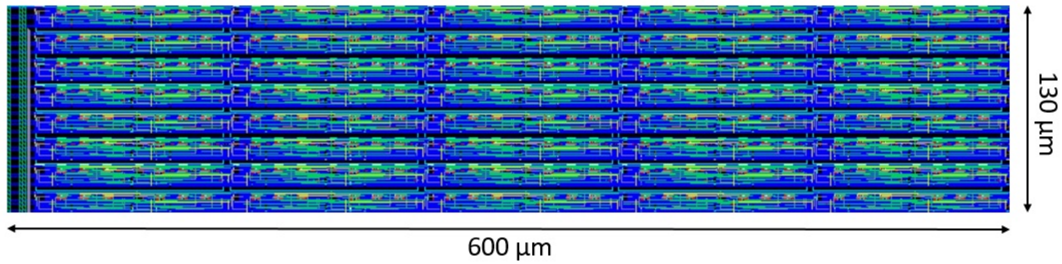


Figure 5.92. – Layout view of the 80-bits SPLIT Triple Redundancy Logic (TRL) with standard cells matrix.

5.4.2.7. SPLIT Triple Redundancy Logic (TRL) with DICE latches

The structure of SPLIT TRL with DICE latches has been designed and implemented in LFoundry also. The schematic of this structure is the same as discussed in section 5.3.2.6. The idea is to increase the distance of the sensitive nodes by placing one DICE latch far from the other two DICE latches. The size of 2 bits SPLIT TRL with DICE cell is 115 μm $\times$ 10 μm and the layout view is shown in figure 5.93. The area of this latch is larger than the latch implemented in the TowerJazz prototype.

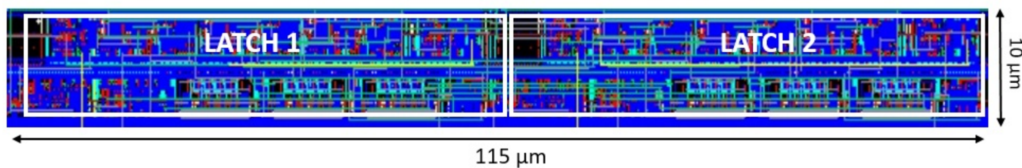


Figure 5.93. – Layout view of 2-bits SPLIT Triple redundancy logic (TRL) with standard latches.

The test results discussed in section 5.2.6 showed a very encouraging performance of the SPLIT TRL with standard latches in the AMS technology. However, we know that a DICE latch is nearly 10-15 times more SEU tolerant than a standard latch. Therefore, we could expect much better performance from this structure. The simulation response for logic "01" at the input is shown in figure 5.94. The layout view of 80 bits SPLIT TRL with DICE latches are shown in figure 5.95. The size of whole matrix is 600 μm $\times$ 130 μm.

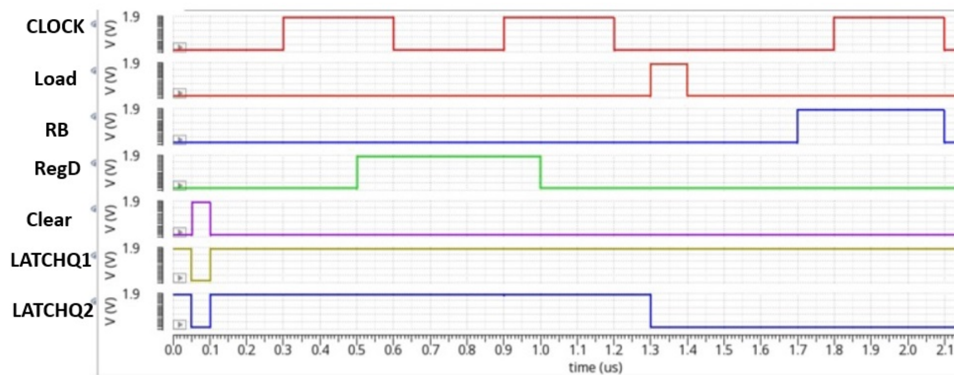


Figure 5.94. – Simulation of 2-bits SLIT-TRL with DICE cells for logic 01 as input.

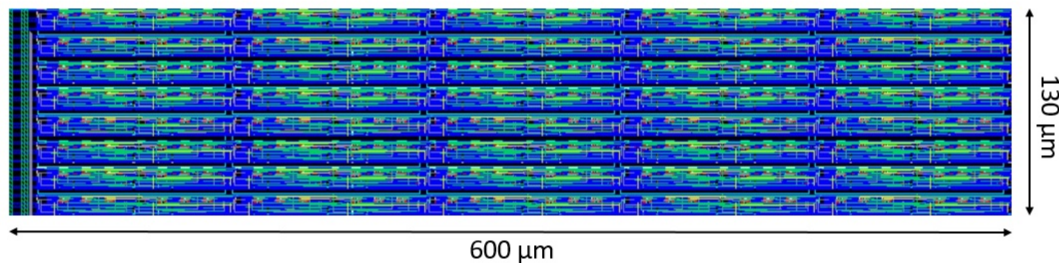


Figure 5.95. – Layout view of the 80-bits SPLIT Triple Redundancy Logic (TRL) with DICE latches matrix.

5.4.2.8. Design of SRAM cell

SRAM is also known volatile memory as it holds data as long as power is applied. From many decades this memory is also used in HEP applications since the memory size is very compact. Nevertheless, there are few drawbacks as the memory is not enough tolerant to SEU when compared to DICE cell. To make the memory more tolerant to SEU, several solutions have been proposed.
In LF-Monopix01 chip, the discriminator fires when the analog signal pulse is more than its threshold. Two gray encoded time stamps, corresponding to the leading edge (LE) and trailing edge (TE) of the discriminator output, are written into two in-pixel RAM cells to record the hit time and pulse width. The schematic and layout of the implemented SRAM cell is shown in figure 5.96. The study and SPICE simulations were done on this design which showed few drawbacks :

- The simulation results showed that the design is not enough robust in terms of SEU and is limited up to a charge of 500 fC on the sensitive nodes.
- In the layout the distance between the output nodes (OUT and OUTB) is very small.

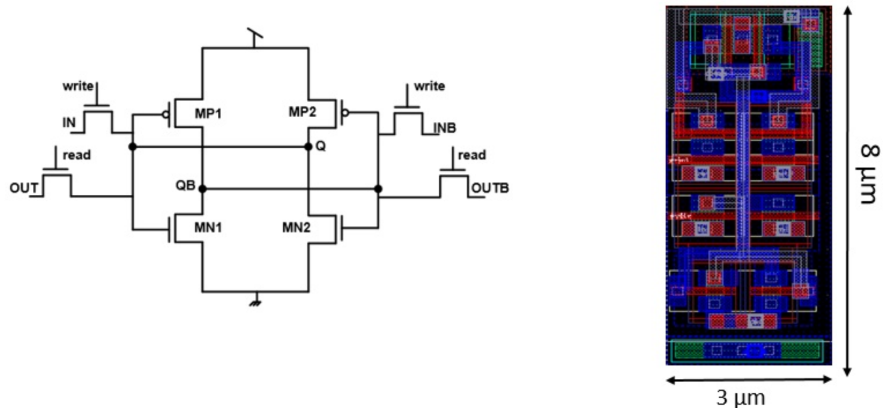


Figure 5.96. – Schematic of dual port SRAM cell inside the LF-Monopix01 chip (Left) and layout view of SRAM cell (Right).

In recent years, a new technique was developed to make the design more SEU tolerant. This technique is already discussed in section 5.1.3. A detailed study was made by injecting a very high charge of 2.5 pC on the sensitive node. The simulations were performed to verify that the memory works correctly in all design process corners. To make the memory tolerant to that value (we targeted 2.5 pC), a capacitor with a minimum value 1 pF was needed. This value of capacitor is not feasible to use inside the pixel because of the area constraints. Therefore, a new design was proposed in which the size of transistors were increased. This resulted in an increase of the area by a factor of 1.5 and making the memory tolerant up to 2.5 pC at all process corners. The major advantage of this design is that it is nearly 5 times more robust than the previous design. Since we have the same test setup as used to test the latches, the goal was to design a memory based on the test setup. This means we need to use the same global signals to perform read and write operations. The block diagram of 1-bit SRAM cell in LFoundry is sketched in figure 5.97. The schematic and layout view of 1-bit SRAM cell is shown in figure 5.98.

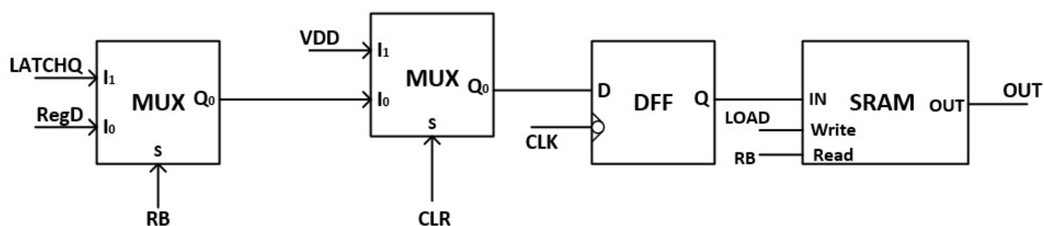


Figure 5.97. – Block diagram of a SRAM cell unit in Lfoundry with reading and writing signals.

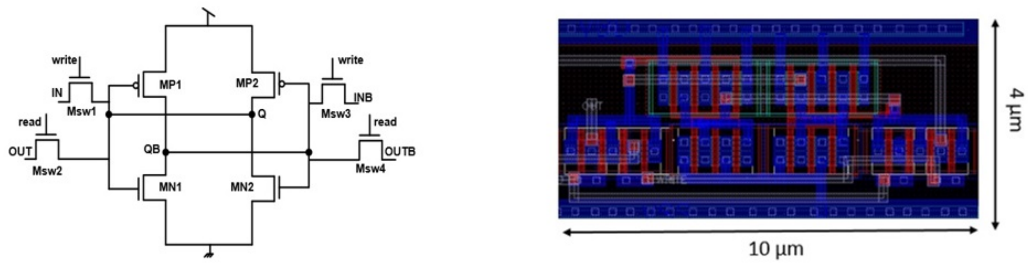


Figure 5.98. – Schematic and layout view of 1-bit SRAM cell in LFoundry.

With each SRAM cell, a sense amplifier is used which acts as a load. The sense amplifier is based on two cross-coupled inverters connected such that the output of one is connected to the input of other. The NMOS transistor M5 acts like a current source which is triggered by the read signal. The write operation is performed by enabling the NMOS transistors Msw1 and Msw3 using write signal. The schematic and the layout of the sense amplifier is shown in figure 5.99.

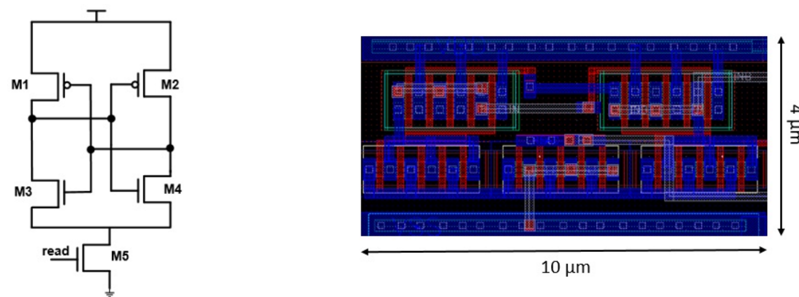


Figure 5.99. – Schematic and layout view sense amplifier acting as a load for SRAM cell.

The layout of the 80-bits SRAM cells matrix is shown in Figure 5.100. The dimensions of the matrix is 300μm $\times$ 130μm. The whole matrix is inside the Deep NWELL.

Table 5.9. – Transistor sizes in the SRAM memory cell

MOS	W (μm)	L (μm)
MP1	3.6	0.15
MP2	3.6	0.15
MN1	2.4	0.15
MN2	2.4	0.15
Msw1	1.2	0.15
Msw2	1.2	0.15
Msw3	1.2	0.15
Msw4	1.2	0.15
M1	5	0.15
M2	5	0.15
M3	2	0.15
M4	2	0.15
M5	2	0.15

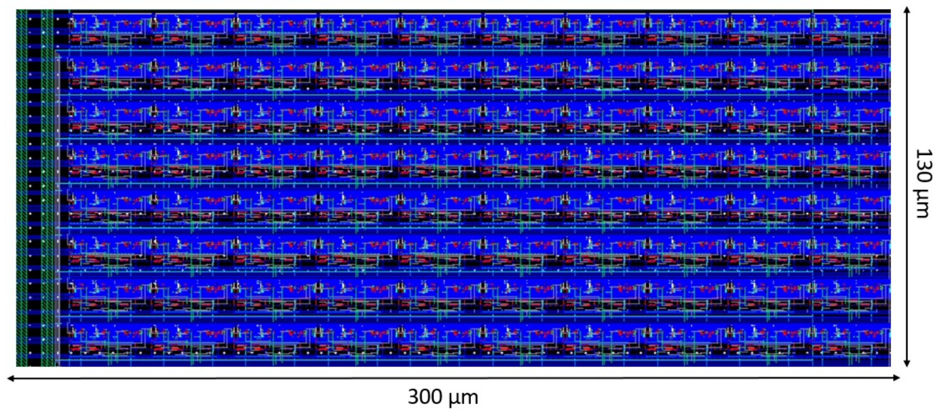


Figure 5.100. – Layout view of the 80 bits SRAM cell matrix.

5.4.3. ASIC layout

The LFoundry SEU tolerant test chip has been submitted to the foundry for fabrication in a CMOS 150 nm technology in January 2019. The total chip size is 1.3 mm × 1 mm and the layout is shown in figure 5.101. The chip contains eight columns with 80 bits in each column. 14 pads located at the bottom of the chip are used for communication and powering. These pads are listed in table 5.10.

Table 5.10. – LFoundry SEU tolerant test chip pads list.

Pad	Name	I/O	Function	Comments
1	VDDIO	Supply	1.8 V	ESD protection
2	GNDIO	Supply	0 V	ESD protection
3	VDD	Supply	1.8 V	Core supply
4	GND	Supply	0 V	Core Supply
5	CMD2	Input	Column selector	Select the column by decoder
6	CMD1	Input	Column selector	Select the column by decoder
7	CMD0	Input	Column selector	Select the column by decoder
8	RDBCK	Input	Readback	Latches data loading in shift register
9	CLK	Input	Clock	Clock to load shift register
10	LD	Input	Load	Data loading in latches
11	CLR	Input	Clear	Reset
12	SIN	Input	Data	Data input
13	SOUT	Output	Data	Data output

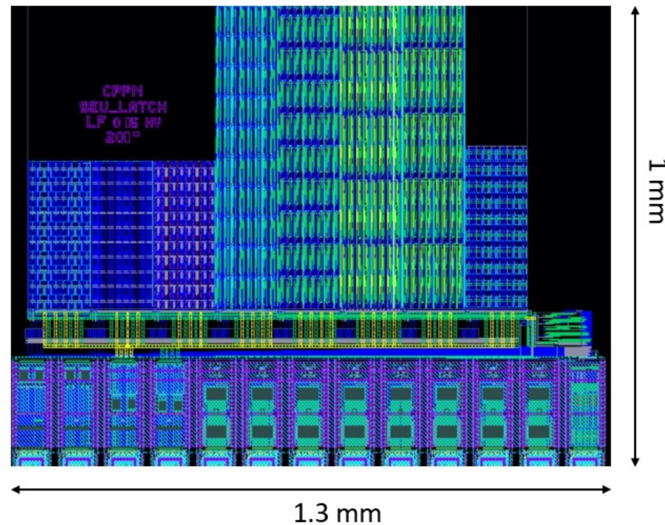


Figure 5.101. – LFoundry SEU tolerant test chip layout. Different SEU tolerant architectures implemented as shown in figure 5.73.

5.4.4. Outlook

Samples of the LFoundry SEU tolerant test chip are expected to be received in November 2019. The samples will be tested in the laboratory with three kinds of bit-stream: all-1s stream, all-0s stream, and "1010..-stream". The irradiation campaign will take place in the beginning of 2020. The cross-section will be calculated for all the architectures and compared with the AMS and TowerJazz SEU tolerant test chips results.

5.5. Summary

In some rare events when a heavy particle strikes the sensor, there is a probability that a lot of charge gets generated. These liberated charge carriers can be collected in the sensitive node of a device. As a result, if the collected charge is greater than the critical charge then there could be a change in the memory state. This mechanism is called a Single Event Upset (SEU).

This chapter started by addressing some of the mitigation techniques at circuit level and at system level for SEU. Hardening at circuit level was achieved by designing structures which could store the data in a redundant way. It was an attractive solution for the CMOS process since with a reduced penalty in terms of area, the memory can be made tolerant to SEU. Moreover, the hardening at system level was achieved by using techniques such as Triple Redundancy Logic (TRL) and temporal redundancy.

A first SEU tolerant test chip with the total size of 1.3 mm $\times$ 1 mm containing different memory structures was produced in AMS aH18 CMOS technology in August 2017. In this test chip, there were six different columns with five different latch structures. The depth of the memories was 80 bits and they were controlled by global signals. Few versions of the Triple Redundancy Logic designs were implemented and compared under the irradiation environment. These designs were made more robust to the upsets by doing special SEU-hard layouts. After receiving few samples of this test chip in August 2018, the samples were tested in laboratory with three kinds of bit-stream: all-1s stream, all-0s stream, and "1010..-stream". Two samples were thereafter selected for the SEU measurements with the 24 GeV proton beam in October 2018. This irradiation campaign was carried out at CERN PS facility for ten days. The DICE and standard latch were tested with the bit-stream of all 0s and all 1s. The cross-section of the proposed DICE latch is 15 times lower than the cross-section of the standard latch.

The second SEU tolerant test chip with the total size of 1 mm $\times$ 1.3 mm, containing different memory structures was produced in TowerJazz 180 nm CMOS technology in August 2018. In this test chip, there were six different columns with six different latch structures. The depth of the memories was similar to the one implemented in the AMS chip. Few samples of the TowerJazz SEU tolerant test chip were received in February 2019. The samples were tested in

the laboratory with three kinds of bit-stream: all-1s stream, all-0s stream, and "1010..-stream". Two irradiation campaigns have been planned in autumn of 2019 at the University of Jyvaskyla and at the KVI-Center for Advanced Radiation Technology KVI-CART (results not available at the time of writing).

The third SEU tolerant test chip with the total size of 1.3 mm $\times$ 1 mm, containing different memory structures was produced in LFoundry 150 nm CMOS technology in January 2019. Few samples of the LFoundry SEU tolerant test chip are expected to be received in November 2019. In the beginning of 2020, an irradiation campaign will take place for few weeks. After calculating the cross-section values for all the architectures, a comparison will be done for the SEU-tolerant designs in all three technologies.

6. Serial Powering Scheme with monolithic CMOS sensors

In 2017, two large demonstrators in TowerJazz 0.18 μm CMOS technology have been developed by CERN [a] and the University of Bonn [b] in collaboration for the ATLAS Phase-II upgrade. After encouraging results from both prototypes, new developments have started on the implementation of a Serial Powering scheme [26] [27] in TowerJazz technology. One of the main challenges for the ATLAS ITk Phase-II upgrade is a low-mass, efficient power distribution for detector modules. Serial Powering is the baseline solution for the ITk pixel system. In section 6.1, we will introduce the TowerJazz sensor technology developments. In section 6.2, we introduce the motivations and concept for the Serial Powering scheme. In section 6.3 implementation of Serial Powering for pixel detectors is described. Section 6.4 deals with the sensor bias generation for serially powered depleted CMOS.

6.1. Developments in TowerJazz 180 nm sensor technology

The standard TowerJazz 180 nm process as shown in figure 6.1 comes with a high resistivity (>1 kΩcm) p-epitaxial layer grown on top of a p-type substrate. An n-well collection electrode of several μm^2 acts as a charge collecting diode for the charges generated by the ionizing particles. CMOS electronics is placed at a minimum 2-4 μm away from the collection electrode and is shielded by a deep p-well. Negative substrate bias is used to increase the depletion region. Ho-

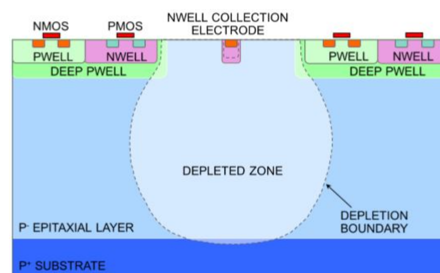


Figure 6.1. – Cross-section of the standard TowerJazz 180 nm CMOS process [35].

wever, for a pixel of a realistic size, the depletion region does not extend up to

a. Group of H. Pernegger.
b. Group of N. Wermes.

the edges of the pixel. There are few ways to achieve full depletion at the edges of the pixel. One of the ways is to increase the size of the n-well collection diode. This would result in junction depletion over the full pixel area. By implementing this approach an increase in the input capacitance (and as consequence in the electronics noise) and power dissipation will be noted, and the dimensions of the pixel might also increase [39]. Another possibility to overcome this problem is to reduce the area of the deep p-well which would reduce the area available for circuitry and hence, increase the complexity of implementing the in-pixel circuitry. Furthermore, it is also possible to achieve full depletion under all parts of the pixel by modifying the process. A low dose deep n-type implant as illustrated in figure 6.2 has been used to implement a planar junction in the epitaxial layer below the deep p-wells within the pixel matrix. The thickness of the p-epitaxial layer is kept between 18 and 40 μm. In the modified process, the charges which are generated by ionization are collected by drift and the sensor fully depletes below the deep p-well. The p-well and the substrate are separated by the depleted sensitive layer and can be biased at different voltages. Having two biasing voltages results in an increased electrical field, better signal charge collection speed and improved radiation tolerance [120]. A number of chips were prototyped within the ALICE ITS upgrade [121] project in this modified TowerJazz 180 nm process to study the analogue performance of monolithic CMOS sensors. Thereafter in 2017, two large demonstrators TJ-MALTA [50] and TJ-Monopix [51] have been produced in the same process with an epitaxial layer of 25 μm for high radiation conditions foreseen in the ATLAS pixel detector for the HL-LHC.

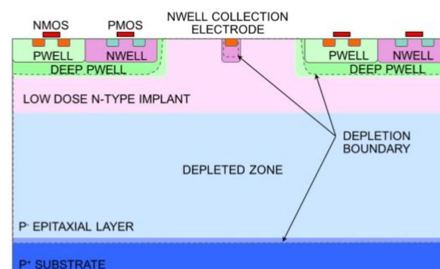


Figure 6.2. – Cross-section of the modified TowerJazz 180 nm CMOS process [35].

Figure 6.3 shows the reticle of the ATLAS TowerJazz 180 nm 2017 chip submission with an area of 31 mm $\times$ 25 mm. The reticle consists of several test chips: TJ-MALTA (pixel pitch of 36.4 μm $\times$ 36.4 μm and asynchronous readout of the 512$\times$512 pixel matrix.), TJ-Monopix (pixel pitch of 36.4 μm $\times$ 40 μm and synchronous readout of the 224$\times$448 pixel matrix.), two versions of the Investigator chip [122], LAPA [123] (5 Gbps LVDS driver), SEU test chip (with different memory structures) and TID test chip (a dedicated transistor level test chip to assess the effects of TID damage).

The same analog front-end designs are implemented inside TJ-MALTA and TJ-Monopix. The analog front-end consists of a charge sensitive amplifier fol-

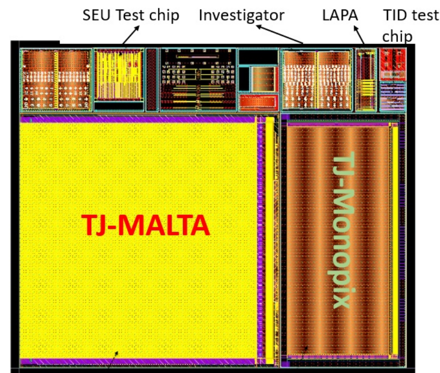


Figure 6.3. – The TowerJazz 180 nm process ATLAS engineering run reticle.

lowed by a discriminator and a hit buffer. The biasing current in the front-end design is 500 nA per pixel, which results in analog power consumption less than 70 mW/cm^2. TJ-MALTA has an asynchronous readout architecture that focuses on low power dissipation and minimal analog to digital crosstalk, whereas TJ-Monopix implements a synchronous readout architecture, well known as the column drain architecture which was used in the FE-I3 readout chip [42]. This readout chip was implemented in a standard 250 nm CMOS process, which was used for three barrel layer ATLAS pixel detector.

Figure 6.4 shows the transient response of the TJ-MALTA analog front-end circuit. The red curve is the signal at the input node (injected 300e^-), which drops by a few milivolts after t = 200 ns, when the charge is collected. This signal is amplified and shown with the blue curve. The green curve shows the signal after the discriminator.

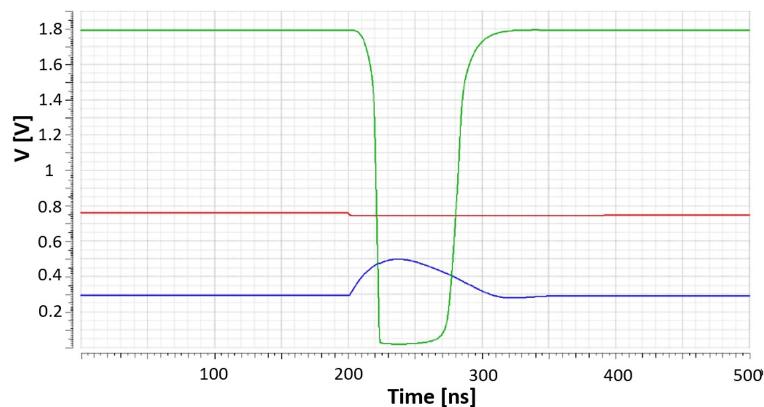


Figure 6.4. – Simulation transient response of the MALTA analog front-end circuit: signals at the input node, the output of the amplifier and the output of the discriminator [124].

6.2. Serial Powering Motivation and Concept

At the HL-LHC, a large number of cables are needed to provide power, data and control signals. The power requirements of the detector are very high and the power consumption of a quad module is around 7.8 W [19]. Parallel powering is the traditional way to power the detectors. In a parallel powering scheme, the modules are connected in a parallel configuration and each module is powered by a constant voltage source. This leads to an independent power supply and a set of cables, for each detector module. The major drawback of this scheme is its very low efficiency with 80% of the power consumed as voltage drop in the cables [26]. If the parallel powering scheme was to be used in the HL-LHC then the number of power cables would increase at large η. This would make the service cables one of the most significant contributions to the material budget in the tracker. These services are already in the present tracker, a dominant source of material as shown in figure 6.5(a) and degrade the performance of subsequent detectors. Moreover, it is thought that the number of cables that would need to be inserted to power the ITk pixel detector if parallel powering would be use can simply not be dealt with.

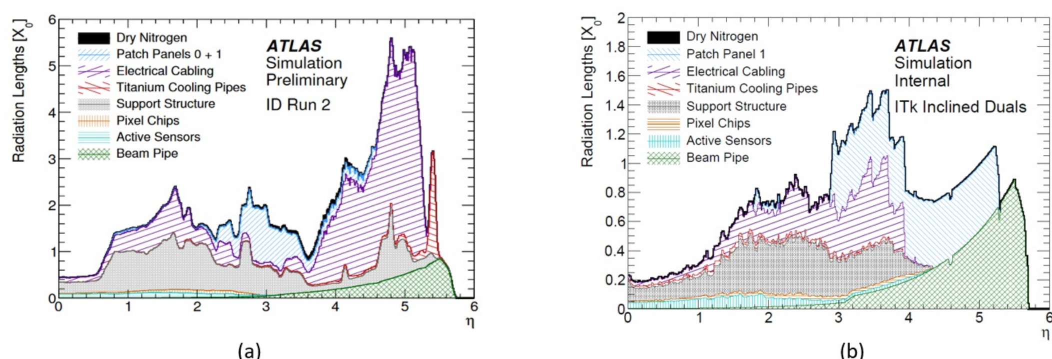


Figure 6.5. – Radiation length X_0 versus the pseudorapidity η. (a) Present ATLAS Tracker [19]. (b) ATLAS ITk Detector [19].

The upgraded pixel detector will consist of about 10000 hybrid pixel modules [125], 5×10^9 channels and there is not enough room to handle all the cable cross-section needed to power all modules if parallel powering scheme is used. The cross-section of these power cables has to be as small as possible, so as to meet the space constraints and lower material budget requirements. Let us assume that A is the cross-section of the cable, I is the transmitted current over a length l of a cable with the electrical conductivity of the conducting material k. The voltage drop V_{drop} on the cable cross-section A can be calculated as:

$$A = l \times \frac{I}{V_{drop}} \times \frac{1}{k} \tag{6.1}$$

From the equation 6.1, having a low cross-section of the cable has for consequence that the V_{drop} increases.
As described above parallel powering is not suitable for the Phase-II upgrade, therefore a new powering approach called Serial Powering has been investigated as the baseline solution for the ITk pixel system which solves the material increase issue, as shown in figure 6.5(b). Comparing the ITk to the present ATLAS Tracker, the material is significantly less for all values of η. The Serial Powering scheme is sketched in figure 6.6. In this scheme, the modules are placed in series and powered by a constant current source. The current I_0 of one module entirely feeds the next module in the Serial Powering module chain, with the local ground of each module acting as the power supply input for the next one. The voltage is generated locally from the input current by using shunt regulators to provide the analog and digital supply voltages needed by the front-end electronics. In ATLAS ITk pixel detector, there are four front-end chips inside the module and the current splits parallel into those chips.

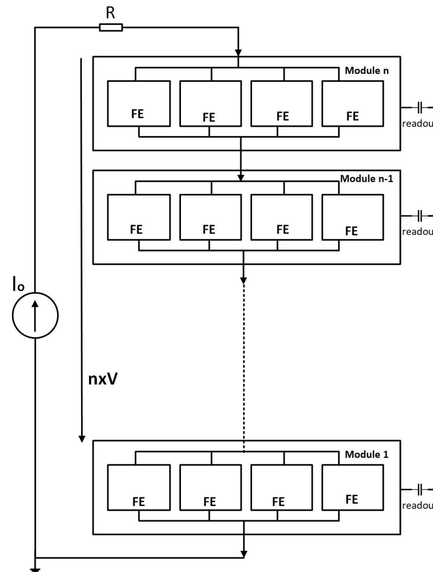


Figure 6.6. – Sketch of the Serial Powering scheme. The modules are connected in series and powered by a constant current I_0.

Let us assume the voltage across the module referred to the local ground is V, which is also the voltage at the input of the regulator. The voltage across the entire chain is n×V. With this powering strategy, the power can be transmitted at low current but high voltage, and a single power cable is used and a constant current source is needed, which leads to a drastic reduction in the number of power lines and therefore in the material budget. At the HL-LHC, Serial Powering will be used for the whole ATLAS pixel detector.

At a system level, Serial Powering also brings some risks and complications. For instance, if there is a fault on the power line it will affect the entire chain.

Faulty modules could also affect the performance of other working modules in the chain. The modules can not be powered off or on individually. And the fact that all the modules in the entire chain have different ground potentials with respect to the power supplies and readout system bring some other system level difficulties. To overcome these issues, a dedicated detector system is developed as discussed in section 6.3.1.2. Studies on Shunt-LDO regulators (combining Shunt and Low Drop Out sections) were performed in the framework of regulator developments for ATLAS hybrid pixel detectors. This R&D was carried out based on the experience gained with the Serial Powering of FE-I3 modules. Finally it should also be noted that the performance of Serial Powering schemes have been demonstrated within the RD53 collaboration for the next generation hybrid pixel detectors at the HL-LHC [126].

6.3. Implementation of Serial Powering for pixel detectors

6.3.1. Serial Powering for Hybrid Pixels

In the Serial Powering scheme, a few requirements are needed to be fulfilled to ensure the reliable powering of the detector modules. First and foremost is the generation of supply voltage for the electronics from the input current. This is achieved by implementing a shunt-LDO regulator. The shunt-LDO regulator is a combination of a shunt and Low Drop-Out (LDO) regulator. Previous developments [127] [27] of shunt-LDO regulators have demonstrated promising results and proved that a shunt-LDO regulator design could be suitable for all layers in the ATLAS pixel detector. Secondly, a bypass scheme with a PSPP (Pixel Serial Powering and Protection) chip [128] could be implemented in order to prevent a fault in the chain. The PSPP chip must be connected in parallel to each module, referenced to the local module ground. Finally, AC-coupled data transmission needs to be implemented since the modules are on different ground potentials.

6.3.1.1. Shunt-LDO regulator

On-chip shunt regulators are used to generate the local supply voltage from the input current. In a FE-I4 quad module, the current split equally between the on-chip regulators which are connected in parallel configuration as illustrated in figure 6.7. This configuration adds redundancy and some safety to the Serial Powering chain from failures of the on-chip regulators. With shunt regulator redundancy, there would be no interruption in the current flow even if one of the regulators fails. But the design of a regulator should then be very robust against process variation and mismatch that allows reliable parallel operation. The regulator should be able to shunt extra current to ensure a constant current

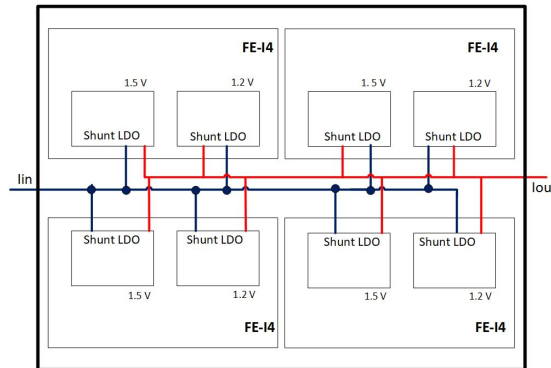


Figure 6.7. – A sketch of current distribution on a FE-I4 quad module.

flow to the next module in a Serial Powering chain. Moreover, the regulators connected in parallel should be able to shunt different amounts of current so that different output voltages can be generated to match the power requirements of the digital and analog domains. All these requirements are met by a dedicated shunt-LDO regulator as described in [129].

6.3.1.2. Bypass scheme

A bypass scheme could be implemented in a Serial Powering chain in case of a fault on the power line. The following requirements should be satisfied with this scheme :

1. Fast response capability to over-voltage across the module.
2. Generation of low voltage when shunting the entire module current in order not to dissipate extra power.

To meet these requirements a PSPP (Pixel Serial Powering and Protection) chip was designed in TSMC 65 nm technology. This dedicated chip has capabilities to bypass an input current up to 8 A. Figure 6.8 shows the connection of the PSPP chips in a Serial Powering chain. This chip could be activated automatically if the voltage exceeds a fixed level. The PSPP chip has been irradiated with an X-Ray machine up to a Total Ionizing Dose (TID) of 600 Mrad. More details on the design and measurement results are discussed in [128].

6.3.1.3. AC-coupled data transmission

In a Serial Powering scheme, the complete current passing through a module goes to the next module in the chain, and the modules are referred to local ground potentials of different absolute values. As a consequence, there is a mismatch between local ground and system ground, and the data transmission has to be adapted for that. In practice, the communication of clock and command

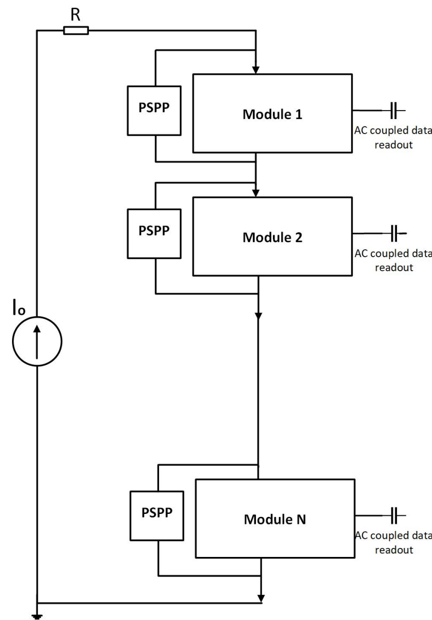


Figure 6.8. – A sketch of key components in the serial powering scheme.

signals to the front-end chips as well as data from the front-end chips are carried out by using Low Voltage Differential Signalling (LVDS) links. Also due to the different ground potentials, the DC voltage (V_{CM}) of the lines in the LVDS pair is also shifted between the transmitter and receiver. The link does not function in a proper way if V_{CM} shifts out of the common mode voltage range at the receiver input. To overcome this issue, an AC-coupled data transmission technique has to be used in a Serial Powering scheme. In an AC-coupling termination scheme,

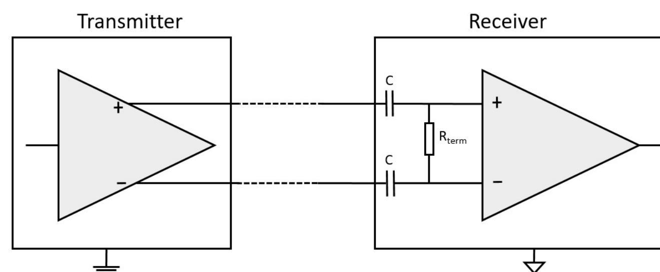


Figure 6.9. – A sketch of a block diagram of the AC-coupled LVDS link. this configuration is implemented with serially powered FE-I4 modules.

capacitors are added in series with both the signals of a differential pair of the LVDS link as sketched in figure 6.9. The AC-coupled link allows blocking the DC component of the signal over the differential pair. The ground differences between the transmitter and receiver are mitigated by using the AC-coupled link. As a result, this link requires self-biased receiver inputs to set the common-mode voltage. The current from the transmitter flows through the coupling capacitors

across the termination resistor R_{term} only during transitions. Preventing the V_{CM} to exit the allowed voltage range is achieved by using DC-balanced signals.

6.3.2. Serial Powering for depleted CMOS sensors

We will now turn to the specific case of the implementation of a Serial Powering scheme in the case of depleted CMOS sensors. The most important requirement is to design a stable shunt regulator. The design of the proposed Shunt-LDO regulator is described in 6.3.2.1.

In contrast to hybrid pixels, the sensor bias for depleted monolithic sensor in a Serial Powering chain is low, which makes the ΔV drop a big concern from one module to the other. A high voltage needs to be set so that full depletion occurs without exceeding the breakdown voltage. One of the possibilities to bias the sensing part is to derive a high voltage locally at module level to deplete the sensor. In the TowerJazz 180 nm modified process, two different voltage levels are used for the purpose of sensor depletion. The bias voltages could be generated on-chip by using a negative charge pump circuit. The charge pump circuit is designed and prototyped to deliver a load current of 500 μA. The design of the proposed negative charge pump is described in section 6.4.3.

6.3.2.1. Shunt-LDO regulator

Similar work to what has been done for hybrid modules, has been carried out in developing a new Shunt-LDO regulator design for the depleted CMOS sensors by CPPM's team [c] [130]. In the depleted CMOS case, each module consists of four CMOS chips in parallel, and each chip has its own shunt-LDO regulator. An ideal Shunt-LDO regulator acts as a perfect voltage source. The current is being split between the on-chip regulators connected in parallel, which are responsible to generate supply voltages needed to power the front-ends as illustrated in figure 6.10.

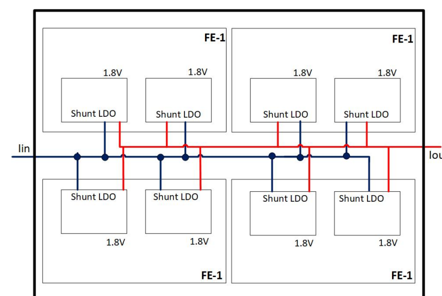


Figure 6.10. – A sketch of current distribution on a quad module.

c. Group of M. Barbero.

Any process mismatch between the regulators would mean that all the input current will flow into the regulator with the lowest output voltage. The design of a Shunt-LDO regulator should be robust against process variation and mismatch that allows reliable parallel operation. A test chip was designed (see figure 6.11(a) and figure 6.11(b) the die photograph.) to test the shunt-LDO developments that were made in CPPM. It was designed to power three independent domains namely: main domain, p-well domain, and p-sub domain. The main domain can be further divided into four sub-domains: LVDS (300 mA), analog (400 mA), digital (500 mA) and charge pumps (60 mA). The p-well (500 μA) and p-sub (500 μA) domains are used to bias the sensor part of the depleted CMOS sensor. The values in parenthesis are what is anticipated to be needed in terms of consumption for a production CMOS sensor chip to be used in the detector.

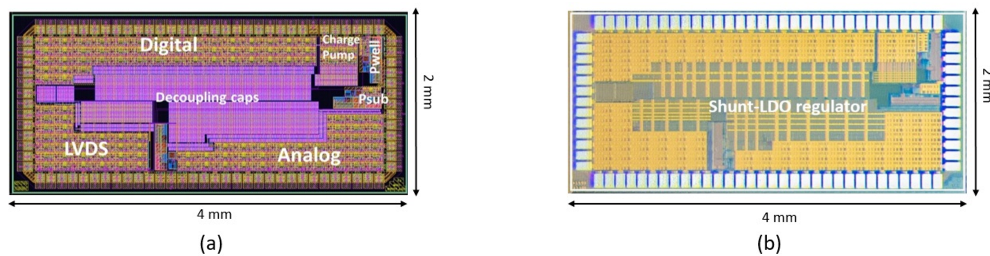


Figure 6.11. – (a) Layout view of Shunt-LDO test-chip submitted to foundry. (b) Die photograph of Shunt-LDO regulator test-chip received from foundry in February 2019.

Each domain is composed of one or more elementary block(s) of Shunt-LDO regulator which is designed to deliver a maximum output current of 10 mA. Each block of the Shunt-LDO regulator is composed of two parts. The first part is a shunt regulator which is sketched in figure 6.12(a). It performs the first regulation with no dropout. The second part is a low-dropout voltage regulator as sketched in figure 6.12(b), which performs the second regulation with a dropout of 200 mV. Both shunt and LDO regulators use the same differential amplifier design. In case of shunt regulator, the differential amplifier controls the gate of the shunt transistor M_S and a resistive divider formed by resistors R1 and R2. The transistor M_S shunts the excess current which is not taken by the load. The width of the transistor M_S is very large and hence the transistor operates in a strong inversion region. The degeneration resistance R_d is added in order to mitigate the effect of mismatch and process variations between parallel chips. The shunt regulator is powered by a constant current I_{in} which is recycled at the next module. The system is stabilized by using decoupling capacitors on the chip.

Biasing circuitry for the amplifier is provided internally with the mirroring ratio B between the first and second stage of the amplifier. The output voltage V_{out} is regulated and can be expressed as $V_{out} = \alpha\, V_{ref}$, where α is the resistive

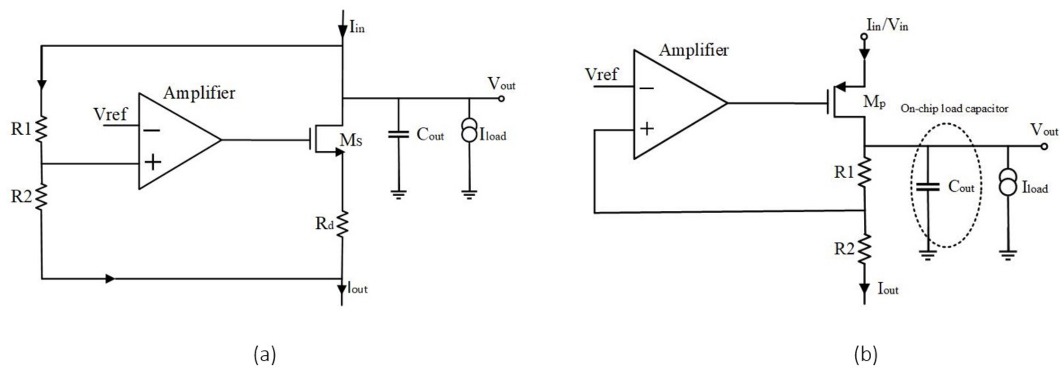


Figure 6.12. – (a) Simplified schematics of the shunt regulator. (b) Simplified schematics of the LDO regulator.

ratio R1/(R1+R2)and V_{ref} is a reference potential which is set at 1 V. The layout view of the Shunt-LDO regulator is shown in figure 6.13. The dimension of one block of the Shunt-LDO regulator is 200 μm $\times$ 100 μm. The role of the author was to design the layout for the Shunt-LDO regulator test-chip.

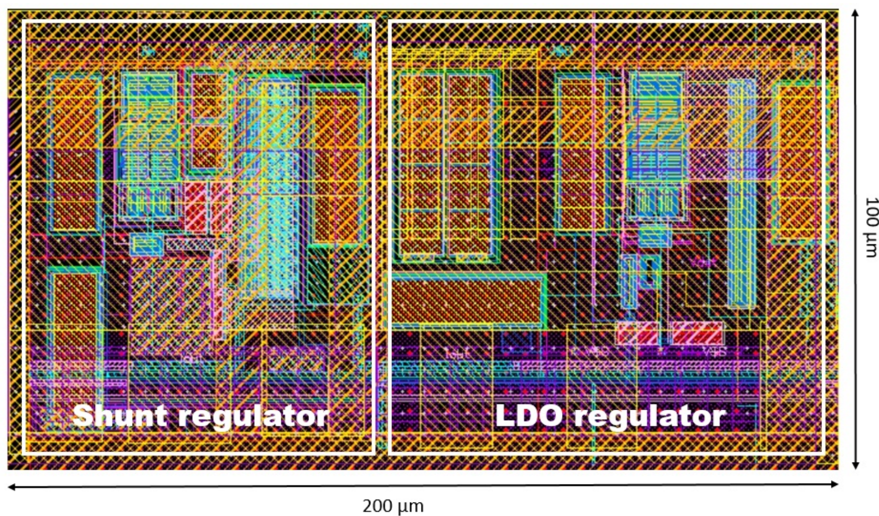


Figure 6.13. – Layout view of one Shunt-LDO regulator block.

Simulations have shown that the design of the Shunt-LDO regulator is stable up to a load capacitance of 10 μF. In DC, the regulator acts as a voltage source in series with a resistance of 175 mΩ. Figure 6.14 shows the simulation response of the analog domain which is made of 40 Shunt-LDO regulator blocks in parallel. The Shunt-LDO regulator test chip consists of 126 elementary blocks of Shunt -LDO regulator which are capable of generating the constant required voltage of 1.8 V with a maximum input current of 1.4 A. More details on the design of the Shunt-LDO regulator are described in [130].

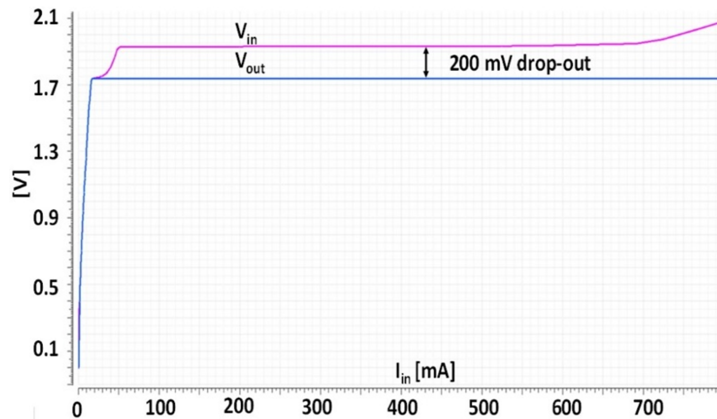


Figure 6.14. – Simulation result of analog sub-domain consists with 40 shunt-LDO regulators.

Figure 6.15(a) represents four regulators connected in parallel and a threshold voltage offset up to 100 mV on shunt transistor M_S of regulator 1. Figure 6.15(b) shows the current distribution between four parallel regulators as a function of applied threshold voltage offset and input current. Current mismatch over 4 regulators are less than 11% for a voltage offset up to 100 mV. Figure 6.15(c) shows the transient response of V_{out} as a result of a step current excitation on I_{load} of 1 mA. This plot is illustrated with three different values of load capacitances (C_L).

Measurement results

For the characterization, the test-chips are mounted on the test boards, wire bonded from the pads to measurement points which are used to measure the voltages at the input and output of the regulators. Figure 6.16 shows the full setup including shunt-LDO test chips, DC load, the power supplies, current sources, and PC. LabView software was used to make communication from the test chip to the PC.

The reference voltage for a Shunt-LDO regulator can be provided in two ways. Firstly, from the bandgap circuit which is implemented inside the test chip and secondly through an external supply. Initially, three samples were taken to test the Shunt-LDO chip. The measured V-I voltage characteristics of a single Shunt-LDO regulator for the p-well domain is shown in figure 6.17. The generated output voltage is 1.6 V with the input voltage of 1.8 V. The output voltage is not as expected (equal to 1.8 V) because of the measured bandgap reference voltage. The value of the bandgap circuit in the simulation was 966 mV whereas, the measured value is 875 mV. The error on the measurements was negligible and all the three boards showed similar behaviour.

Figure 6.18 shows the measured V-I characteristics for the analog domain. The output voltage is regulated to 1.6 V with a drop-out of 200 mV. As the load

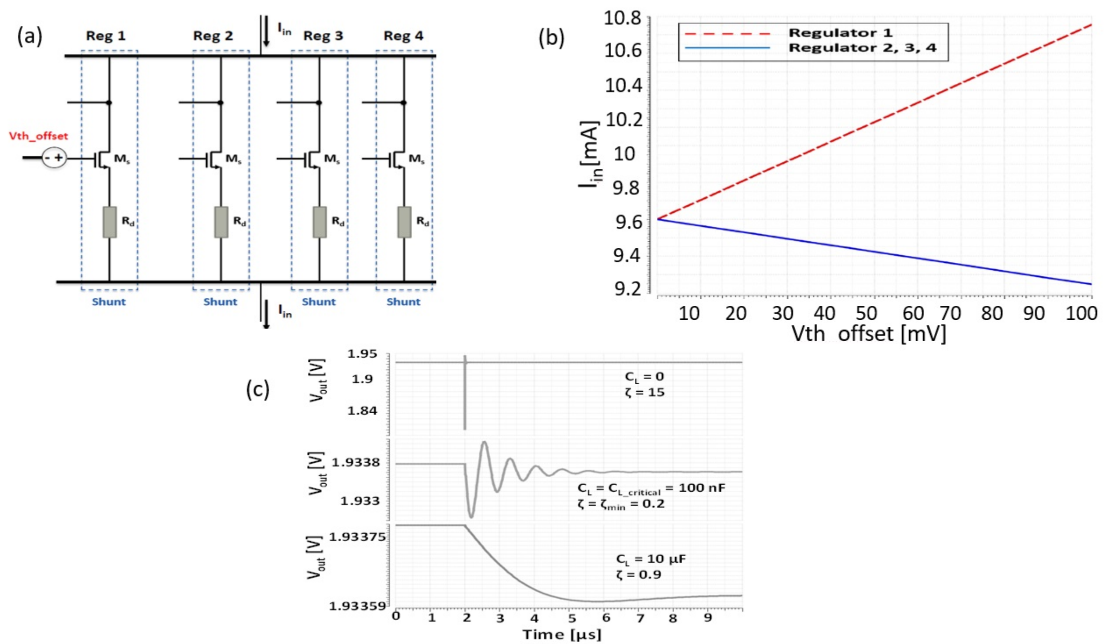


Figure 6.15. – (a) A sketch of four regulators connected in parallel with an offset on shunt transistor M_S of regulator 1. (b) Simulated current distribution over four shunt-LDO regulators. (c) Output voltage response to a load current step excitation of 1 mA.

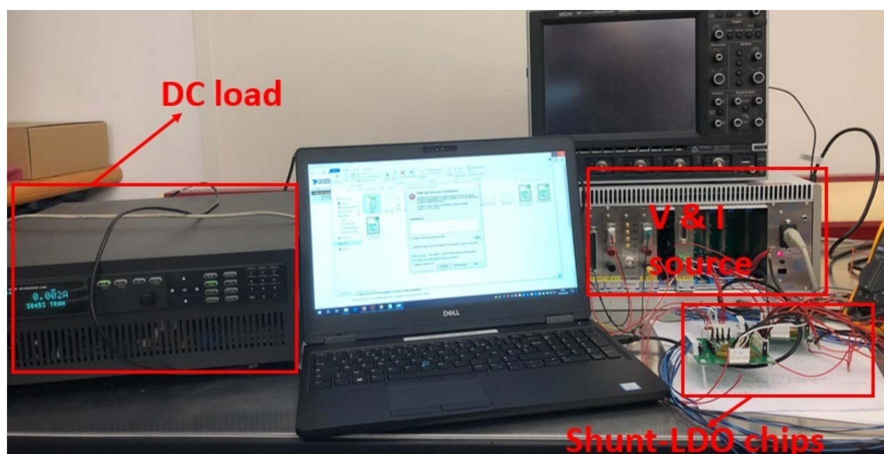


Figure 6.16. – Laboratory test setup for Shunt-LDO regulator.

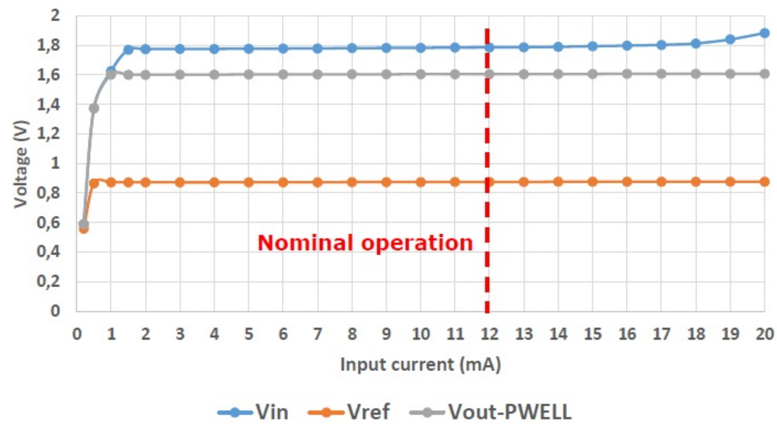


Figure 6.17. – Measured V-I characteristics of one Shunt-LDO regulator block under no load current.

current was increased up to 320 mA, the variation in the output voltage was less than 0.3%.

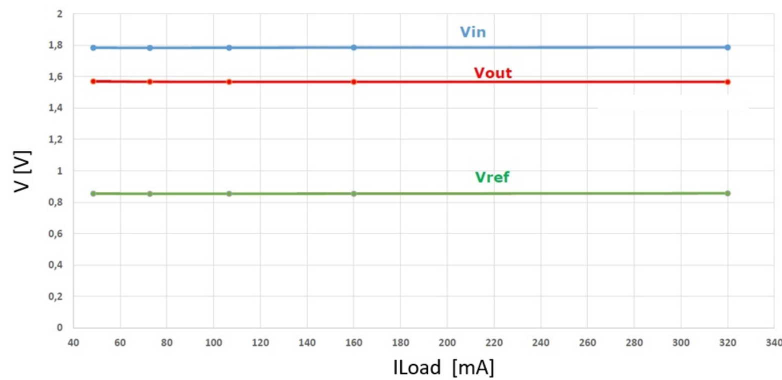


Figure 6.18. – Measured load regulation for the analog domain under load current. Analog domain consists of 40 Shunt-LDO regulator blocks connected in parallel.

6.4. Sensor bias generation for serially powered depleted CMOS

To meet the requirements of modified TowerJazz sensor, design activity was started to generate the bias voltage for the CMOS sensor. A charge pump test-chip was designed and prototyped in the modified TowerJazz 180 nm CMOS imaging technology to generate the bias voltages for sensor depletion. The detailed charge pump design is described in section 6.4.3.

6.4.1. Motivation and overview of Charge Pump

The modules in a Serial Powering chain have different ground potentials, so a specific biasing scheme for the sensors needs to be considered. A sketch of high voltage distribution for a Serial Powering chain is illustrated in figure 6.19. We cannot use the same bias for all the modules. Since the local ground of the module Vss is shifted from one module to the other, Vss_n is shifted every module and in order to polarize all sensors in the same way, Vss_n – $Vbias_n$ must be constant. A simple way would be to use an individual high voltage power supply for each module. However, due to a large number of modules to power, this is not a practical solution as this would lead to many more cables to be used, and many more power supplies to bias the sensing part of the modules.
In the modified TowerJazz 180 nm, the p-well in the pixel matrix and the sub-

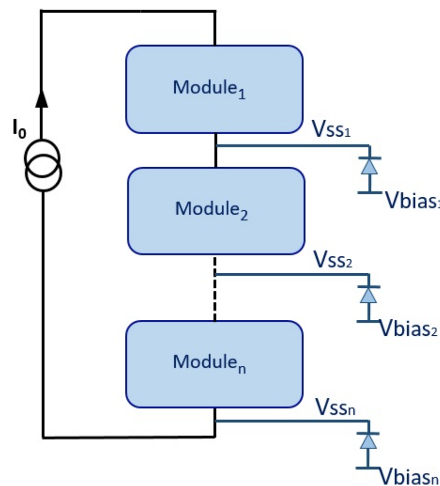


Figure 6.19. – A sketch of the high voltage distribution for a serial powering chain.

strate are separated by the depleted sensitive layer and can be biased at different voltages. The NMOS transistors in this deep p-well can not tolerate more than −6 V because of the breakdown of the bulk-source and bulk-drain junctions. The substrate can be biased much more negatively up to −20 V, which increases the electric field and the speed of the signal charge collection and improves the radiation tolerance. The bias voltages can be generated on-chip in a final design by using a negative charge pump circuit. The charge pump gives additional flexibility because these bias voltages can be generated locally on the front-end chip.

Charge pumps are one of the building blocks of a power management unit. They are also popular as DC-DC converters which are used to generate DC voltages which can be higher or lower than the power supply. They are extensively used in applications such as non-volatile memories [131] [132], RF MEMS devices [133], driving LCDs [134], among many others [135]. They are easy to de-

sign as they require a diode or a MOS transistor and capacitors. These capacitors are used to store the energy. The conventional charge pump which was proposed by Dickson [136] in mid 1970's has a disadvantage in the generated output voltage because of the threshold voltage drop and body effect of the diodes which leads to a limited voltage pumping gain. In the last three decades, researchers have made a lot of developments in order to eliminate the threshold voltage drop problem. The idea was to design a more power efficient charge pump in which MOS transistors were used as charge transfer switches. To have a high voltage gain, different topologies have been studied. However, these charge pump topologies introduce undesirable charge transfer during the clock transitions which results in power loss in charge pumps. In general, the power efficiency (η, given in %) of a charge pump is expressed as [137]:

$$\eta = \frac{P_{out}}{P_{in}} \times 100 \tag{6.2}$$

where P_{out} is the output power and P_{in} represents the input power of the charge pump. The input power is basically the sum of three components shown below.

$$P_{in} = P_{dynamic} + P_{shortcircuit} + V_{DD} \cdot I_{leakage} \tag{6.3}$$

where $P_{dynamic}$ is the average dynamic power consumption, $P_{shortcircuit}$ is the average short-circuit power consumption, V_{DD} is the voltage supply, and $I_{leakage}$ is the reverse bias current caused between the nMOS drain region and the p-type substrate.
The $P_{dynamic}$ is expressed as:

$$P_{dynamic} = C_{load} V_{DD}^2 f_{clk} \tag{6.4}$$

C_{load} is the load capacitance, V_{DD} is the voltage supply, and f_{clk} is the operating frequency.
The $P_{shortcircuit}$ is expressed as [138]:

$$P_{shortcircuit} = \frac{k \cdot \tau \cdot f_{CLK}}{12} (V_{DD} - 2V_T)^3 \tag{6.5}$$

where k is product of three terms μ, C_{ox} and $\frac{W}{L}$, τ is the input transition times, V_{DD} is the voltage supply, V_T is the threshold voltage of the transistor, and f_{clk} is the operating frequency.

To have a high power efficiency, P_{losses} needs to be minimized. The easiest way by which the power loss can be reduced is to vary the switching frequency according to the load. The dynamic power dissipation contributes more percentage to the total power because of the charging and discharging of these capacitors

in the charge pump. If the switching frequency and width of the charge transfer switches are fixed then dynamic power for charging and discharging the gate of these transistors are also fixed. The width of the transistors used as charge transfer switches in the charge pump is directly proportional to the load current. Based on the load current, the transistor width or switching frequency is chosen. From equation 6.6, for a low load current if we use high switching frequency, the output voltage increases. This results in power losses in charge transfer switches and hence less power is delivered to the load. An overview on design strategies is discussed in [139].

$$V_{out} = -n \times V_{DD} + \frac{I_L}{f \times C} \tag{6.6}$$

where V_{DD} is the voltage supply, n is the number of stages in the charge pump design, I_L is the load current, f is the pumping frequency, C is the value of the pumping capacitor.

6.4.2. Principle of Charge Transfer

The one-stage charge pump is made of a pumping capacitor C, two switches S_1 and S_2 which are driven by two complementary clocks, a load current represented by I_L and a load capacitance C_L. Figure 6.20 shows the basic one-stage charge pump topology.

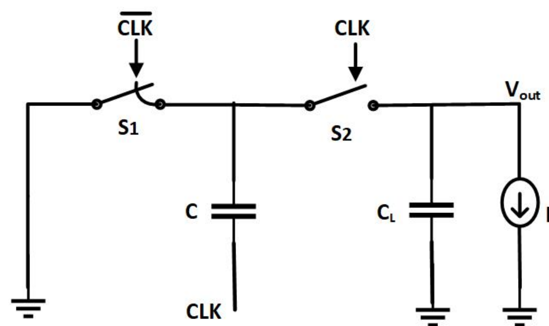


Figure 6.20. – Ideal one-stage charge pump.

Figure 6.21 illustrates the operation of a one-stage charge pump. During the first half period between 0 to T/2, S_2 is open since the clock signal is 0 V and switch S_1 is closed since $\overline{CLK}$ is V_{DD}, while the output node is discharged by the load current I_L, which sinks a charge $I_L \times$ T/2.

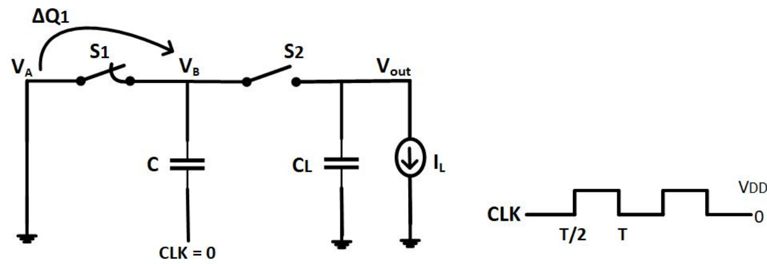


Figure 6.21. – one-stage charge pump during the first half period.

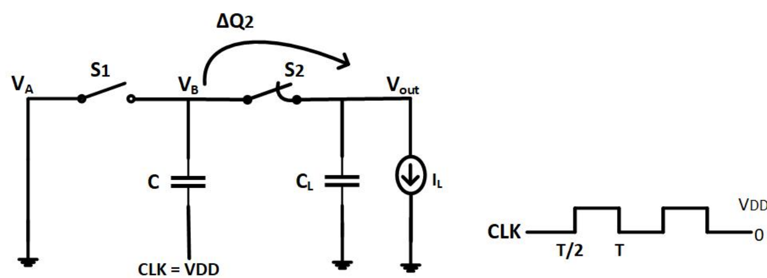


Figure 6.22. – one-stage charge pump during the second half period.

In the second half period from T/2 to T, the switches will change their state and S_1 is now open since the clock is brought to V_{DD} and the switch S_2 is closed since $\overline{CLK}$ is 0. So the charge stored in the pumping capacitor C is transferred to the output node at V_{out}. The operation is shown in figure 6.22.
The charge transferred in the two time periods can be given by (if no charge loss has been recorded in the sequence):

$$\Delta Q_1 = \Delta Q_2 \tag{6.7}$$

$$I = \frac{dQ}{dt} \tag{6.8}$$

$$dQ = \int_0^{T/2} I dt \tag{6.9}$$

$$dQ = I \times T/2 \tag{6.10}$$

ΔQ is the amount of charge which is being transferred from the input to the output node. Hence after several clock cycles, the output voltage will approach the asymptotic value. The simulated transient response of the two-stage ideal charge pump is shown in figure 6.28. From the plot, the step increment of the output voltage in each clock period in this ideal case becomes smaller and finally will reach its final value.

The final asymptotic value is calculated as [139]:

$$V_{out} = -2V_{DD} + \frac{I_L \cdot T}{C} \tag{6.11}$$

where V_{DD} is the power supply, I_L is the load current, T is the clock time period, C is the value of the pumping capacitor. In equation 6.11, the second term is purely the losses while charging and discharging the pumping capacitor C. For a fix load current, the second term could be minimized by increasing the operating frequency or the value of the pumping capacitors or even both.

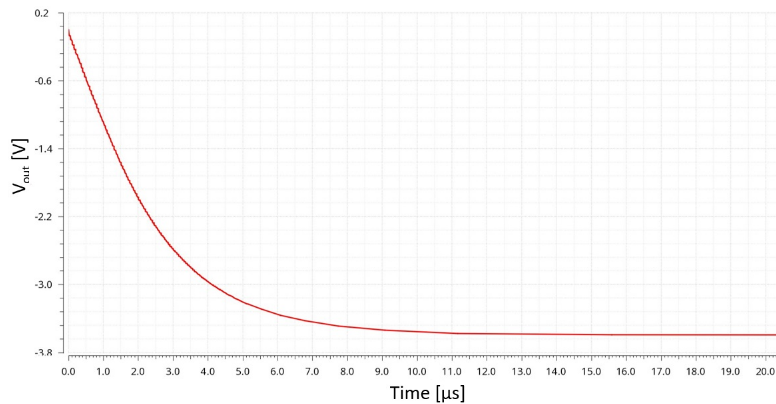


Figure 6.23. – Simulation response of ideal two-stages charge pump.

N-Stage Charge Pump

The one-stage charge pump topology can be generalized by connecting additional cascaded stages as shown in figure 6.24. Each stage consists of one switch S_i and one pumping capacitor C_i. The principle of the N-stage charge pump is similar to the one-stage charge pump. When the clock signal CLK is V_{DD}, the odd switches are closed at the same time. In the second half period, the clock signal CLK is equal to 0 V which makes the even switches to close. All the capacitors placed between the stages give the charge to the capacitor in the next stage. In one clock period, each charge pump capacitor receives the charge from the left side and transfers it to the right side.

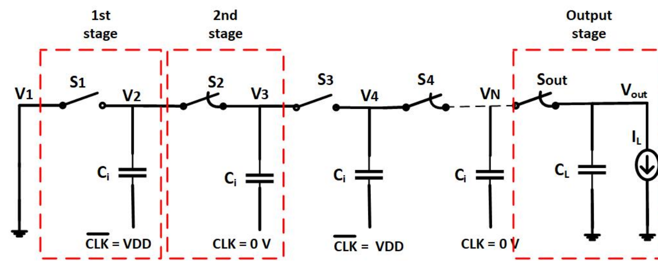


Figure 6.24. – Schematic of N-stage charge pump.

Ideally, the output of the n-stage charge pump under no load condition can be expressed as:

$$V_{out} = -n \cdot V_{DD} \tag{6.12}$$

6.4.3. Proposed Charge Pump

A charge pump circuit is proposed to bias the 180 nm modified TowerJazz process. Our charge pump uses 4 charge transfer switches with 2 pumping capacitors on each side and a start-up switch (see section 6.4.4) as sketched in figure 6.25. Transistors used as charge transfer switches eliminate the threshold voltage drop problem which is discussed in [136].

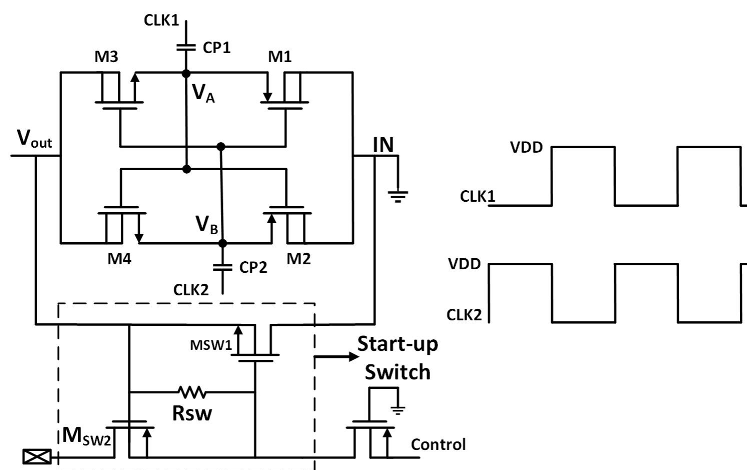


Figure 6.25. – Schematics of 1 stage charge pump. Start up switch is used to avoid latch-up.

The charge transfer switches are designed with two parallel, complementary cross-coupled transistors operating in opposite phases, each part providing the control signal to each other [140]. This means the gates of NMOS and PMOS

Table 6.1. – Sizes of the transistors in a charge pump.

MOS	W (μm)	L (μm)
M1	14	0.18
M2	14	0.18
M3	4	0.18
M4	4	0.18

transistors in one part are self boosted by the outputs of the pumping capacitors in its counter path. A simple two-phase clocking scheme is used, with two complementary clocks CLK1 and CLK2. One charge pump stage works in two phases. In the first phase when CLK1 is high and CLK2 is low, both M1 and M4 transistors will be turned ON in counter path. As a result, there will be a transfer of charge from the input to the V_A node. In the second phase, when CLK1 is low and CLK2 is high, both M2 and M3 transistors will be turned ON in counter path and thereby "pumping" the node V_A to $-$VDD. The size could be as listed in table 6.1. Higher negative voltages can be generated by cascading a certain number of stages (n). The two clocks are generated by using a 2-phase clock driver circuit inside the chip. The schematic of the 2-phase clock driver for the charge pump is sketched in figure 6.26. The size of the transistors in this driver circuit is chosen such that the input transition times (τ_{rise} and τ_{fall}) of the clock signals are reduced [138]. This minimizes the short circuit current from the supply to the ground. Hence, it helps in reducing the power dissipation from the circuit. The size of the transistors used in designing the 2-phase driver circuit is listed in table 6.2.

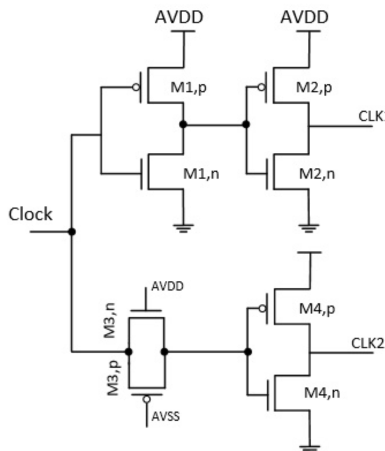


Figure 6.26. – Schematic of 2-phase clock driver for charge pump.

Ideally, the output voltage from an n-stage negative charge pump is $-$n$\times$VDD. The area of a single stage charge pump is dominated by the value of the pumping

Table 6.2. – Sizes of the transistors inside the 2-phase clock driver.

Name of transistor	W (μm)	L (μm)
M1,p	10	0.18
M2,p	30	0.18
M3,p	5	0.18
M4,p	30	0.18
M1,n	4.33	0.18
M2,n	13	0.18
M3,n	2	0.18
M4,n	13	0.18

capacitor. The width of the charge transfer switches is chosen such that it delivers high load current. To reduce the parasitics and power consumption, metal-oxide-metal (MOM) capacitors are used as pumping capacitors with a value of 2.35 pF in each stage. The charge pump is designed with the operating frequency of 640 MHz. This high speed clock signal is received from an LVDS receiver which was implemented inside the LAPA test-chip [123]. By operating at a higher frequency, the Equivalent Series Resistance (ESR) losses caused by the pumping capacitors are reduced which leads to higher voltage gain. Two prototypes have been designed, one with 6-stages and one with 19-stages, to provide negative bias down to -6 V and -20 V, respectively. Both charge pumps are designed to deliver a load current of 500 μA. From the simulations, in the open loop charge pump (consists of 6 identical stages in series) when the load current is increased from 0 to 500 μA, the following sequence occurs:

- The output voltage of the charge pump drops by increasing the load current.
- Increasing the value of pumping frequency and pumping capacitors causes more power dissipation.

In many different architectures, various schemes have been discussed to handle the issue of the body effect in the charge pump. The three different methods to mitigate this issue are floating-well [141], adaptive body biasing circuit [142] and body-source junction diode [143]. All three methods are sketched in figure 6.27. In a floating well approach, the p-well and n-well are connected to the ground. The substrate leakage current degrades the performance of the circuit. In adaptive body biasing circuit, the body effect is mitigated by connecting its body to the highest or lowest voltage. This results in additional transistors on the chip. The third is the body-source diode connection where the drain is always connected to the body of the transistor. By using this strategy, the charge transfer switches can be completely turned off. The advantages of this approach are

that it is simple, area-efficient and has better conduction speed. This technique is implemented in our proposed design.

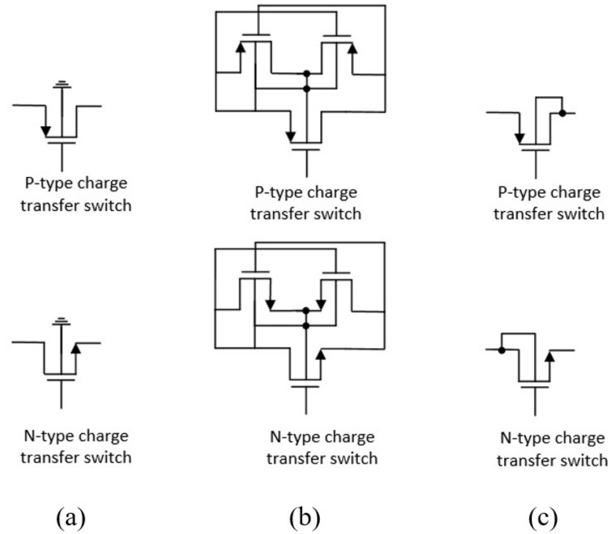


Figure 6.27. – A sketch of three body biasing methods for charge transfer switches inside the charge pump circuit. (a) floating well, (b) adaptive body biasing circuit and (c) body-source junction diode approach.

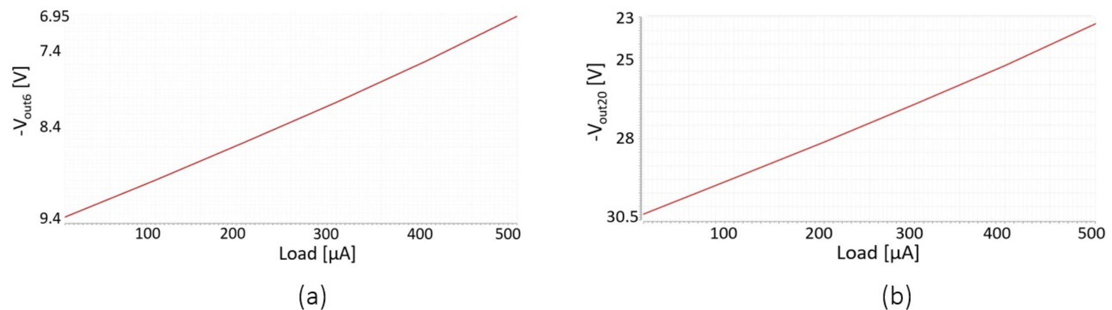


Figure 6.28. – Post-layout simulation response of the open loop charge pump. (a) Simulated output voltage as a function of load current for the 6-stage charge pump. (b) Simulated output voltage as a function of load current for the 19-stage charge pump.

The post-layout simulation response of the two charge pumps with 6-stage and 19-stage are plotted in figure 6.28 (a)(b) respectively as a function of the load current. From these plots, the output voltage of the charge pumps drops by increasing the load current. In order to reduce the parasitic capacitance caused by the pumping capacitors, the layout of the pumping capacitors was done by using metal-2 to metal-5 layers. The metal-1 layer was used for shielding which reduces the parasitics. The value of parasitic capacitance between "V_A" and ground nodes was 15 fF.

As seen from the figure 6.28(a), the open loop charge pump gives an output response up to -7 V at 500 μA of load current. The output voltage has a dependency on the load current, and it is evident that to bias the p-well region to an extend of -6 V, we need to regulate the output voltage. A closed loop charge pump was implemented for this purpose. The output voltage is regulated in a closed-loop system which consists of an open-loop charge pump, amplifier, resistive divider and an adjustable load consisting of a string of PMOS transistors M_{AL0}-M_{ALN} as represented in figure 6.29. The string of PMOS transistors acts as an artificial load in the closed-loop system. A voltage divider with resistors R1

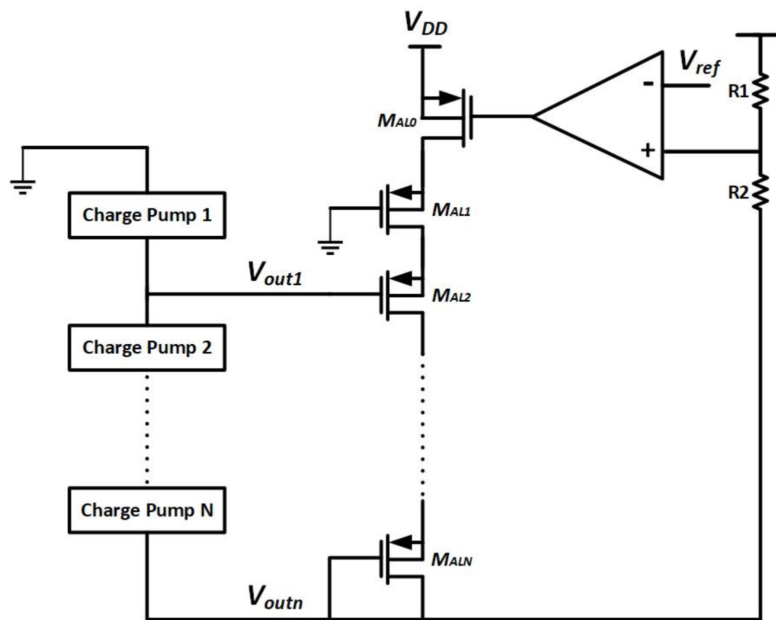


Figure 6.29. – Block diagram of regulated charge pump.

and R2 helps in regulating the output voltage. The value of the output voltage is calculated by using equation 6.13. The intermediate node voltage is given to the positive terminal of the amplifier. The amplifier controls the gate of transistor M_{AL0}. The design of the amplifier is a classical one-stage amplifier.

$$V_{outn} = \left(1 + \frac{R_2}{R_1}\right) V_{ref} - \frac{R_2}{R_1} V_{DD} \tag{6.13}$$

In this particular implementation, for the 6-stage charge pump: V_{DD} = 1.8 V, R1=50 K and R2=450 K and for 19-stage charge pump: V_{DD} = 1.8 V, R1=50 K and R2=1335 K. In past years, the regulation of the charge pump has been carried out by using different techniques.

There are various techniques implemented for regulating the output voltage.

Regulation using the supply voltage is accomplished by varying the amplitude of CLK 1 and CLK 2 [144] [145]. Another technique using variable frequency is implemented and discussed in [146]. In this work, we proposed a new technique for regulating the output voltage. The advantages of using this technique are that it is simple, it allows to bias the sensor irrespective to the leakage current, the output voltage can be varied by changing the voltage of the amplifier input.

Figure 6.30 shows the simulated transient response of the regulated 6-stage charge pump with the load current from 100 μA to 500 μA. Figure 6.31 shows the simulated transient response of the regulated 19-stages charge pump with the load current from 0 to 500 μA. The simulation was carried out with a load capacitance of 2 nF. The value of the load capacitance is calculated by the equation $C_{Load} = (\mathcal{E}_{Si} \times A)/d$, where $\mathcal{E}_{Si}$ is the dielectric constant of silicon which is equal to 11.7 $\times$ $\mathcal{E}_0$, A is the area of the final TowerJazz CMOS chip with the dimensions of 2 cm $\times$ 2 cm, d is the depth of the p-epitaxial layer (18-25 μm). A start-up switch circuit was designed to avoid any latch-up issues. To properly define the sensor bias during start-up when the charge pumps are not yet operational, special start-up switches are implemented in each stage of the charge pumps. The design of the start-up switch circuit is described after this section. Figure 6.32 shows the simulated regulated output response of the 6-stage and the 19-stage charge pumps. Both these versions show stable response with respect to the load current. The design was simulated at the different temperature and corners available in the simulation library.

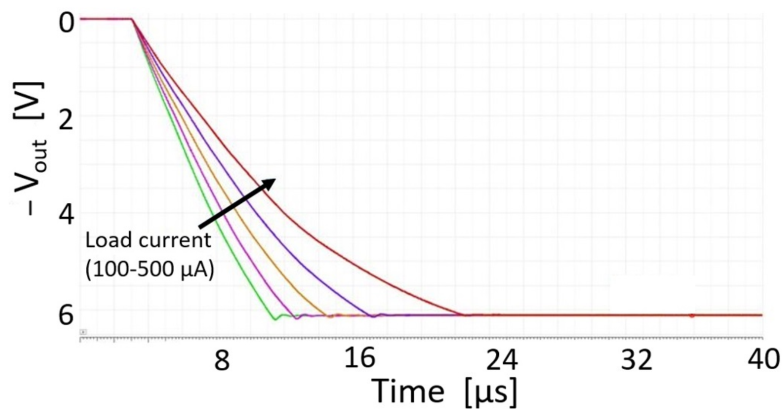


Figure 6.30. – Simulated transient response of the 6-stage closed loop charge pump with the pumping frequency of 640 MHz. Simulated for load currents between 100 μA and 500 μA in steps of 100 μA.

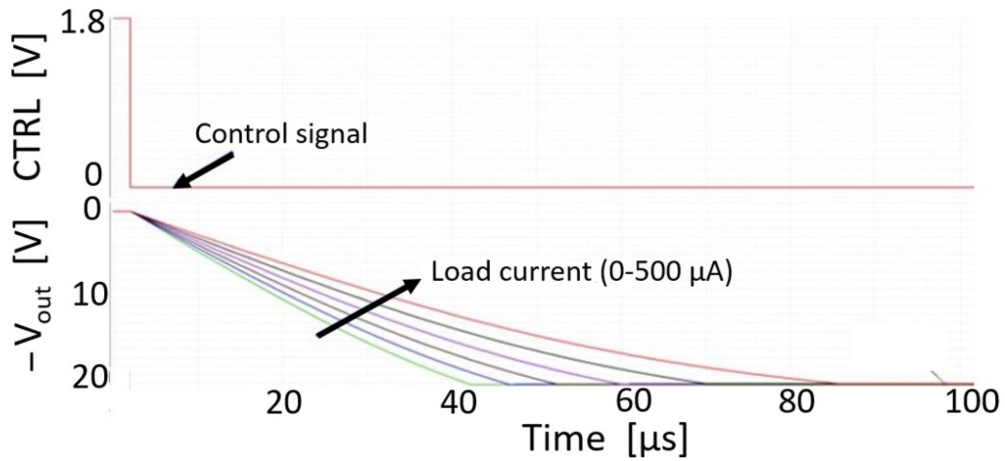


Figure 6.31. – Simulated transient response of the 19-stage closed loop charge pump with the pumping frequency of 640 MHz. Simulated for load currents between 0 and 500 μA in steps of 100 μA.

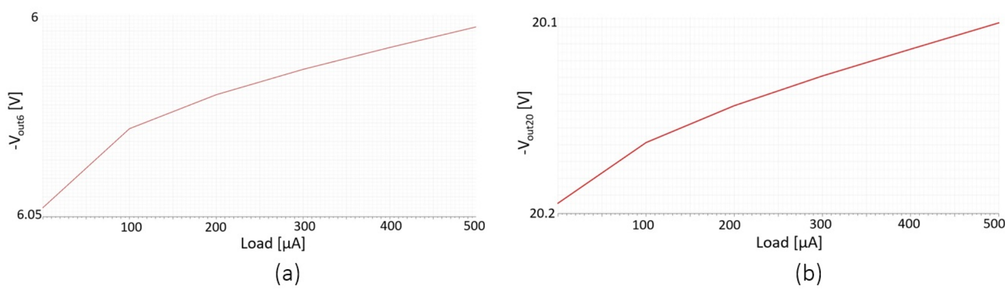


Figure 6.32. – (a)(b) Regulated output voltages for the 6-stage and the 19-stage charge pumps with increasing load current up to 500 μA.

6.4.4. Design of the start-up circuit

A start-up circuit is needed to ensure proper pumping action and to avoid latch-up when the power supply of the chip is turned on. We need a special switch that can cope with -6 V and -20 V when the charge pumps are not operational. This was not possible by using a single transistor since if we would do so the junctions inside the transistor would breakdown. Figure 6.33 shows the sketch of the start-up circuit. This start-up circuit has several switches which are stacked together. A single stage switch consists of a PMOS transistor, an NMOS transistor and a resistor. The resistor acts as a pull-up and pull-down resistor depending on the mode of operation. The value of the resistor was chosen as 20 KΩ. The gate of transistor MP0 is always connected to ground. The start-up switches are implemented in each stage of the charge pumps. Let us assume that the output of a 6-stage charge pump is connected to this switch. When the control signal is logic 0, the source of the transistor MP0 will be logic 1 and this creates a V_{GS} of -1.8 V which would turn ON the transistor MP0. At the same time, the resistors will act as a pull-up device and pull the -6 V in different stages. In this way, the voltage across each transistor will be less than -1.8 V. Conversely, when the control signal is logic 1, the source of the transistor MP0 is logic 0. This makes the transistor MP0 to go in OFF state. The resistor in each stage now acts as a pull-down device and makes the charge flow through the path of NMOS transistors. By applying the control signal to logic 1, these switches tie the p-well and the substrate voltages to ground, which defines the output voltage of the charge pump before activation. The transistors MN1-MN6 operate in the linear region and the simulated on-resistance of the start-up switch is 51 Ω (respectively 56 Ω) for the 6-stage (respectively 19-stage) charge pump variant.

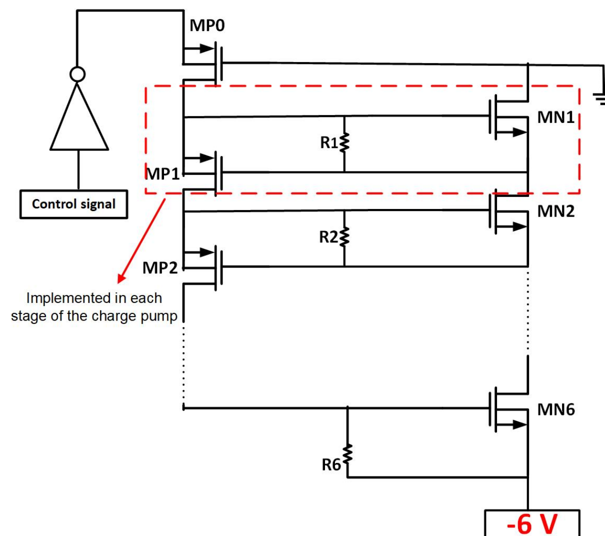


Figure 6.33. – Schematic of the start-up circuit.

Charge Pump ASIC Layout

The charge pump test chip was submitted to the foundry for fabrication. The size of the test chip is 3 mm × 500 μm and the layout is shown in figure 6.34. There are 21 pads located at the bottom of the chip which are used for powering and communicating. These pads are listed in table 6.3. The core is powered with a supply of 1.8 V.

Table 6.3. – Charge pump pads list

Pad	Name	Function
1	RON	ON-resistance of switch test structure
2	$VTCRL_{SW}$	Control for switch test structure
3	IN_{SW}	Input for switch test structure
4	OUT_{20}	Output of 19-stage charge pump
5	SUB	Substrate
6	AVDD	Power supply
7	AVSS	Ground
8	$VCTRL_{20}$	Control of the start-up switch for 6-stage charge pump
9	$VREF_{20}$	Reference voltage for 6-stage charge pump
10	IN_{20}	Input for 19-stage charge pump
11	$IBIAS_{20}$	Biasing current for 19-stage charge pump
12	OUT_6	Output of 6-stage charge pump
13	AVDD	Power supply
14	AVSS	Ground
15	$VCTRL_6$	Control of the start-up switch for 6-stage charge pump
16	$VREF_6$	Reference voltage for 6-stage charge pump
17	IN_6	Input for 6-stage charge pump
18	$IBIAS_6$	Biasing current for 6-stage charge pump
19	RX_{BIAS}	Current for the LVDS receiver
20	IN_N	Differential negative input
21	IN_P	Differential positive input

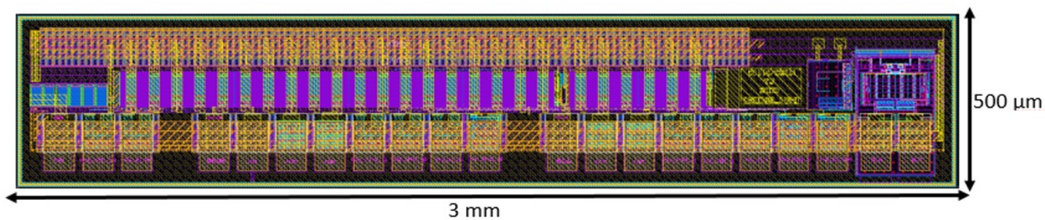


Figure 6.34. – Charge Pump test chip layout.

6.4.5. Experimental results

Five charge pump test chip samples were received in February 2019. In the first part of this section, the laboratory experimental setup used to test the charge pump is described. In the second part, the laboratory measurement results are shown. The charge pump test chip contains three test structures: the 6-stage charge pump, the 19-stage charge pump, and the start-up switch.

Experimental Setup

The test setup to characterize the charge pump test chip is schematized in figure 6.35. A dedicated LabVIEW software was developed as GUI to provide and monitor that the correct voltage and current values are sent to the chip. A Picosecond Pulse Labs Model 12050 clock generator was used to provide the square wave clock differential signals to the LVDS receiver placed inside the test chip. This instrument can provide differential clock signals with a range of 400 MHz to 6.25 GHz in terms of frequency. The output voltages of the charge pumps were captured using a digital oscilloscope. The DC power supply, reference voltage and biasing current values were provided from a power supply system (set of different modules). Only one test structure was tested at a time. The measurements were performed at room temperature (20°C).

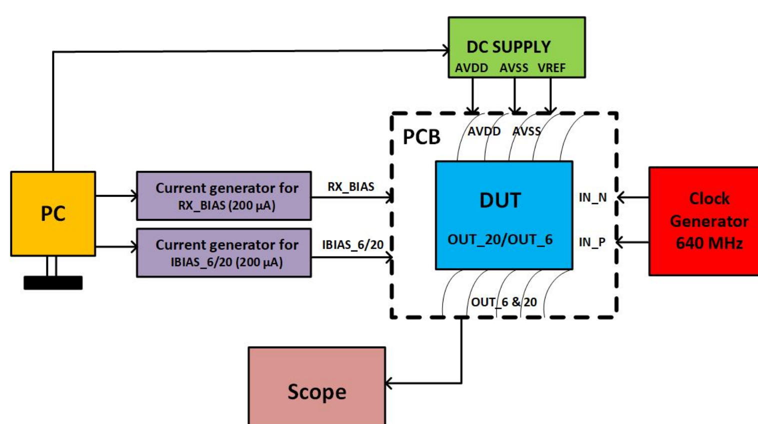


Figure 6.35. – Charge pump test setup diagram.

Measurement results

A die photograph of the fabricated charge pump test chip is shown in figure 6.36. The charge pump was characterized and the measured results were compared with the simulation results. Measurements were carried out with an external load ceramic capacitor of 2.2 nF. Figure 6.37(a)(b) shows the measured transient responses of the closed loop 6-stage charge pump and the 19-stage charge pump respectively with the pumping frequency of 640 MHz. From

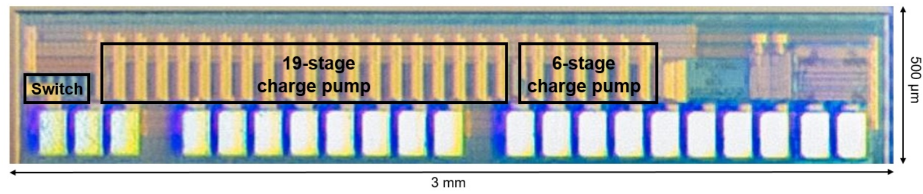


Figure 6.36. – A die photograph showing circuits designed in a charge pump test chip.

these plots, we could conclude that during the start-up, the switch keeps the output voltage for both the 6-stage and the 19-stage charge pump to 0 V. Once the control signal of the switch is disabled then the charge pumps are operational and regulate to their respective voltages. The proposed charge pump circuit

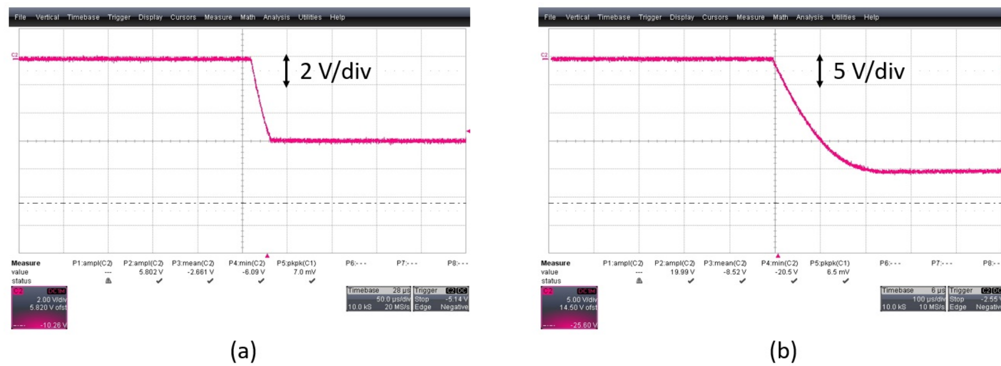


Figure 6.37. – (a) Measured transient output response of the 6-stage charge pump. (b) Measured transient output response of the 19-stage charge pump.

has additional flexibility in the design. The output voltage of the charge pump can be varied by changing the voltage of the amplifier input. Figure 6.38 (a)(b) shows the measured output voltage as a function of V_{ref} for the 6-stage and the 19-stage charge pumps respectively. Furthermore, the output voltages for both charge pumps were measured for different load currents. The load current was increased from 0 to 500 μA. Figure 6.39 (a)(b) shows the measured output voltage response by varying the load current of the 6-stage and the 19-stage charge pumps respectively. The 6-stage charge pump regulates the output voltage to -6 V up to the load current of 500 μA, whereas the output voltage of the 19-stage charge pump is regulated to -20 V up to 300 μA and then gradually decreases with higher load current. By increasing the number of stages in the charge pump circuit, the pumping efficiency goes down and this behaviour needs to be carefully investigated in the future design. The simulated value was above 50 Ω

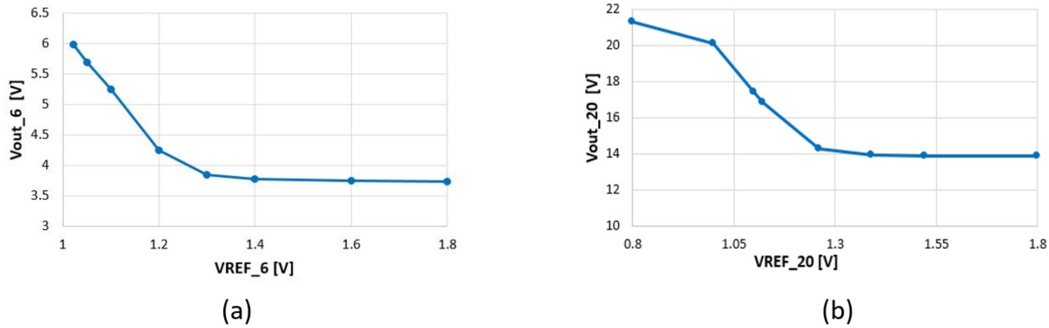


Figure 6.38. – (a) Measured output voltage as a function of V_{ref} for the 6-stage charge pump. (b) Measured output voltage as a function of V_{ref} for the 19-stage charge pump.

because of the presence of a 50 Ω resistor inside the pad. The measured on-resistance is around 60 Ω.

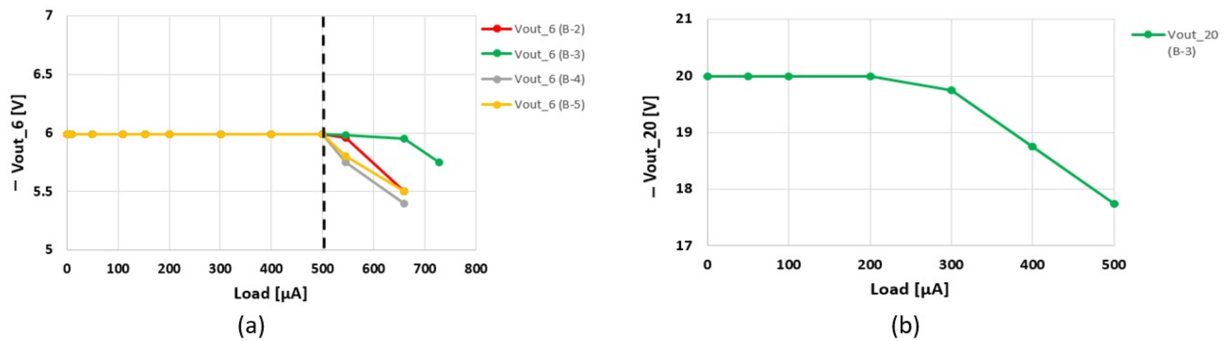


Figure 6.39. – (a) Measured output voltage as a function of load current for the 6-stage charge pump. (b) Measured output voltage as a function of load current for the 19-stage charge pump.

6.5. Summary

This chapter began with a short description of the developments in TowerJazz 180 nm sensor technology. These indicate that the depletion region could be extended up to the edges of the pixel if slight modifications were made to the process. Based on this process modification, two large demonstrators: TJ-MALTA and TJ-Monopix were produced on a high-resistivity material for the ATLAS Phase-II upgrade. After getting promising results from these demonstrators while characterizing them in the laboratory, new developments started on

the implementation of a Serial Powering scheme.

Within the ATLAS collaboration, new developments occurred for Serial Powering with monolithic CMOS sensor in the TowerJazz technology with the design of two main blocks: a Shunt-LDO regulator and a charge pump. Both circuits were prototyped in TowerJazz 180 nm CMOS technology with a chip area of 4 mm $\times$ 2 mm and 3 mm $\times$ 500 μm respectively. The proposed Shunt-LDO regulator was designed to polarize the pixel matrix and all the peripheral blocks. The charge pump takes care of the sensor biasing. The Shunt-LDO regulator was composed of elementary blocks, which supply specific power domains. The Shunt-LDO regulator block was composed of two parts. The first one was the shunt regulator itself, which performs the first regulation and shunts the excess current with no dropout. The second one was the voltage LDO (low-dropout) regulator, which performs the second regulation with a dropout of 200 mV. The test chip consisted of 126 elementary Shunt-LDO regulator, divided into four domains and is capable of generating the constant required voltage of 1.8 V with a maximum shunt current of 1.4 A. In monolithic CMOS detectors, biasing of the sensing part requires deriving a high voltage locally at module level to deplete the sensor. In the TowerJazz modified process, the pwell and the substrate were separated by the depleted sensitive layer and could be biased at different voltages. When the substrate was biased much more negatively, it resulted in an increased electrical field, better signal charge collection speed and improved radiation tolerance. Two charge pump variants were designed to deliver 500 μA each at up to -6 V and -20 V to bias the TowerJazz sensor [147].

After receiving the prototype shunt-LDO and charge pump blocks in February 2019, a single block of shunt-LDO regulator was first tested independently with varying the DC input current from 0 to 20 mA. The measurements agree well with the simulation, with the exception that the bandgap value was different from the one expected from simulations. Various measurement on different bandgaps of different chips showed that the reference voltage "Vref" measurements were consistent among themselves with a mean value of 870 mV, which was less by around 100 mV than the simulated value. Secondly, a charge pump test chip was also characterized in the laboratory. The charge pump test chip contained three test structures: the 6-stage charge pump, the 19-stage charge pump, and the start-up switch. The measurements of the 6-stage charge pump matches very well with the simulations while the 19-stage charge pump is regulated to -20 V up to 300 μA and then gradually decreased with higher load current. This effect can be easily studied and corrected in future submissions.

Conclusion

New generation silicon pixel detectors will be an essential part of the ATLAS ITk detector where they will be used for tracking and vertexing. In this PhD thesis research work, design and characterization for the depleted CMOS sensors in the LFoundry 150 nm, AMS 180 nm and TowerJazz 180 nm technologies have been performed. Linearity simulations of the analog front-end were carried out for two large demonstrators LF-CPIX (based on a hybrid pixel concept) and LF-Monopix1 (based on a monolithic pixel concept) using LFoundry 150 nm CMOS technology. The LF-CPIX demonstrator comes on a high resistivity wafer, and was characterized intensively in the laboratory and also irradiated under a proton beam up to 150 MRad at room temperature. The chip has shown a very promising behaviour and proved to have good radiation hardness up to 150 MRad of 24 GeV protons (NIEL: 2.7×10^{15} n_{eq}/cm^2). The chip was properly cooled and all the flavours inside the chip were functional with a very limited increase in the noise, mean threshold value and leakage current.

The second aim of this thesis was to study and design Single Event Upset (SEU) tolerant memories in different depleted CMOS sensor technologies. Three test chips in AMS 180 nm, TowerJazz 180 nm and LFoundry 150 nm CMOS technology were designed for the upgraded ATLAS pixel detector. In order to reach the desired specifications, several SEU and TID-hardening techniques were evaluated, and a final approach was chosen and implemented for the first time in the test chips for assessment. CAD simulations have been carried out to investigate the sensitivity of the memories to SEU. To minimize the risk of SEU, the memories were designed such that they are compact and the critical charge to generate an SEU becomes as large as possible. This was implemented in various ways such as increasing the transistor dimensions and the distance between two sensitive nodes. Furthermore, because of the relevance of the SEU problem in the HL-LHC environment, few versions of various architectures (DICE and Triple Redundancy Logic designs) were designed in order to compare them under the irradiation environment. The AMS and TowerJazz prototypes which were designed were fully functional after reception from the foundry, whereas the LFoundry prototype is expected to be received by November 2019. The AMS SEU tolerant chip was also exposed to 24 GeV protons at Proton Synchrotron in CERN up to a TID of 165 MRad to measure the SEU cross-section. The irradiation test results obtained demonstrate good robustness of the DICE and TRL circuits which make it suitable for the target environment. The designed DICE latch was 15 times more tolerant to SEU when compared to the standard latch. According to the specifications, the hit rate in the fifth layer of ITk is given as 3.5×10^7 pr/sec/cm^2. The estimated AMS CMOS-1 chip will consist of a pixel matrix of 57288 pixels. Inside the pixel, 5-bit memory will be used. Therefore, the total number of bits

for the whole chip will be 286440. Using the cross-section values obtained from measurements, the mean time between 2 upsets (MTBU) for DICE latches in 1 front-end chip containing around 58 K pixels can be estimated to 49 s. The two other test chips in TowerJazz 180 nm and LFoundry 150 nm CMOS technology are planned to be irradiated in Q4 of 2019 under a proton beam to measure the SEU cross-section.

Serial Powering is foreseen as the new powering scheme for the Phase-II upgrade of the ATLAS pixel detector. Compared to parallel powering, the proposed Serial Powering scheme allows a significant reduction in power losses and material budget. On-chip shunt regulators are used to generate the local supply voltage from the input current to provide power to the integrated circuits. A Shunt-LDO regulator prototype has been implemented and produced in the TowerJazz 180 nm CMOS technology. Moreover, in the modified process of TowerJazz 180 nm CMOS technology, the p-well and the p-substrate must be kept at a constant potential with respect to the module's ground potential. Two different voltage levels are used since the p-well cannot tolerate being biased to less than -6 V while the p-substrate can be biased much more negatively. A simple and robust solution for biasing the monolithic CMOS sensor by using a negative charge pump was proposed. Two prototypes operating with a pumping frequency of 640 MHz, with 6-stage and 19-stage charge pumps were designed and fabricated in the modified TowerJazz 180 nm technology to provide negative bias of -6 V and -20 V, respectively. Both the variants of the charge pump were designed to produce a stable response up to 500 μA of load current. Few samples of the charge pump test chip were characterized and the measured results demonstrate good performance which could be used to bias the CMOS sensor. The next steps include the characterization of the charge pump prototype and the construction of test systems with several ICs in series to demonstrate the functionality of the charge pump in conditions similar to the experiment. Furthermore, some additional improvements are also possible in the design depending on the specifications. This solution could be used for CMOS modules in ATLAS ITk or in other future applications. In the framework of this thesis, several of the major challenges of pixel detector developments for HL-LHC have been addressed for the first time in a monolithic technology.

A. Appendix

Tracking and vertexing in HEP

At LHC, tracking is a basic tool for experiments used for momentum and vertex measurements. In order to separate interesting physics events from the pile-up, we need to focus on measuring the transverse momentum of the charged particles and also reconstructing the primary vertices of a collision. Moreover, tracker plays a vital role in the detection of secondary vertices for the identification of jets from hadrons containing heavy quarks as well as τ-leptons.

Radiation length

When a highly charged particle interacts with the nucleus of the target atom, a fraction of its kinetic energy is emitted in form of photons. This mechanism is called bremsstrahlung and is shown in figure A.1. During this process, the energy loss per unit length is directly proportional to the incident particle and is given by:

$$-\left(\frac{dE}{dx}\right) = \frac{E}{X_0} \tag{A.1}$$

where X_0 is the radiation length. Thus, after traversing a material of thickness x, the energy of a particle with an incident energy E_0 can be calculated in the following way:

$$E(x) = E_0 \times e^{-\frac{x}{X_0}} \tag{A.2}$$

The radiation length can be defined as the mean distance after which the charge particle energy is reduced to $\frac{E_0}{e}$ due to bremsstrahlung. It is a material property and can be approximated by [148]:

$$\rho X_0 = \frac{716.408gcm^{-2} \times A}{Z(Z+1) \times log(287/\sqrt{Z})} \tag{A.3}$$

where ρ is the density, A is the mass number and Z is the atomic number of the material.

The radiation length is a quantity used to define the material budget of the detector. It is also commonly used to quantify the detector mass, also referred in the following as material budget. The detector material is then expressed as a thickness is units of X0. Moreover, it is also used to characterize electromagnetic process that takes place in the Coulomb field of the nucleus.

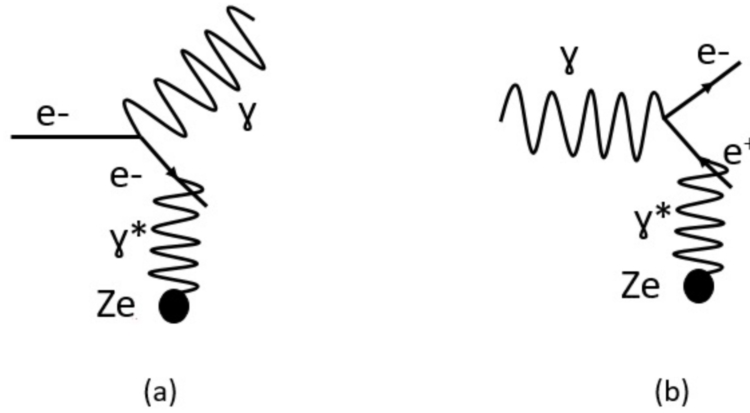


Figure A.1. – Feynman diagrams for (a) bremsstrahlung and (b) photon conversion.

Multiple scattering

When a charged particle traverses a material, it is scattered many times due to the interactions with the Coulomb field of nuclei. This effect is called multiple scattering. Moliere theory is used to describe the distribution of scattering angles. It behaves like Gaussian at small angles, and like Rutherford scattering at larger angles. Using the Gaussian approximation, on any plane the projected distribution of the scattering angle is given by:

$$f(\theta_{plane})d\theta_{plane} = \frac{1}{\sqrt{2\pi}\theta_0} exp\left(\frac{\theta_{plane}^2}{2\theta_0^2}\right) d\theta_{plane} \tag{A.4}$$

where f(θ_{plane}) is centred around zero and is shown in figure A.2. The standard deviation θ_0 is the width of the distribution and is calculated by [149] :

$$\theta_0 \approx \frac{13.6MeV}{p \times v} \times \sqrt{\frac{l}{X_0}} \tag{A.5}$$

where p is the momentum, v the velocity of the incident particle and $\frac{l}{X_0}$ is the thickness of the scattering medium in radiation lengths.

The particle trajectory has a random deflection caused by the multiple scattering that can reduce the accuracy of the track position measurement. As a consequence, the resolution of the tracker is degraded with the effect being the strongest for low momentum particles. According to equation A.5 the standard deviation of the scattering angle distribution is decreased by using a material with large radiation length.

Energy deposition of photons

There are mainly three processes by which photons interacts with a material, namely: pair production, photoelectric effect and Compton effect. In the pair

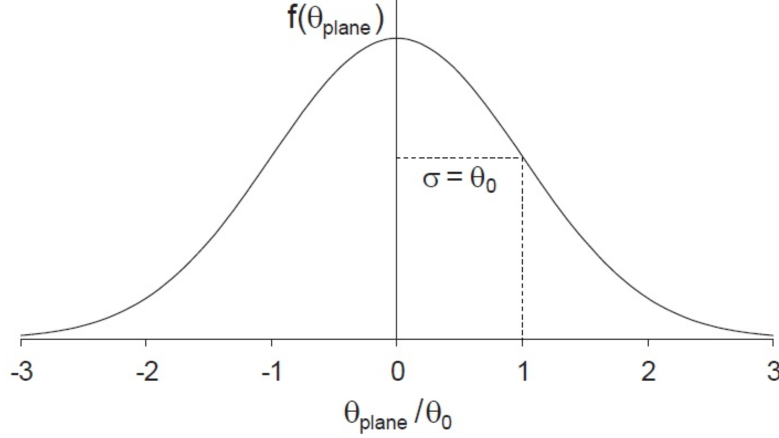


Figure A.2. – Angular distribution of the multiple scattering angle projected on a plane.

production process, the minimum energy of a photon in pair production process must be greater than the sum of twice the rest mass of an electron and the recoil energy of an electron. For physics measurements at LHC experiments, the photons which more than 1 GeV of energy are relevant. It makes difficult for a low energy photon to enter the calorimeter system and then it is more difficult to reconstruct it from electron and positron tracks. However, for a large photon energies, the pair-production cross section can be approximated in the following way [148]:

$$\sigma_{pair} \approx \frac{7}{9} \times \frac{A}{\rho N_A} \times \frac{1}{X_0} \tag{A.6}$$

where X_0 is the radiation length.

Transverse momentum resolution

According to [150] the transverse momentum resolution is shown in figure A.3 and calculated by the quadratic sum of point and multiple scattering and is given as:

$$\frac{\sigma_{p_T}}{p_T} = \sqrt{\left(\frac{\sigma_{p_T}}{p_T}\right)^2_{point} + \left(\frac{\sigma_{p_T}}{p_T}\right)^2_{MS}} \tag{A.7}$$

For a detector with layers equally spaced at radii r_0, r_1..., r_N from the interaction point, the point resolution can be calculated as:

$$\left(\frac{\sigma_{p_T}}{p_T}\right)_{point} = p_T \times \frac{\sigma}{0.3BL^2} \times \sqrt{\frac{720N^3}{(N-1)(N+1)(N+2)(N+3)}} \tag{A.8}$$

where N+1 is the number of layers inside a positive sensitive detector, B is the magnetic field, L is the detector length and σ is the intrinsic spatial resolution of the elementary elements. Thus, a high value of the resolution is achieved by low value of p_T. Moreover, strong magnetic field and large value in the length also improves the resolution.
The contribution from the multiple scattering in the detector material can be calculated by:

$$\left(\frac{\sigma_{p_T}}{p_T}\right)_{MS} = \frac{1}{0.3B} \times \frac{0.0136}{\beta} \times \sqrt{\frac{C_N}{X_0 L}} \tag{A.9}$$

where C_N is a coefficient dependent on the number of layers inside the detector and is equal to 1.3 within a 10% accuracy [151]. According to the equation A.9, when the multiple scattering dominates, the relative momentum resolution has a weak dependency on the spectrometer length.

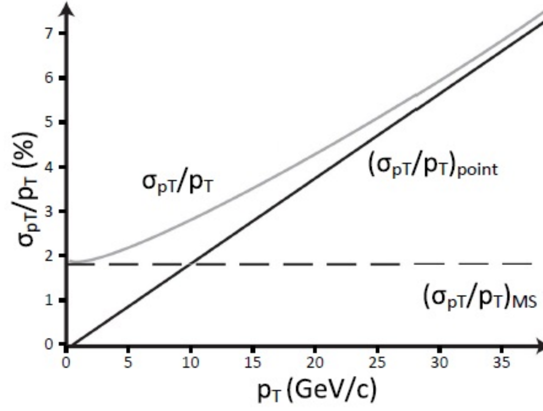


Figure A.3. – The total transverse momentum resolution.

Vertex resolution
As described in [152], by using a one-dimensional detector arrangement, the vertex resolution can be derived and is illustrated in figure A.4. The 2 detector layers are placed at a distance r_1 and r_2 from the interaction point, with $r_2 > r_1$ and resolutions σ_1 and σ_2. The vertex resolution can be calculated as the sum of two quadratic terms and is given by :

$$\sigma_{vtx} = \sqrt{\left(\frac{r_1}{r_2 - r_1} + 1\right)^2 \sigma^2 + (2r_1 - r_0)^2 (13.6MeV)^2 \frac{x}{X_0} \frac{1}{p^2}} \tag{A.10}$$

where σ is the intrinsic spatial resolution for both layers, r_0 is the radius of the beam pipe. The major contribution comes from the multiple scattering which is described by the last term. The large thickness of the detector and low mo-

mentum particles are dominated by multiple scattering. To improve the vertex resolution, the material budget has to be minimized.

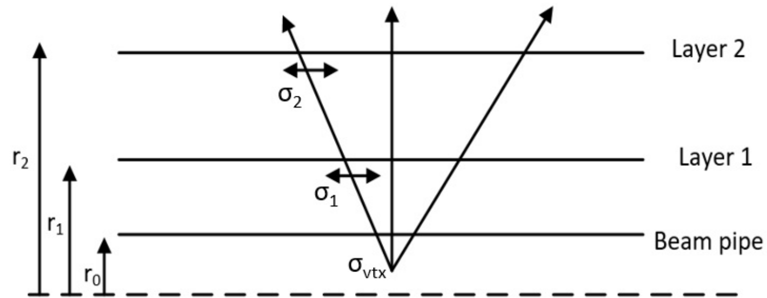


Figure A.4. – Sketch of a one-dimensional vertex detector arrangement with 2 layers which are placed at a distance r_1 and r_2 from the interaction point.

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