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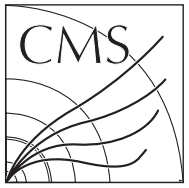

**The Compact Muon Solenoid Experiment**

**Conference Report**

Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland

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# Time Digitization firmware for the new Drift Tubes electronics for HL-LHC

Alvaro Navarro Tobar for the CMS Collaboration

**Abstract**

The electronics of the CMS Drift Tube (DT) chambers will need to be replaced in order to cope with the increased occupancy and rates at the high luminosity phase in the HL LHC (High-Luminosity Large Hadron Collider). A new electronic system is being designed, that will allow forwarding signals from all DT chambers at the maximum resolution to the backend system, where improved trigger primitives generation will take place. The on-detector boards, which will be attached to the DT chambers inside the CMS wheels are called OBDT (On Board electronics for Drift Tubes) and are built around a Microsemi Polarfire FPGA that performs the time digitization of the chamber signals at $\sim$ 1 ns resolution, and forwards them to a high-speed link, optimizing bandwidth and latency. Thirteen prototypes of this board have been installed in parallel to the present system in the CMS detector, fully instrumenting one out of sixty sectors, and are taking data routinely integrated in the CMS DAQ chain. The firmware implementation of this FPGA performs the time digitization of up to 240 input channels, the high-speed link implementation and several slow control functionalities, including a very thorough clock and reset signals distribution that allows ensuring that the time measurements are stable across power cycles and reconfigurations of all the CMS clock chain. The description and implementation details, together with the results of the performance of this firmware in the data taking campaigns at CMS are presented in this contribution.

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# Time Digitization firmware for the new Drift Tubes electronics for HL-LHC

Álvaro Navarro-Tobar on behalf of the CMS Collaboration

***Abstract*– The electronics of the CMS Drift Tube (DT) chambers will need to be replaced in order to cope with the increased occupancy and rates at the high luminosity phase in the HL-LHC (High-Luminosity Large Hadron Collider). A new electronic system is being designed, that will allow forwarding signals from all DT chambers at the maximum resolution to the backend system, where improved trigger primitives generation will take place. The on-detector boards, which will be attached to the DT chambers inside the CMS wheels are called OBDT (On Board electronics for Drift Tubes) and are built around a Microsemi Polarfire FPGA that performs the time digitization of the chamber signals at ~1 ns resolution, and forwards them to a high-speed link, optimizing bandwidth and latency. Thirteen prototypes of this board have been installed in parallel to the present system in the CMS detector, fully instrumenting one out of sixty sectors, and are taking data routinely integrated in the CMS DAQ chain. The firmware implementation of this FPGA performs the time digitization of up to 240 input channels, the high-speed link implementation and several slow control functionalities, including a very thorough clock and reset signals distribution that allows ensuring that the time measurements are stable across power cycles and reconfigurations of all the CMS clock chain. The description and implementation details, together with the results of the performance of this firmware in the data taking campaigns at CMS are presented in this contribution.**

## I. Introduction

The DT chambers are responsible for identifying, measuring and triggering muons in the central region of the CMS [1] detector, and are expected to continue doing so safely during HL-LHC [2]. However, the operating conditions during HL-LHC will be much harsher, with increased occupancy, radiation and Level 1 trigger rates that will change from 100 kHz to 750 kHz. Particularly, this last feature will force to replace the DT on-detector readout electronics with a new system, called OBDT [3], [4], as part of what is known as the Phase-2 upgrade of the detector. These new electronics will replace the existing system during the Long Shutdown 3, which is expected in 2024-2026, right before the start of HL-LHC.

Profiting from the new electronic developments and high-speed links, the new electronics attached to the DT chambers will perform the time digitization of all of the incoming signals and transmit them at the maximum resolution without data reduction through high speed optical links to the backend electronics. This backend, away from the harsher radiation environment, will be built with high-performance digital electronics that allow building complex trigger primitive algorithms operating in real time. It will perform full-resolution trigger algorithm [5], similar to the present offline muon segment reconstruction, and will buffer the data for event building and delivery to the CMS Data Acquisition system upon Level 1 trigger reception. A diagram of the different architecture between present system and the expected in HL-LHC is shown in Fig. 1.

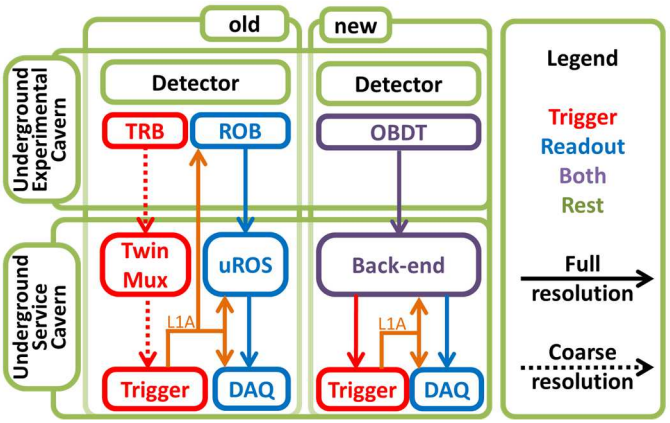


Fig. 1. Diagram showing the differences between the present and upgraded data acquisition architecture for the CMS DT subdetector.

## II. The OBDT Board

Two types of boards with very similar functionality are foreseen, one board that will process the signals from the Phi view of the DT chamber (OBDT-phi) and one for the Theta view (OBDT-theta) which requires among others, different input connectors. Both of them are based on the same prototype board (OBDTv1) which is the one in which we have developed the present work and that is the one currently being used for the validation campaigns at the CMS detector, in the so-called DT Slice Test [6]. An image of the OBDTv1 board is shown in Fig. 2.

The OBDT electronics will need to be installed attached to the DT chambers, in an area of high integration and reduced cooling (which will be carried out through conduction to water pipes). Accordingly, apart from requirements of radiation tolerance and high integration (~240 channels are required per board), minimizing the power consumption is an important characteristic of the new electronics.

The time resolution required for the DT signals is around 1 ns, which is attainable by a FPGA-based TDC (Time to Digital Converter). The OBDT is foreseen to be built around the Microsemi Polarfire FPGA MPF300T-1FCG1152E, in which we have implemented a multi-channel TDC that

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performs the time digitization of the input signals with a resolution of 25/30 ns (0.833 ns).

Fig. 2. Image of the OBDT v1 prototype board for the time digitization of the CMS DT chamber signals.

The signals that arrive to the OBDT come from the FEB (Front End Boards), located inside the DT gas volume, that contain the amplifiers, shapers and discriminators of the chamber signals, delivering 50-ns-wide LVDS-like pulses for each muon that crosses the chamber. These signals are received as differential pairs and each OBDT is capable of digitizing up to 240 input channels.

The OBDT is responsible for digitizing these signals and merging them into a serialized stream that is sent to the backend electronics through a dedicated optical link.

The communications of the OBDT are carried over high-speed optical links. The OBDTv1 prototype uses two different commercial optical modules: a SFP+ module and a QFSP. In the successive versions, however, the commercial optical transceivers will be replaced by the CERN's VTRX+ [7].

The OBDTv1 has a GBTX chip from CERN [8], which is in charge of the CMS clock distribution and fast synchronization commands. It maintains a bi-directional 4.8 Gbps link to the control and monitoring back-end, using the aforementioned SFP+ optical transceiver. In the next OBDT versions, it is planned to replace the GBTX by the LpGBT ASIC, which works at 10.24 Gbps [9]. These chips are in charge of receiving the fast synchronization, receiving the LHC clock and delivering it to the FPGA. It also carries communication channels to the FPGA and the SCA chip.

The SCA (Slow Control Adapter) chip is a CERN-developed ASIC, performing detector control tasks [8]. It incorporates several channels of ADC, DAC, I2C and GPIO interfaces, and is used, among other tasks, for monitoring tasks (temperature, voltages), generation of the FEB threshold and pulse width values, generation of the calibration signals for the DT chambers and remote FPGA reprogramming.

The OBDTv1 features a power supply subsystem based on an array of linear DC regulators and basic power safety system. This safety system has been further developed and redesigned for the next prototypes.

## III. OBDT Firmware Overview

The core of the firmware at the Microsemi Polarfire FPGA in the OBDT is devoted to the time digitization of the input signals, and that is where most of the logic resources are used for. This time digitization is performed by sampling the input signal from the FEB with the input deserializer in the FPGA's Input-Output Digital (IOD) block, and detecting the bit transitions in the parallel output word. The reference high-speed clock runs at 600 MHz and deserialization is performed at double-data rate, thus sampling the input signals at 1200 MHz. A diagram of this TDC is shown in Fig. 3.

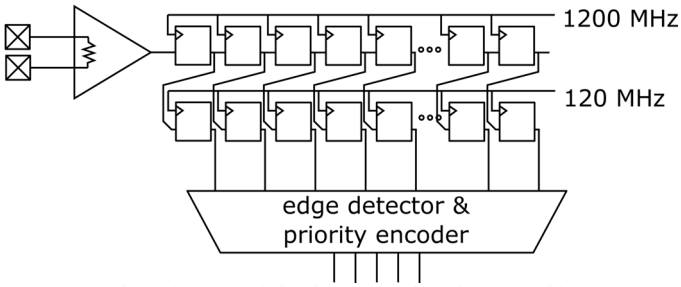


Fig. 3. Schematic view of the deserializer-based TDC architecture. Note that the input differential buffer incorporates a termination resistor only in General Purpose I/O (GPIO) banks; in High-Speed I/O (HSIO) banks' inputs, the lines are terminated with a discrete external resistor. The edge detector and priority encoder are implemented in the FPGA fabric resources.

The FPGA input deserializers are typically conceived and designed for application in high-speed serial data communications, and thus their utilization as time digitizers imposes some differences in the operating conditions that must be taken into account.

In data reception, the sampling is typically done on the center of the eye, whereas in time digitization the transition edge has a uniform probability distribution across the sampling period. This results in a higher probability of coincidence of the edge with the sampling, which may cause metastability in the first flip-flop that has to be characterized, and its effect included in the accuracy of the TDC.

Additionally, in high-speed serial data transmission applications, there's the possibility to use the control characters to align the phase of the transfer to the slow clock domain to the word boundaries by producing bit-slips in the output registers. This process is dynamic, and thus, the default reset configuration of the deserializer is not designed to achieve a perfect phase reproducibility.

In TDC applications, however, reproducibility and time stability across reboots is a key parameter. Unlike with data reception, it cannot be calibrated by inspection of the incoming data, unless it is possible to produce an electrical reference signal after each reset, which is an additional undesirable operation constraint for the system. We have managed to cope with this challenge by fine-tuning the clock and reset distribution in the FPGA, achieving < 1 least significant bit reproducibility across system reboots.

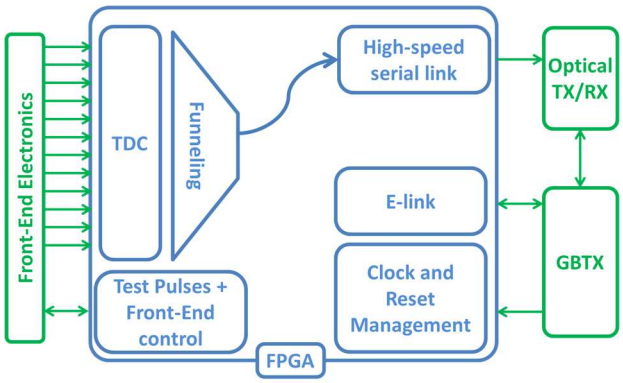


Fig. 4. Schematic diagram of the main functions of the FPGA firmware, as well as connections to external components or systems.

In addition to the time digitization, the OBDT firmware needs to perform hit funneling and merging for sending the data to the next level in the electronics chain. Each OBDT can accept a maximum single-channel rate of 2 MHz, which corresponds to the maximum output rate of the FEB.

A readout mechanism has been designed to arbitrate the delivery of these hits into an output data stream that will be sent to the backend electronics. Because the OBDT data are part of the trigger chain, care must be taken to minimize the maximum latency and data loss, which occurs when the firmware fails to deliver hits before the maximum latency budgeted for this stage. In the current firmware, the latency is limited by incorporating shallow buffer elements in the different stages of the funneling, which produce overflows under high load, and thus discard data that would be sent with excessive delay.

The data are transferred out of the experimental cavern using high-bandwidth serial protocols developed by CERN for their GBTX and LpGBT chips. Although not strictly necessary, because this data stream does not go through the GBTX chip, it was chosen to implement the FPGA version of its protocol for the delivery of the hits to the Data Acquisition backend. This protocol runs at 4.8 Gbps, and is able to deliver 3 hits per BX. Link reliability tests have been performed with no errors in the lab for several hours. In the CMS experiment, also, all of the links are stable for hours except for one link that has errors seemingly be related to a different clock distribution scheme in the detector. At present the LpGBT firmware has also been implemented in the Polarfire FPGA, which has allowed performing tests in the laboratory with an OBDT sending the data at 10.24 Gbps.

The clock is received from the GBTX chip, and up-converted to the needed frequencies (120 MHz, 600 MHz) at the FPGA PLLs (Phase-Locked Loop).

Also through the GBTX chip, a communication channel is established to the backend for control and monitoring. The so-called E-Link offers a bidirectional 320 Mbps channel. It is used to configure different parameters inside the Polarfire FPGA and also to monitor the status of the occupancy of the different buffers and specific statistics, and is able to deliver 8 bits per LHC Bunch Crossing (BX). Out of these 8 bits, three are reserved for future use, one is used for word alignment, two are used to transmit the Bunch and Orbit Counter Reset signals (BC0, OC0), one for the so-called Test Pulse calibration signal and a final one is devoted to a low-speed serial link for configuration and monitoring. The BC0 signal is used to synchronize the electronics to the start of the LHC orbit and sets an origin to which all of the time measurements are referred. The slow serial link allows interaction with a set of configuration and monitoring registers, as well as producing custom-duration pulse signals for control of different parts of the FPGA (e.g. per-module logic resets). The command issued from the remote control system is protected by some degree of redundancy, so that register data are protected from accidental transmission errors. The configuration registers allow to control different aspects of the performance of the firmware (dead time, channel masking...). The monitoring registers cover most of the parameters that allow to assess the correct function of the different firmware sub-modules, and the performance of the system, for development, debugging, and for operation of the system.

Finally, the FPGA is also in charge of the generation of some signals used for control of the FEB, the others being controlled, as already mentioned, by the SCA chip. In particular, the FPGA takes care of producing signals for triggering the activation of Test Pulses for system calibration, and the signals required to mask them. Also, it communicates via I2C to some electronic systems that require custom low-speed communication, which is not possible with the SCA chip.

## IV. Firmware Performance at the Slice Test

The Slice Test is the first installation of the DT HL-LHC electronics in the CMS detector, which took place during Long Shutdown 2 period (2019-2021). Both the OBDT prototypes (13 boards) and 5 backend prototype boards (called AB7) have been installed covering the 4 DT chambers of sector 12 of the CMS wheel +2, and implementing the readout and triggering of the sector. This system has been fully integrated in the CMS infrastructure, using the CMS timing and data acquisition systems.

Cosmic data taking has been carried out routinely since June 2019, allowing for an extensive validation of the system, which is showing very good performance.

One of the major challenges of this slice test was to ensure that the time digitization was correct, and, particularly, that the measured time reference was not changing with reconfigurations and/or power cycles, which could take place not only in the OBDT, but also in the CMS Timing and Control Distribution System (TCDS). When this system is rebooted, the clock in the digital systems is momentarily lost, and the system needs to recover from that event. To evaluate the robustness of the electronics against these events, the calibration system of the legacy DT electronics has been used. This system allows generating simultaneous signals in all of the chamber channels. Data taking is performed aiming at measuring always the same value in this calibration signals. Results are shown in Fig. 5 in which the time measurements of

all the channels in the MB4 Superlayer 3 chamber are shown for different runs. Between runs, several reboot and power cycle actions took place. As it can be seen, the difference in time of the measured values is within the resolution of the system.

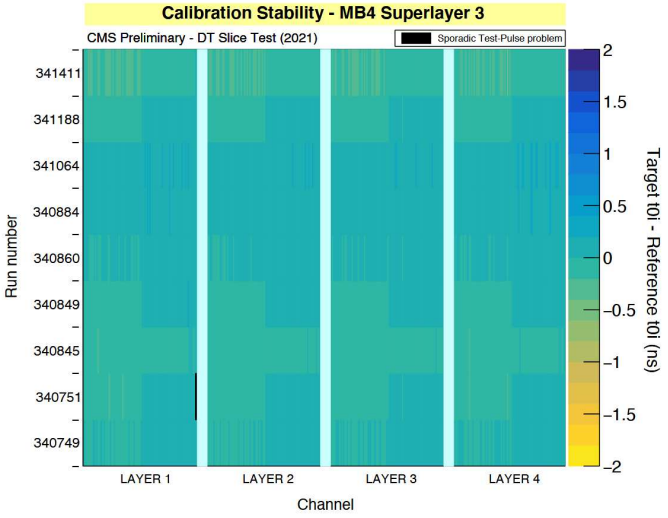


Fig. 5. Calibration stability plot for a DT Superlayer of the Slice Test (2x OBDTv1 boards). 1 wire/bin represented in the x-axis. The color indicates the difference in time calibration in Test Pulse runs for the run corresponding to the row w.r.t. a reference run. The runs were taken over several weeks, and across complete power cycles of the system (detector + OBDT + back-end) [10].

Once the time digitization and its reproducibility were validated, the readout hits could be used to reconstruct real muons coming from cosmic rays. From the time measurement of the chamber signals, and assuming a constant drift velocity, the position of the muon trajectory can be obtained. The time of the passage of the muon is an unknown quantity and can be obtained from this fit. In Fig. 6 this crossing time, obtained from the reconstruction of the muon segments on each DT chamber, is shown. As can be seen, the distribution is relatively wide within 25 ns because the muons from cosmic rays do not arrive synchronized to the 40 MHz LHC clock and thus are distributed throughout all the clock cycle range. The comparison with the results obtained from the present Phase 1 electronics is shown and, as can be seen, they are basically identical with small variations due to the fact that the time digitization resolution of both systems is different.

This, among other results, shows the excellent performance of the system in real conditions. For the following months, we plan to run the HL-LHC parallel system in collisions during Run 3, which will allow to test final pre-production prototypes under realistic conditions (radiation, magnetic field) and further refine trigger algorithms.

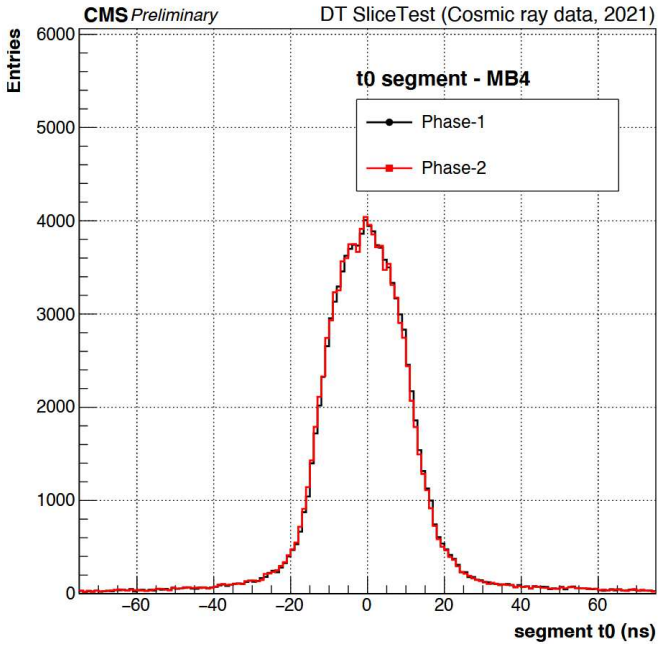


Fig. 6. Comparison of the crossing time of cosmic muons, as calculated by offline reconstruction, using Phase-1 and Phase-2 systems. The plot shows excellent agreement; small differences are due to the intrinsic precision of the calibration procedure and the different TDC resolution in both systems.

## V. Conclusions

A first prototype of the on-detector electronics for the readout of the CMS DT during HL-LHC has been built, and the firmware in charge of digitization and readout has been developed. This prototype has been installed in the CMS detector and has been taking cosmic data for the past two years showing very good performance results. As a consequence, the design and the firmware implementation of the OBDT prototype have been validated and are considered to work very satisfactorily.

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