The VELO optical and power board

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Abstract

The optical and power boards (OPB) are part of the on-detector electronics system for the LHCb Vertex Detector (VELO) and they are used in LHCb upgrade 1 which is installed in the second long LHC shutdown period. The OPBs are assembled printed circuit boards (PCBs) that are located immediately outside of the VELO detector vacuum tank, in custom made mechanical crates. They perform the following main functions: optical-electrical conversion of the high-speed data and control signals that are sent to and from the detector module; DC/DC conversion of the supply voltage that is distributed to the detector module and to the components on the OPB; local slow control of the detector module and the OPB; and monitoring of the temperatures and supplied voltages of on the detector module and the OPB. The OPB operates in an environment with radiation, a magnetic field and limited cooling facilities, which is reflected in the design. This document gives and overview of the VELO electronics system and describes in detail the design of the OPB, providing diagrams to illustrate the functionality and tables to define the connectivity.

Table of Contents

List of Figures

List of Tables

1 Introduction

This document describes the functionality of the optical and power board (OPB) for the VELO upgrade [1], used in the first upgrade of the LHCb Experiment [2] which is installed in the second long LHC shutdown 2018-2021. The OPBs are part of the on-detector electronics system of the VELO and they are the interface between the detector modules located inside the detector vacuum and the off-detector electronics located at 60 m cable distance. They interface the off-detector electronics in two ways. The control, trigger and DAQ systems are interfaced via optical fibres, and the low voltage power supplies and temperature monitoring system via copper cables. The document also gives and overview of the VELO on-detector electronics and gives some details of the other parts of that system.

Section 1.1 gives a general overview of the board and Sections 2 to 6 describes each functional block in detail. The principal design of the parts is illustrated with diagrams and the connectivity of all the components, mainly in tables. Section 7 describes the CTLE equalisation of the high-speed link and Section 8 gives the pin-out of all the connectors of the board. The schematics and design files for the OPB can be found in Ref. [3].

1.1 Optical and power board overview

The optical and power boards (OPBs) are located immediately outside the VELO detector vacuum, placed in custom crates mounted on the vacuum tank. They provide the following functionality:

- Electrical to optical conversion for the data sent from the detector module;
- Electrical to optical conversion of the timing, trigger and fast control signals;
- Electrical to optical conversion of the control signals for the components of the OPB;
- DC/DC conversion of the supply voltages for the hybrids and OPB itself;
- Monitoring of the supplied voltages on the OPB and detector module;
- Routing of the temperature monitoring signals (NTCs) from the detector module and the OPB.

Each OPB services the front-end hybrid circuits that are attached on the two sides of a VELO detector module. It communicates with the control interface boards (SOL40) [4,5] through three bidirectional optical links and transmits the data to the DAQ boards (TELL40) [5,6] through 20 optical links. It is supplied by five low voltage power supply channels, each with a voltage of 6 – 9 V[1]. A schematic overview of the on-detector parts of VELO detector is shown in Figure 1, and a schematic view of the VELO electronics and the OPB is shown in Figure 2.

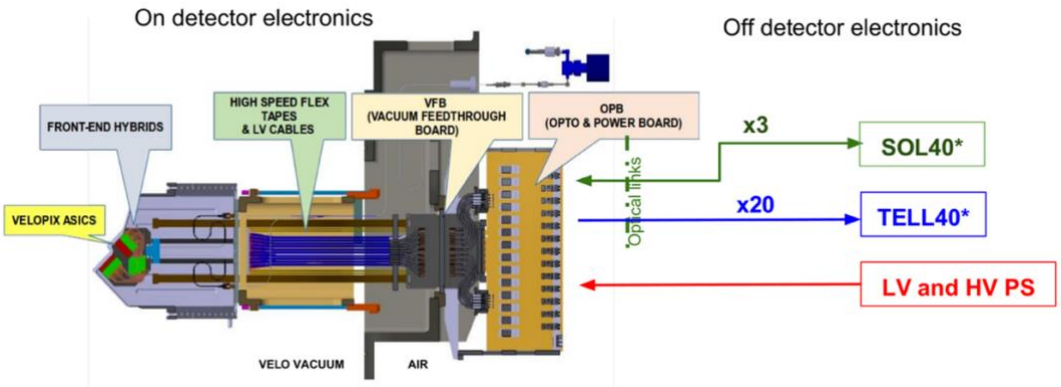


Figure 1: Schematic view of the components of the VELO on-detector electronics.

[1] The minimum is given by the minimal voltage required by the DC/DC converters to produce a reliable output. The maximum is given by the voltage dividers from the input voltage used for enable signals (absolute max 10 V).

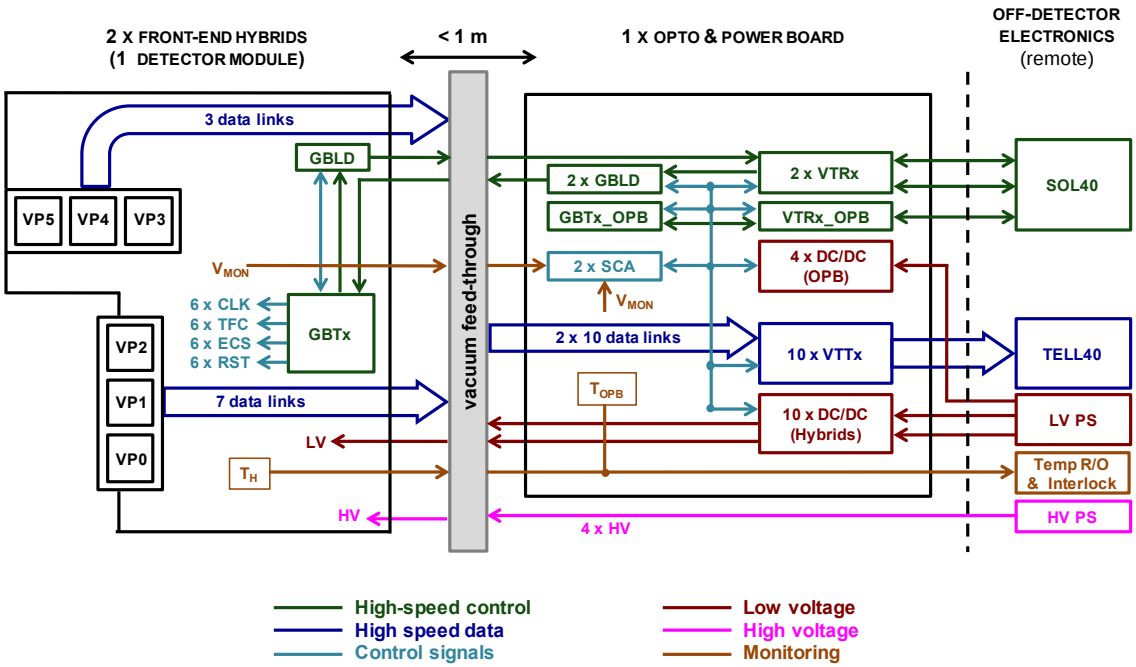


Figure 2: Overview of the VELO Upgrade electronics showing the role and functionality of the OPB. The main components on the OPB and the hybrid are shown as boxes where the colours of the boxes and lines indicate the type of signal or supply it represents: dark blue indicate the 5.12 Gbit/s data links; dark green indicate the 4.8 Gbit/s control links; light blue (or turquoise) indicate slower control signals, either 40 MHz clock and control, I^2C configuration or logical signals; red indicate low voltage supply; magenta indicate high voltage supply; and brown indicate analogue voltage or temperature monitoring signals.

The OPBs are mounted in custom crates on the VELO vacuum tank where the vacuum feedthrough are placed at the back of the crate. The data and control signals are transmitted to the front-end hybrids through flexible high-speed data tapes and the low voltage is supplied on separate cables. The high voltage supply is not routed through the OPB, it is connected directly to the same vacuum feedthrough and routed on separate cables to the detector module. There are additional temperature monitoring signals for the cooling system that are routed through separate cables as well.

The three bidirectional optical control links are received by VTRx transceivers [7-9] operating at 4.8 Gbits/s. One link is connected to a GBTx ASIC [10-12] that provides the local control of the OPB, through the two slow control adaptor ASICs (GBT-SCA) [13,14]. These SCA ASICs provide the I^2C buses to configure the laser drivers (GBLD) [15-17] on the VTTx and VTRx modules and the logical I/O signals required for the DC/DC converters [18-21]. The other two control links are connected to the two front-end hybrids. As the VTRx transceiver is not designed to drive the signals to a remote GBTx (located on the detector module) the signals are driven by the GBLD ASICs [15-17].

The 20 high-speed data links are routed from the backplane (PCIe) connector to the 10 VTTx optical transmitter modules mounted on the OPB [7-9].

The ten voltages needed for the front-end hybrids on one module are provided by separate DC/DC converters, one analogue and one digital voltage for each of the four tiles and voltages for the GBTx and GBLD that are shared between the two sides of the module. The OPB itself require four voltages that are provided by DC/DC converters. Five LV supply channels are needed to power the system. Analogue power is supplied on separate channels for the front and back hybrids. The digital voltages of each hybrid share a power supply channel with the electronics on the OPB that are mostly associated with that side of the module. The electronics on the OPB is not strictly divided between the front and back side of the module due to routing constraints. The control electronics for the OPB itself, that is required to be always on to communicate with the board, is supplied from a separate OPB input LV channel.

2 LV supply and monitoring

2.1 Grounding and powering scheme of the production OPB

The input voltage to the OPB is 6 – 9 V, which is given by the minimum input voltage required by the DC/DC converters [18-20] and the maximum tolerated by the inputs fed from voltage dividers derived from the supply voltage. There are four DC/DC converters providing the voltages for the OPB and eight DC/DC converters used to supply the voltages for the VeloPix ASICs, and two DC/DC converters that the supply voltages for the GBTx [10-12] and GBLD [15-17] on the hybrid shared between the two sides of the module. The powering schemes of the front and back hybrids are shown in Figure 3 and Figure 4 .

DC/DC converters that are supplied from the same LV channel have the same ground reference even though they regulate independent output voltages. Moreover, the distance between the DC/DC converters and the hybrid implies that there is a non-zero impedance in the supply line. These two facts are important considerations when defining the grounding and powering scheme.

The analogue VeloPix [22-23] voltages are supplied through separate LV channels for the front and back side hybrids with no ground reference on the OPB. This ensures that the analogue return currents from the two hybrids are separate and not mixed with the digital return current.

The digital grounds on the hybrid and the OPB have to be firmly linked since the shield ground planes on the high-speed links have to be connected to digital grounds of both the sender and receiver. Hence the digital supply voltages of the hybrid and the electronics on the OPB associated to that hybrid are provided by the same LV channel. The remaining electronics that do the local control of the OPB is powered from a separate LV supply channel. There is only one digital ground on the OPB, common to these three supply channels. The DC/DC converters, the maximal current consumption of the components they supply, and their supply voltages are summarised in Table 1.

The analogue and digital grounds of all the supplies are linked on the on the module, from both sides of the module. There is a shield ground on the OPB that is linked to the crate and the mechanical structure, that can be connected to the OPB digital ground through a resistor, capacitor or inductor. This defines the ground reference for the different LV supply channels on the OPB.

Table 1: Summary of the active components indicating which DC/DC converter that supplies them, with upper limits of their current consumption. The table also indicate which LV PS channel that supplies each DC/DC converter.

Powering components	Supply	V [V]	I_{max} [A]	DC/DC converter
VTRx_OPB	OPB common	2.5	0.3	DCDC_OPB_VTRx
GBTx_OPB, SCA_OPB_1, SCA_OPB_2		1.5	1 + 2 x 0.3	DCDC_OPB_CTRL
VTRx_FH, GBLD_FH, VTTx_5 – VTTx_8	DIG front hybrid	2.5	0.3 + 0.2 + 5 x 0.4	DCDC_OPB_LINK2
GBTx on both hybrids		1.5	2 x 1	DCDC_GBTx_H
GBLD on both hybrids		2.5	2 x 0.2	DCDC_GBLD_H
Tile 0 front hybrid digital		1.3	3 x 1	DCDC_VPD0
Tile 3 front hybrid digital		1.3	3 x 1	DCDC_VPD3
VTRx_BH, GBLD_BH, VTTx_1 – VTTx_4	DIG back hybrid	2.5	0.3 + 0.2 + 5 x 0.4	DCDC_OPB_LINK1
Tile 2 back hybrid digital		1.3	3 x 1	DCDC_VPD2
Tile 1 back hybrid digital		1.3	3 x 1	DCDC_VPD1
Tile 0 front hybrid analogue	ANA front hybrid	1.3	3 x 1	DCDC_VPA0
Tile 3 front hybrid analogue		1.3	3 x 1	DCDC_VPA3
Tile 2 back hybrid analogue	ANA back hybrid	1.3	3 x 1	DCDC_VPA2
Tile 1 back hybrid analogue		1.3	3 x 1	DCDC_VPA1

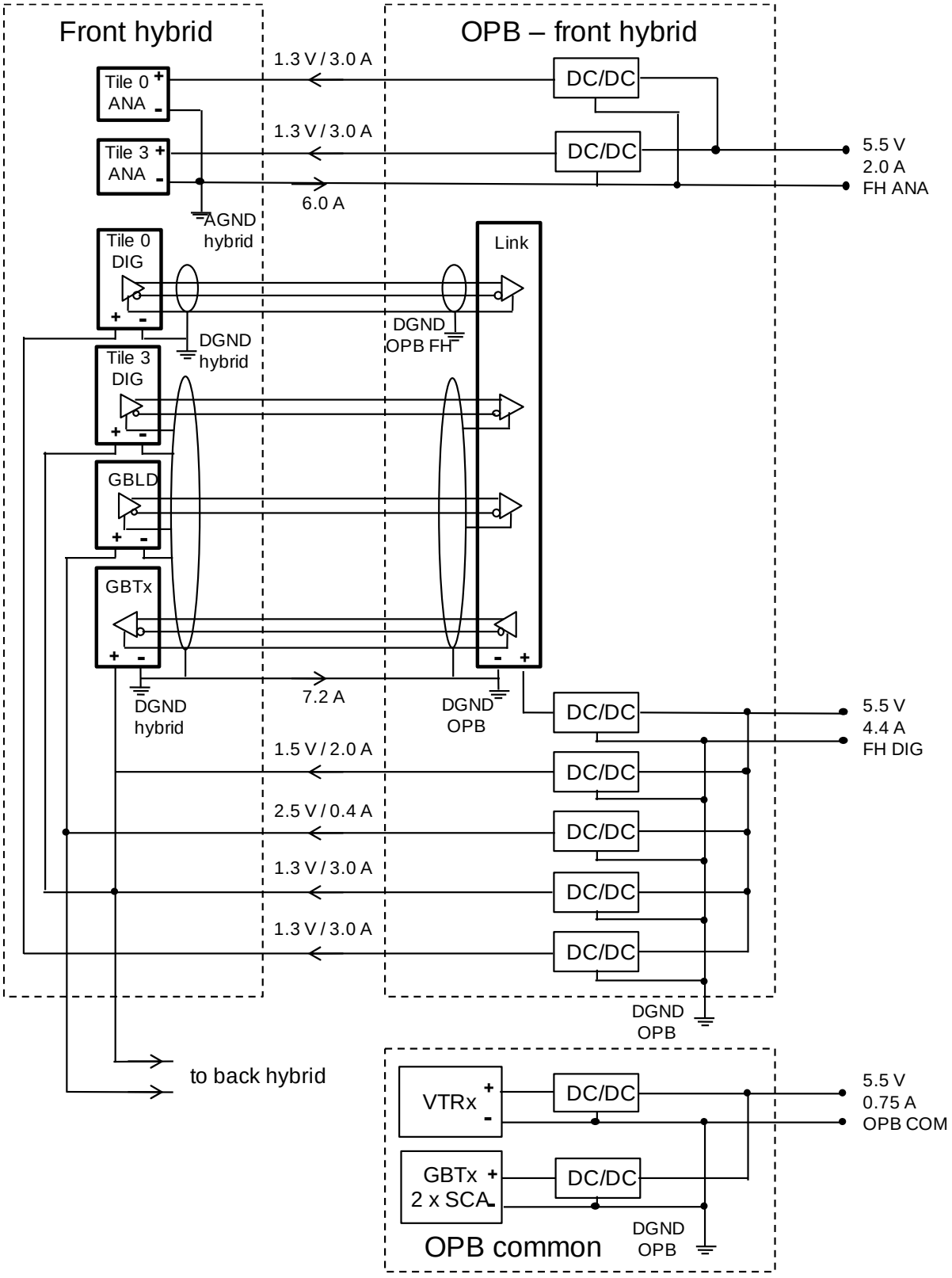


Figure 3: Grounding and powering scheme of the front hybrid and the electronics on the OPB related to the front hybrid. The figure also includes the common electronics on the OPB.

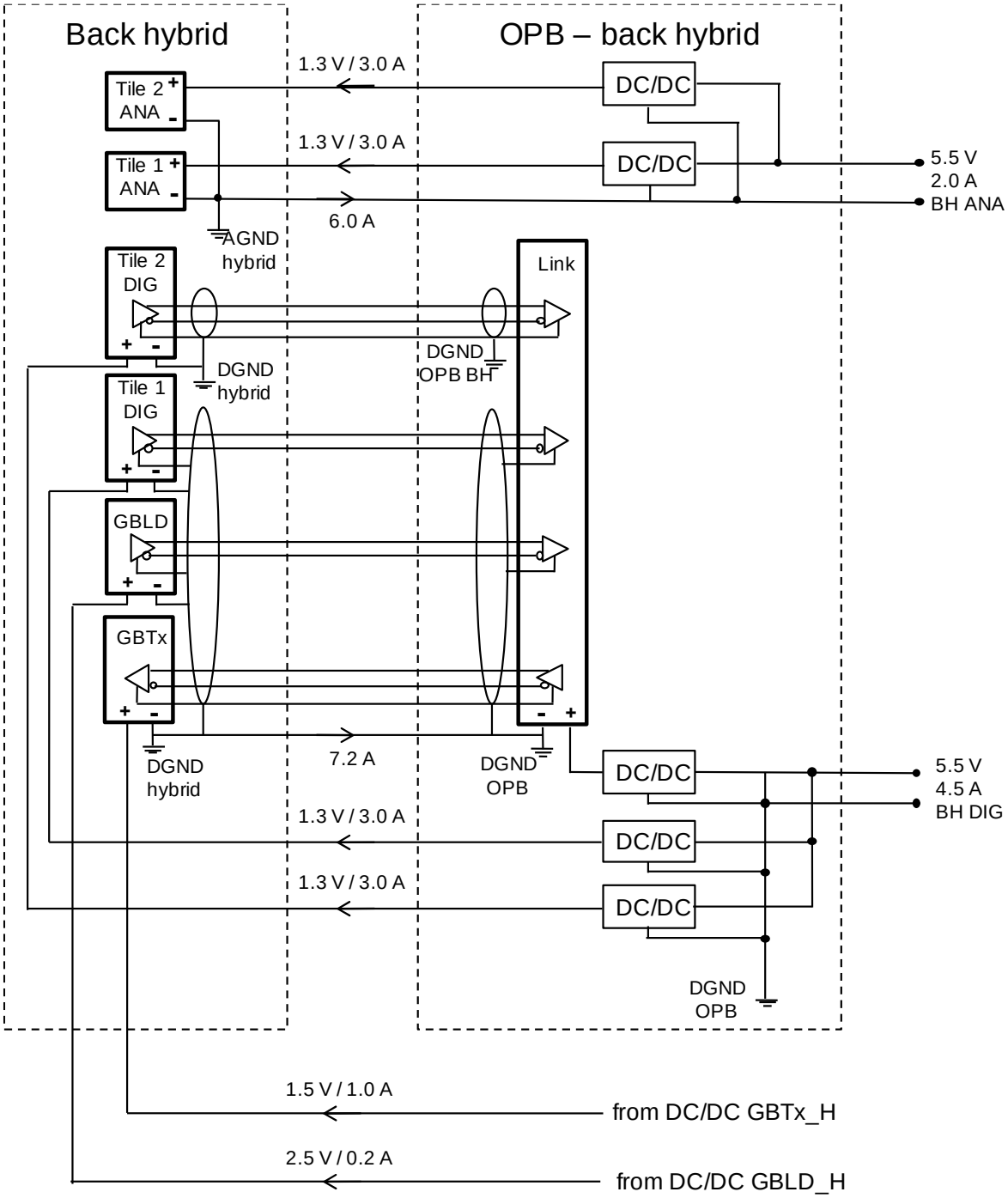


Figure 4: Grounding and powering scheme for the back hybrid and the electronics on the OPB related to the back hybrid.

2.2 Power dissipation estimates

The power dissipation estimates of the detector module and the OPB are shown in Table 2. These estimates are based on the maximum values given in the data sheets of the components and hence are upper limits used for the design of the system. The estimated power dissipation on the OPB includes the losses in the DC/DC converters, where the assumed efficiencies vary between 0.70 and 0.85 depending on the output voltage and current as specified in the data sheet.

A fully configured OPB and detector module were measured in systems tests during the production phase, which gave a power consumption of 26 W for the detector module and 14 W for the OPB. This is significantly lower than the 35 W and 34 W estimated in Table 2 and provides a good operational margin for the system. The power consumption is expected to increase with increased occupancy during operation, hence this margin is necessary.

Table 2: Power dissipation estimates, where the values in the columns correspond to the dissipation on the detector module, the OPB and in total. The dissipation estimates are split by power supply channel and summed up for the module, the detector half and the full VELO. This is assuming 6.0 V input voltages to the OPB, maximal current consumption for all components (as given in Table 1) and the DC/DC conversion efficiencies from the datasheet.

Supply voltage (6.0 V)	I [A]	P module [W]	P OPB [W]	P total [W]
OPB common	0.66	0	4.0	4.0
Front hybrid digital	4.0	12	12	24
Front hybrid analogue	1.9	7.8	3.3	11
Back hybrid digital	3.1	7.8	11	19
Back hybrid analogue	1.9	7.8	3.3	11
Total (one module)		35	34	69
Total (detector half)		915	875	1790
Total (VELO)		1830	1750	3580

2.3 LV supply and cable requirements

The low voltage power supplies are located in D3 which is approximately 60 m cable distance from the detector. Each OPB is supplied with five voltages with the specifications given in Table 2, adding up to a total of 260 power supply channels for the whole VELO. The voltage supplies are regulated to compensate for the voltage drops in the cables. Table 3 shows the requirements of the power supply channels using an estimate of the cabling. The output capacity of each LV channel for the EASY A3009 supplies used for the current VELO are I_{max} = 9 A, V_{max} = 8 V and P_{max} = 45 W.

Table 3: Voltage, current and power requirements on the LV power supplies. These estimates are based on the planned LV cabling as detailed in Ref [24] and assumes a 6.0 V input voltage to the OPB.

Supply voltage (6.0 V)	Cable cross section	Cable resistance	Voltage drop	Cable power	PS output voltage	PS output power
OPB common	2/10/2.5 mm^2	0.40 Ω	0.26 V	0.17 W	6.3 V	4.1 W
Front hybrid digital	3/10/2.5 mm^2	0.36 Ω	1.43 V	5.7 W	7.4 V	30 W
Front hybrid analogue	3/10/2.5 mm^2	0.36 Ω	0.67 V	1.3 W	6.7 V	12 W
Back hybrid digital	3/10/2.5 mm^2	0.36 Ω	1.13 V	3.5 W	7.1 V	22 W
Back hybrid analogue	3/10/2.5 mm^2	0.36 Ω	0.67 V	1.3 W	6.7 V	12 W

Total (one module)	12 W	81 W
Total (VELO)	616 W	4200 W

The DC/DC converters regulate the voltage at their output on the OPB, hence the voltage supplied to the hybrid will be reduced by the voltage drop over the cables in the vacuum. The minimum required surface area of these cables and the estimated voltage drops are given in Table 4.

Table 4: Voltage drops and dissipated power over the cable through the VELO vacuum. The estimated voltage drops assume 10 mΩ for the cables and 2 mΩ each for the OPB, feedthrough and hybrid, including contact resistances. The estimated resistances are consistent with but slightly larger than the measured values of the prototype system.

Supply voltage	Output voltage	Current	Total resistance	Voltage drop	Cable power	Supplied voltage
VeloPix DIG 0/2	1.3 V	3.0 A	16 mΩ	47 mV	86 mW	1.21 V
VeloPix DIG 1/3	1.3 V	3.0 A	16 mΩ	47 mV	86 mW	1.21 V
2 x GBTx	1.5 V	2 A	13 mΩ	25 mV	27 mW	1.43 V
2 x GBLD	2.5 V	0.4 A	13 mΩ	5 mV	1 mW	2.45 V
Digital return	N/A	7.2 A	6 mΩ	6 mV	165 mW	N/A
VeloPix ANA 0/2	1.3 V	3.0 A	16 mΩ	47 mV	86 mW	1.21 V
VeloPix ANA 1/3	1.3 V	3.0 A	16 mΩ	47 mV	86 mW	1.21 V
Analogue return	N/A	6.0 A	16 mΩ	47 mV	86 mW	N/A

Total per hybrid	26.4 A	0.71 W
Total per module	52.8 A	1.42 W
Total per VELO half	1373 A	37 W

2.4 DC/DC converter implementation

The common connections for the DC/DC converters are given in Table 5 and the specific connections for the individual converters are given in Table 6. The ADC of the GBT-SCA [13,14] is referenced to the digital ground of the OPB which may be at a small DC offset compared to the analogue grounds on the OPB due to the voltage drop over the cables between the OPB and the hybrid. Hence, two ADC channels are used to monitor voltage and ground of the analogue DC/DC converter, for both the input and output voltages. These voltages are divided down to match the range of the GBT-SCA ADC, as illustrated in Figure 5. The digital voltages are referenced to the same ground as the GBT-SCA and hence divided down to the ADC range and monitored by a single channel.

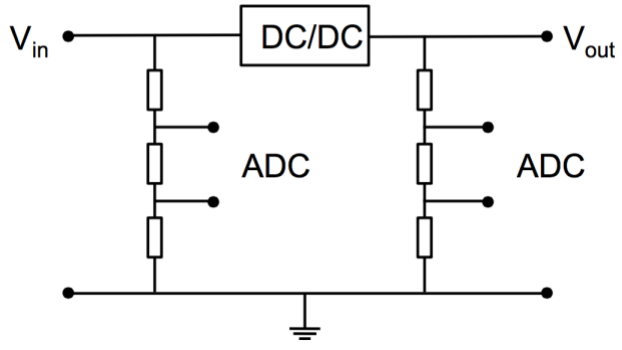


Figure 5: Illustration of the voltage dividers used to bring the analogue voltages into the range of the ADC in the GBT-SCA (0 - 1 V) Two channels are used since the ground reference is not the same as that of the ADC.

Table 5: Connections for the DC/DC converters supplying the OPB and the hybrids. The specific connection pads, labelled k, l, m, n, p and q are given in Table 6.

DCDC converter	
Pin	Name
12	En
1	PGood
7-11, 18-22	Vout
2, 3, 13, 14	Vin

SCA_OPB_FH, SCA_OPB_BH
Name
GPIO_pad<k>
GPIO_pad<l>
ADC_in_pad<m>, <n>
ADC_in_pad<p>, <q>

7-11, 18-22	Vout
4-6, 15-17	GND
2, 3, 13, 14	Vin

Power connections
OPB/Hybrid power
GND
LV PS connector

Table 6: Overview of DC/DC converters on the production OPB listing the output voltage and maximum output current, the LV PS channel and its specific connections to the GBT-SCA. The enable signals for DCDC_OPB_VTRx and DCDC_OPB_CTRL are also connected via jumpers to the E-Fuse programming connector pins 8 and 6 respectively to enable power cycling during programming.

DC/DC name	V_{out} [V]	I_{max} [A]	LV PS channel	SCA_X: GPIO channel		SCA_X: ADC channel	
				En	PGood	V_{in}	V_{out}
DCDC_VPA0	1.3	3	FH ANA	1:7	1:16	2:1,2	1:5,6
DCDC_VPA3	1.3	3		2:8	2:16		2:8,9
DCDC_VPD0	1.3	3	FH DIG	1:7	1:18	2:3	1:4
DCDC_VPD3	1.3	3		2:8	2:18		2:4
DCDC_GBTX_H	1.5	2		1:9	1:20		1:11
DCDC_GBLD_H	2.5	0.4		1:11	1:21		1:12
DCDC_OPB_LINK2	2.5	2.5		2:12	2:15		2:10

				SCA_X GPIO channel		SCA_X: ADC channel	
				En	PGood	V_{in}	V_{out}
DCDC_VPA1	1.3	3	BH ANA	1:8	1:19	1:1,2	1:8,9
DCDC_VPA2	1.3	3		2:7	2:19		2:5,6
DCDC_VPD1	1.3	3	BH DIG	1:8	1:17	1:3	1:7
DCDC_VPD2	1.3	3		2:7	2:17		2:7
DCDC_OPB_LINK1	2.5	2.4		1:10	1:15		1:10

				SCA_FH GPIO		SCA_FH ADC	
				En	PGood	V_{in}	V_{out}
DCDC_OPB_VTRx	2.5	0.3	OPB COM	N/A	1:24	1:0	1:13
DCDC_OPB_CTRL	1.5	1.6		N/A	1:25		1:14

2.5 Monitoring of the VeloPix voltages

The voltages supplied to the VeloPix ASICs [22] are monitored through a circuit implemented in the VeloPix ASIC. The analogue and digital supply voltages to each VeloPix ASIC are divided across the resistor bridge shown in Figure 6, giving the voltages $V_{1a,1d}$ and $V_{2a,2d}$. The four voltages from each VeloPix ASIC are routed through an analogue multiplexer to an output pad that can be configured to be in either high-impedance mode or provide a voltage output. The voltage monitoring pads for all the VeloPix ASICs for one tile are connected to a bus line that is routed out to the OPB. These four lines are connected to the SCA ADC (tile 0: SCA_2 ADC<27>, tile 1: SCA_1 ADC<27>, tile 2: SCA_1 ACD<28> & tile 3: SCA_2 ADC<28>) which gives access to the all the supply voltages on the hybrids by appropriately configuring the analogue multiplexers in the VeloPix ASICs. Assuming that the three resistors are identical, the ground and supply voltages can be calculated from

$$VDD_{a,\,d} = 2 \times V_{1a,\,1d} - V_{2a,\,2d,}$$

$$GND = 2 \times V_{2a,\,2d} - V_{1a,\,1d,}$$

$$VDD_{a,\,d} - GND = 3 \times (V_{1a,\,1d} - V_{2a,\,2d}).$$

The analogue multiplexer also provides access to the outputs of the internal DAC in the VeloPix ASIC, which can be used to monitor their performance. These voltages are read out through the same ADCs on the SCA that are used for the supply voltage monitoring and are accessed by selecting the appropriate input for the analogue multiplexer. See the VeloPix operations manual for details [23].

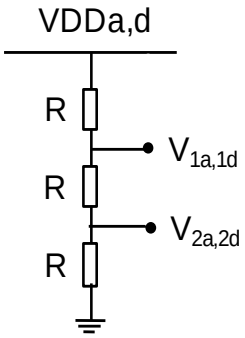


Figure 6: Voltage divider internal to the VeloPix ASIC [22] providing the two voltages per supply that are multiplexed out for voltage monitoring.

3 The versatile transceiver (VTRx) implementation

There are three versatile transceivers on the OPB, one for the local control of the OPB described in Section 3.1 and two for the control of the detector module described in Section 3.2.

3.1 The versatile transceiver for the OPB control signals

The electro-optical transceiver used for the control of the OPB (VTRx_OPB) [7-9] is connected to the GBTx [10-12] located on the OPB (GBTx_OPB) which together with the GBT-SCA [13-14] provide the signals necessary to configure and monitor the OPB. The connections of this VTRx are given in Table 7.

Table 7: Connections for the VTRx o/e transceiver that is connected to the GBTx located on the OPB.

VTRx_OPB		Comment	GBTx_OPB	
Pin	Name		Name	Pin
		N/C	LDRST	J7
5	SCL	1.5V pull-up	LDSCL	K8
4	SDA	1.5V pull-up	LDSDA	H8
12	RD+		RXINP	T1
13	RD-		RXINN	U1
18	TD+		TXOUTP	E1
19	TD-		TXOUTN	D1

					SCA_1	
					Name	Pin
8	RSSI		Connected as shown in Figure 7		ADC_in_pad<26>	N5

					Power connections
3	Tx_Disable				GND
6	Mod_ABS				GND
15	V_{CCR}				2.5 V supply from DCDC_OPB_VTRx
16	V_{CCT}				
10,11,14	V_{EER}				GND
1,17,20	V_{EET}				GND
2,7,9	N/C				N/C

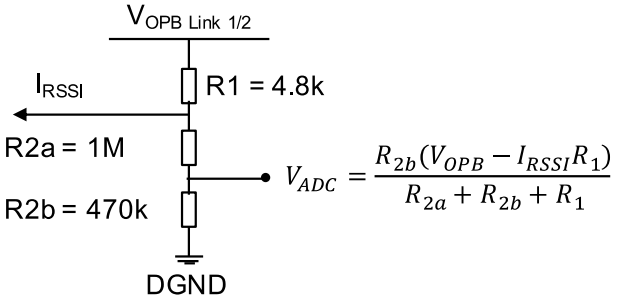


Figure 7: Voltage divider to monitor current proportional to the received optical power (I_{RSSI}). The schematic shows its connection to the ADC on the GBT-SCA [13,14].

3.2 The versatile transceivers for the detector module control signals

The OPB has one versatile transceiver [7-9] for each hybrid it provides signals for, labelled VTRx_FH and VTRx_BH for the front and back hybrids. These two VTRx are connected to the SCA_1, SCA_2, GBLD_FH, GBLD_BH, the high-speed hybrid connector and power as specified in Table 8. The two component names (_FH and _BH) and the two pin numbers correspond to the two different optical transceivers supplying the two hybrids.

Table 8: Connections for the VTRx transmitting the signals for the two front-end hybrids. The SCA_FH (SCA_BH) and GBLD_FH (GBLD_BH) are connected to the VTRx transmitting the signals for the front (back) hybrid.

VTRx_FH, VTRx_BH		Comment	SCA_2(FH), SCA_1 (BH)	
Pin	Name		Name	Pin
5	SCL	1.5V pull-up	SCL_pad<14>	L3
4	SDA	1.5V pull-up	SDA_pad<14>	L2
3	Tx_Disable		GPIO_pad<0>	B13
8	RSSI	Connected as shown in Figure 7	ADC_in_pad<25>	M5
			Power connections	
6	Mod_ABS		GND	
15	V_{CCR}	Decoupling	2.5 V supply from DCDC_OPB_LINK	
16	V_{CCT}	Decoupling		
10, 11, 14	V_{EER}		GND	
1, 17, 20	V_{EET}			
2, 7, 9	N/C		N/C	
			GBLD_FH, GBLD_BH	
			Name	Pin
12	RD+		DIN+	10
13	RD-		DIN-	9
			PCIe connector	
			Name	Pin
18	TD+	VFT con: F2-50, B2-50	CTRL_UP_FH_P, _BH_P	A25, A68
19	TD-	VFT con: F2-49, B2-49	CTRL_UP_FH_N, _BH_N	A24, A69

4 The versatile twin transmitter (VTTx) implementation

The OPB supports 20 data links converted to optical signals by 10 VTTx optical transmitters [7-9]. The common pin connections of the VTTx modules are given in Table 9, the specific connections for each VTTx are given in Table 10 and Table 11 for the 20 optical transmitters on the OPB.

Table 9: Common connections for the 10 VTTx optical transmitters on the OPB. The pin connections differ between the individual VTTx are given in Table 10 and Table 11.

VTTx_N connection		Comment	Common connections
Pin	Name		Name
6	Mod_ABS		GND
16	V_{CCT}	Decoupling	2.5 V from DCDC_OPB_LINK1/2
15	V_{CCT2}	Decoupling	
1, 10, 11, 14, 17, 20	V_{EET}		GND
2, 8	N/C		N/C

Table 10: Connections for the first set of VTTx optical transmitters reading out the two tiles close to the 'long' edge of the module. The common connections are given in Table 9.

Optical transmitter (VTTx_N)				Signal name or SCA_1 input pad	PCIe or SCA_1 pin	Hybrid pin	Feedthrough pin
Number	Pin	Name					
						HSC_B2	
	18	TD1+		DTA_VP113_N	A77	24	37
	19	TD1-		DTA_VP113_P	A76	23	38
	12	TD2+		DTA_VP123_N	B79	28	33
	13	TD2-		DTA_VP123_P	B78	27	34
1	5	SCL		SCL_pad<1>	C2		
	4	SDA		SDA_pad<1>	C1		
	7	SCL2		SCL_pad<2>	D2		
	9	SDA2		SDA_pad<2>	D1		
	3	Tx_Disable		GPIO_pad<1>	A13	HSC_B2 / HSC_F1	
	18	TD1+		DTA_VP003_P	A73	3	58
	19	TD1-		DTA_VP003_N	A72	4	57
	12	TD2+		DTA_VP103_N	B75	20	41
	13	TD2-		DTA_VP103_P	B74	19	42
2	5	SCL		SCL_pad<3>	E2		
	4	SDA		SDA_pad<3>	E1		
	7	SCL2		SCL_pad<4>	D3		
	9	SDA2		SDA_pad<4>	C3		
	3	Tx_Disable		GPIO_pad<2>	B12	HSC_F1	
	18	TD1+		DTA_VP013_P	A55	11	50
	19	TD1-		DTA_VP013_N	A54	12	49
	12	TD2+		DTA_VP012_P	B57	7	54
	13	TD2-		DTA_VP012_N	B56	8	53
3	5	SCL		SCL_pad<5>	F2		
	4	SDA		SDA_pad<5>	F1		
	7	SCL2		SCL_pad<6>	F3		
	9	SDA2		SDA_pad<6>	E3		
	3	Tx_Disable		GPIO_pad<3>	A12	HSC_F1	
	18	TD1+		DTA_VP021_P	A51	19	42
	19	TD1-		DTA_VP021_N	A50	20	41
	12	TD2+		DTA_VP020_P	B53	15	46
	13	TD2-		DTA_VP020_N	B52	16	45
4	5	SCL		SCL_pad<7>	G2		
	4	SDA		SDA_pad<7>	G1		
	7	SCL2		SCL_pad<8>	G4		
	9	SDA2		SDA_pad<8>	G3		
	3	Tx_Disable		GPIO_pad<4>	C11	HSC_F1	
	18	TD1+		DTA_VP023_P	A47	27	34
	19	TD1-		DTA_VP023_N	A46	28	33
	12	TD2+		DTA_VP022_P	B49	23	38
	13	TD2-		DTA_VP022_N	B48	24	37
5	5	SCL		SCL_pad<9>	H2		
	4	SDA		SDA_pad<9>	H1		
	7	SCL2		SCL_pad<10>	H4		
	9	SDA2		SDA_pad<10>	H3		
	3	Tx_Disable		GPIO_pad<5>	B11		

Table 11: Connections for the second set of VTTx optical transmitters reading out the two tiles close to the 'short' edge of the module. The common connections are given in Table 9.

Optical transmitter (VTTx_N)				Signal name or SCA_2 input pad	PCIe or SCA_2 pin	Hybrid pin	Feedthrough pin
Number	Pin	Name					
						HSC_B1	
	18	TD+		DTA_VP213_N	A43	23	38
	19	TD-		DTA_VP213_P	A42	24	37
	12	TD2+		DTA_VP223_N	B45	27	34
	13	TD2-		DTA_VP223_P	B44	28	33
6	5	SCL		SCL_pad<1>	C2		
	4	SDA		SDA_pad<1>	C1		
	7	SCL2		SCL_pad<2>	D2		
	9	SDA2		SDA_pad<2>	D1		
	3	Tx_Disable		GPIO_pad<1>	A13	HSC_B1	
	18	TD+		DTA_VP203_N	A39	15	46
	19	TD-		DTA_VP203_P	A38	16	45
	12	TD2+		DTA_VP212_N	B41	19	42
	13	TD2-		DTA_VP212_P	B40	20	41
7	5	SCL		SCL_pad<3>	E2		
	4	SDA		SDA_pad<3>	E1		
	7	SCL2		SCL_pad<4>	D3		
	9	SDA2		SDA_pad<4>	C3		
	3	Tx_Disable		GPIO_pad<2>	B12	HSC_B1	
	18	TD+		DTA_VP201_N	A35	7	54
	19	TD-		DTA_VP201_P	A34	8	53
	12	TD2+		DTA_VP202_N	B37	11	50
	13	TD2-		DTA_VP202_P	B36	12	49
8	5	SCL		SCL_pad<5>	F2		
	4	SDA		SDA_pad<5>	F1		
	7	SCL2		SCL_pad<6>	F3		
	9	SDA2		SDA_pad<6>	E3		
	3	Tx_Disable		GPIO_pad<3>	A12	HSC_F2 / HSC_B1	
	18	TD+		DTA_VP303_P	B19	19	42
	19	TD-		DTA_VP303_N	B18	20	41
	12	TD2+		DTA_VP200_N	A21	3	58
	13	TD2-		DTA_VP200_P	A20	4	57
9	5	SCL		SCL_pad<7>	G2		
	4	SDA		SDA_pad<7>	G1		
	7	SCL2		SCL_pad<8>	G4		
	9	SDA2		SDA_pad<8>	G3		
	3	Tx_Disable		GPIO_pad<4>	C11	HSC_F2	
	18	TD+		DTA_VP323_P	B15	27	34
	19	TD-		DTA_VP323_N	B14	28	33
	12	TD2+		DTA_VP313_P	A17	23	38
	13	TD2-		DTA_VP313_N	A16	24	37
10	5	SCL		SCL_pad<9>	H2		
	4	SDA		SDA_pad<9>	H1		
	7	SCL2		SCL_pad<10>	H4		
	9	SDA2		SDA_pad<10>	H3		
	3	Tx_Disable		GPIO_pad<5>	B11		

5 The GBLD implementation

The GBLD [15-17] is designed as a laser driver and is one of the components on the VTRx and VTTx modules [7-9]. In addition, they are used as stand-alone differential line drivers on the OPB and the on the hybrid to drive the control link signals between the VTRx transceivers on the OPB and the GBTx ASICs [10-12] on the front-end hybrids.

They require configuration via I^2C and a reset provided by the GBT-SCA [13-14]. The GBLDs are configured to be enabled and to come up in the default low-power mode. The connections of the two GBLDs on the OPB are given in Table 12.

Table 12: Connections for the two GBLD ASICs driving the signals between the VTRx on the OPB and the GBTx on the hybrid. The components are labelled _FH or _BH depending on if they are driving signals for the front or back hybrid.

GBLD_FH, GBLD_BH			SCA_2, SCA_1	
Pin	Name		Name	Pin
5	SCL	Pull-up to VDDc	SCL_pad<14>	L3
6	SDA	Pull-up to VDDc	SDA_pad<14>	L2

			VTRx_FH, VTRx_BH	
			Name	Pin
9	DIN-		RD-	13
10	DIN+		RD+	12

				Connector pin	
			Name	HSC_F2/B2	PCIe
20	MODB+		N/C		
21	MODA+	CTLE circuit and AC coupling	CTRL_DN_FH_P, _BH_P	46	B22, B70
22	MODA-		CTRL_DN_FH_N, _BH_N	45	B23, B71
23	MODB-		N/C		

			Power connections
1	RST	Active low	LOGIC_RESET (SCA_1 GPIO and button)
14	I2C_A2		N/C to give the same I^2C address as a VTTx (0x7E)
15	I2C_A3		
4	DIS		Pull-down to GND
13	HIMODE		Pull-down to GND
18	IBIAS		560 Ohm resistor to V_OPB_LINK1/2
7,12	VDDc	Decoupling	Net for I^2C pull-up
2,8,11,17	GND		GND
3,16,19,24	VDD	Decoupling	2.5 V supply from DCDC_LINK1/2

6 GBT-SCA and GBTx implementation

The connections to the GBT-SCA [13,14] are partially defined from the tables of connections to the other components, since the connections to the GPIO, ADC channel or I^2C bus are shown in those tables. This section defines the connections to the other pins and the connections between the GBTx [10-12] and the GBT-SCA. The connections for the two GBT-SCAs on the OPB are given in Table 13 and Table 14 lists the connections to the GBTx. The non-connected inputs are pulled with 10 kΩ to VDD and GND for the positive and negative inputs, respectively. The non-connected outputs are left floating. These are all labelled N/C in the table.

Table 13: Connections to the two GBT-SCA ASICs on the OPB, omitting the GPIO, ADC, I^2C and power connections.

Pin name(s)	Pin #	Connection	Comment
GPIO_EXTCLK	A14	N/C	External clock for GPIO sampling, not used
auxPortSDA, auxPortSCL, auxPortEn	H12, J12, K12	N/C (pull-up)	Aux serial control port, used for testing and daisy chaining SCAs
SPI bus pads	B14, C14, D14, C12, D12, E12, F12, C13, D13, E13, E14	N/C	SPI bus not used
TX_SD_AUX, TX_SD_AUX_N, RX_SD_AUX, RX_SD_AUX_N, LINK_CLK_AUX_N, LINK_CLK_AUX	F13, F14, G13, G14, H13, H14	N/C	Auxiliary GBTx-SCA link, not used
LINK_AUX_DISABLE	L12	pull-up 4.7 kΩ	Disable auxiliary GBTx-SCA link
TX_SD_N	J13	SCINN (GBTx P13) for SCA_1 DINN16 (GBTx G18) for SCA_2	
TX_SD	J14	SCINP (GBTx P12) for SCA_1 DINP16 (GBTx F18 for SCA_2	
RX_SD_N	L13	SCOUTN (GBTx P3) for SCA_1 DOUTN16 (GBTx H18) for SCA_2	
RX_SD	L14	SCOUTP (GBTx P4) for SCA_1 DOUTP16 (GBTx J18) for SCA_2	
LINK_CLK_N	K13	SCCLKN (GBTx R6) for SCA_1 DCLKN16 (GBTx L17) for SCA_2	
LINK_CLK	K14	SCCLKP (GBTx P6) for SCA_1 DCLKP16 (GBTx K17) for SCA_2	
FuseProgramPulse	M13	N/C	E-fuse for default register values not used for the SCA
PWR3_3	G12		
RESET_B	M14	Power-on reset	Generated by 5kΩ/100nF RC on GBTx & SCA supply (DCDC_OPB_CTRL), push button or SCA_1 GPIO ch<6>
DAC_OUT<0-3>	N3, N2, P3, P2	N/C	DACs not used
JTAG pads	P1, N1, M1, L1, K1	N/C	JTAG not used

Table 14: Connections to the GBTx on the OPB, omitting power connections.

Pin name(s)	Pin #	Connection	Comment
CLOCKDES<0-7>N/ P	Multiple	N/C	Output clocks, not used
DCLKN/P<0-15, 17-39>	Multiple	N/C	E-links not used
DINN/P<0-15,17-39>	Multiple	N/C	E-links not used
DION/<0-15,17-39>	Multiple	N/C	E-links not used.
DCLKN/P<16>	L17, K17	SCA_2 LINK_CLK(_n)	Control link between GBTx and SCA_2
DINN/P<16>	G18, F18	SCA_2 TX_SD(_n)	
DOUTN/P<16>	H1, J18	SCA_2 RX_SD(_n)	
CONFIGSELECT	K7	Switch to V_{DD}/GND	Configuration via I^2C interface, used for USB dongle programming and E-Fuse burning
EFUSEPOWER	P14	Switch: 3.3 V supply and EFuse connector pin 2 when burning fuses, 1.5 V supply otherwise	For E-Fuse burning
EFUSEPROGRMPULSE	P11	EFuse connector pin 4	For E-Fuse burning
I2CADDRESS<0-3>	L8, N6, N7, P5	N/C	Default address 0000001 is OK, set by internal pull-up/down resistors.
LDRESET	J7	N/C	Not used
LDSCL	K8	VTRx OPB SCL (pin5)	I^2C bus for VTRx configuration, pulled up with 750 Ω to 1.5 V
LDSCA	H8	VTRx OPB SDA (pin 4)	
MODE<0-3>	N5, L7, L10, P10	Optional pull-up (4.7k) and GND via resistors	Sets the transmission mode, expected mode for VELO is 0010 (FEC Transceiver)
REFCLKN/P	K1, L1	N/C	Local reference clock not used
REFCLKSELECT	J9	GND	Take reference clock from PLL or XOsc. GBT has to be set in XOsc mode by setting bit 7 in Reg 313, 314, 315 to 0.
RESETB	M10	Power-on reset	Generated by 5 kΩ/100nF RC on GBTx & SCA supply (DCDC_OPB_CTRL), SCA_1 GPIO<6> or push-button.
RXDATAVALID	N9	LED driven by transistor, not mounted for the production boards.	Indicate if received header is ‘Data’ or ‘Idle’
RXRDY	N10		Indicate that the GBTx is ready to receive.
TXRDY	L13		Indicate that the GBTx is ready to transmit.
RXINN/P	U1, T1	VTRx OPB RD+/- (12, 13)	4.8 GBit/s control link input
TXOUTN/P	D1, E1	VTRx OPB TD+/- (18, 19)	4.8 GBit/s control link output
TXDATVALID	N11	Pull-up/down options via resistors	Sets if ‘Data’ or ‘Idle’ header is transmitted
RXLOCKMODE<0,1>	J8, M9	Optional pull-up (4.7k) and GND via resistors	Sets receiver lock mode, preferred mode is 01, automatic DAC frequency calibration
SCCLKN/P	R6, P6	SCA_1 LINK_CLK_N/P	Control link between GBTx and SCA_1
SCOUTN/P	P3, P4	SCA_1 RX_SD_N/P	
SCINN/P	P13, P12	SCA_1 TX_SD_N/P	
SCL, SDA	G5, H5	EFuse connector 7 & 5 750 Ω pull-up to 1.5 V	I^2C control port, only used for EFuse programming
autoReset	H15	Resistor to V_{DD} or GND	Default autoReset should be enabled
STATEOVERRIDE	H9	GND	Disable state override (debugging feature)
TCK, TDI, TDO, TMS, TRESETB	N8, P7, P9, P8, M8	N/C	JTAG interface not used
TESTCLOCKIN1/2	H7, J15	N/C	Test clock not used
TESTCLOCKOUT	H6	SMA connector	Clock output on SMA for debugging
TESTOUTPUT	K10	N/C	Signal output on SMA for debugging
XTALN/P	M2, J2	N/C	Crystal integrated in package

7 Transmission line equalisation

The high-speed data links are driven by the GWT wireline transmitter circuit [25] implemented in the VeloPix ASIC [22] and control links are driven by the GBLD laser drivers [15-17]. These high-speed links have a continuous time linear equaliser (CTLE) implemented to compensate for the transmission losses between the hybrid and OPB. Since the transmission line primarily attenuates the high-frequency component of the signal, the CTLE will attenuate the low-frequency component. The CTLE is a passive circuit which is shown in Figure 8, where the L-R-L circuit at the input CTLE is there to ensure 100 Ω input impedance for all frequencies. The CTLE of the data link is located at the input of the VTTx modules (see Figure 8), hence the receiving side of the link. The CTLE of the control link to the hybrid (CTRL_DN_FH/BH) is located at the output of the output of the GBLD (see Figure 8), hence on the sending end of the link. A similar circuit for the control link in the other direction (CTRL_UP_FH/BH) is located on the hybrid. Since the CTLE for the control links is located on the sending end of the link the L-R-L circuit to adjust the input impedance is not needed. However, a series capacitance (10 nF) is required to AC couple the control links. There are already series capacitors on the VTTx modules [7-9] hence no further AC coupling is needed for the data links.

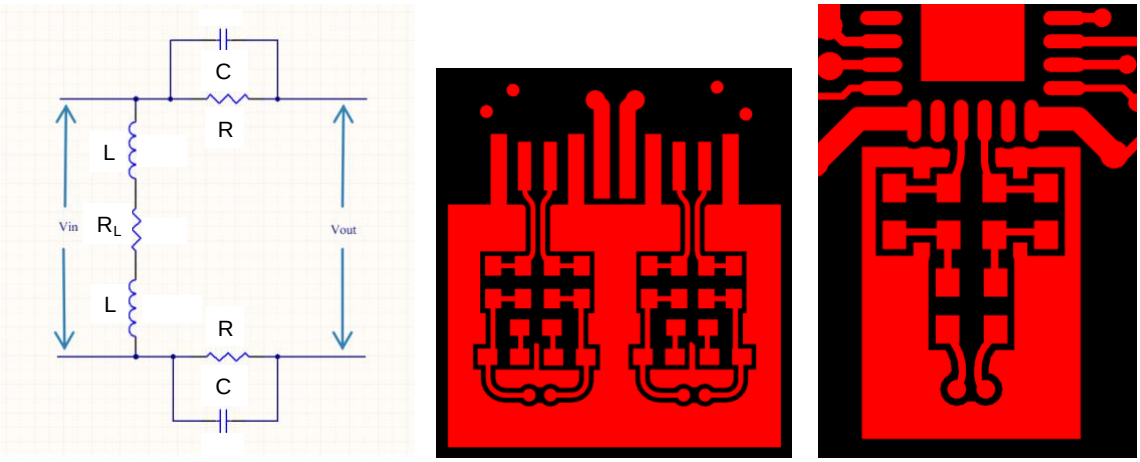


Figure 8: Schematic (left) and layout of the CTLE circuit for the data (middle) and control (right) links, as implemented on the OPB.

The component values for R and C are tuned to compensate for the frequency response of the link and the values for R_L and L are chosen to give a matched impedance. The values for these components, together with the parameters of the CTLE are given in Table 15, and the magnitude of the transfer function of the CTLE is shown in Figure 9. The components for the CTLE were optimised independently for the data and control links, but for simplicity the values optimised for the data links are used for both on the production boards.

Table 15: Values for the CTLE components and the parameters of the filter.

Component	Data links	Control links
R	100 Ω	88 Ω
C	2.2 pF	2.7 pF
R_L	150 Ω	161 Ω
2 x L	11 nH	13.5 nH
Zero f_z	0.719 GHz	0.724 GHz
Pole f_p	1.90 GHz	2.17 GHz
DC gain	0.38 (-8.4 dB)	0.33 (-9.5 dB)
Gain @ 2.5 GHz	0.83 (-1.6 dB)	0.79 (-2.1 dB)

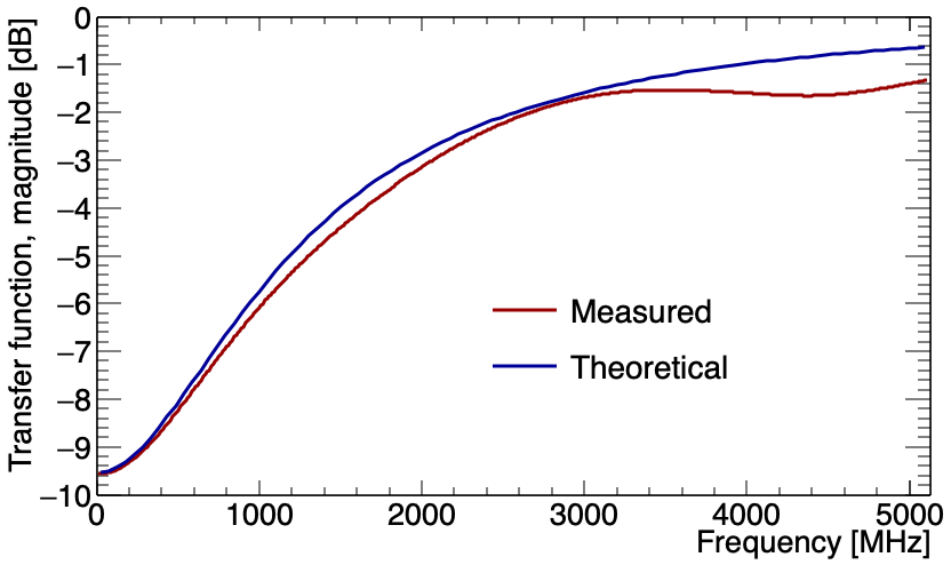


Figure 9: Transfer function of the CTLE circuit on the OPB, magnitude in dB versus frequency, with the component values for the data links given in Table 15. The blue curve gives the theoretical transfer functions, and the red curves gives the transfer function measured on a prototype circuit.

8 Connector definitions and pinouts

The OPBs are located in crates mounted directly on the VELO vacuum tank. The vacuum feedthrough act as the crate backplane and the OPB slides directly on to that while being held by a custom crate. The OPBs have three connectors facing the feedthrough: one PCIe 16x (164 pins) connector carrying the high-speed links and the control and monitoring signals and two LV connectors carrying the hybrid supply voltages. The pin-out of the PCIe connector is given in Section 8.1 and the pinouts of the LV connectors are given in Section 8.2.

The signals are transmitted between the vacuum feedthrough to the hybrid via flexible high-speed data tapes. The connectors on these tapes and the matching connectors on the vacuum feedthrough and hybrids are described in Section 8.3. The OPB front-panel have a connector for the input supply voltages which is described in Section 8.4. There are three monitoring connectors on the OPB. One on the front-panel providing access to read out the thermistors on the OPB and the hybrids and two for debugging purposes giving access to all voltages and thermistors described in Section 8.5. There is provision for direct electrical communication with the GBTx on the OPB via a USB dongle, which is also used for burning the E-Fuses with default start-up configuration of the GBTx, described in Section 8.6.

An overview of the connectors and cabling is given in Figure 10 and Figure 11 for the OPBs, feedthroughs and front-end hybrids.

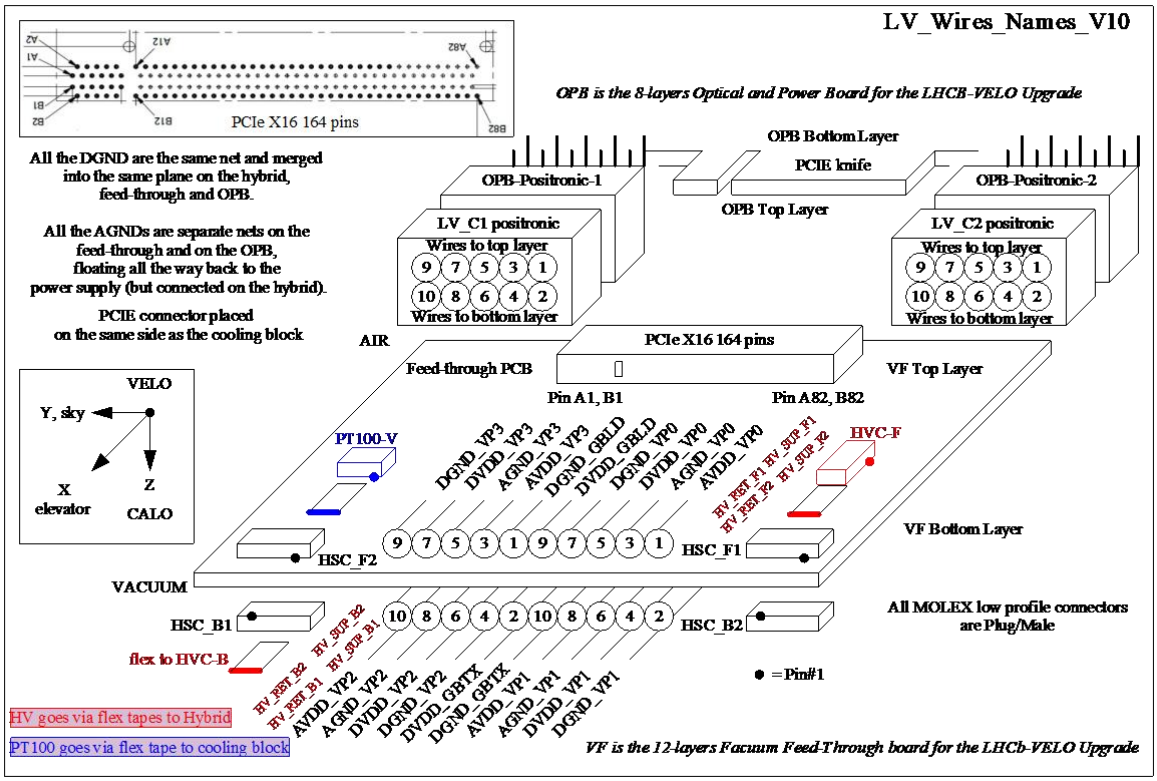


Figure 10: 3D view of the connectors on the production vacuum feedthrough with signal names.

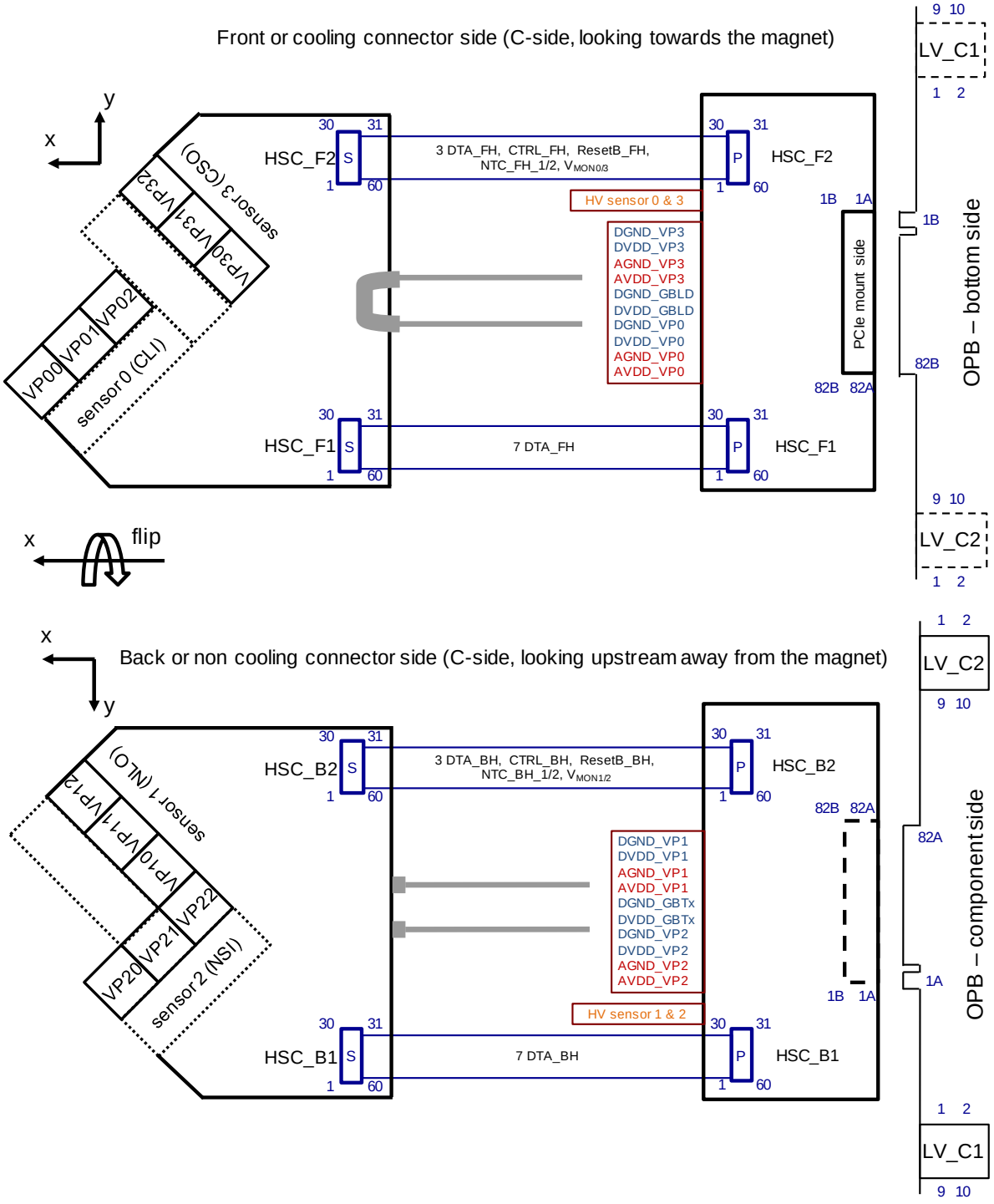


Figure 11: Overview of the detector module, cables and feedthrough for the production boards, defining sensor numbers, VeloPix numbers and connector orientations. The letters P and S stand for plug and socket, which defines the connector gender on the PCBs with pin numbers as indicated. The hybrids on the modules are implemented as three separate flex circuits to reduce the mechanical stresses that arise from differences in thermal expansion coefficients.

8.1 PCIe connector interfacing the OPB to the vacuum feedthrough

Table 16: Pin-out for the 16x PCIe on the OPB interfacing the feedthrough.

Pin	Side A	Side B
1	DGND	DGND
2	DGND	DGND
3	DGND	DGND
4	DGND	DGND
5	DGND	DGND
6	DGND	DGND
7	DGND	DGND
8	DGND	DGND
9	DGND	DGND
10	DGND	DGND
11	DGND	DGND
key notch		
12	DGND	DGND
13	DGND	DGND
14	DGND	DTA_VP323_N
15	DGND	DTA_VP323_P
16	DTA_VP313_N	DGND
17	DTA_VP313_P	DGND
18	DGND	DTA_VP303_N
19	DGND	DTA_VP303_P
20	DTA_VP200_P	DGND
21	DTA_VP200_N	DGND
22	DGND	CTRL_DN_FH_P
23	DGND	CTRL_DN_FH_N
24	CTRL_UP_FH_N	DGND
25	CTRL_UP_FH_P	DGND
26	DGND	VMON3_FH
27	DGND	DGND
28	RESETB_FH	VMON0_FH
29	DGND	DGND
30	DGND	NTC_FH_COM
31	DGND	NTC_FH_VP3
32	DGND	NTC_FH_GBTX
33	DGND	NTC_FH_VP0
34	DTA_VP201_P	DGND
35	DTA_VP201_N	DGND
36	DGND	DTA_VP202_P
37	DGND	DTA_VP202_N
38	DTA_VP203_P	DGND
39	DTA_VP203_N	DGND
40	DGND	DTA_VP212_P
41	DGND	DTA_VP212_N

Pin	Side A	Side B
42	DTA_VP213_P	DGND
43	DTA_VP213_N	DGND
44	DGND	DTA_VP223_P
45	DGND	DTA_VP223_N
46	DTA_VP023_N	DGND
47	DTA_VP023_P	DGND
48	DGND	DTA_VP022_N
49	DGND	DTA_VP022_P
50	DTA_VP021_N	DGND
51	DTA_VP021_P	DGND
52	DGND	DTA_VP020_N
53	DGND	DTA_VP020_P
54	DTA_VP013_N	DGND
55	DTA_VP013_P	DGND
56	DGND	DTA_VP012_N
57	DGND	DTA_VP012_P
58	DGND	DGND
59	DGND	DGND
60	DGND	NTC_BH_VP1
61	DGND	NTC_BH_GBTX
62	DGND	NTC_BH_VP2
63	DGND	NTC_BH_COM
64	DGND	DGND
65	RESETB_BH	VMON2_BH
66	DGND	DGND
67	DGND	VMON1_BH
68	CTRL_UP_BH_P	DGND
69	CTRL_UP_BH_N	DGND
70	DGND	CTRL_DN_BH_P
71	DGND	CTRL_DN_BH_N
72	DTA_VP003_N	DGND
73	DTA_VP003_P	DGND
74	DGND	DTA_VP103_P
75	DGND	DTA_VP103_N
76	DTA_VP113_P	DGND
77	DTA_VP113_N	DGND
78	DGND	DTA_VP123_P
79	DGND	DTA_VP123_N
80	DGND	DGND
81	DGND	DGND
82	DGND	DGND

8.2 LV connectors interfacing the OPB to the vacuum feedthrough

The pin-out of LV connector on the OPB that is interfacing the vacuum feedthrough is given in Table 17. The connector is made by Positronic and has the part number SP1EYY1F83091.

Table 17: Pin-out of LV connectors facing the vacuum feedthrough on the production boards.

LV connector C1				
Pin	Voltage Name		Voltage name	Pin
1	DGND		DVDD_GBLD_H	2
3	AVDD_VP3		DGND	4
5	AGND_VP03		DVDD_VP2	6
7	DVDD_VP3		AGND_VP12	8
9	DGND		AVDD_VP2	10

LV connector C2				
Pin	Voltage Name		Voltage Name	Pin
1	AVDD_VP0		DGND	2
3	AGND_VP03		DVDD_VP1	4
5	DVDD_VP0		AGND_VP12	6
7	DGND		AVDD_VP1	8
9	DVDD_GBTx_H		DGND	10

8.3 High speed data tape connectors

The connectors on the high-speed data tapes are Molex 60 pin, 0.4 mm pitch SlimStack connectors with 1 mm mated height (5024266010). The high-speed signals are routed as differential pairs and the static signals are transmitted on single traces. There are four high-speed connectors on the vacuum feedthrough, connecting to four data tapes, where each tape carries the data links from one VeloPix tile. The data links are labelled with the sensor, VeloPix and link number, as defined in Figure 11. The naming convention for the data links is DTA_VP<sensor #><VeloPix #><link #>.

The position of the VeloPix ASICS and numbering of the data links are shown in Figure 12. The first high-speed connector on each side carries the seven serial data links originating from the VeloPix tile that is closest to the beam. The pin-out for the first connector on the cooling connector side of the module is given in Table 18, carrying the seven data links from the VeloPix tile 0. There is an identical connector for the other side of the module carrying the data links from VeloPix tile 2, with a pin-out given in Table 20.

The second high-speed connector carries the three data links from the tile further away from the beam, the control links, the reset and the monitoring signals. The pin out for the connector on the cooling connector side of the module is given in Table 19, carrying the signals from VeloPix tile 3. The connector pinout for the other side of the module carrying the data links for VeloPix tile 1 is given in Table 21.

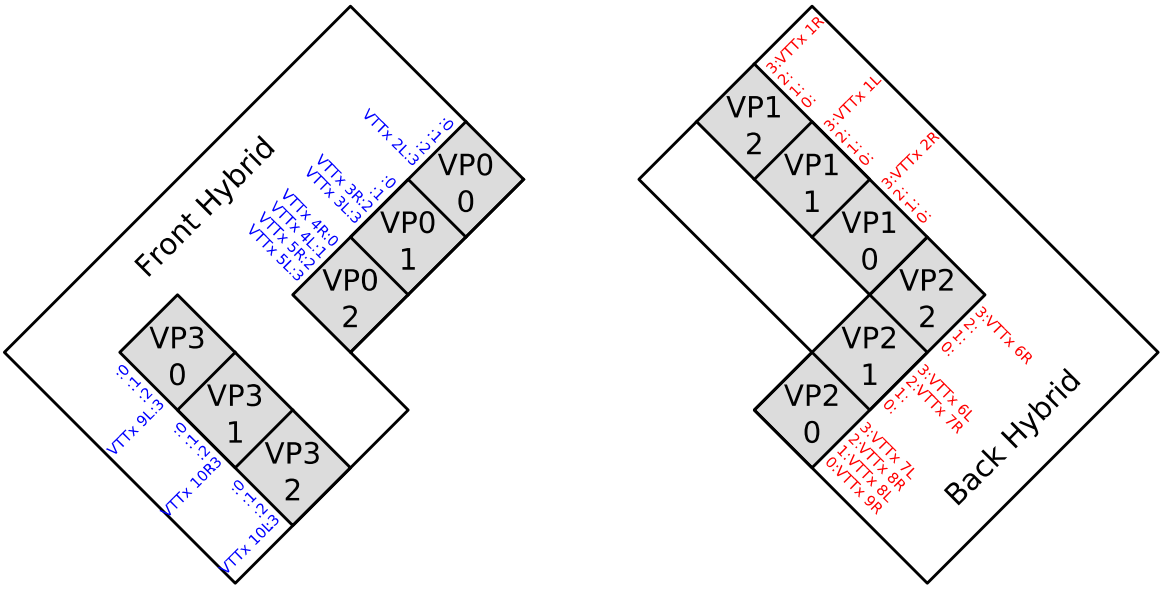


Figure 12: Schematic overview of the position of the VeloPix tiles, their numbering and the numbering of the data links. The picture also indicates which VTTx module each VeloPix data link is routed to through the data tapes, vacuum feedthrough board and OPB. The number gives the number of the VTTx module on the OPB and L and R means the left and right-hand side port on the module, where L means pins TD+/- and R means pins TD2+/-.

Table 18: Pin-out of the front (cooling connector) side high-speed connectors close to the 'long' edge of the module (HSC_F1) for the production boards. All non-listed pins are connected to GND.

Name	Hybrid pin	Feedthrough pin	VTTx number	VTTx pin name	VTTx pin
DTA_VP003_N	4	57	2	TD1-	19
DTA_VP003_P	3	58		TD1+	18
DTA_VP012_N	8	53	3	TD2-	13
DTA_VP012_P	7	54		TD2+	12
DTA_VP013_N	12	49	3	TD1-	19
DTA_VP013_P	11	50		TD1+	18
DTA_VP020_N	16	45	4	TD2-	13
DTA_VP020_P	15	46		TD2+	12
DTA_VP021_N	20	41	4	TD1-	19
DTA_VP021_P	19	42		TD1+	18
DTA_VP022_N	24	37	5	TD2-	13
DTA_VP022_P	23	38		TD2+	12
DTA_VP023_N	28	33	5	TD1-	19
DTA_VP023_P	27	34		TD1+	18

Table 19: Pin-out of the front (cooling connector) side high-speed connector close to the 'short' edge of the module (HSC_F2) for the production boards. All non-listed pins are connected to GND. NB: CTRL_UP has a logic inversion due to routing constraints (corrected for in the firmware).

Name	Hybrid pin	Feedthrough pin	PCIe pin		Name	Pin
					VTRx_FH	
CTRL_UP_FH_N	12	49	A24		TD-	19
CTRL_UP_FH_P	11	50	A25		TD+	18
					GBLD_FH	
CTRL_DN_FH_P	15	46	B22	Logic NOT	MODA-	22
CTRL_DN_FH_N	16	45	B23		MODA+	21
					OPB_MON_CON	
NTC_FH_GBTX	3	58	B32		NTC_FH_GBTX	10
NTC_FH_VP0	2	59	B33		NTC_FH_VP0	12
NTC_FH_COM	5	56	B30		NTC_FH_COM	6
NTC_FH_VP3	4	57	B31		NTC_FH_VP3	8
					SCA_2	
RESETB_FH	7	54	A28		GPIO_pad<10>	C9
VMON0	6	55	B28		ADC<27>	P5
VMON3	8	53	B26		ADC<28>	M4
				VTTx	VTTx pin name	VTTx pin
DTA_VP303_P	19	42	B19	9	TD1+	18
DTA_VP303_N	20	41	B18		TD1-	19
DTA_VP313_P	23	38	A17	10	TD2+	12
DTA_VP313_N	24	37	A16		TD2-	13
DTA_VP323_P	27	34	B15	10	TD1+	18
DTA_VP323_N	28	33	B14		TD1-	19

Table 20: Pin-out of the back (non-cooling connector) side high-speed connector close to the 'short' edge of the module (HSC_B1) for the production boards. All non-listed pins are connected to GND. NB: all data lines have a logic inversion due to routing constraints (corrected for in the firmware).

Name	Hybrid pin	Feedthrough pin	VTTx number	VTTx pin name	VTTx pin
DTA_VP200_P	4	57	9	TD2-	13
DTA_VP200_N	3	58		TD2+	12
DTA_VP201_P	8	53	8	TD1-	19
DTA_VP201_N	7	54		TD1+	18
DTA_VP202_P	12	49	8	TD2-	13
DTA_VP202_N	11	50		TD2+	12
DTA_VP203_P	16	45	7	TD1-	19
DTA_VP203_N	15	46		TD1+	18
DTA_VP212_P	20	41	7	TD2-	13
DTA_VP212_N	19	42		TD2+	12
DTA_VP213_P	24	37	6	TD1-	19
DTA_VP213_N	23	38		TD1+	18
DTA_VP223_P	28	33	6	TD2-	13
DTA_VP223_N	27	34		TD2+	12

Table 21: Pin-out of the back (non-cooling connector) side high-speed connector close to the 'long' edge of the module (HSC_B2) on the production boards. All non-listed pins are connected to GND. NB: all data lines and CTRL_UP have a logic inversion due to routing constraints (corrected for in the firmware).

Name	Hybrid pin	Feedthrough pin	PCIe pin		Pin	Name
					VTRx_BH	
CTRL_UP_BH_N	12	49	A69	Logic NOT	TD+	18
CTRL_UP_BH_P	11	50	A68		TD-	19
					GBLD_BH	
CTRL_DN_BH_P	15	46	B70		MODA+	21
CTRL_DN_BH_N	16	45	B71		MODA-	22
					OPB_MON_CON	
NTC_BH_VP1	2	59	B60		NTC_BH_VP1	11
NTC_BH_GBTX	3	58	B61		NTC_BH_GBTX	9
NTC_BH_VP2	4	57	B62		NTC_BH_VP2	7
NTC_BH_COM	5	56	B63		NTC_BH_COM	5
					SCA_1	
RESETB_BH	7	54	A65		GPIO_pad<10>	C9
VMON2	6	55	B65		ADC<28>	M4
VMON1	8	53	B67		ADC<27>	P5

				VTTx	VTTx pin name	VTTx pin
DTA_VP103_P	19	42	B74	2	TD2-	13
DTA_VP103_N	20	41	B74		TD2+	12
DTA_VP113_P	23	38	A76	1	TD1-	19
DTA_VP113_N	24	37	A77		TD1+	18
DTA_VP123_P	27	34	B78	1	TD2-	13
DTA_VP123_N	28	33	B79		TD2+	12

8.4 OPB input LV power supply connector

The power supply connector pin-out for the OPBs is given in Table 22, the connector is a Molex with part number 172064-0010.

Table 22: Pin-out of the power supply connector for the production OPB, Molex 172064-0010.

LVCON_PS			DC/DC converter
Pin	Description		
8	Supply	VeloPix 0 & 3 digital, Link 2 and GBLDs on the hybrids	DCDC_VPD0
			DCDC_VPD3
3	Return		DCDC_OPB_LINK2
			DCDC_GBLD_H
7	Supply	VeloPix 1 & 2 digital, Link 1 and GBTxs on the hybrids	DCDC_VPD1
			DCDC_VPD2
2	Return		DCDC_OPB_LINK1
			DCDC_GBTX_H
6	Supply	VeloPix 0 & 3 analogue	DCDC_VPA0
1	Return		DCDC_VPA3
9	Supply	VeloPix 1 & 2 analogue	DCDC_VPA2
4	Return		DCDC_VPA1
10	Supply	OPB common supply	DCDC_OPB_CTRL
5	Return		DCDC_OPB_VTRx

8.5 Monitoring connectors

The production version of the OPB has a temperature monitoring connector that gives access to the NTC thermistors located on the hybrid and the OPB, with a pin-out given in Table 23. The connector is a Samtec TFM-107-01-L-D-RA. The OPB also has two monitoring connectors located on the face of the PCB, one giving access to the supplied voltages with pin-out given in Table 24 and one giving access to the regulated voltages and hybrid monitoring voltages with pin-out given in Table 25. These two connectors are intended for production tests and debugging purposes. NB: The three NTCs on each side of the module are read out through four wires, with one side common.

Table 23: Pin-out of the front-panel connector for the temperature monitoring of the production OPB, Samtec TFM-107-01-L-D-RA.

Pin	Signal Name	Signal Name	Pin
1	NTC_OPB_1N	NTC_OPB_2N	2
3	NTC_OPB_1P	NTC_OPB_2P	4
5	NTC_BH_COM	NTC_FH_COM	6
7	NTC_BH_VP2	NTC_FH_VP3	8
9	NTC_BH_GBTX	NTC_FH_GBTX	10
11	NTC_BH_VP1	NTC_FH_VP0	12
13	DGND	DGND	14

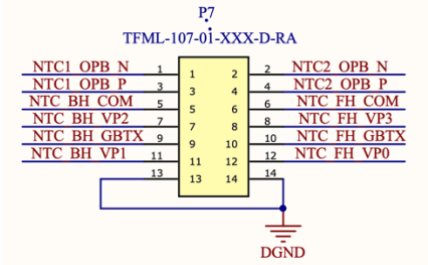


Table 24: Pin-out of the on-PCB monitoring connector for the supply voltages for the production OPB.

Pin	Signal Name	Signal Name	Pin
1	AGND_VP03	VPS_A_FH	6
2	DGND	VPS_D_BH	7
3	DGND	VPS_D_FH	8
4	AGND_12	VPS_A_BH	9
5	DGND	VPS_OPB	10

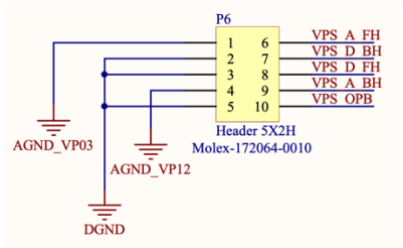
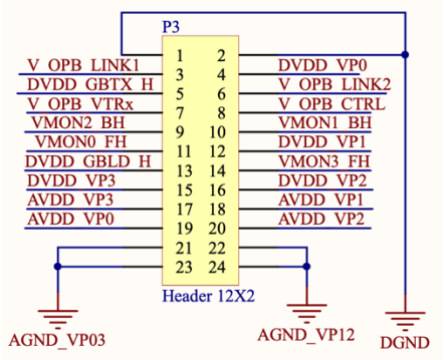


Table 25: Pin-out of the on-PCB monitoring connector for the temperature (NTC) signals, DC/DC output voltages and hybrid monitoring voltages for the production OPB.

Pin	Signal Name	Signal Name	Pin
1	DGND	DGND	2
3	V_OPB_LINK1	DVDD_VP0	4
5	DVDD_GBTx_H	V_OPB_LINK2	6
7	V_OPB_VTRx	V_OPB_CTRL	8
9	VMON2_BH	VMON1_BH	10
11	VMON0_FH	DVDD_VP1	12
13	DVDD_GBLD_H	VMON3_FH	14
15	DVDD_VP3	DVDD_VP2	16
17	AVDD_VP3	AVDD_VP1	18
19	AVDD_VP0	AVDD_VP2	20
21	AGND_VP03	AGND_VP12	22
23	AGND_VP03	AGND_VP12	24



8.6 USB programming and E-Fuse burning connector

The GBTx communication via the USB dongle and the E-Fuse burning is done through a Samtec connector MTLW-104-07-L-D-250 with the pinout given in Table 26. The programming also requires an external 3.3 V power supply through Phoenix connector MSTBA2,5/2-G-5,08 where pins 2 and 1 are supply and return respectively. This connector is identical for the prototype and production boards.

Table 26: Pin-out of the E-Fuse programming connector, compatible with the USB programming dongle.

Pin	Signal
1	1.5 V (from DCDC_OPB_CTRL)
2	3.3 V (from external supply connector)
3	DGND_OPB
4	EFUSEPROGRAMPULSE
5	GBTx_SDA
6	DCDC_OPB_CTRL Enable
7	GBTx_SCL
8	DCDC_OPB_VTRx Enable

9 Mechanical design and OPB crate

The OPBs are manufactured with eight metal layers in a PCB with the dimensions 400x150 mm^2, excluding the 10 mm protrusion for the PCIe connector. The dielectric layers surrounding the high-speed signal layers are made with the low-loss dielectric Isola I-Tera MT40[2], and the remaining layers are made with standard FR4. An overview of the layout is shown in Figure 13, which excludes the full metal layers. The Gerber files and the schematics of the board are available in Ref. [3].

The OPBs are mounted in custom crates on the VELO vacuum tank, as illustrated in Figure 14. The backplane consists of the PCIe connector mounted on the vacuum feedthrough PCB, which is integrated in the VELO vacuum tank, and the LV connectors. The frame holding the OPBs is attached to the vacuum tank and it has rails that guides the boards to the correct position for the backplane connectors. The OPB has a front-panel with openings for the optical fibre connectors, LV supply connector and temperature monitoring connector. The front-panel is screwed into the frame to hold the boards in place.

The OPBs are not aligned in the z-direction with the modules they serve, they are mounted at a regular pitch of 30 mm. This is done to provide sufficient distance between each board to fit the components and to make the mechanical design simpler. The difference is z-position between the OPBs and the detector modules are taken up by the cable routing inside the vacuum tank.

The power dissipation of the OPB takes mainly place in the DC/DC converters, the GBTx ASIC and the VTTx and VTRx electro-optical converters. The OPB has an aluminium plate mounted on the back of the PCB to provide a thermal path from the components to the frame of the crate. This plate has milled openings to provide clearance for through-hole components and is mounted with a sheet of thermal rubber to provide good contact. The thermal connection between the metal plate and the VTTx and VTRx electro-optical converters is poor due to their plastic housing. Hence an additional cooling is provided through a forced vertical air flow through the crates.

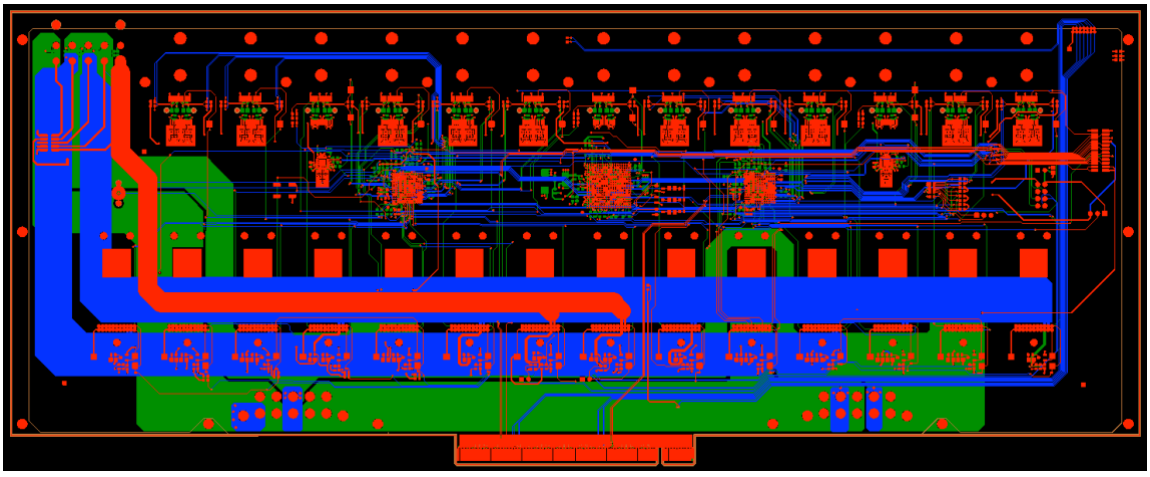


Figure 13: Overview of the metal layers in the OPB, excluding the full metal planes. The orange line marks the edge of the board, where the PCIe connector is visible at the bottom and the electro-optical transceivers are mounted at the top edge.

[2] From Isola Group

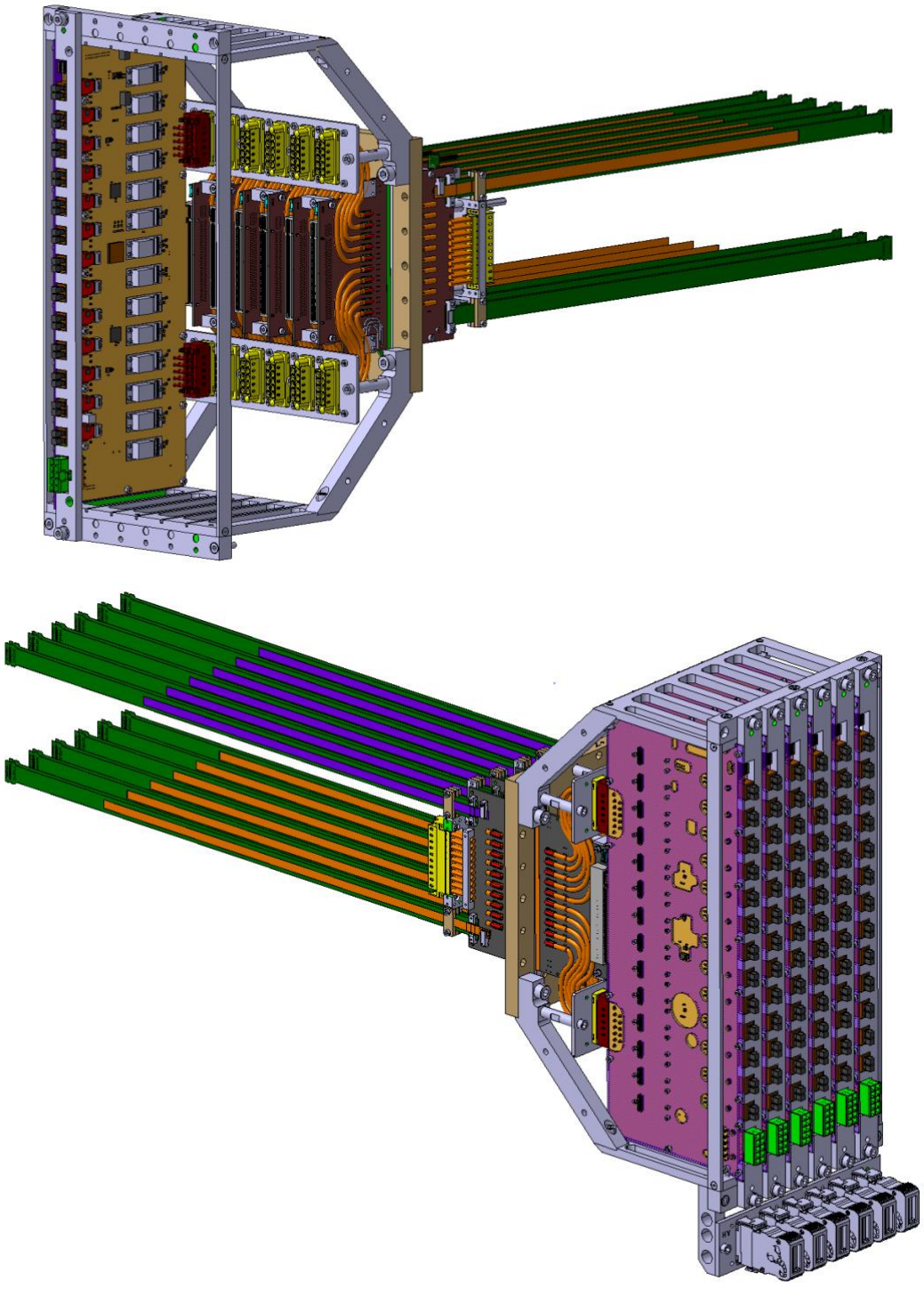


Figure 14: Mechanical view of the OPBs mounted in the crate, showing the LV and PCIe connectors, the vacuum feedthrough, and the HV and data tapes. The lower figure shows the metal plate mounted at the back of the board (pink) to conduct the heat from the components to the frame of the crate.

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