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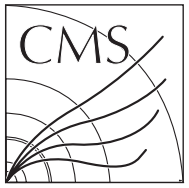

The Compact Muon Solenoid Experiment

Conference Report

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First measurements with the CMS DAQ and Timing Hub prototype-1

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Abstract

The DAQ and Timing Hub is an ATCA hub board designed for the Phase-2 upgrade of the CMS experiment. In addition to providing high-speed Ethernet connectivity to all back-end boards, it forms the bridge between the sub-detector electronics and the central DAQ, timing, and trigger control systems. One important requirement is the distribution of several high-precision, phase- stable, and LHC-synchronous clock signals for use by the timing detectors. The current paper presents first measurements performed on the initial prototype, with a focus on clock quality. It is demonstrated that the current design provides adequate clock quality to satisfy the requirements of the Phase-2 CMS timing detectors.

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PROCEEDINGS OF SCIENCE

First measurements with the CMS DAQ and Timing Hub prototype-1

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The DAQ and Timing Hub is an ATCA hub board designed for the Phase-2 upgrade of the CMS experiment. In addition to providing high-speed Ethernet connectivity to all back-end boards, it forms the bridge between the sub-detector electronics and the central DAQ, timing, and trigger control systems. One important requirement is the distribution of several high-precision, phase-stable, and LHC-synchronous clock signals for use by the timing detectors.

The current paper presents first measurements performed on the initial prototype, with a focus on clock quality. It is demonstrated that the current design provides adequate clock quality to satisfy the requirements of the Phase-2 CMS timing detectors.

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1. Introduction

The CMS detector will undergo a major upgrade for Phase-2 of the LHC program: the HiLumi LHC, starting around 2026. The upgraded CMS detector will be read out at an unprecedented data rate of up to 50 Tb/s with an event rate of 750 kHz, selected by the level-1 hardware trigger, and an average event size of 7.5 MB. The Phase-2 CMS back-end electronics will be based on the ATCA standard, with node boards receiving the detector data from the front-ends via optical links. An ATCA hub board, the DAQ and Timing Hub (DTH), will provide the interface between the back-end nodes and the central Trigger, Timing, and DAQ systems. This paper presents the first measurements performed on the initial prototype production, with a focus on clock quality. More detail about the Phase-2 CMS Trigger-DAQ design can be found in [1, 2].

The CMS DAQ and Timing Hub will connect to all back-end node boards. It is responsible for the distribution of clock, trigger, and fast-control data from the central trigger control system to all back-end electronics and the handling of throttling signals in the other direction. The DAQ interface for the event data uses point-to-point optical links connected to back-end node boards and runs a custom lossless 'SlinkRocket' protocol. The event data are aggregated in the DTH and transmitted via standard commercial network (with links of 100 Gb/s or higher) and protocol (such as TCP/IP) to event building computer nodes at the surface.

The introduction of timing detectors for Phase-2 CMS, aiming for a 30 ps precision on individual detector hits, strongly tightens the requirements on the clock and timing information distributed throughout the experiment, with different sub-detectors introducing different requirements.

2. The DTH development program

At TWEPP 2018 the design of the first DTH prototype (P1) was presented, together with some of the design challenges encountered [3]. Other contributions summarised the phase noise studies performed as part of the component selection for the DTH.

The final DTH needs to fulfill three main tasks: the distribution of clock and timing signals to and from the back-end electronics, the aggregation and transmission of event data from the back-ends to the commercial data-to-surface network, and the management of the 1 Gbit/s Ethernet connectivity required for each of the node slots. The P1 is designed to demonstrate the DAQ and timing functions, whereas an independent prototype has been designed to develop a managed Ethernet switch. The different development lines will later be merged into the final DTH design.

The DTH P1 board features an FPGA (KU15P) with ancillary components for clock recovery and jitter-cleaning, and serial links to the back-plane implementing the clock, timing, trigger and throttling functions. A second FPGA (KU15P) with mid-board optics (FireFly) connecting to the back-end boards, and QFSP+ cages connecting to the standard commercial network, implements the DAQ event flow functions.

On the DAQ side, proof-of-principle has been shown of the sharing of multiple TCP streams through a single 100 GbE link. Optimisation in order to achieve the required throughput is currently under way, as well as studies with high bandwidth in-FPGA memory.

3. The role of the DTH in the clock distribution

The baseline clock distribution scheme for the Phase-2 CMS upgrade foresees the encoding of the LHC bunch clock in a high-speed serial stream (at $\approx 10\,\mathrm{Gbit/s}$) from the upgraded Trigger Control and Distribution System (TCDS) to the DAQ and Timing Hub board present in each sub-system back-end crate. The DTH recovers and cleans this embedded clock, and then distributes two phase-locked clocks over the backplane to all node slots: the 40 MHz LHC bunch clock for beam-synchronous logic, and a precision 320 MHz clock for use as high-speed transceiver (MGT) reference. Timing and synchronization signals are extracted from the incoming serial stream and distributed on dedicated backplane lines to all node slots. The sub-detector back-end electronics in turn distribute the sampling clock embedded in an lpGBT or GBT serial stream to the front-ends. This scheme requires the DTH be capable of 1. recovering an LHC bunch clock and a higher-speed MGT reference clock of sufficient quality from the incoming serial stream from the TCDS master, and 2. reliably reproducing a fixed phase relationship between these clocks and the TCDS master.

Figure 1 shows a simplified overview of the DTH clock paths. The $\approx 10\,\mathrm{Gbit/s}$ serial stream from the TCDS master is received by an FPGA MGT via a standard SFP. The recovered 320 MHz clock is passed into the FPGA fabric, where it is divided down to recreate the 40 MHz LHC bunch clock. This bunch clock is output through the global clock network and used as input to the master PLL/jitter attenuator, from where all on-board and backplane clocks are generated. In addition the recovered 320 MHz clock can be output straight from the MGT and, after a pass through a jitter cleaner, used as MGT reference for all backplane TCDS links.

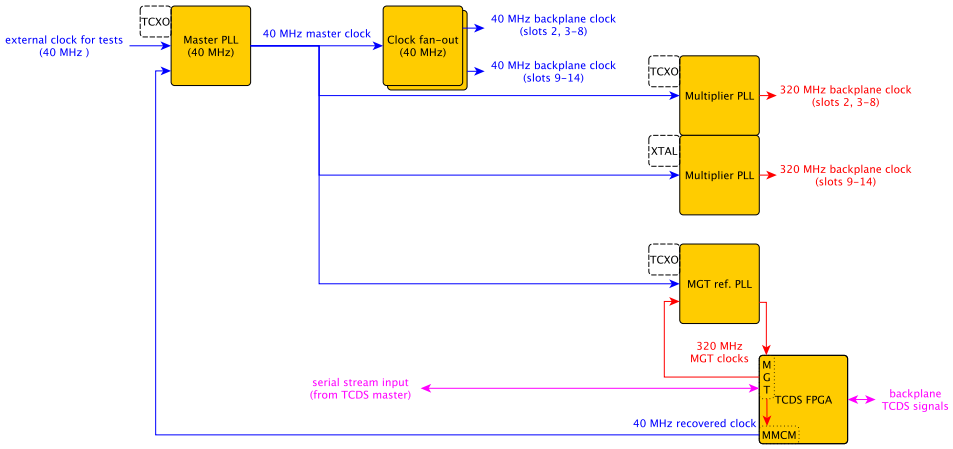

Figure 1: Overview of the clock distribution paths on the DTH P1. In the baseline scheme the DTH receives a high-speed serial stream from the TCDS master, containing both clock and synchronization information. The clock is recovered from the serial stream, divided down to the LHC bunch crossing frequency, and cleaned by the on-board master PLL. For test and evaluation purposes the P1 DTH prototype is also equipped with a direct clock input to the master PLL, and several jitter attenuators have been equipped with different crystal and/or TCXO references.

4. Backplane clock quality

For the requirements of the Phase-2 CMS timing detectors the clock quality is characterized

in terms of phase noise and the corresponding RMS jitter. High-frequency phase noise can be cleaned using appropriate jitter attenuators, but low-frequency wander cannot. Therefore it is of utmost importance that the design and implementation of the clock distribution do not introduce any significant low-frequency noise.

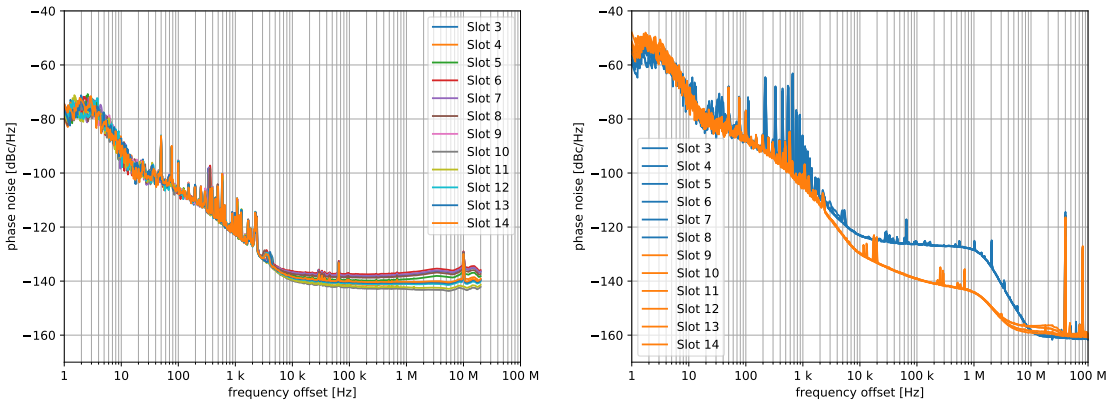

Figure 2: Phase noise curves for the 40 MHz (left) and 320 MHz (right) backplane clocks in all node slots of the shelf. The former show minor slot-to-slot variations due to backplane attenuation affecting the signal slew rate. The latter clearly form two groups, corresponding to the two jitter cleaners disciplined by a TCXO (slots 3-8) and a crystal (slots 9-14).

As part of the performance characterization of the DTH P1, a clean input clock was sourced to the auxiliary input of the master PLL, and the backplane clock signals were inspected with the help of a commercial break-out board. Figure 2 shows the phase noise spectra of the 40 MHz and 320 MHz backplane clocks. The high-frequency plateaus of the 40 MHz clock spectra show small slot-to-slot variations that can be traced down to frequency-dependent attenuation on the backplane affecting the signal slew rate as a function of distance. The results from the 320 MHz clocks clearly separate into two distinct groups corresponding to two jitter cleaners on the board: one disciplined by a TCXO and one disciplined by a plain crystal. (See also Fig. 1.) A comparison between these two groups shows two design/implementation features. The additional spurs between 200 Hz and 2 kHz in the TCXO-driven case seem to be related to imperfections in the power and PCB design of the DTH. The next iteration of the design aims to address these imperfections. The phase noise plateau from 10 kHz to 1 MHz is a feature of the chosen TCXO. The behavior at low frequencies is in all cases determined by the phase noise contents of the input clock. The worst case jitter for the 40 MHz (320 MHz) clocks shows an RMS of 4.9 ps (3.7 ps) when integrated over $[1\,\text{Hz}, 20\,\text{MHz}]$.

Given the relatively poor performance of the TCXO-based part of the design, combined with the good results obtained with the crystal-driven cleaner, the final DTH design will most likely rely on crystals to discipline all jitter attenuators.

5. Clock distribution proof-of-principle

A first two-DTH setup was used to demonstrate the board-to-board clock distribution. A 'sender' DTH generates a high-speed PRBS stream from an auxiliary clock, and a 'receiver' DTH recovers 40 MHz and 320 MHz clocks from this PRBS stream. Figure 3 shows a phase-noise

comparison between the bunch clock at the output of the master PLL on the 'sender', and the same clock signal on the 'receiver', as well as the spectra of two intermediate 320 MHz clocks. This measurement demonstrates that 1. the DTH P1 does not introduce any significant low-frequency phase noise, and that 2. the quality of the LHC bunch clock is almost unaffected by the encoding and recovery procedure.

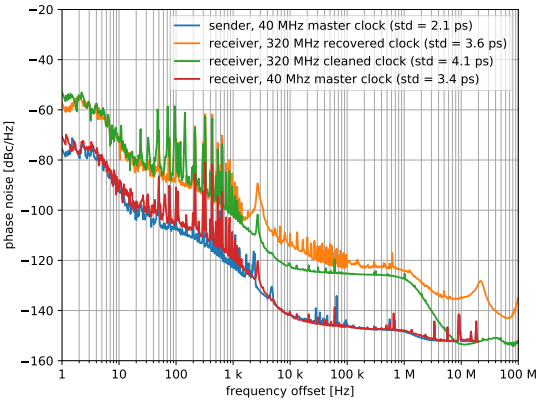

Figure 3: Results of the first dual-DTH measurements. One DTH was configured as 'sender', using an auxiliary 40 MHz clock to distribute a 10.24 MHz PRBS31 stream to a second 'receiver' DTH. This second DTH recovered the 40 MHz and 320 MHz clocks from the incoming serial stream. The numbers in the legend represent the RMS jitter as integrated over $[1\,\text{Hz}, 20\,\text{MHz}]$. These results show that the clock quality is not significantly affected by the serial encoding/decoding.

6. Conclusion and outlook

The development plan of the Phase-2 CMS DAQ and Timing Hub is well under way. All measurements and verifications performed so far with the first prototype clearly indicate that the hardware design meets the requirements for high-quality clock distribution imposed by the CMS timing detectors. The next step is to demonstrate that this still holds true when using the TCDS2 protocol, and that in addition a fixed phase of all distributed clocks can be guaranteed even across resets and power-cycles.

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