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Hybrids Acceptance Tools for the CMS Phase-2 Tracker Upgrade

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Abstract

Up to fifty thousand front-end and service hybrids are required for the CMS Tracker Phase-2 Upgrade. These hybrids are built on carbon fibre stiffened circuits and contain several flip-chip ASICs, that will be glued in module structures, making repairs almost impossible. Due to their complexity, testing within production is a very important aspect. A multiplexed testing infrastructure, based on custom crates and test cards will be presented. This testing hardware is supported by software tools to enable the exhaustive verification of hybrids at the manufacturing sites and for their acceptance within the collaboration.

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ABSTRACT: Up to fifty thousand front-end and service hybrids are required for the CMS Tracker Phase-2 Upgrade. These hybrids, which are built on carbon fibre stiffened circuits and contain several flip-chip ASICs, will be glued in module structures, making repairs almost impossible. Due to their complexity, testing within production is a very important aspect. A multiplexed testing infrastructure, based on custom crates and test cards will be presented. This testing hardware is supported by software tools to enable the exhaustive verification of hybrids at the manufacturing sites and for their acceptance within the collaboration.

KEYWORDS: Front-end electronics for detector readout; Manufacturing; Detection of defects.

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1. Introduction

The design of the Phase-2 CMS Outer Tracker is based on two main types of modules (**Figure 1**): the strip-strip (2S) and the pixel-strip (PS) modules [1]. Each module is composed of two stacked silicon sensors and several hybrid printed circuits. There are two types of hybrids for the 2S module: the 2S Front-End Hybrid (2S-FEH) and the 2S Service Hybrid (2S-SEH). The 2S-FEH houses the ASICs responsible for hit detection and hit data transmission. It contains two types of ASICs: the CBC (CMS Binary Chip) and the CIC (Concentrator Integrated Circuit). The CBC reads out the strip sensors while the CIC aggregates the digital data coming from the readout chips and formats the data for transmission to the lpGBT (Low Power Giga Bit Transceiver). The 2S-SEH is responsible for providing power to the two FEHs and for the optical readout and control of the module.

There are three types of hybrids for the PS module: the PS Front-End Hybrid (PS-FEH), the PS Read-Out Hybrid (PS-ROH) and the PS Power Hybrid (PS-POH). The PS-FEH again houses the ASICs responsible for hit detection and hit data transmission. Three types of ASICs form the PS Front-End data path: the already mentioned CIC, the SSA (Short Strip ASIC) and the MPA (Macro Pixel ASIC). The SSA and MPA are both sensor readout chips. The PS-ROH is responsible for the optical readout and control of the module, and the PS-POH provides power to both the FEHs and the ROH.

In total, 27,900 2S type hybrids and 26,960 PS type hybrids are required for the full Tracker construction [2]. Modules assembled with faulty hybrids are not repairable and will

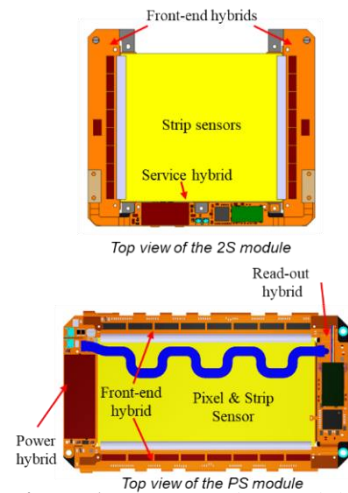


Figure 1: Outer Tracker module types: 2S (top) and PS (bottom) with the constituting hybrids

have to be discarded. For this reason, testing is a crucial step of the hybrids' manufacturing process.

2. Test system requirements and overview



Figure 2: Multiplexing crate with inserted test cards.

The multiplexing crate turns on one plug-in card at a time and multiplexes the data lines to it. A plug-in card can test one hybrid per test run. The complete test system will consist of three crates, allowing 36 hybrids to be tested in one test run.

Every single hybrid must be tested at least once, by the manufacturer. After reception at CERN, a fraction of each batch will be re-tested for status confirmation. This sets the need for a test system that allows for high throughput testing. To this end, a multiplexing test system was devised. The system is hosted in a standardised 3U crate into which plug-in cards can be inserted (**Figure 2**). Up to twelve plug-in cards can be inserted in the crate.

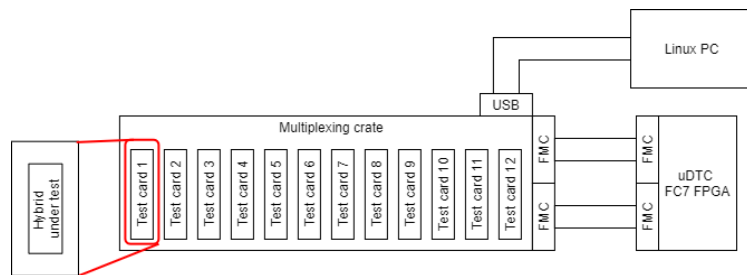


Figure 3: Test system general architecture.

The system architecture is shown in **Figure 3**. The crate is connected to an *FC7* back-end board and a Linux PC. The *FC7* is a μ TCA compatible FPGA carrier board [3] that interfaces with the hybrid and controls the multiplexing crate. The PC runs the test procedure and interfaces with the *FC7* and the test card.

3. Test system hardware

3.1 Multiplexing system

The multiplexing crate has three “backplanes”. Each backplane is designed to multiplex four plug-in cards. They are connected together to form a 12-card multiplexer hosted in the crate, as shown in **Figure 4**. The backplanes are responsible for multiplexing 50 LVDS lines, eight LVC MOS lines and the USB port between the plug-in cards and the *FC7* and computer.

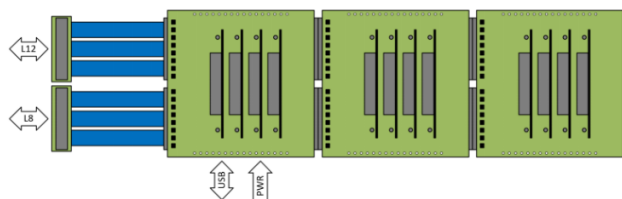


Figure 4: Three backplane interconnection scheme.

Five different plug-in test cards were designed, to test the five different types of hybrids. This paper covers the test cards for the 2S and PS FEHs, the PS-ROH and the PS-POH. Information on the test card for the 2S-SEH is available in [4].

There are some common features shared across all the designs. All the test cards use the same USB to SPI Bridge. This chip allows for the control of the test card features and for the identification of the card by the test software. The cards interface with the hybrids via

“consumable” jumper cables. This allows for the lifetime of the test card to be independent from the lifetime of the connectors, as the jumper cables are replaced periodically.

3.2.1 2S-FEH test card

The 2S-FEH test card (**Figure 5**) will verify the following 2S Front-End Hybrid parameters:

- Integrity of digital input and outputs lines of the ASICs,
- Functionality of the ASICs,
- Presence of open or shorted CBC analogue input channels using test features integrated in the ASICs and in the hybrid [5],
- Temperature and power consumption during operation.
- Performance of the 2S-FEH under different powering conditions.

3.2.2 PS-FEH test card

The parameters tested on the PS-FEH are the same as the tested on the 2S-FEH, but there is a fundamental difference when testing the input and output lines of the ASICs.

The MPAs are bump bonded to the pixel sensors of the PS Module and are therefore external to the PS-FEH hybrid (**Figure 7**). This implies that the MPA is not present for the testing of the PS-FEH individually (not as part of a module). To test the input lines of the CIC and the output lines of the SSA, a spring-loaded socket (POGO socket) allows connecting these lines to the FC7 card. The POGO socket connects to a test pattern included in the design of the PS-FEH (**Figure 6**).

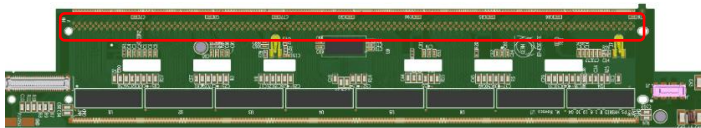


Figure 6: Unfolded PSFEH with POGO pattern (marked in red).



Figure 8: Side view of the PS-FEH test card. The top and bottom pushers of the mechanical assembly are visible, as well as the POGO connector (blue) and the hybrid.

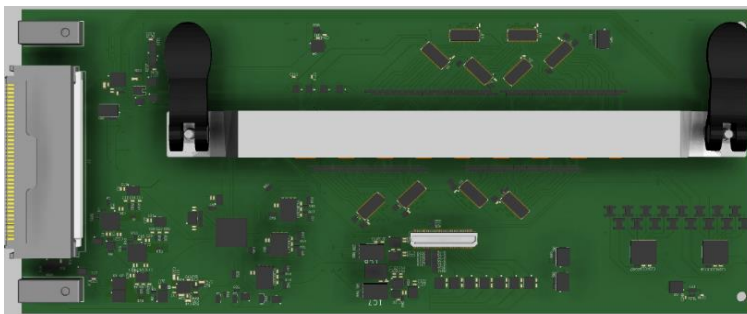


Figure 9: Top view of the PS-FEH test card with the POGO mechanical assembly.



Figure 5: 2S-FEH Test Card with 2S-FEH-R hybrid.

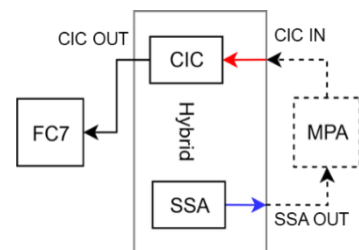


Figure 7: Digital path of the PS-FEH. Dotted elements are NOT present during hybrid

The SSA can output a test sequence that is then verified by the FC7. Similarly, the FC7 can emit a test pattern into the CIC and read it back. A mechanical assembly (**Figure 8**, **Figure 9**) couples with the POGO socket to ensure its correct connection to the pattern in the hybrid.

3.2.3 PS-ROH test card

As can be seen in **Figure 10**, two types of data paths need to be tested on the PS-ROH. To achieve this, two FC7 are used for the testing. The first one connects with the crate, to test the electrical signals going between the lpGBT and the FEHs. The second one will test the optical links between the lpGBT (via the VTRx+) and the back end.

The VTRx+ will be part of the test card assembly. The optical fibre is terminated on an MPC connector in the front panel of the test card. The optical FC7 connects to it.

The PS-ROH test card (**Figure 11**) will verify the following PS-ROH parameters:

- Integrity of the input and output lines to the lpGBT,
- Functionality of the lpGBT.
- Performance of the readout hybrid for different powering conditions,
- Monitoring of the power consumption and temperature during operation.

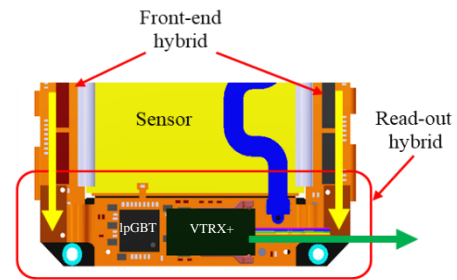


Figure 10: Top view of the PS module. The electrical data flow is indicated by the yellow arrows and the optical data flow by the green arrow.

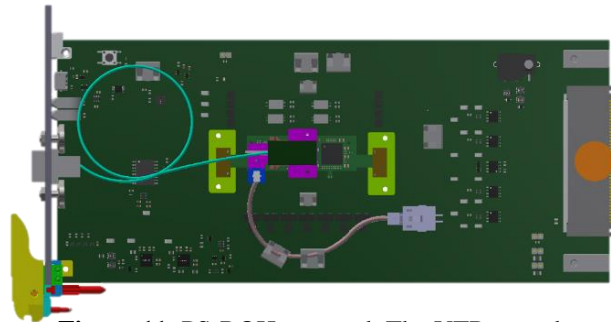


Figure 11: PS-ROH test card. The VTRx+ and MPC connector on the front panel are visible.

3.2.4 PS-POH test card

The PS-POH test card (**Figure 12**) has six constant current loads, to emulate the different voltage rails of the two FEHs and the ROH. These loads are adjustable from zero current to slightly above the maximum current uptake of the hybrid.

The parameters tested on this hybrid are:

- Output voltage under current load for all outputs for different loads and different inputs. The measurement has an accuracy of 0.25%,
- Power efficiency of the hybrid for different loads and different inputs with an accuracy of 1 percentage point,
- Output ripple for different loads, as a check for the stability of the output,
- Temperature in four different points of the hybrid and the test card,
- Setup time of the outputs (with a resolution of 10 μ s) to validate the power sequencing.

The testing of the PS-POH, due to the nature of the hybrid itself, involves greater power consumption than the other hybrids, and therefore needs dedicated power dissipation. For this reason, a heatsink is present on this test card. The hybrid is held in place with a bracket that presses it onto the heatsink, with a thermal pad in-between.



Figure 12: PS-POH Test Card.

4. Test system software ecosystem

A software ecosystem completes the crate-based test system to provide a system that is transparent to the tester. To achieve this, a single tool is used to test all the hybrids in a crate. The software structure of the system is shown in **Figure 13**. Each hybrid type is tested using specific software and firmware. The test procedure is part of the Phase 2 Acquisition and Control Framework, which encapsulates the FC7 firmware and ASIC interfacing layers. A custom USB library is used to control the test card.

The system allows for the testing of different hybrid types in the same crate. The hybrid type is encoded in an OTP field of the USB Bridge on the test cards. The top layer of the software, the Test Manager, selects the necessary hybrid-specific software and firmware. The Test Manager maps the position of each test card in the crate and the hybrids mounted on them. The only inputs needed from the operator are the serial numbers of both test card and hybrid, for each assembled test card. At

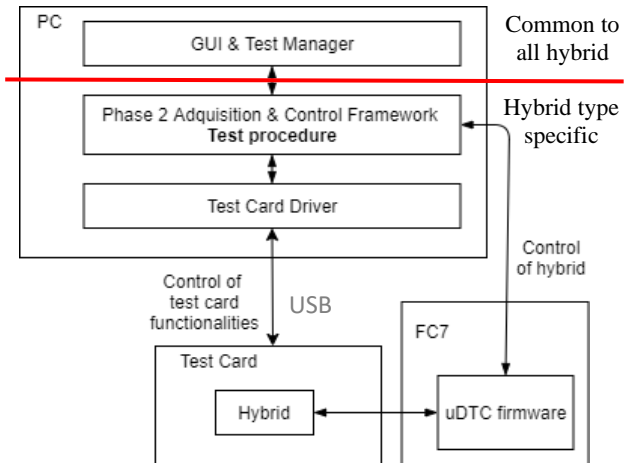


Figure 13: Software architecture of the test system.

the end of a test run, the results are uploaded to the CMS Construction Database and the test results are presented to the operator for proper classification of the hybrids.

The software ecosystem allows for the test system to be operated by non-experts increasing its versatility and decreasing the complexity of the qualification process.

5. Summary

A complete test system has been developed to support the manufacturing of the hybrid circuits for the Phase 2 Upgrade of the Outer Tracker of CMS. This test system consists of a multiplexing crate that can hold 12 plug-in cards. There are five different plug-in cards, one for each type of hybrid. An accompanying software tool encapsulates the testing firmware and procedures for all the hybrid types.

References

- [1] CMS Collaboration, "The Phase-2 Upgrade of the CMS Tracker Technical Design Report," CERN-LHCC-2017-009 / CMS-TDR-014.
- [2] Mark Istvan Kovacs et al, "A High Throughput Production Scale Front-End Hybrid Test System for the CMS Phase-2 Outer Tracker Upgrade," *PoS*, vol. TWEPP2019, p. 082.
- [3] M. Pesaresi et al, "The FC7 AMC for generic DAQ & control applications in CMS," *JINST*, vol. 10, no. 03, p. C03036, 2015.
- [4] Alexander Josef Pauls, "Test system for the Service Hybrid of the 2S Module for the CMS Phase-2 Outer Tracker Upgrade," in these proceedings.
- [5] Tomasz Gadek et al, "Testing of the front-end hybrid circuits for the CMS Tracker upgrade," *JINST*, vol. 12, no. 01, p. C01010, 2017.